# Research and Development Activities in RF and mm-Wave IC Design

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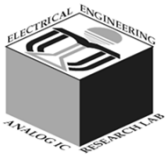


# Outline

- Research Focus
- Summary of Activities in RFIC and Single-Chip Systems
  - RF and mmW IC Building Blocks
  - Single-Chip Transceiver Systems for Wireless Applications
- IP and Publication
  - Books
  - Patents
  - Journal of Solid-State Circuits (JSSC)
  - International of Solid-State Circuit Conference (ISSCC)
- Appendix
  - Information about Completed and On-Going Projects



# Research Focus

- New design ideas and techniques for RF and analog integrated circuits and systems for wireless applications:
  - System architecture
  - Circuit implementation
- Key focus and features:
  - Standard digital CMOS processes → Lowest cost
  - Low voltage
  - Low power
  - High integration level
  - No off-chip components (inductors, filters, baluns)



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## RF and mmW Synthesizers (I)

- Low-Voltage Low-Power CMOS RF and mmW ***Synthesizers*** and ***Building Blocks*** (GSM, Bluetooth, RFID, NFC, WLAN, Cable TV Tuner, UWB, SDR, P2P, mm-Wave, sub-THz)
  - Transformer-Feedback VCOs and Frequency Dividers
  - Fully-Integrated CMOS PLLs and Frequency Synthesizers
    - Dual-Loop, Integer-N, and Fractional-N Synthesizers
    - SSB-Mixed-Based Fast-Settling Synthesizer for UWB
    - All-Digital Frequency Synthesizers
  - 60-GHz VCOs and Frequency Dividers
  - SDR Frequency Synthesizers (covering all existing standards from 50MHz to 10GHz and from 57GHz to 66GHz)
  - LO Generation for 4-Path 60-GHz Phased-Array Receivers
  - 21GHz-48GHz Low-Phase-Noise Synthesizer for P2P

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## RF and mmW IC Building Blocks (II)

- Low-Voltage Low-Power CMOS RF and mmW ***IC Building Blocks*** (GSM, Bluetooth, RFID, NFC, WLAN, Cable TV Tuner, UWB, RFID, SDR, mm-Wave, sub-THz)
  - LNAs: Narrow-band, Ultra-wide-band, SDR
  - Mixers: Narrow-band, Ultra-wide-band, SDR, image-rejection
  - On-Chip Image-Rejection and Channel-Selection Filters
  - Sigma-Delta Bandpass Analog-To-Digital Converters
  - Time-To-Digital Converters (TDC)
  - Fully-Integrated CMOS Power Amplifiers
  - All-Digital Power Amplifiers

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## Single-Chip Transceiver Systems (I)

- Single-Chip CMOS 900-MHz GSM Transceiver *(completed)*
  - Integrate ALL Building Blocks On-Chip
  - Design in a 0.5-μm Standard Digital CMOS Process
  - Demonstration of Single-Chip GSM Transceiver
  - Highest On-Chip Image Rejection and Smallest Chip Area
- CMOS 1-V 5.2-GHz Wireless Transceiver for WLAN Applications (IEEE 802.11a) *(completed)*
  - System-On-Chip with IQ ADC and DAC
  - Single 1-V Supply
  - Low Power ( < 50 mW for Receiver and Transmitter)
  - Embedded Power-Management Circuitry

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## Single-Chip Transceiver Systems (II)

- Single-Chip CMOS TV Tuners (Cable, DVB-T/H) *(completed)*
  - Frequency Band (54 MHz – 880 MHz)
  - Wide Bandwidth (6 MHz)
  - Novel Single-Conversion Architecture without Tracking Filter
  - Integrate On-Chip 44-MHz Channel-Selection Filter
  - Small Chip Area, Low Power, Low Cost
- CMOS Ultra-Wideband (UWB) Transceiver *(completed)*
  - Frequency Band (3.1 GHz – 10 GHz)
  - Wide Bandwidth (> 500 MHz)
  - High Data Rate and Low Power
  - Single-Chip

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## Single-Chip Transceiver Systems (III)

- Passive UHF 900-MHz RFID Readers and Tags *(completed)*
  - Low Cost, Low Power, Multiple Standards
  - Single-Chip RFID UHF Readers with Wireless Connectivity (WLAN, Bluetooth, Zigbee)
  - System-On-Chip Passive RFID Tags with Advanced Features:
    - Embedded Temperature Sensors
    - Memory (OTP, rewritable)
- WCDMA/WLAN Digital Polar Transmitter with AM Replica Feedback for Linearization (*completed*)
- An 86GHz-94.3GHz (W-Band)Transmitter with 15.3dBm Output Power and 9.6% Efficiency in 65nm CMOS *(completed)*

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## Single-Chip Transceiver Systems (IV)

- Reconfigurable CMOS Software-Defined Transceiver *(on-going)*
  - Frequency band (50 MHz – 10 GHz, 60GHz)
  - Reconfigurable bandwidth (200 KHz – 500 MHz, 2GHz)
  - Reconfigurable performance
- Beyond-60GHz and sub-THz Systems *(on-going)*
  - Dual-band vehicle radar control (22GHz and 77GHz)
  - 60-GHz 4-path phased-array receivers
  - mm-Wave and sub-THz imaging systems
- Envelope-Tracking LTE PAs and Transmitters *(on-going)*
- Energy-Efficient Transceivers and Building Blocks for Biomedical and Implantables *(on-going)*

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## Sing-Chip CMOS Transceivers for Wireless Communications

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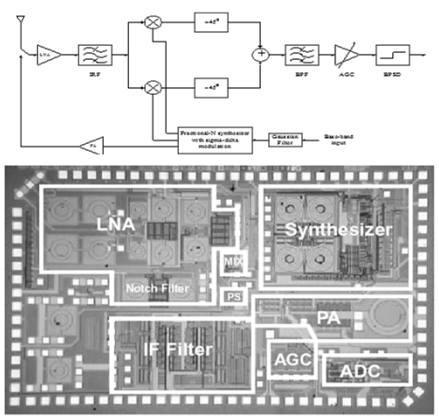
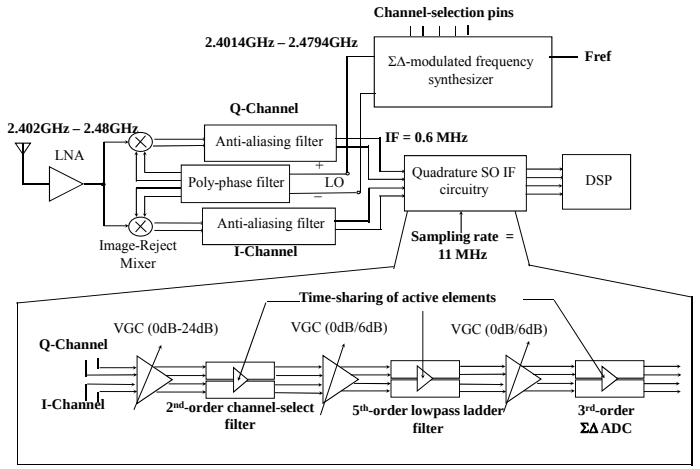
## 900-MHz GSM Transceiver [Guo, JSSC '02]




| | |
|---|---|
| Process | 0.5μm CMOS |
| Sensitivity | -90dBm |
| SNR | 9dB |
| NF | 22dB |
| IIP3 | -25dBm |
| Image Rejection | 79dB |
| Output Power | 55mW |
| PAE | 21% |
| Power Consumption | 227mW |

## 1-V 10-mW Bluetooth Receiver [Cheung, JSSC '03]



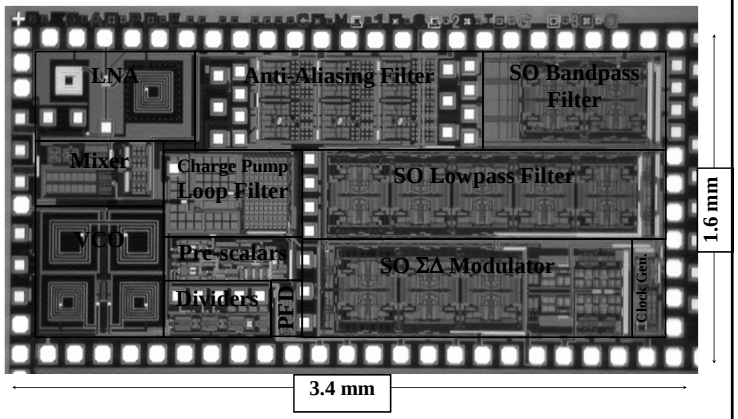



## 1-V 10-mW Bluetooth Receiver [Cheung, JSSC '03]

| | |
|---|---|
| Technology | 0.35-μm double-poly 4-metal CMOS process ($V_{TN}$: 0.6V, $V_{TP}$: -0.77V) |
| Supply Voltage | 1 V |
| Input Frequency | 2.402GHz – 2.480 GHz |
| Channel Bandwidth | 1 MHz |
| Sensitivity | -70 dBm |
| SNR | 18 dB with -70-dBm Input Signal |
| Noise Figure | 26 dB |
| Linearity (IIP3) | - 22 dBm @ Max. Gain |
| Image Rejection | 28 dB |
| Variable-Gain-Control | 0dB to 36dB (6dB per step) |
| Power Consumption | Receiver: 10 mW |
| Chip Area | 3.4 x 1.6 $mm^2$ |

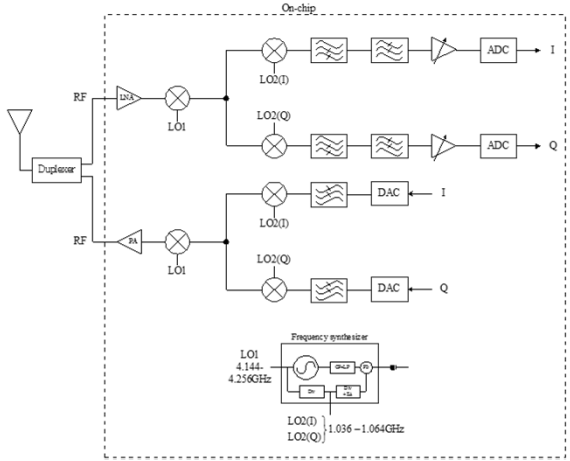


## 1-V 10-mW Bluetooth Receiver [Cheung, JSSC '03]

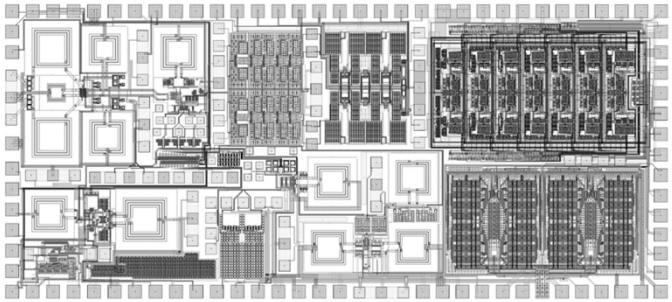





## 1-V 5.2-GHz WLAN 802.11a Transceiver [Leung, JSSC '07]



1-V 5.2-GHz WLAN 802.11a Transceiver [Leung, JSSC '07]



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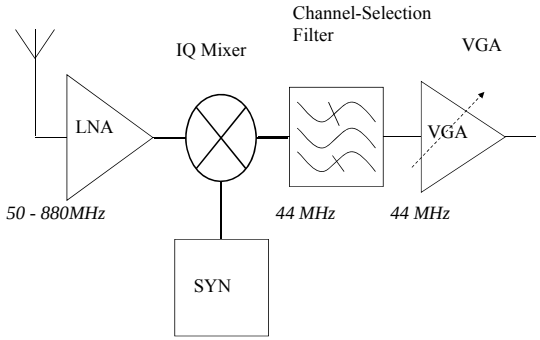
1.8-V 531-mW Single-Chip Single-Conversion CMOS Cable TV Tuner [Wang, A-SSCC'05]

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1-V 5.2-GHz WLAN 802.11a Transceiver [Leung, JSSC '07]

| | Existing Solutions | Proposed Transceiver |
|---|---|---|
| Supply Voltage | ≥ 1.8V | 1.0V |
| Power Consumption | ≥ 150 mW (RX)<br>≥ 180 mW (TX) | < 50 mW (RX)<br>< 50 mW (TX) |
| Chip Area | ≥ 13 $mm^2$ | ~ > 10 $mm^2$ |
| Including Power-Management Circuitry | No | Yes |
| Including ADC & DAC | No | Yes |
| Process | SiGe, BiCMOS, CMOS | CMOS |

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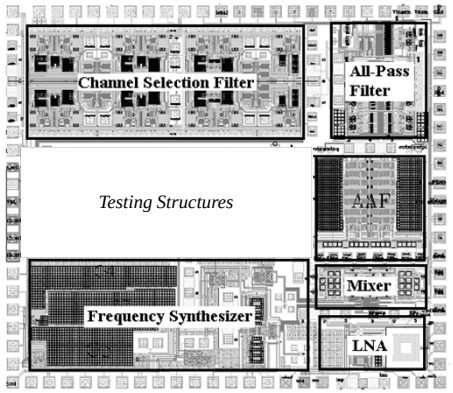
1.8-V 531-mW Single-Chip Single-Conversion CMOS Cable TV Tuner [Wang, A-SSCC'05]

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## 1.8-V 531-mW Single-Chip Single-Conversion CMOS Cable TV Tuner [Wang, A-SSCC'05]

- Novel Single-Conversion Architecture with Image Rejection Larger than 60 dB (without trimming)
- Full Integrated in a CMOS Single-Chip
- Single Frequency Synthesizer with Single Wideband VCO
- Integrated 44-MHz Switched-Capacitor Channel-Selection Filter
- Low Power Consumption (~ 500 mW as compared to ~ > 2.0 W for Existing Solutions)

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## 1.8-V 531-mW Single-Chip Single-Conversion CMOS Cable TV Tuner [Wang, A-SSCC'05]

| | Existing Solutions | Proposed Tuner |
|---|---|---|
| Process | SiGe, BiCMOS, SOI CMOS | CMOS |
| Supply Voltage | ≥ 1.8V | 1.8V |
| Power Consumption | ≥ 2000 mW | ~ 531 mW |
| On-Chip Channel-Selection Filter | No | Yes |
| Chip Area | > 12 $mm^2$ | ~ 7.1 $mm^2$ |

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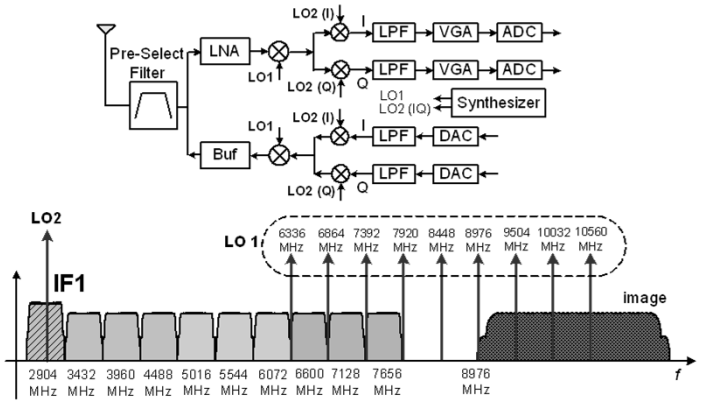
## Proposed UWB Transceiver [Zheng, JSSC '09]

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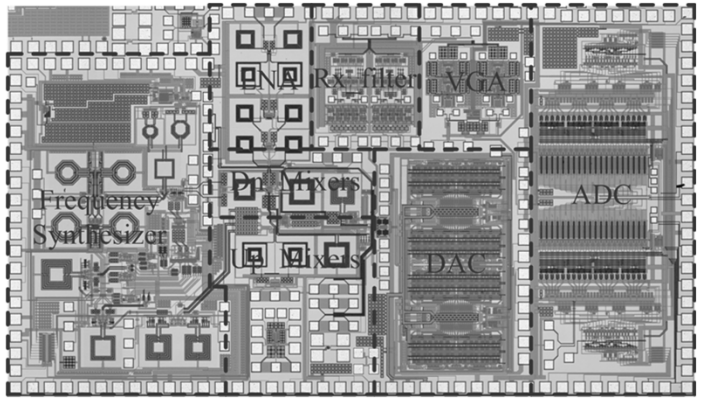


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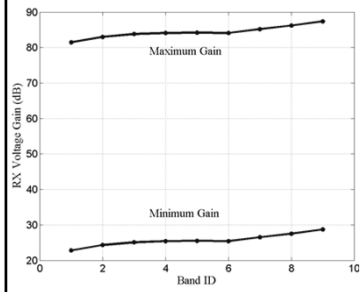
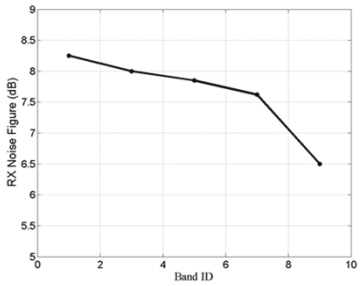
# UWB Receiver - Measurements



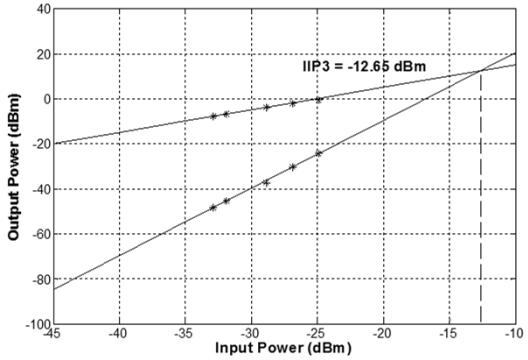

Receiver Gain




Receiver NF



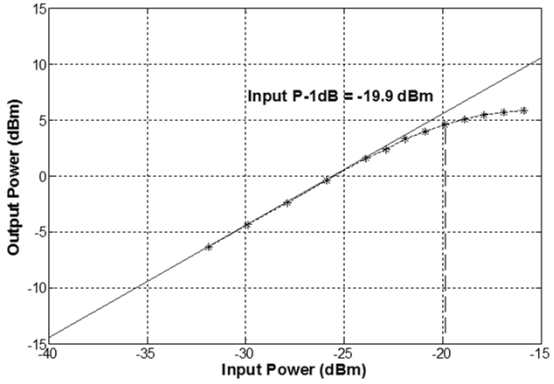
# UWB Receiver - Measurements




IIP3 @ low gain



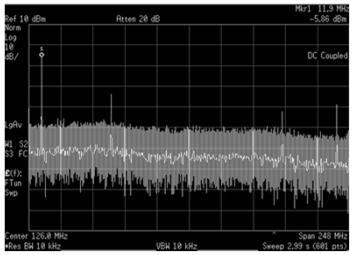
# UWB Receiver - Measurements



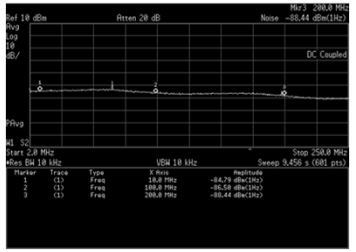

Input P-1dB @ low gain



# UWB Receiver - Measurements



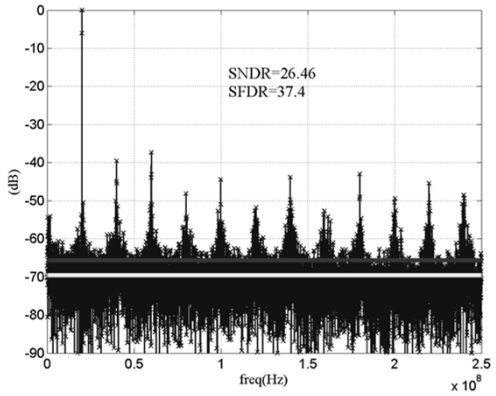
Receiver output spectrum



Noise spectral density

✓Output SNR = -3.34 dB @ LNA Single-ended input power of -82.9 dBm

# UWB ADC – Measurement at 500 Mbps

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# UWB Transceiver's Performance [Zheng, JSSC '09]

| | Band Group 1 (3.1 – 4.75 GHz) | Band Group 2 (4.75 – 6.3 GHz) | Band Group 3 (6.3 – 7.9 GHz) |
|---|---|---|---|
| **Receiver** | | | |
| Voltage Gain (dB) | >81.5 | >84.1 | >85.2 |
| NF (dB)* | 8.12 | 7.85 | 7.04 |
| S11 | < -13 | < -18 | <-20 |
| In-Band IIP3 (dBm)** | -12.65 | -13.7 | |
| Input P-1dB (dBm)** | -19.9 | -21.7 | -22.6 |
| In-Band IIP2 (dBm) | 22 | | |
| **Transmitter** | | | |
| Output P-1dB (dBm) | -9.3 | -9.2 | -10 |
| Output Sideband Rejection (dBc) | <-33.3 | <-33.9 | <-33.6 |
| **Synthesizer** | | | |
| PN @ 10MHz (dBc/Hz) | < -129.7 | < -127.3 | < -126.7 |
| LO Sideband Rejection (dBc) | < -36 | < -28 | < -27.9 |
| **Other Parameters** | | | |
| Supply Voltage | 1.8 V | | |
| Current Consumption (mA) | 101 mA (RX w/o ADC); 20 mA (TX w/o DAC)<br>57 mA (Synthesizer)<br>109 mA (IQ ADC); 20 mA (IQ DAC) | | |
| Process | TSMC 0.18-μm CMOS | | |
| Chip Area | 5.2×2.94 mm² | | |

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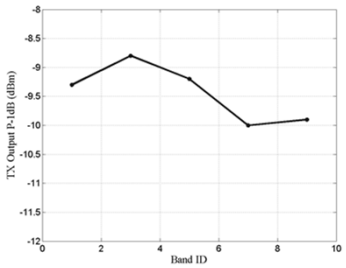
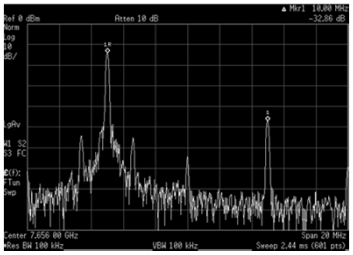
# UWB Transmitter – Measurements



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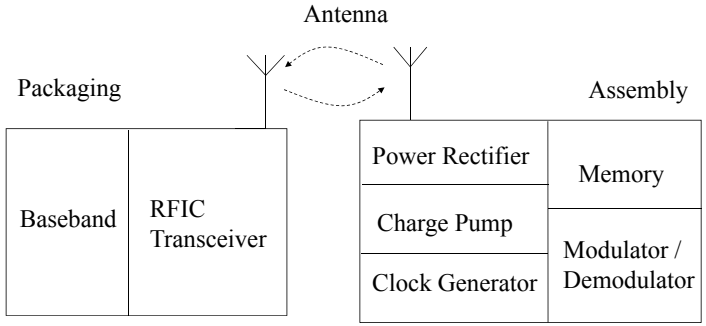
# Passive UHF RFID System Block Diagram




*RFID Reader / Interrogator*

*RFID Tag / Transponder*

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## Passive UHF RFID Reader - Specification

| System Parameters | Specification | |
|---|---|---|
| Standard | EPC G2 | |
| Transmitter channel bandwidth | 500 KHz for US | 200 KHz for Europe |
| Frequency range | 860 MHz – 960 MHz | |
| BER | $10^{-3}$ | |
| Output SNR | 7 dB | |
| Sensitivity | -90 dBm | |
| Maximum input signal | -10 dBm | |
| Noise Figure | < 9 dB | |
| Linearity (IIP3) | -1 dBm | |
| Maximum gain | 96 dB | |
| Phase noise of LO | -117dBc/Hz @ 100kHz | |
| Output power | 10 dBm – 20 dBm (32 steps) | |
| Supply voltage | 1V or 1.8V if necessary | |

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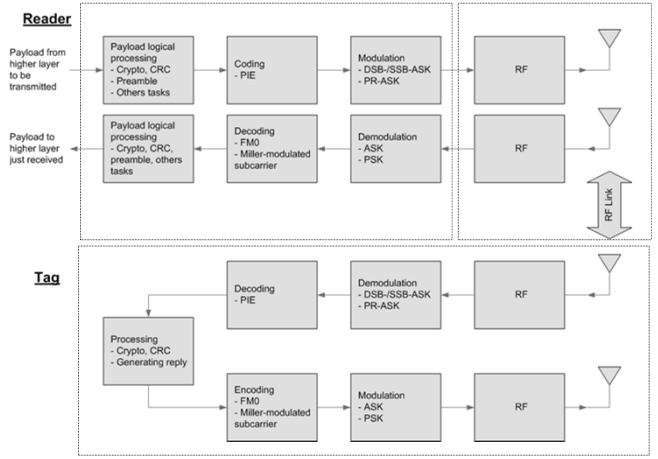
## Passive UHF RFID System Block Diagram

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## Passive UHF RFID Tag - Specification

| System Parameters | Specification | |
|---|---|---|
| Standard | EPC G2 | |
| Transmitter channel bandwidth | 500 KHz for US | 200 KHz for Europe |
| Frequency range | 860 MHz – 960 MHz | |
| Minimum input power | ~ 50 µW | |
| Minimum reflected power | ~ - 90 dBm | |
| Read/Write Distance | ~ 3 m - 10 m | |

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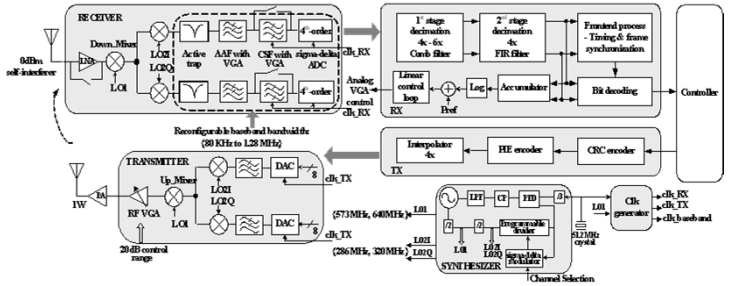
## Single-Chip RFID Reader's Architecture – Transceiver + Digital Baseband [Wang, JSSC '08]

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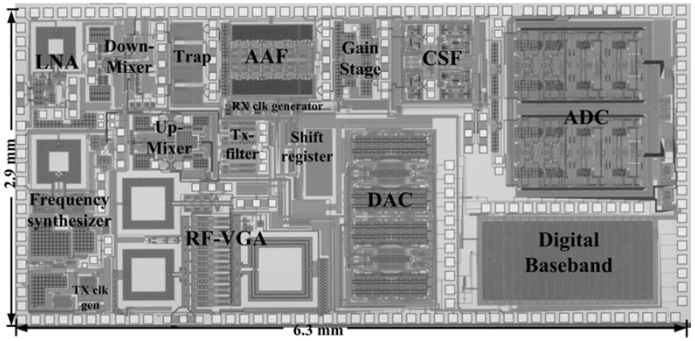
## RFID Reader with Baseband [Wang, JSSC '08]




*Process: 0.18-μm CMOS, Chip Area: ~ 2.9 mm x 6.3 mm*

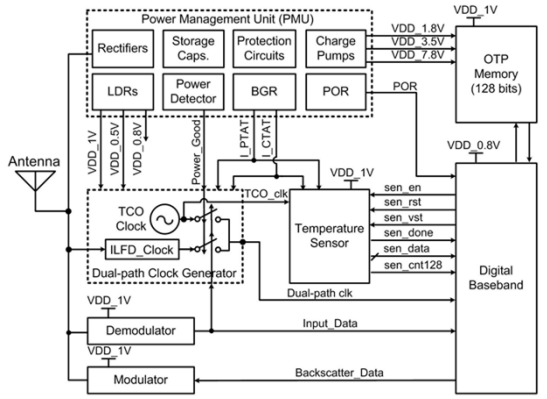


## RFID Reader's Performance [Wang, JSSC '08]

| | | | |
|---|---|---|---|
| Operating Frequency | | 860 MHz to 960 MHz | |
| RX's channel bandwidth | | 80 KHz to 1.28 MHz | |
| RX's noise figure (dB) | | BW=1.28 MHz | **13.4** |
| | | BW=640 KHz | **15.1** |
| | | BW=320 KHz | **17.4** |
| RX's IIP3 (dBm) | | BW=1.28 MHz | **–4.5** |
| | | BW=640 KHz | **–5** |
| | | BW=320 KHz | **–6** |
| RX's gain | | 14 dB to 77 dB | |
| RX front-end's input P-1dB | | –9.4 dBm | |
| TX's side-band rejection | | –33 dBc | |
| TX's output P-1dB | | w/ external PA | **>30 dBm** |
| | | w/o external PA | **10.4 dBm** |
| Synthesizer's phase noise | | –110dBc/Hz @ 200kHz (from 880MHz) | |
| Power dissipation | Receiver | Max ($f_{clk}$=40.96MHz, CSF on, ΣΔ ADC 4th-order) | **153.8 mW** |
| | | Min ($f_{clk}$=2.56MHz, CSF off, ΣΔ ADC 2nd-order ) | **80.6 mW** |
| | Transmitter | 136 mW | |
| | Synthesizer | 7.4 mW | |

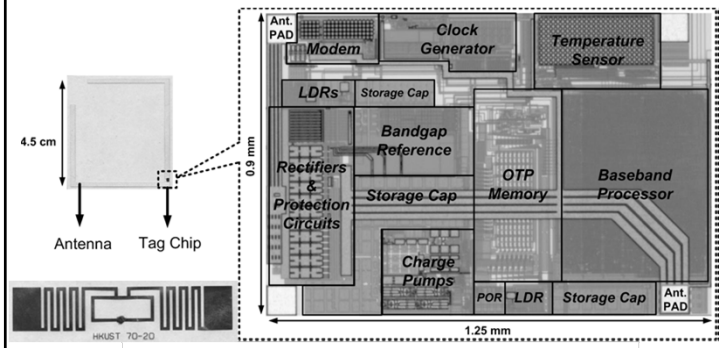


## System-On-Chip Passive UHF RFID Tag with Temperature Sensor [Yi, ISSCC '10]



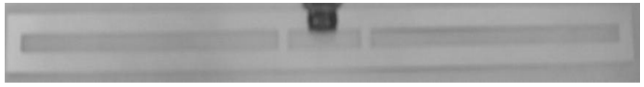


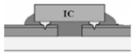

## System-On-Chip Passive UHF RFID Tag with Temperature Sensor [Yi, ISSCC '10]



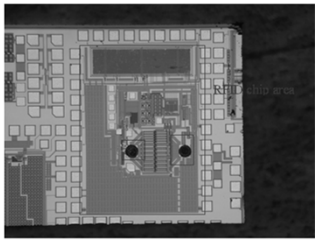

*Process: 0.18-μm CMOS, Chip Area: 0.9 mm x 1.25 mm*

# RFID Tag's Assembly

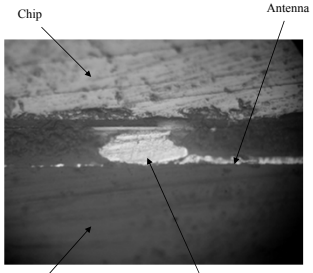





Schematic of Au stub bump flip chip



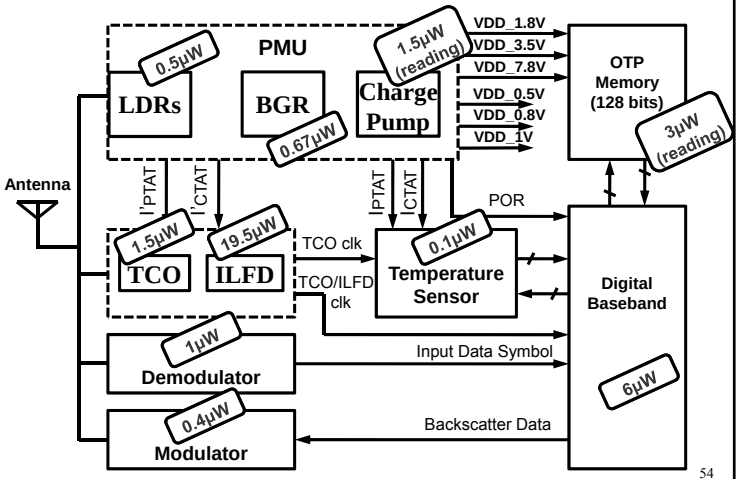

Au stub bumped RFID chip




Au stub bump and silver paste antenna



# Power Breakdown





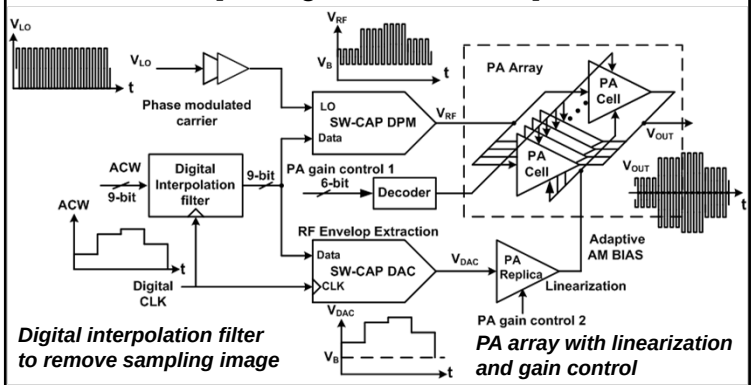

# Performance Summary

| | Cold-Chain Tag | Human-Body Tag |
|---|---|---|
| Process | 0.18 μm CMOS | 0.18 μm CMOS |
| Tag Chip Area | 1.1 mm$^2$ | 1.2 mm$^2$ |
| Frequency | 860-960 MHz | 860-960 MHz |
| Memory Size | 512 bits | 512 bits |
| Sensing Sensitivity | -7.0 dBm | -4.4 dBm |
| Sensing Distance (EIRP 4W) | 4.0 m | 3.0 m |
| Temperature Range | -40 to 60 $^o$C | 35 to 45 $^o$C |
| Sensing Step | 0.3 $^o$C | 0.05 $^o$C |
| Sensing Error | -1.2 $^o$C /+ 0.9 $^o$C | - 0.15 $^o$C / +0.05 $^o$C |



# Proposed Digital Polar TX

[Zheng, JSSC 7/2015]

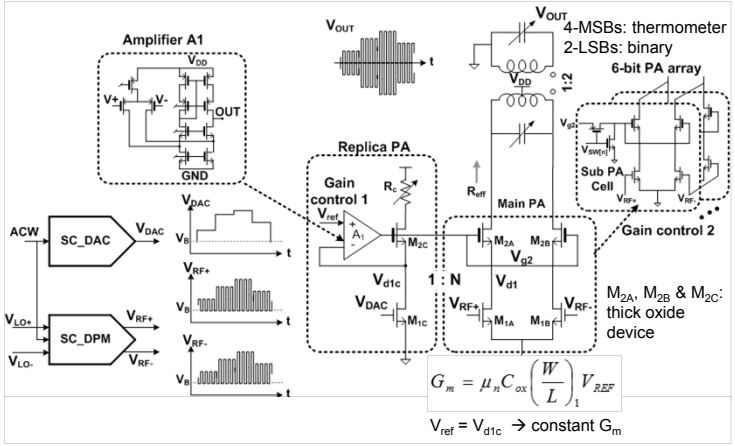



***Digital interpolation filter to remove sampling image***

***PA array with linearization and gain control***

***SW-CAP DPM and DAC***

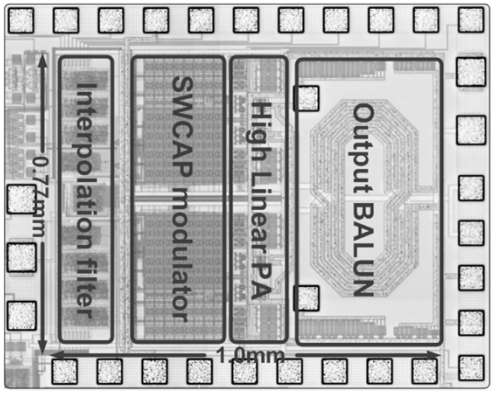
# Proposed PA Linearization




$$G_m = \mu_n C_{ox}\left(\frac{W}{L}\right)_1 V_{REF}$$



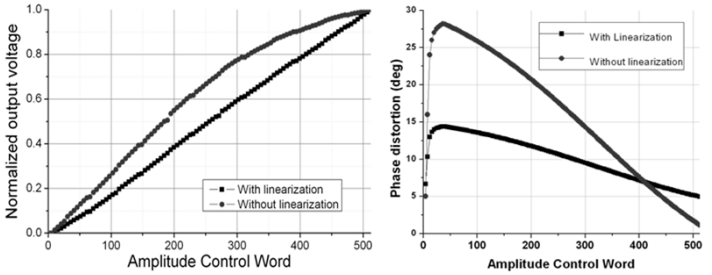
# Proposed DPA – Die Photo




- 65nm 1P6M CMOS with active area 1.0mm x 0.77mm



# Measured AM-AM and AM-PM Distortion

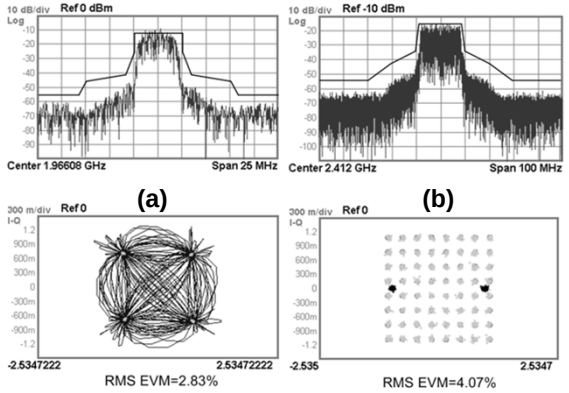



| Linearization | AM-AM INL error | AM-PM distortion |
|---|---|---|
| Off | 18.6% | 27.1° |
| On | 3.2% | 9.6° |

* Measured w/ a 2GHz carrier and maximum power of 13dBm

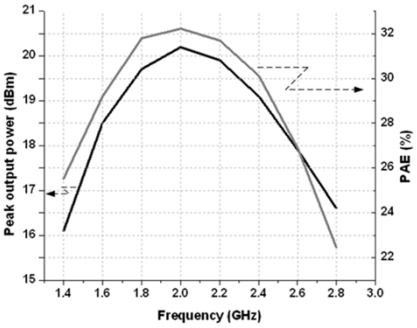


# Measured Emission Mask and EVM




(a) WCDMA, (b) WLAN 802.11b/g 54Mbps 64-QAM OFDM

## Output Power, Efficiency, Power




| Block | Supply [V] | Power [mW] |
|---|---|---|
| Digital Filter | 1.2 | 2.5 |
| SW-CAP DAC | 1.2 | 2.5 |
| DPM | 1.2 | 10 |
| LO Buffer | 1.2 | 12 |
| Replica Bias | 2 | 12 |
| PA array | 2 | 16 |
| Total | -- | 55mW |

for 0-dBm output power

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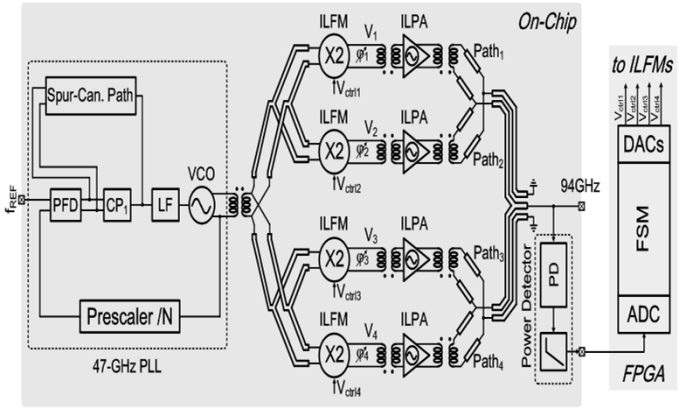
## Proposed W-Band Transmitter
[Chao, ISSCC 2016]

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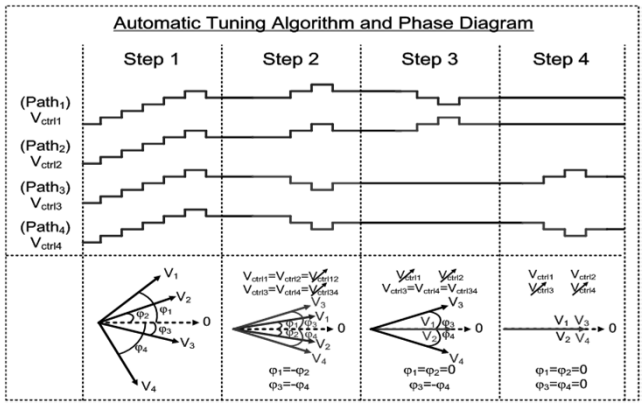
## Summary and Comparison

| Reference | Presti *JSSC* 10/07 | Yoo *JSSC* 12/11 | Chowdhury *JSSC* Aug 11 | This work |
|---|---|---|---|---|
| Technology | 0.13um CMOS SOI | 90nm CMOS | 65nm CMOS | 65nm CMOS |
| Frequency [GHz] | 0.8~2 | 1.8~2.8 | ~2.25 | 1.5~2.7 |
| Supply [V] | 1.2~2.1 | 1.5/3 | 1 | 1.2/2 |
| Modulation | EDGE / WCDMA / WiMAX | 20M-WLAN | 20M-WLAN | WCDMA / 20M-WLAN |
| Predistortion | Yes | Yes | Yes | No |
| EVM (RMS) | 1.53% (5M WiMAX) | 2.6% | 4.0% | 2.8%(WCDMA) 4.1% (WLAN) |
| Output Matching Network | Off-chip | Off-chip | On-chip | On-chip |
| Peak Output Power [dBm] | 25 | 25.2 | 21.7 | 20.4 |
| Peak PAE | 47% | 45% | 36% | 32.3% |

## Proposed Automatic Phase Calibration Algorithm

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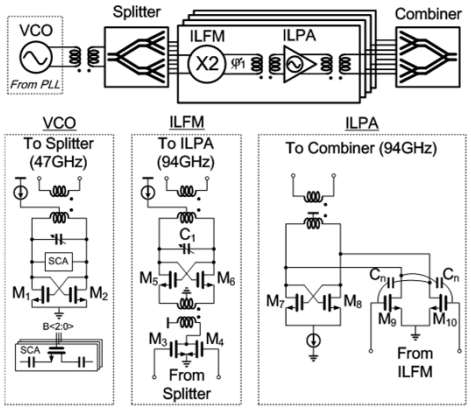
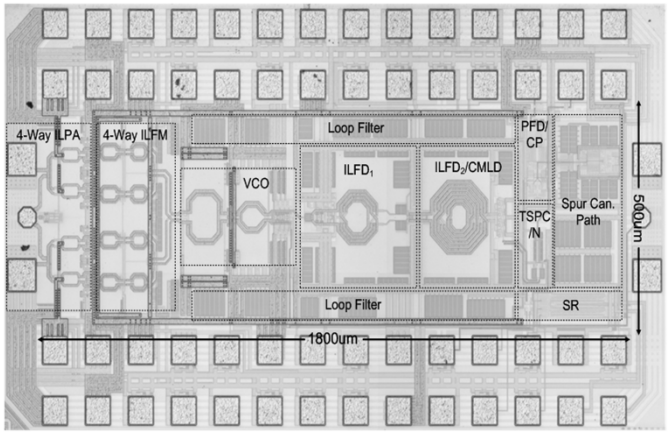
## Proposed W-Band Transmitter - Building Block Implementation



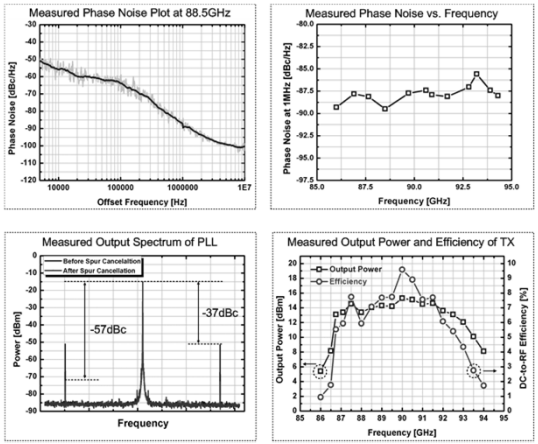



## Proposed W-Band Transmitter – Die Photo






## Proposed W-Band Transmitter - Measurements






## Synthesizer – Summary and Comparison

| | This work | Tsai, ISSCC 2009 | Xu, RFIC 2010 | Voinigescu, JSSC 2011 | Wang, TMTT 2012 |
|---|---|---|---|---|---|
| Freq. [GHz] | 90.2 | 96 | 74 | 89 | 96 |
| Type | Sub-harmonic | Fundamental | Fundamental | Fundamental | Sub-harmonic |
| Division Ratio | 512 | 256 | 1024 | 128 | 768 |
| Loop BW. | 100kHz | 2MHz | 300kHz | 1.72MHz | 1MHz |
| Locking Range | 9.2% | 1.5% | 10.8% | 6.7% | 10.9% |
| PN @ 1MHz [dBc/Hz] | -89.5 | -76 | -83 | -82 | -92 |
| Spur [dBc] | -57 | -51 | -49 | N/A | -52 |
| Supply [V] | 1.2 | 1.2/1.3 | 1 | 1.8/2.5 | 1.8/2.5 |
| Power [mW] | 69.7[1] | 43.7 | 65 | 550 | 140 |
| FoM[2] [dBc/Hz] | -170.2 | -159.2 | 162.3 | -153.6 | -170.1 |
| Technology | CMOS 65nm | CMOS 65nm | CMOS 65nm | SiGe 130nm | SiGe 130nm |

[1] including the power of PLL and one ILFM for fair comparison

[2] FoM=PN+20lg($f_{osc}/f_{offset}$)+10lg($1/P_{diss,mW}$)

## Transmitter – Summary and Comparison

| Ref. | Tech. | Freq. [GHz] | LO | PN [dBc/Hz] | $P_{out}$ [dBm] | $P_{dc}$ [mW] | h [%] | VDD [V] | Area [mm$^2$] |
|---|---|---|---|---|---|---|---|---|---|
| ISSCC 2009 Kawano | CMOS 90nm | 73.5 - 77.1 | VCO | -86 (1MHz) | 6.3 | 660 | 0.6 | 1.2 | 0.36[1] |
| JSSC 2010 Lee | CMOS 65nm | 75.6 - 76.3 | PLL | -85 (1MHz) | 5.1 | 188 | 1.7 | 1.2 | n/a |
| ISSCC 2010 Sandstrom | CMOS 65nm | 75-95 | Off chip | n/a | 6.6 | 120 | 3.8 | 1.2 | 1.2 |
| CICC 2011 To | CMOS 65nm | 74-84 | VCO | -87 (1MHz) | 13.5 | 420 | 5.3 | 1 | 1.8 |
| VLSI 2013 Huang | CMOS 65nm | 77 | PLL | -83 (1MHz) | 9 | n/a | n/a | 1.2 | n/a |
| JSSC 2013 Arbabian | SiGe 130nm | 87-97 | PLL | -102 (1MHz) | <13[2] | 898 | 2.2 | 1.2-4 | n/a |
| ISSCC 2014 Giannini | CMOS 28nm | 71-84 | ILO | n/a | 11 | 121 | 10.4 | 0.9 | 1.32 |
| TMTT 2014 Adnan | CMOS 65nm | 99-110 | VCO | -92.8 (1MHz) | 4.5 | 54 | 5.3 | 1.2 | 0.23[1] |
| VLSI 2014 Chen | 65nm CMOS | 92.2 | VCO | n/a | 5 | 112 | 2.9 | 1.2 | 0.55[1] |
| This work | 65nm CMOS | 86 - 94.3 | PLL | -89.5 (1MHz) | 15.3 | 353.3 | 9.6 | 1.2 | 0.9[1] |

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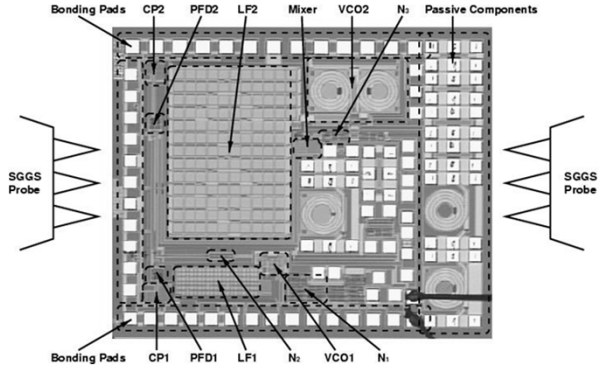
## Dual-Loop GSM Synthesizer [Yan, JSSC '01]

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# Fully-Integrated CMOS RF Frequency Synthesizers

## Dual-Loop GSM Synthesizer [Yan, JSSC '01]

| Design | [Craninckx 98] | [Ali 96] | [Parker 98] | This Work |
|---|---|---|---|---|
| Architecture | Fractional-N | Fractional-N | Fractional-N | Dual-Loop |
| Process | 0.4-µm CMOS | 25-GHz BJT | 0.6-µm CMOS | 0.5-µm CMOS |
| Carrier Frequency | 1.8 GHz | 900 MHz | 1.6 GHz | 900 MHz |
| Channel Spacing | 200 kHz | 600 kHz | 600 kHz | 200 kHz |
| Reference Frequency | 26.6 MHz | 9.6 MHz | 61.5 MHz | 1.6 & 205 MHz |
| Loop Bandwidth | 45 kHz | 4 kHz | 200 kHz | 40 & 27 kHz |
| Chip Area | 3.23 mm$^2$ | 5.5 mm$^2$ | 1.6 mm$^2$ | 2.64 mm$^2$ |
| 600-kHz Phase Noise | -121 dBc/Hz | -116.6 dBc/Hz | -115 dBc/Hz | -121.83 dBc/Hz |
| Spurious Level | -75 dBc | < -110 dBc | -83 dBc | -79.5 dBc |
| Switching Time | < 250 µs | < 600 µs | N. A. | < 830 µs |
| Supply Voltage | 3 V | 2.7 to 5 V | 3 V | 2 V |
| Power | 51 mW | 50 mW | 90 mW | 34 mW |

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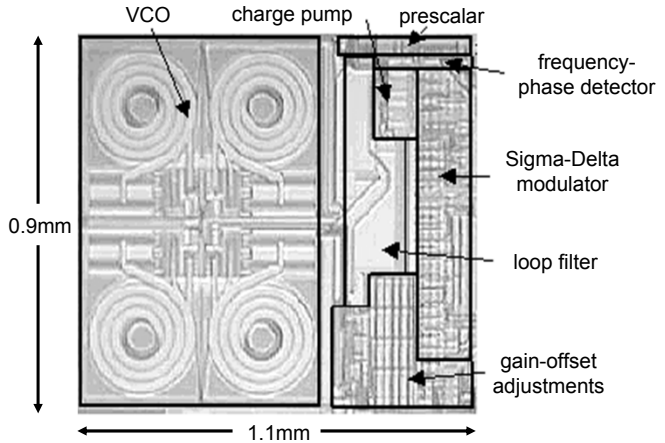
## Fractional-N GSM Synthesizer [Lo, JSSC '02]



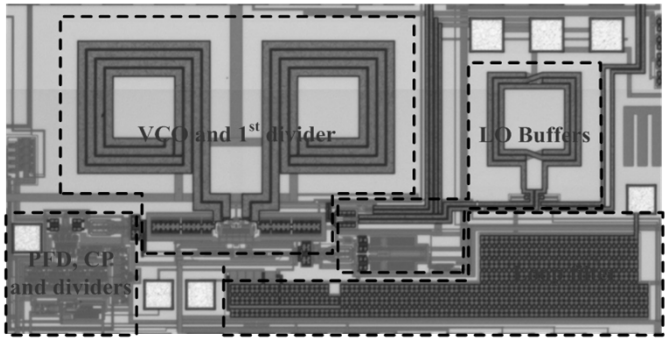



## Fractional-N GSM Synthesizer [Lo, JSSC '02]

| | JSSC 98 Steyaert | JSSC 96 Tham | This work |
|---|---|---|---|
| Center frequency | 1.8GHz | 900MHz | 900MHz (857.6-922.8MHz) |
| Channel spacing | 200kHz | 600kHz | 200kHz (25kHz min) |
| No. of Channel | 124 | 41 | >124 |
| Process | 0.4μm CMOS | 25GHz BJT | 0.5μm CMOS |
| Architecture | FN | FN | FN & SCA |
| Supply voltage | 3V | 2.7-5V | 1.5V |
| Power consumption | 51mW | 50mW | 30mW |
| Reference Freq. | 26.6MHz | 9.6MHz | 25.6MHz |
| Chip area | 3.23mm$^2$ | 5.5mm$^2$ | 0.99mm$^2$ |
| On chip filter | Yes | No | Yes |
| Loop Bandwidth | 45kHz | 4kHz | 80kHz |
| Phase noise@600kHz | -121dBc/Hz | -116.6dBc/Hz | -118dBc/Hz |
| Spurs | -75dBc | <-110dBc | -67dBc |
| Switching time | <250μsec | <600μsec | 150μsec |



## 1-V 5.2-GHz CMOS Synthesizer for WLAN Applications (802.11a) [Leung, JSSC '07]

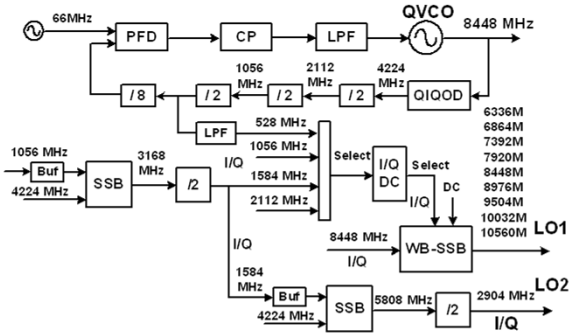





## 1-V 5.2-GHz CMOS Synthesizer for WLAN Applications (802.11a) [Leung, JSSC '07]

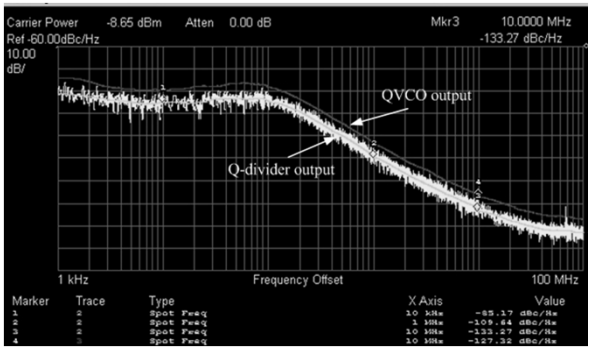
| | [D. Su, JSSC '02] | [P. Zhang, ISSCC '03] | [G. Leung, JSSC '04] | **This work** |
|---|---|---|---|---|
| Supply (V) | 2.5 | 1.8 | 1 | 1 |
| Process (μm) | 0.25 | 0.18 | 0.18 | 0.18 |
| Frequency (GHz) | 4.13 - 4.27 | 5.15 - 5.35 | 5.45 - 5.65 | 4.11 - 4.35 |
| Phase noise (dBc/Hz @ 20MHz) | -138 | -139 | -137 | -139 |
| Spurs (dBc) | NA | -66 @13.3MHz | -80 @11MHz | -63 @16MHz |
| Area (mm$^2$) | NA | NA | 0.99 | 1.28 |
| Power (mW) | 180 | 56 | 27.5 | **9.68** |

## UWB Synthesizer [Zheng, JSSC '07]





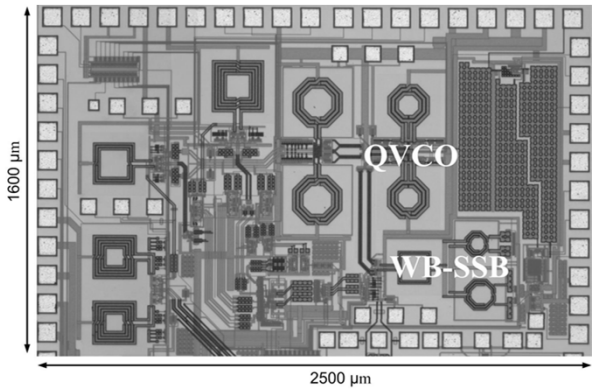

## UWB Synthesizer - Phase Noise Plot




- Integrated PN: 4.4 degree at QVCO output
- PN at QIQO divider output: 6 dB lower



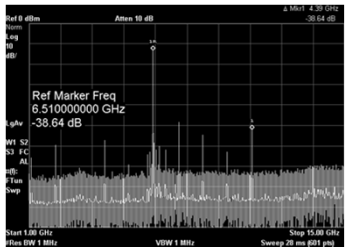
## UWB Synthesizer [Zheng, JSSC '07]



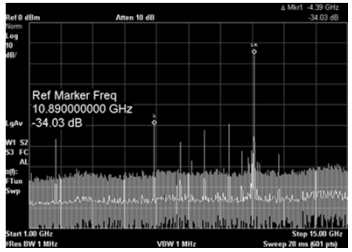

- Fabricated in TSMC 0.18-µm process with 6 metal layers



## UWB Synthesizer – LO1 Spectrum

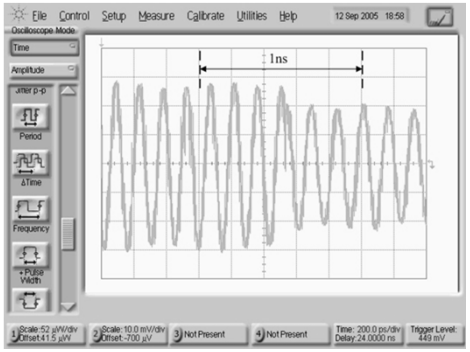



- Lowest band: Sideband rejection - 38.6 dB




- Highest band: Sideband rejection - 34 dB

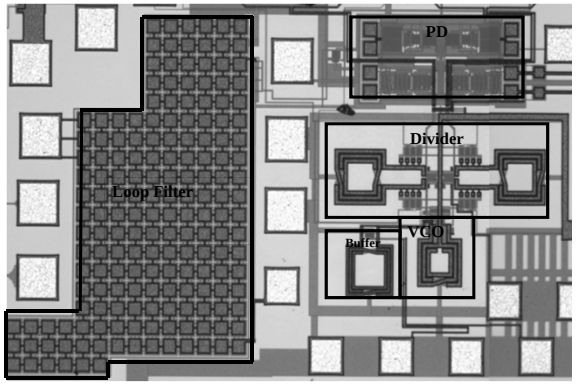
## UWB Synthesizer - Switching Time




- Measured switching plot from 6.864 to 6.336 GHz
  - Switching time < 1ns



## 1-V 24-GHz Phase-Locked Loop [Ng, JSSC '06]



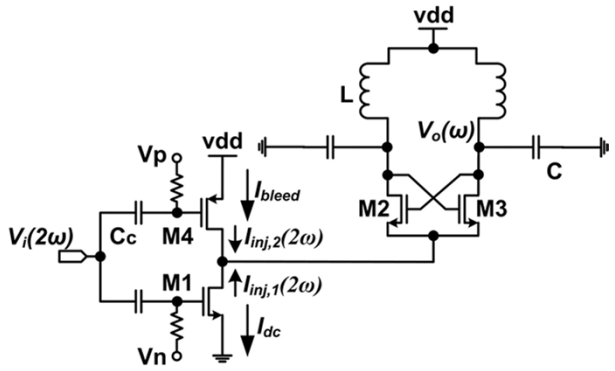



## 1-V 24-GHz Phase-Locked Loop [Ng, JSSC '06]

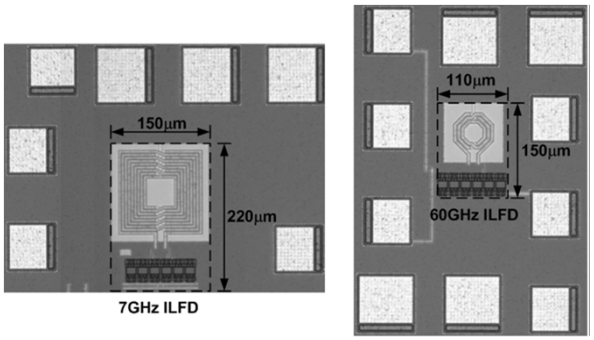
| | Measurement Result |
|---|---|
| Technology | TSMC 0.18$\mu$m CMOS |
| Supply Voltage | 1V |
| Power Consumption | Total: 17.5mW<br>VCO + Divider: 14.5mW<br>PD: 3mW |
| Frequency | 24.2GHz |
| VCO tuning range | 6% |
| VCO phase noise | -119.4dBc/Hz@10MHz |
| PLL in-band Phase Noise | -106.3dBc/Hz@100kHz |
| PLL out-band Phase Noise | -119.1dBc/Hz@10MHz |
| Active Core Area | 0.55 mm$^2$ |



## 7-GHz and 60-GHz Dividers with Enhanced Locking Rang – Block Diagram [Rong, ISSCC '09]



## 7-GHz and 60-GHz Dividers with Enhanced Locking Rang – Chip Photo [Rong, ISSCC '09]




- 7GHz and 60GHz prototypes in 0.13-μm CMOS
- Core area: 0.033mm$^2$ (7GHz), 0.0165mm$^2$ (60GHz)



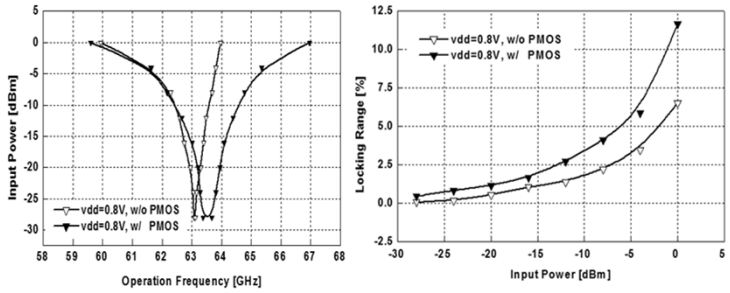
## 60-GHz Dividers– Summary [Rong, ISSCC '09]

| | Tech. | Freq. [GHz] | Input Power [dBm] | Locking Range [GHz]/[%] | Supply Voltage [V] | Power [mW] | FOM$^2$ |
|---|---|---|---|---|---|---|---|
| T. Shibasaki JSSC 03/08 | 90nm CMOS | 20 | 4 | 5.1/25.5 | 1.2 | 3.2[1] | 1.6 |
| Q. Gu JSSC 04/08 | 90nm CMOS | 57 | 0 | 7.4/13.0 | - | 2.5[1] | 3.0 |
| J.-C. Chien ISSCC 07 | 0.18μm CMOS | 40 | 0 | 10.6/26.5 | 1.0 | 6 | 1.8 |
| K.-H. Tsai ISSCC 08 | 90nm CMOS | 90 | 0 | 11/12.2 | 1.2 | 3.5 | 3.1 |
| A. Mazzanti JSSC 09/04 | 0.18μm CMOS | 4 | 0 | 0.6/15 | 1.8 | 3.6 | 0.2 |
| Proposed ILFD-1 | 0.13μm CMOS | 7 | 0 | **2.4/34.3** | **0.8** | **0.9** | **2.7** |
| Proposed ILFD-2 | 0.13μm CMOS | 63 | 0 | **7.4/11.7** | **0.8** | **1.6** | **4.6** |

1. 1/2 x power reported for quadrature-output divider
2. 2. FOM=Locking range [GHz] / Power consumption [mW]



## 60-GHz Dividers with Enhanced Locking Rang – Input Sensitivity [Rong, ISSCC '09]

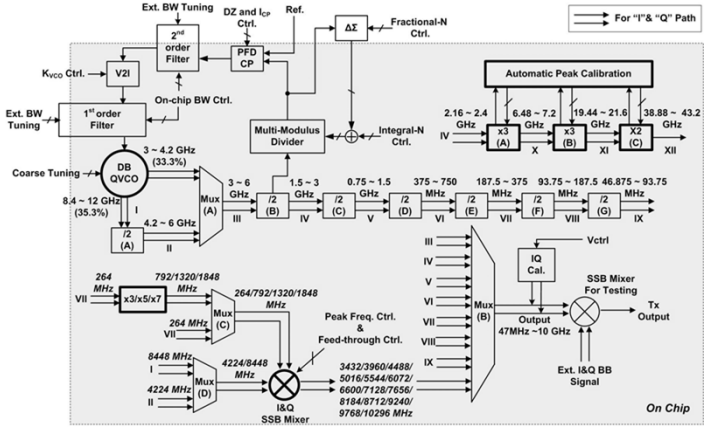



Locking range (0dBm input power, 2mA from 0.8V):

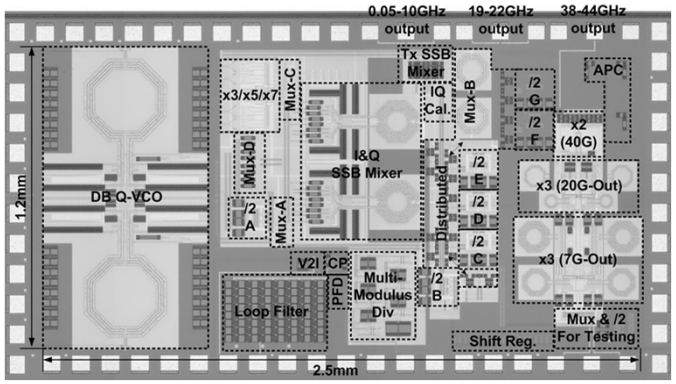
- Without PMOS: 59.93GHz ~ 63.97GHz (6.5%)
- With PMOS: 59.60GHz ~ 66.96GHz (11.6%)



## Proposed SDR Synthesizer – Block Diagram [Rong, ISSCC '11]



## SDR Synthesizer – Chip Photo [Rong, ISSCC '11]




Fabricated in 0.13um 1P6M CMOS: 2.5 mm x 1.2 mm

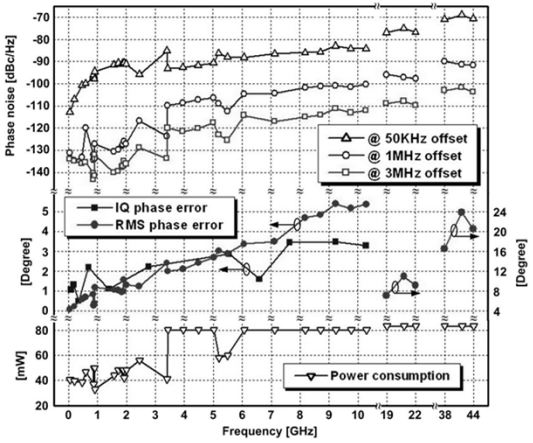


## SDR Synthesizer - Summary [Rong, ISSCC '11]

| Reference | [Koukab, JSSC, 7/06] | [Borremans, JSSC, 12/08] | [Yu, RFIC, 6/09] | [Razavi, JSSC, 8/10] | [Osmany, JSSC, 9/10] | This work |
|---|---|---|---|---|---|---|
| Output Frequencies [GHz] | 0.8~1.1<br>1.5~2.1<br>2.3~3.1<br>4.7~6.2 | 0.8~1<br>1.6~2<br>2.2~2.8<br>4.4~5.6 | 0.125~<br>26 | 1.4/1.8/2.0/<br>2.2/2.3/2.9/<br>3.5/4.4/4.7/<br>5.8/7.0/8.8 | 0.6~4.6<br>5~7<br>10~14<br>20~28 | **0.047~10<br>19~22<br>38~44** |
| In-band phase noise @ 10KHz ($f_c$=1.7GHz) [dBc/Hz] | -79.8 | N/A | -91.6 | N/A | -109.9[4] | **-91~-98** |
| Out-band phase noise @ 3MHz ($f_c$=1.7GHz) [dBc/Hz] | -138.5 | -129.6[3] | -137.2[34] | -129.8 | -136.5[34] | **-139.6** |
| Power [mW] | 6.2<br>(VCO) | 60 | 1283 | 31 | 680 | 33~83 |
| Area [mm$^2$] | 2.55 | 0.06 | 4.4 | 0.29 | 4.8 | 3.0 |
| Technology | 0.25μm<br>BiCMOS | 90nm<br>CMOS | 0.18μm<br>BiCMOS | 90nm<br>CMOS | 0.25μm<br>BiCMOS | 0.13μm<br>CMOS |

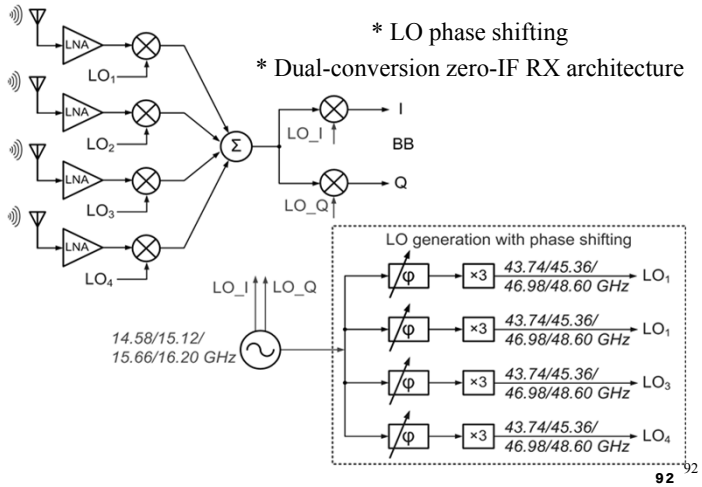


## SDR Synthesizer - Measurements [Rong, ISSCC '11]

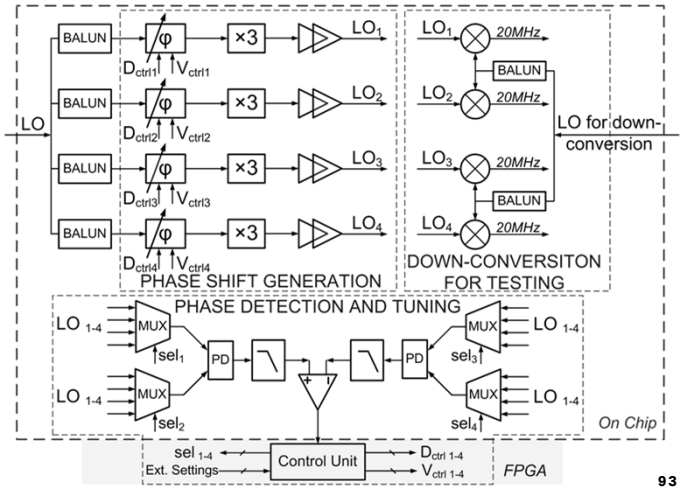





## 4-Path 60-GHz Phased-Array Receiver

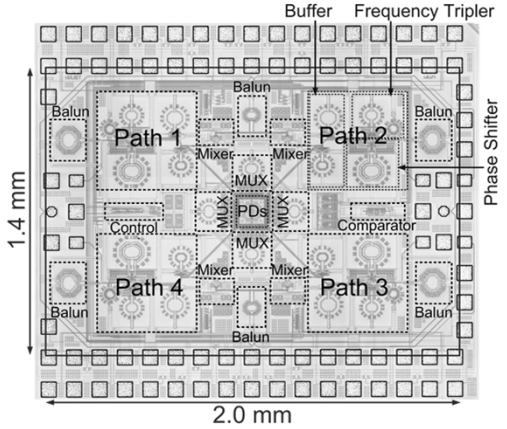


## 4-Path LO Generation System [ISSCC '12]






## LO Generation - Chip Micrograph [ISSCC '12]




- Fabricated in 65nm 1P6M CMOS (core area: 2.0×1.4 mm$^2$)



## LO Generation - Key Features [ISSCC '12]

- System architecture and design techniques:
  - Frequency tripler in LO path to reduce the linear phase range required for phase shifter
  - Linear phase shifter based on injection-locked oscillator
  - Locking range enhancement for frequency tripler
  - Automatic successive phase tuning without dedicated reference voltages for phase detection
- LO generation measures phase resolution of 22.5° and phase error < 1.5° with amplitude variations < ±0.35dB.



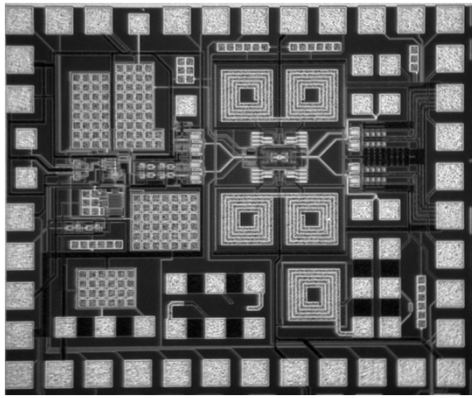
## LO Generation - Summary & Comparison

| Ref. | Natarajan JSSC '06 | Scheir JSSC '08 | Hashemi TMTT '05 | Chan ISSCC '10 | This work |
|---|---|---|---|---|---|
| Frequency [GHz] | 50.3 ~ 55.5 | 43.7 ~ 51.7 | 18.8 ~ 21.0 | 57.0 | 42.8 ~ 49.5 |
| Amplitude Mismatch [dB] | 1.5 | -4.0 ~ 1.6 | N/A | N/A | **± 0.35** |
| Phase Resolution [°] | N/A | 45.0 | 22.5 | N/A | **22.5** |
| Phase Error [°] | 0.5 * | 5.7 | N/A | N/A | **< 1.5** |
| Path Number | 4 | 2 | 8 | 4 | 4 |
| Supply [V] | 2.5 | 1.2 | 2.5 | 1.0 | **1.0** |
| Current [mA] | 56 | 28.7 | 76.4 ** | 310 | 55 (core)<br>30 (auto. tuning) |
| Technology | 120nm SiGe BiCMOS | 90nm CMOS | 180nm SiGe HBT CMOS | 65nm CMOS | 65nm CMOS |

* Simulation for 5-bit DAC
** Including a phased-locked loop

# IC Development Projects and Industrial Contracts

## A 1-V 2.5-GHz Phase-Locked Loop



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## Industrial Collaboration and Support

- Integrated-Circuit Industrial Consortium (http://ic2.ee.ust.hk/)
- Patents and Intellectual Properties on IC Modules and Systems Available for Licensing and Technology Transfer
- Provide IC Design Services and Support:
  - IP Licensing
  - Consultancy, Workshop, and Engineer Training
  - Engineer-In-Residence Program
  - Work on IC Technology Transfer and Product Development:
    - 1-V 2.5-GHz PLL *(Completed)*
    - 488-MHz Synthesizer *(Completed)*
    - 2.4-GHz Low-Phase-Noise PLL *(Completed)*
    - 22GHz–44GHz Low-Phase-Noise Synthesizer *(Completed)*
    - Passive RFID Tag with Temperature Sensor *(On-going)*
    - MEMS Oscillators and Clock Generators *(On-going)*

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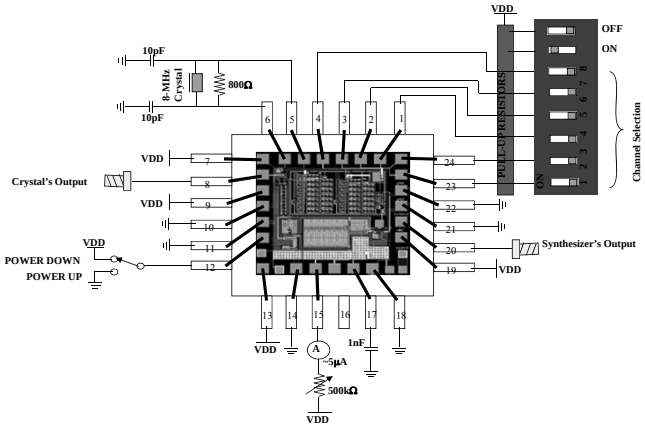
## A CMOS 488-MHz Frequency Synthesizer

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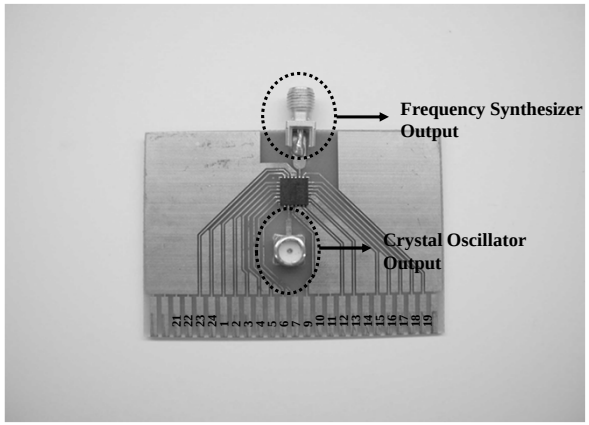
## A CMOS 488-MHz Frequency Synthesizer

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## A CMOS 488-MHz Frequency Synthesizer

| | | |
|---|---|---|
| Supply Voltage | | 2.7V - 3.3V |
| Number of Channels | | 63 |
| Frequency Range | | 458-520MHz |
| Frequency Resolution | | 1MHz |
| Spurious Tone | | -35.3dBc@1MHz |
| Frequency Accuracy of Crystal | | ±10kHz w/supply=2.7V-3.3V |
| Power Consumption | Crystal Oscillator | ≤7mW |
| | Frequency Synthesizer | ≤38mW (w/o crystal oscillator)* |
| Output Power | Crystal Oscillator | -9.4dBm@50Ω |
| | Frequency Synthesizer | -12dBm@50Ω |
| Phase Noise | Crystal Oscillator | -139 dBc@500kHz |
| | Frequency Synthesizer | -93.5dBc@500kHz |

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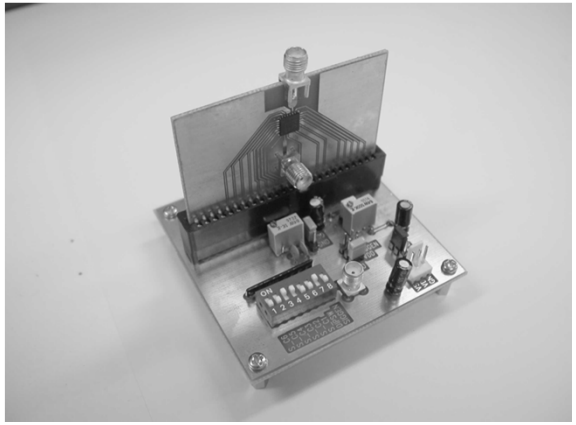
## A CMOS 488-MHz Frequency Synthesizer



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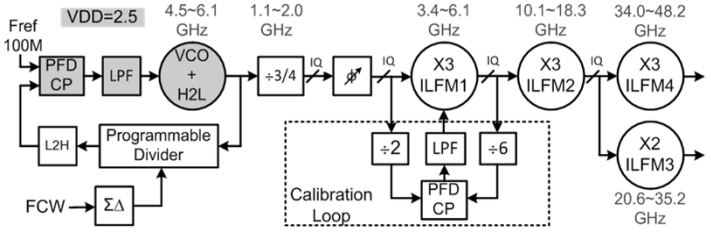
## A CMOS 21GHz-48GHz Frequency Synthesizer [Li, JSSC 8/2014]

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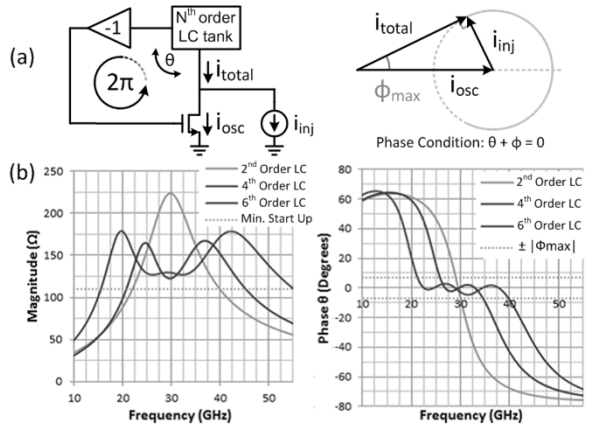
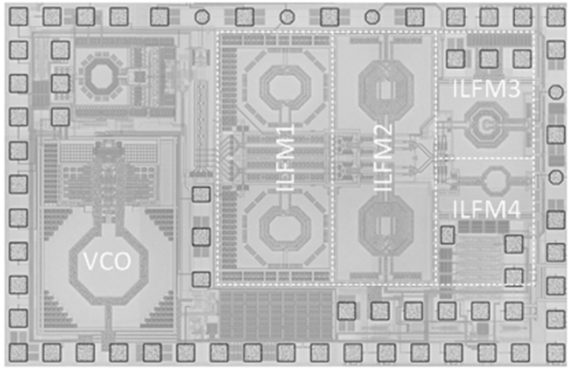
## 21GHz-48GHz Frequency Synthesizer – UWB Injection-Locked Frequency Multipliers





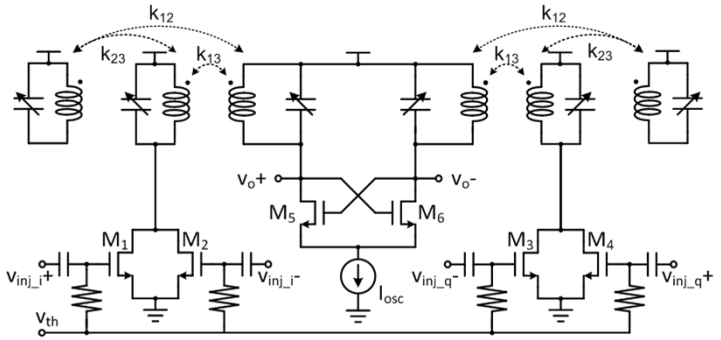

## A CMOS 21GHz-48GHz Frequency Synthesizer




Fabricated in a 65nm CMOS process with area: 1.85 x 1.1 mm2

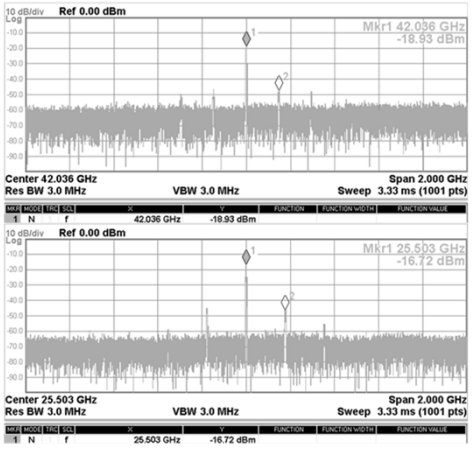


## 21GHz-48GHz Frequency Synthesizer – UWB Injection-Locked Frequency Multipliers

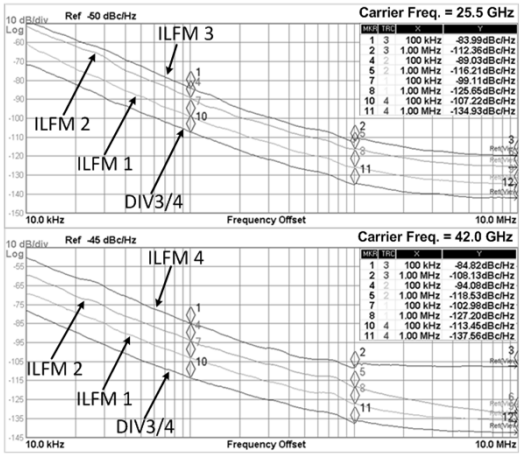





## A CMOS 21GHz-48GHz Frequency Synthesizer – Measured Output Spectrum



## 21GHz-48GHz Frequency Synthesizer – Measured Phase Noise

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## A CMOS 21GHz-48GHz Frequency Synthesizer – Performance Summary [Li, JSSC 8/2014]

| | This Work | D. Murphy JSSC 7/2011 | O. Richard ISSCC 2010 | A. Musa ASSC 11/2011 | S. Pellerano ISSCC 2008 |
|---|---|---|---|---|---|
| Frequency (GHz) | 42.0 | 43.20 | 20.88 | 60.48 | 41.247 |
| Output Frequency Range (GHz) | **20.6- 48.2** | 42.1 - 53 | 17.5 - 21<br>35 - 41.9 | 58 - 63 | 39.1 - 41.6 |
| fref (MHz) | 100 | 54 | 36 | 36 | 50 |
| Out-band phase noise (dBc/Hz) | **-103.58 @ 1MHz** | -85.67 @ 1MHz | -100 @ 1MHz | -96 @ 1MHz | -90 @ 1MHz |
| Integrated Jitter (s) | **1.056 ps** | n/a | n/a | n/a | n/a |
| Power (mW) | 148.3 | 72 | 80 | 77.5 | 64 |
| Process | 65nm CMOS | 65nm CMOS | 65nm CMOS | 65nm CMOS | 90nm CMOS |
| Architecture | Fractional-N (VCO @ 5.26GHz) | Integer-N (VCO @ 50.11GHz) | Integer-N (QVCO @ 20.88GHz) | Integer-N (VCO @ 20GHz) | Fractional-N (VCO @ 41.247GHz) |

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