A 2-V 1.8-GHz fully-integrated CMOS frequency synthesizer for DCS-1800 wireless systems

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Abstract

A 2-V 1.8-GHz fully-integrated CMOS frequency synthesizer for DCS-1800 wireless systems

A 2-V 1.8-GHz fully integrated CMOS frequency synthesizer is designed and tested for use in DCS-1800 wireless systems. The synthesizer employs a dual-loop architecture to realize a monolithic design with more optimal trade-off among phase noise, channel spacing, reference frequency and settling time compared to the conventional integer-N phase-locked loop architecture.

One of the critical challenges in designing such a dual-loop synthesizer is to design a voltage-controlled oscillator with a very wide frequency tuning range and a low phase noise. A ring oscillator (VCO) has been proposed to achieve these tough specifications and will be presented.

The synthesizer employs a dual-path active loop filter to minimize its chip area. The prototype is fabricated in a standard 0.5-μm CMOS process without any external components. The measured phase noise is -111 dBc/Hz at 600-kHz offset from a 1.87-GHz carrier. With an active chip area of 2000 x 1000 μm^2, the test chip consumes 95mW.

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Chapter 1 Introduction

1.1 Motivation

Wireless communication has undergone an incredible development over the past few years. In the past, transceivers were built with discrete elements. However, due to the high cost, big size and large power consumption, the design is not optimal. In order to meet a growing demand for mobile wireless communication, it is desirable to implement some transceivers monolithically with the help of improving large-scale low-cost integration technology. While some transceivers have been made by BJT, GaAs or other high-quality integration process, standard digital CMOS process is more attractive over other technologies because of the possibility to offer the lowest cost solution. Moreover, CMOS technology has the potential to realize the addition of digital function with the front-end circuit. Owing to the serious high-frequency parasitic effects and high noise of standard digital CMOS process, all-CMOS transceivers were only recently implemented. However, the fully integrated CMOS solution of some systems such as GSM and DCS is still an active research topic. One of the bottlenecks in realizing the all-CMOS transceivers is the on-chip low-noise frequency synthesizer. Due to the close separation between the channels in wireless communication systems, RF synthesizers employed in wireless transceivers have very stringent frequency

accuracy specification and have restrictive phase noise requirements to reduce the effect of other large blocking signals. The high frequency operation and the stringent requirements pose big design challenges on the design of on-chip CMOS synthesizers. One of the possible solutions is to use dual-loop architecture. This architecture can improve the trade-off among phase noise, channel spacing, reference frequency and the locking speed. The design of a 1.8-GHz dual-loop synthesizer in a standard CMOS process will be presented in this thesis. The target wireless communication system of the design is DCS-1800.

1.2 Thesis Organization

In Chapter 2, an overview of the basic requirements on the local oscillators in communication system will be given. Several frequency synthesis methods will be discussed. In particular, the in-direct phase-locked technique will be reviewed. The specific system requirements of DCS-1800 are described in chapter 3 to serve as the basis of the synthesizer design. Later part of Chapter 3 will deal with the system design issues, such as the analysis of the dual-loop architecture and noise consideration, of the whole synthesizer. After the system consideration of the synthesizer, the detailed design of building blocks, which include the LC oscillator, the ring oscillator, frequency dividers, phase-frequency detectors and single-sideband mixer, will be discussed in Chapter 4. The layout floor planning will be presented in Chapter 5. The measurement results of the passive components, the individual building blocks and the whole synthesizer will be given in Chapter 6. Finally, the conclusion and further possible improvement will be drawn.

Chapter 2 Synthesizer Background

2.1 General Consideration

For an ideal oscillating source, a sharp impulse is expected in the frequency spectrum. However, due to random fluctuations in the oscillating source, expressed in term of phase noise, the spectrum exhibits “skirts” around the carrier. In order to quantify the phase noise, the noise power per unit bandwidth at an offset frequency ($\Delta\omega$) with respect to the carrier frequency (ω_0) is compared with the carrier power, and this quantity is expressed in the unit of dBc / Hz. In contrast to phase noise, sidebands are deterministic non-ideal components in the output spectrum and have no harmonic relationship with the carrier. Sidebands are usually specified with their frequency and their magnitude relation to that of the carrier [1]. The plots of the phase noise and sidebands in the frequency domain are shown in Figure 2.1.

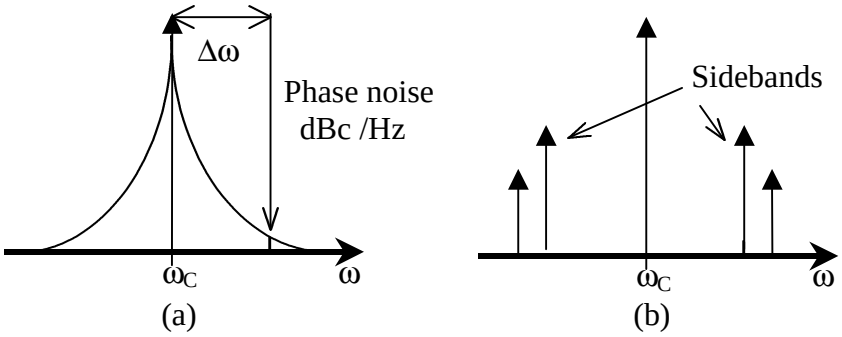


Figure 2.1 (a) Phase noise and (b) sidebands of an imperfect timing source.

To demonstrate the effect of phase noise and sidebands in wireless communication, a simple generic transceiver as depicted in Figure 2.2 is considered. The receiver consists of a low-noise amplifier, a band-pass filter and a downconversion mixer, and the transmitter comprises an upconversion mixer, a band-pass filter and a power amplifier. The output signal of a local oscillator (LO) is used to drive mixing circuits, which up-convert baseband signal and down-convert the received RF signal, respectively [2].

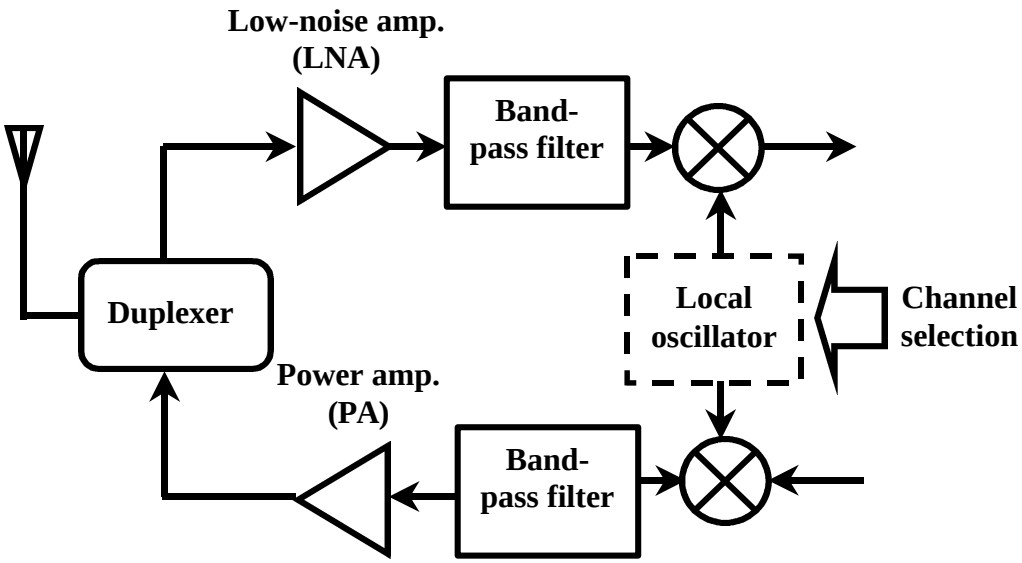
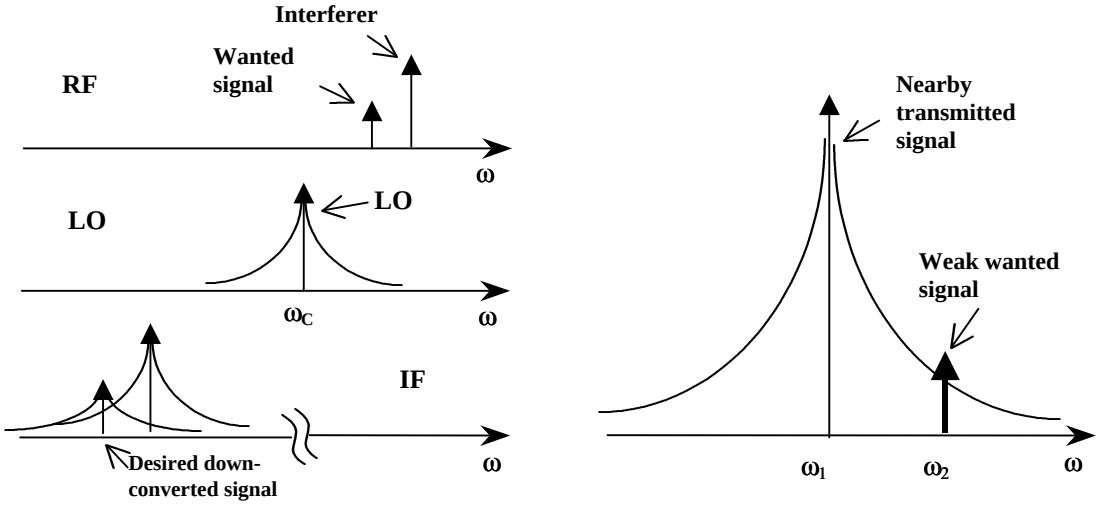


Figure 2.2 A generic transceiver block diagram.

The phase noise of the local oscillator corrupts both the up-converted and down-converted signals. Ideally, the signal band is converted with an impulse in the frequency domain into the desired intermediate frequency (IF) in the receiver. However, in reality, the local oscillator exhibits finite phase noise. Furthermore, there may exist large interferers in adjacent channels, which can be only a few tens of kilohertz away from the wanted signal. When the wanted signal and the interferer are mixed with the non-ideal LO output signal, the tail of the interferer spectra corrupts the down-converted signal band of interest and thus reduces the signal-to-noise ratio. This effect is called “reciprocal mixing”. In the transmitter, large-power transmitted signals with substantial phase noise can corrupt weak nearby signals.

Figure 2.3 illustrates the impact of LO phase noise in the receive and the transmit paths. Therefore, the output spectrum of the LO must be extremely sharp, and a set of stringent phase noise requirements must be satisfied in the wireless communication system.



Receive path Transmit path

Figure 2.3 Effect of phase noise on the receive and the transmit paths.

The effect of unwanted sideband is another problem in the receive path as shown in Figure 2.4. Suppose the oscillator output consists of a carrier at ω_C and a sideband at ω_S, while the received signal at ω_{RF} is accompanied by an interference signal at ω_{INT}. If the difference between ω_C and ω_{RF} is equal to that between ω_S and ω_{INT}, the down-converted interferer falls into the desired channel as the wanted signal and corrupts the resulting IF output. Typically, wireless communication systems require that spurs be approximately 60 dB below the carrier. Phase noise and spurious tones in the oscillator signal can limit the ability to receive a desired signal in the presence of strong interferers and this ability is called "selectivity". The carrier frequency of oscillators in RF transceiver must also have very high absolute accuracy throughout a wide range of temperature and be stable for a long period of time. In a wireless communication system, the lower and upper edges of each channel can

tolerate an error of no more than a few hundred Hertz.

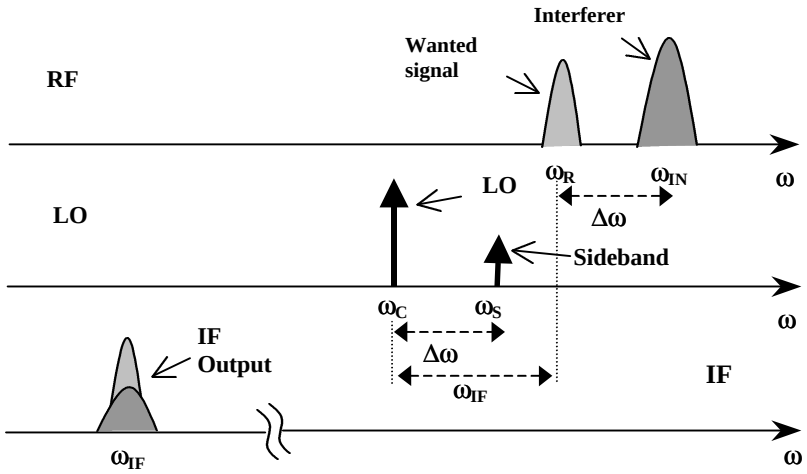


Figure 2.4 Effect of sideband in a receiver.

In a wireless transceiver, to change from receive channel to transmit channel, the LO frequency may be required to vary by a few tens of megahertz, and the oscillator requires a finite time to establish the new stable frequency reference. The settling time of the timing source is a critical design parameter for some systems such as frequency-hopped spread-spectrum systems. The settling time required in a typical RF system varies from a few tens of microseconds to a few tens of milliseconds.

2.2 Frequency Synthesis

In order to generate a variable precise timing reference for the systems, a frequency synthesizer is required. Generally, common frequency synthesizer types include direct analog synthesizer (DAS), direct digital synthesizer (DDS), and indirect or phase-locked synthesizer. In this section, each of them will be described briefly, and their merits and weaknesses for use in monolithic transceivers will be compared.

2.2.1 Direct Analog Synthesizer (DAS)

The direct analog synthesizer employs multiplication, mixing, filtering, switching and division to synthesize the desired frequency from a simple coherent reference or from multi-incoherent references. The reference source is a single crystal reference (XTAL), which typically oscillates from 3 MHz to 120 MHz. Figure 2.5 shows an example of a direct analog synthesis approach.

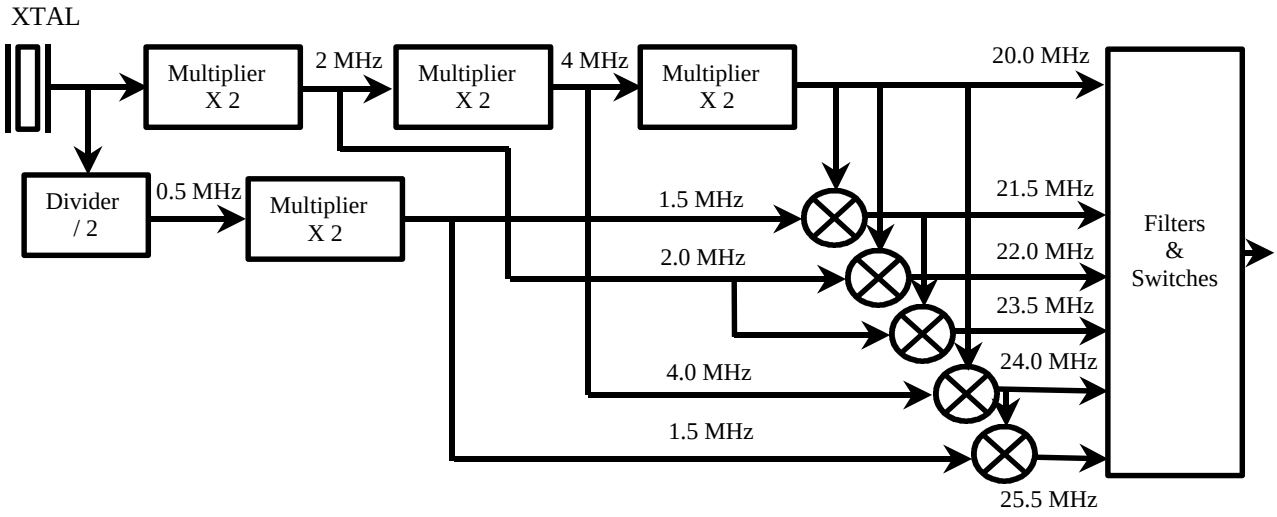


Figure 2.5 An example of coherent direct analog synthesizer

The advantages of this synthesizer type are the ability of rapid frequency change and the pure output spectrum as that of the reference source. However, the circuit has a large number of components, such as filters and multipliers, and thus the direct synthesizers are bulky and power-hungry. Moreover, the number of components increases with the number of channels and the channel spacing of the system. In a monolithic wireless communication system such as GSM, its large number of channels and small channel spacing make the use of a direct analog synthesizer impractical and undesirable.

2.2.2 Direct Digital Synthesizer (DDS)

In this type of synthesizer, the output waveform is generated by using the digital values stored in a memory. A simplified block diagram is shown in Figure 2.6. A number $\Delta\theta$ represents the phase change per clock period is shifted into the accumulator, which has a capacity corresponding to one complete output cycle. The output of the accumulator, which represents the phase of the signal, is used as the address for the table-loop-up memory. The output of the desired frequency signal is synthesized by using a digital-to-analog converter (DAC) to convert the memory output. The high frequency spurs resulting from the digital-to-analog conversion are attenuated by a low-pass filter (LPF)

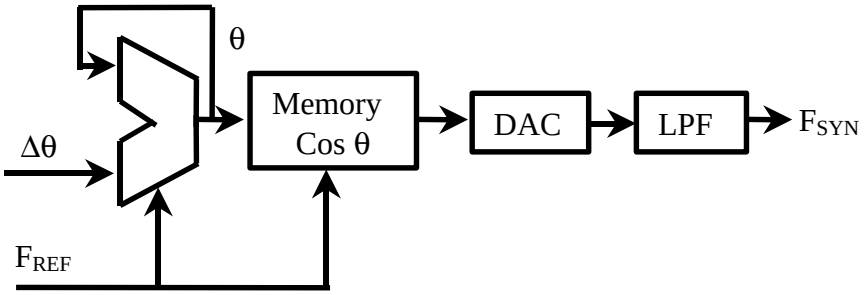


Figure 2.6 Simplified Block diagram of DDS.

This type of synthesizer allows very fast switching of the frequency and fine resolution over a wide frequency range. However, the large size of the table-look-up memory required for fine resolution makes the synthesizer bulky and not desirable for the use in monolithic transceivers. Moreover, the output of the synthesizer contains spurs resulting from digital operation as well as non-linearities associated with the DAC. Furthermore, the high frequency operation is not possible due to the limited speed of high-resolution DAC. One solution is to combine DDS with a fixed oscillator using a mixer to obtain high frequency output [2]. However, the large spurs in the DDS output still seriously affect the performance of the synthesizer. At the same time, if the oscillator is fabricated on the same chip as the DDS

circuit, the substantial substrate and the supply noise produced by DDS would pollute the VCO output. It makes a barrier for monolithic transceiver using DDS.

2.2.3 Phase-Locked Loop Synthesizer

As the direct synthesizers are not suitable for monolithic RF transceivers, indirect phase-looked loops (PLLs) become the dominant architecture for frequency synthesis We describe some common indirect synthesizer architectures briefly in this section. As PLL is an important building block of these frequency synthesizers, its operation principle and characteristics are examined in detail in the next section.

2.2.3.1 Integer-N Architecture

A simple PLL incorporating an integer-N programmable divider in the feedback path is shown in Figure 2.7. The voltage-controlled-oscillator (VCO) output frequency is divided by the number *N* in the divider. The divided frequency is compared to the crystal reference frequency by the phase detector (PD). The low-pass filtered output of the PD provides the phase difference information to adjust the VCO output frequency to the more precise desired frequency.

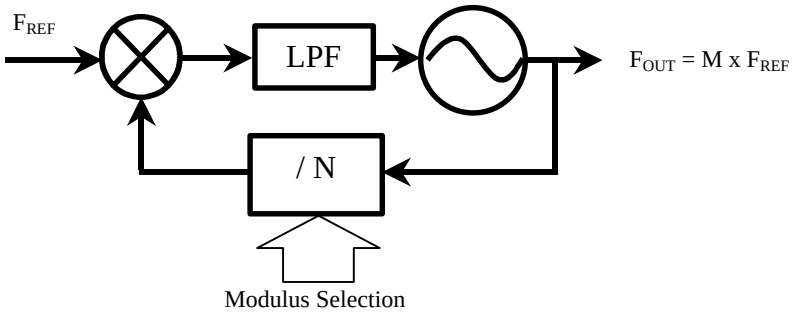


Figure 2.7 Block diagram of integer-N synthesizer

The PLL frequency synthesizer is suitable for integration in a standard integrated circuit

(IC) process due to its low-power consumption and reasonable chip area. This type of synthesizer is inherently slower than a direct synthesizer due to the feedback action requiring time to acquire its steady-state operation. The loop filter and the reference frequency play a very important role in the design of PLL-type synthesizer and they will be discussed in detail in next section. Larger loop bandwidth can attenuate the phase noise of the VCO for frequency offsets roughly within the loop bandwidth. Moreover, fast frequency change is only possible when the loop bandwidth is large. On the other hand, the loop bandwidth is typically limited to one tenth of the reference frequency due to stability requirement. In an integer-N synthesizer, the output frequency changes by only integer multiples of the reference frequency. As a result, the close channel spacing in a wireless communication system limits the reference frequency and the loop bandwidth. The periodic disturbance of the VCO control due to sampling action of the reference frequency in the PD creates unwanted sidebands in the VCO output and, to attenuate the magnitude of these reference spurs sufficiently, in many cases, it places further limitation on the loop bandwidth. Furthermore, the phase noise contributed from the reference source to the output is increased by approximately *N* times in the loop, which is large if the desired output frequency is much higher than the channel frequency spacing. Therefore, many techniques have been proposed to overcome the trade-off among frequency division ratio, loop bandwidth and reference frequency.

2.2.3.2 Fractional-N Architecture

In fractional-N synthesizer, the divider architecture is modified in order to obtain the frequency change by a fraction of the reference frequency. Therefore, the tradeoff in the PLL synthesizer with an integer divider does not apply to fractional-N synthesis. The fraction division is obtained by occasionally or periodically changing the division value of the divider and this can be done by pulse inserting, pulse removing, pulse interpolating or modulating the

divider ratio. Figure 2.8 shows the block diagram of a fractional-N synthesizer with a dual-modulus divider as an illustration. For instance, if the VCO output is divided by *M* for *N* output pulses and by *M+1* for *P* output pulses, then the average equivalent divide value is equal to $[N / (N+P)] * M + [P / (N+P)] * (M+1) = M + [P / (N+P)]$. Thus, the division value can vary between *M* and *M+1*.

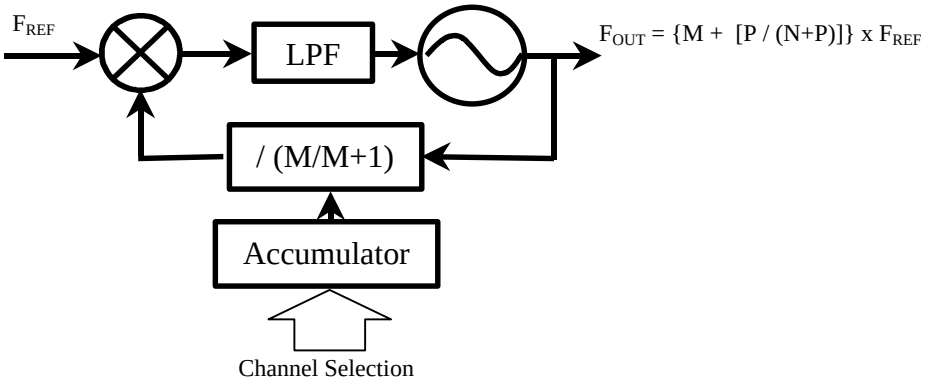


Figure 2.8 Fractional-N synthesizer using dual-modulus divider

The modification allows a larger loop bandwidth compared to that in the case of integer-N synthesizer under the same channel separation. Thus, it increases the locking speed of the synthesizer and provides more suppression of the VCO output phase noise close to the carrier. The drawback is the existence of large fractional spurs at the output and the locations of the spurs vary with the divide value. Many spur reduction methods, such as phase estimation by DAC and noise shaping by Σ-Δ modulation with multi-modulus divider, have been proposed. However, those methods make the design of fraction-N synthesizer more complicated.

2.2.3.3 Dual-loop Architecture

Employing two or more loops can alter the relationship between the channel spacing and the reference frequency of integer-N synthesizers. There are mainly two types of dual-loop synthesizers, which are combination of two PLLs by a single-side-band (SSB) mixer in

parallel and in series. Example of each type is shown in Figure 2.9. The basic idea is to add a low variable frequency to a high fixed offset frequency. The frequency change of the synthesizer therefore only requires the change of the divide ratio in the low-frequency loop. In the parallel configuration, a fixed frequency is mixed with the changeable frequency by the SSB mixer at the output and therefore it suffers from large spurs during mixing. In the series configuration, a changeable frequency is added inside the loop. Although this configuration needs longer time to settle, the sideband from the mixer can be greatly attenuated by the loop.

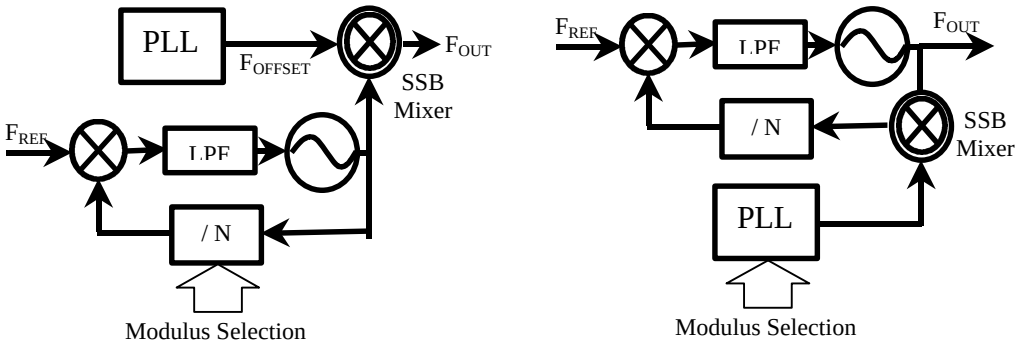


Figure 2.9 Examples of dual-loop architecture

The advantage of this architecture over integer-N topologies is that the loop bandwidth of the high-frequency loop chosen can be large. Because the VCO in the high-frequency loop operates at a higher frequency, the phase noise performance is expected to be worse than that in a low-frequency loop. Therefore, a larger loop bandwidth can provide more reduction of the phase noise close to the carrier to compensate the phase noise performance of the high frequency VCO. Moreover, because of the fixed offset frequency, the division number of the divider is also reduced. The possible drawbacks are mainly the sidebands produced from non-ideal SSB mixing and probable larger power consumption than single loop. In this project, dual-loop architecture in series is chosen and more detailed merits and design will be discussed in Chapter 3.

2.3 Phase-Locked Loop

Since phase-locked loop is an important basic building block of frequency synthesizers, the details of loop dynamics, its linear model and noise characteristics will be discussed in this section. Figure 2.10(a) shows the block diagram of a PLL, consisting of a phase detector, a low-pass filter, a divider and a VCO. One of the advantages of the PLL architecture is the ability to realize excellent phase noise performance over a wide tuning range, while simultaneously having good frequency accuracy. The circuit is named phase-locked loop because the feedback operation automatically adjusts the phase of the VCO output frequency according to the phase of the more stable reference frequency. The phase detector (PD) serves as an error amplifier in the feedback loop to minimize the phase difference between x(t) and z(t). In the normal locked condition, the PD forces the frequency at the output of the divider to be equal to the reference frequency and therefore the output frequency is *N* times that of the reference source. The low-pass filter suppresses high-frequency components in the PD output, allowing the low-frequency component and the dc component to control the VCO frequency. The filter also compensates for loop stability in most of the cases. The acquisition range is defined as the maximum value of frequency change $\Delta\omega$ either in the reference source or in the VCO for which the loop can be still kept locking and depends on the magnitude of the component at $\Delta\omega$ at the LPF output.

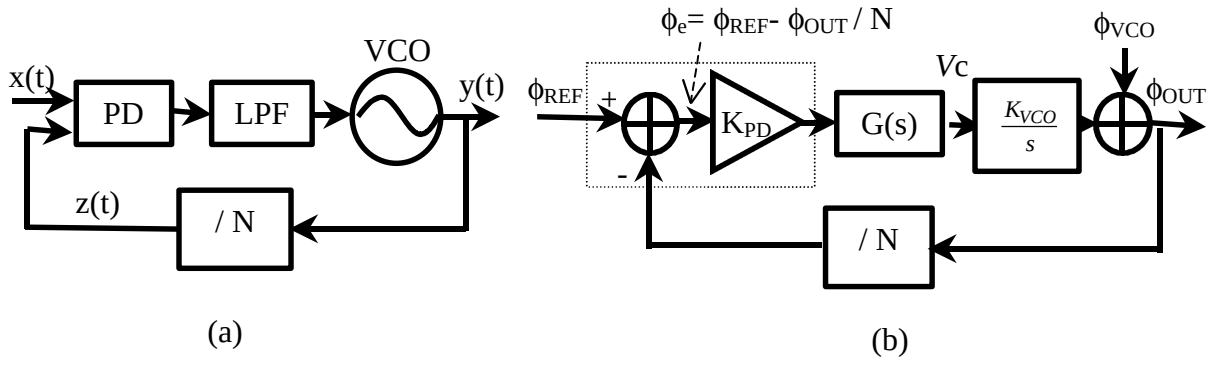


Figure 2.10 (a) Block diagram and (b) linear model of phase-locked loop

In many applications, the PD is replaced by a phase-frequency detector (PFD), which can detect frequency difference between the reference frequency and the divider output, to increase the acquisition range and lock speed of the PLL.

As PLL is locking the phase between reference frequency and the output frequency, when the loop is in lock, it is easier to study the phase relationship of this circuit by the linear model as shown in Figure 2.10(b). The PD is represented by a subtractor following a gain stage. The linearized small-signal gain of the phase-detector is K_{PD}, whose units are typically volts / radian. The LPF is modeled by its voltage transfer function G(s). The ratio of change in output frequency to change in VCO control voltage is known as the VCO gain factor K_{VCO} in unit of radian / Volts. Since frequency is the derivative of phase, the VCO operation can be described as Eq. 2.1.

$$\frac{d\mathrm{f}_{OUT}}{dt} = K_{VCO} \cdot v_c(t) \qquad (2.1)$$

By taking the Laplace transforms we obtain

$$\mathrm{f}_{OUT}(s) = \frac{K_{VCO} \cdot V_c(s)}{s} \qquad (2.2)$$

The open loop transfer function A(s) of the loop equals

$$A(s) = \frac{K_{VCO} \cdot K_{PD} \cdot G(s)}{N \cdot s} \qquad (2.3)$$

Basically, the noise coming from the reference source and noise generated in the VCO will mainly dominate the noise in the PLL. The phase change at the VCO output and that at the reference source output are represented by $\phi_{VCO}(t)$ and $\phi_{REF}(t)$, respectively. Using the

small-signal phase model, the closed-loop response to a VCO noise signal is

$$\frac{f_{OUT}(s)}{f_{VCO}(s)} = \frac{1}{1+A(s)} = \frac{N \cdot s}{N \cdot s + K_{PD} \cdot G(s) \cdot K_{VCO}} \qquad (2.4)$$

whereas the closed-loop response to the reference noise signal is

$$\frac{f_{OUT}(s)}{f_{RREF}(s)} = \frac{A(s)}{1+A(s)} = \frac{N \cdot K_{PD} \cdot G(s) \cdot K_{VCO}}{N \cdot s + K_{PD} \cdot G(s) \cdot K_{VCO}} \qquad (2.5)$$

In order to gain more insight from the equations, suppose that the loop filter is just a constant, i.e. G(s) = K, where K is a constant Eqs (2.4) and (2.5) then reduce to

$$\frac{f_{OUT}(s)}{f_{VCO}(s)} = \frac{1}{1+\frac{K_F}{N \cdot s}} = \frac{s}{s+\omega_p} \qquad (2.6)$$

$$\frac{f_{OUT}(s)}{f_{REF}(s)} = \frac{\frac{K_F}{N}}{1+\frac{K_F}{N \cdot s}} = \frac{N \cdot \omega_p}{s+\omega_p} \qquad (2.7)$$

where $K_F = K_{PD} \times K_{VCO}$ and ω_p is defined as the crossover frequency at which the open loop gain is unity. The PLL becomes a type-one first order loop because the open-loop gain has only one dominant pole at zero frequency.

As shown in Eq. 2.6, the noise transfer function from VCO to the output is a high-pass function. Noise at a high frequency pass un-attenuated, while the low frequency noise is reduced by the loop because the feedback action of the loop is too slow to tackle with high-frequency noise. However, at a lower frequency, there is a first-order role-off to attenuate the low-frequency noise from the VCO. The change of this noise characteristic occurs at ω_p. This situation is depicted in Figure 2.11(a). The solid line represents a typical output noise spectral

density (PSD) of the oscillators, while the dotted line is the PSD after the suppression effect of the loop. The output noise spectrum of the oscillators can be divided into three regions. At the frequency far from the carrier, a flat noise floor is obtained from the white noise sources. As the frequency offset is closer and closer to the carrier, there is another region that the phase noise decreases quadratically with the offset frequency. This region is due to the white noise sources around the carrier being amplified by the positive feedback of the oscillator. Finally, there is a ω^{-3} region close to the carrier because the low frequency 1/f noise is up-converted by non-linearities in the oscillator components. The larger the loop bandwidth, the more noise close to the carrier can be reduced. It is noted that the 1/f corner of CMOS devices is quite large and thus CMOS oscillators may have wide ω^{-3} noise region [3].

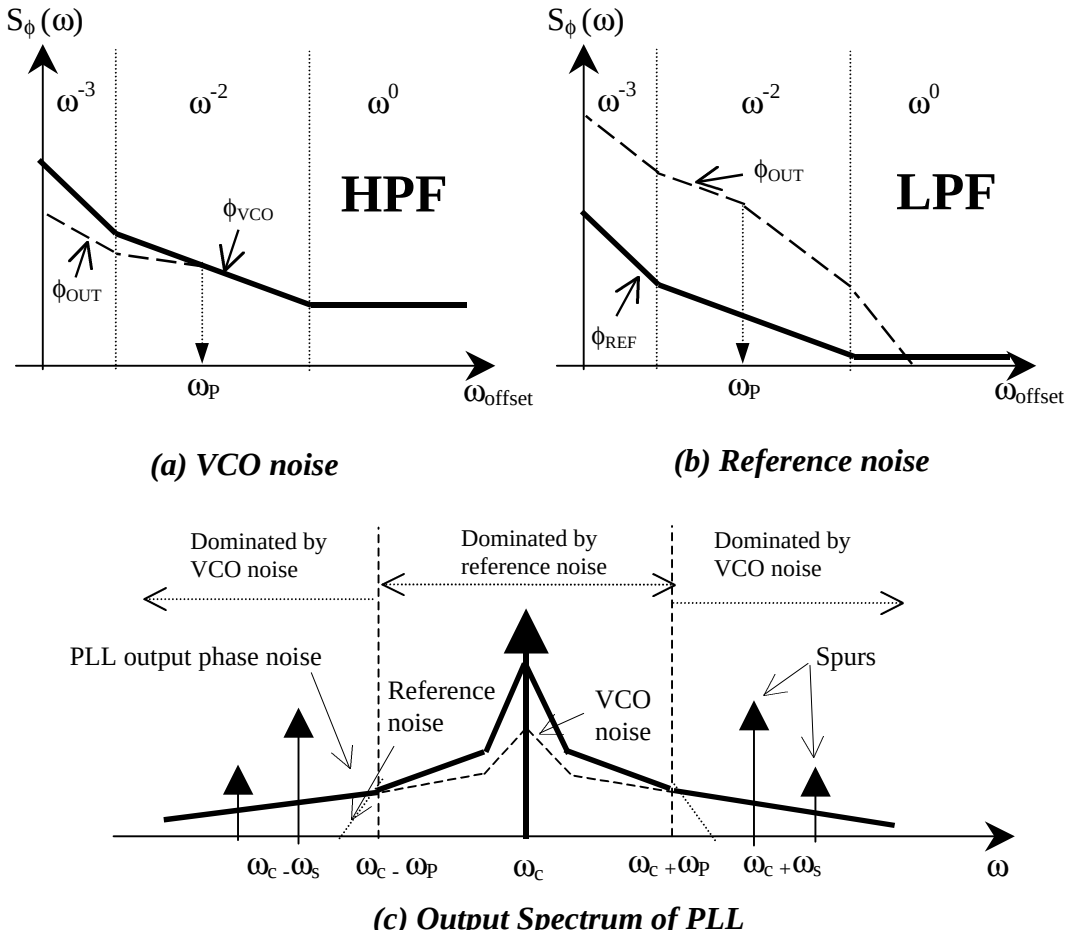


Figure 2.11 Phase noise in PLL: (a) VCO noise; (b) Reference noise; (c) Overall output spectrum

Figure 2.11(b) shows the noise spectrum of the reference source, which is represented by the dotted line and that of the PLL output with a noiseless oscillator, which is drawn as the solid line. Eq. 2.7 shows that the noise transfer function from reference to the output is a low-pass function, while that of the VCO is a high-pass function. The high-frequency noise from the reference source, from PD and from divider will be attenuated by the low-pass loop filter, while the low-frequency noise passes to the output. The 3-dB cut-off frequency of this characteristic is also ω_p. Generally, the high-quality reference source used in frequency synthesis has phase noise performance much better than the oscillators. However, the divider in the loop amplifies the noise by a factor of *N* for the frequencies lower than ω_p as shown in Eq. 2.7. The resulting possible output spectrum with both the noise sources is shown in Figure 2.11(c). It should be pointed out that generally noise close to the carrier is dominated by noise from the reference source, the PD and the divider, while the phase noise far from the carrier is mainly dominated by the VCO noise. To achieve an optimal noise performance, the loop bandwidth must be optimized carefully to minimize the total output noise. In the application of frequency synthesis, the reference is generally a high-quality crystal oscillator and the phase noise should be dominated only by that of the VCO. Therefore, larger bandwidth is desirable for the noise performance.

As shown in Figure 2.11(c), the output also has some sidebands due to the large-amplitude reference source. The sidebands are created by the sampling action of the PD during the comparison of the phase difference and the periodic disturbance of the VCO control signal occurs. The locations of the sidebands depend on the reference frequency as well as the PD type used. For instance, when a tri-stage PFD is used and mismatch exists between up and down signal of the PFD output, the main sideband will be in the frequency offset equal to the reference frequency. The other sidebands are due to FM modulation of the

VCO by this main component. In order to reduce the spurs, the loop bandwidth can be reduced to obtain significant attenuation on them.

The other important situation in a frequency synthesizer is how long does the loop take for the output frequency in order to settle to the new desired frequency when the division modulus *N* is changed. Suppose there is a step change $\Delta\omega$ of frequency at reference input and then the input phase change $\phi_{REF}(t)= \Delta\omega \times t$. For a first-order loop, the following calculation can be made:

$$\mathrm{f}_{err}(s) = \frac{1}{1+A(s)}\mathrm{f}_{REF}(s) = \frac{s}{s+\mathrm{w}_p}\cdot\frac{\Delta\mathrm{w}}{s^2} = \frac{\Delta\mathrm{w}}{s(s+\mathrm{w}_p)} \qquad (2.8)$$

$$\mathrm{f}_{err}(t) = \frac{\Delta\mathrm{w}}{\mathrm{w}_p}\cdot(1-e^{-\mathrm{w}_p t}) \qquad (2.9)$$

From Eq. (2.9), the final frequency is obtained following an exponential behavior with time constant $\tau = 1/\omega_p$. Therefore, the setting time T_ε can be calculated as follows:

$$T_{\mathrm{e}} = -\frac{\ln \mathrm{e}}{\mathrm{w}_p} \qquad (2.10)$$

where ε is the accuracy of the output frequency compared to the final desired value. This equation shows that in order to have a faster setting of the loop, a larger loop bandwidth is desirable.

In conclusion, a smaller loop bandwidth is preferred to reject more noise from the reference source, and to suppress the spurs, while a larger bandwidth is needed to attenuate the VCO noise and to have a faster settling response. This design trade-off also applies to the reference frequency because the loop bandwidth is limited by typically one tenth of this frequency in order to obtain a stable loop response. The larger value of the reference

frequency in a simple integer-N synthesizer is bounded by the channel spacing of the wireless communication system. Therefore, the parameters in the loop should be chosen in order to obtain optimal conditions between the output phase noise and settling time. Normally, a high order loop should be used for the design of the synthesizer in order to reduce more noise and spurs power with more degrees of design freedom. However, the same design trade-off discussed previously will also be held.

References

[1] Behzad Razazvi, “RF Microelectronics”, Prentice Hall, New Jersey, 1998.

[2] Behzad Razazvi, “Challenges in Design of Frequency Synthesizers for Wireless Applications”, *Proc. of the IEEE 1997 Custom Integrated Circuits*, pp.395-402, 1997.

[3] Behzad Razazvi, “A Study of Phase noise in CMOS Oscillators”, *IEEE Journal of Solid-State Circuit*, Vol. 31, No. 3, pp.331-43, March 1996.

Chapter 3 Synthesizer System Design

3.1 DCS-1800 System Specification

DCS-1800 is the target wireless communication system for this synthesizer design. It uses GMSK modulation with channel bit rate of 270.833 kb/sec. The up-link transmit band (TX) is at 1805-1880 MHz and the receiving band (RX) is at 1710-1785 MHz. There is a 45-MHz TX/RX spacing. In each band, there are 375 channels with 200kHz spacing. The DCS-1800 system is a time-multiplexed system with eight time slots and each time slot is 577 μsec wide. The time slot diagram is shown in Figure 3.1.

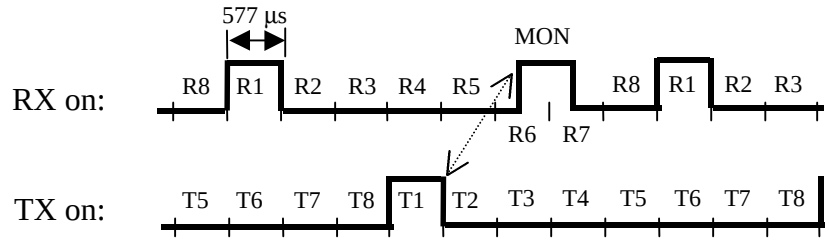


Figure 3.1 DCS-1800 receive (RX) and transmit (TX) time slots

The mobile terminal receives data in slot R1 and transmits in slot T1. A monitor slot MON is received at one and a half time slot after T1. Therefore, the synthesizer has to switch from the transmit band to the receive band in time shorter than 865 μsec, which is the worst case situation for loop settling. From Eq. (2.10), the minimum loop bandwidth of a first-order loop that required for this situation with a 100-MHz step change and a final accuracy of 100 Hz ($\varepsilon=10^{-6}$) is around 2.5 kHz.

Figure 3.2 shows the relationship between in-band blocking signals and the phase noise requirements of the LO signal in DCS-1800 system [1].

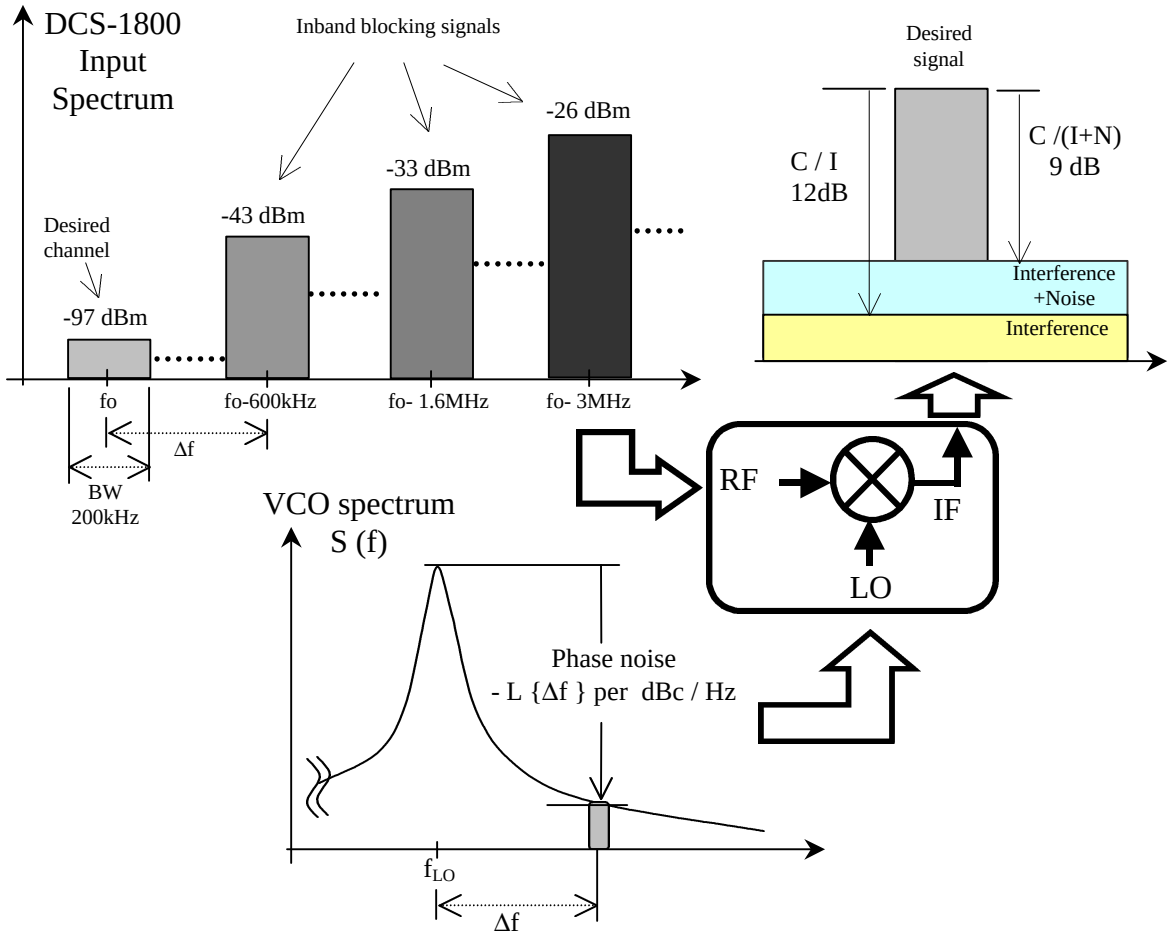


Figure 3.2 Relationship between blocking signal and phase noise of the oscillators.

The phase noise requirements are mainly set by the received desired signal and other blocking signals. The desired in-band signal is set to –97 dBm by the system specification. The closest adjacent channel of the desired one in the same mobile cell is located at three channels apart, or 600 kHz apart. The receiver must maintain a 10^{-3} BER or equivalently 9 dB carrier-to-noise & interference ratio C/(I+N) at the IF output. The minimum carrier-to-interference ratio C/I is set to 3 dB larger than C/(I+N) to ensure the desired performance of the receiver. The phase noise of the oscillator required at offset frequency (Δf) from the

carrier in unit of dBc / Hz can be estimated using,

$$Phase\ noise\ L\{\Delta f\} = S_{siganl} - S_{blocker}(\Delta f) - C/I_{\min} - 10\log(BW) \qquad (3.1)$$

where $S_{blocker}(\Delta f)$ is the magnitude of the blocker in dBm at Δf frequency offset from the desired channel. The required phase noise performance is summarized in Table 3.1. The phase noise requirements of the dual-band receiver for GSM and DCS-1800 are also shown. The differences between two specifications are the signal level of wanted signal, which is –99 dBm for GSM and the signal levels of the blockers [2].

Offset from Carrier	Phase noise required for DCS-1800	Phase noise required For dual-band
600 kHz	-119 dBc /Hz	-122 dBc /Hz
1.6 MHz	-129 dBc /Hz	-132 dBc /Hz
3 MHz	-136 dBc /Hz	-137 dBc /Hz

Table 3.1 Required phase noise performance of the oscillator

According to the specifications, the unwanted signal can have a blocking level of –26 dBm, which is 71 dB higher than the minimum signal level of –97 dBm. Thus, the spurious level should be lower than –83 dBc in order to preserve 12-dB margin for sufficient C/I ratio.

3.2 Architecture of the Synthesizer

In this project, dual-loop in series architecture [3] is chosen. As discussed in Chapter 2, this type of architecture offers excellent output spectrum purity and fast switching speed. The block diagram of the synthesizer is shown in Figure 3.3. The unwanted sidebands resulting from mismatches and non-linearities of the SSB mixing can be alleviated by placing the SSB mixer inside the feedback loop. The sidebands at the mixer output are suppressed by the low-

pass filter of the upper loop and the prescalar N. The SSB mixer is used to subtract the output frequency of VCO2 from that of prescalar X and to suppress the unwanted sideband during mixing. The resulting output frequency can be calculated as follow:

$$f_{OUT} = f_{OFF} + M \times \left(\frac{f_{REF2}}{X} \right) = N \times f_{REF1} + M \times \left(\frac{f_{REF2}}{X} \right) \qquad (3.2)$$

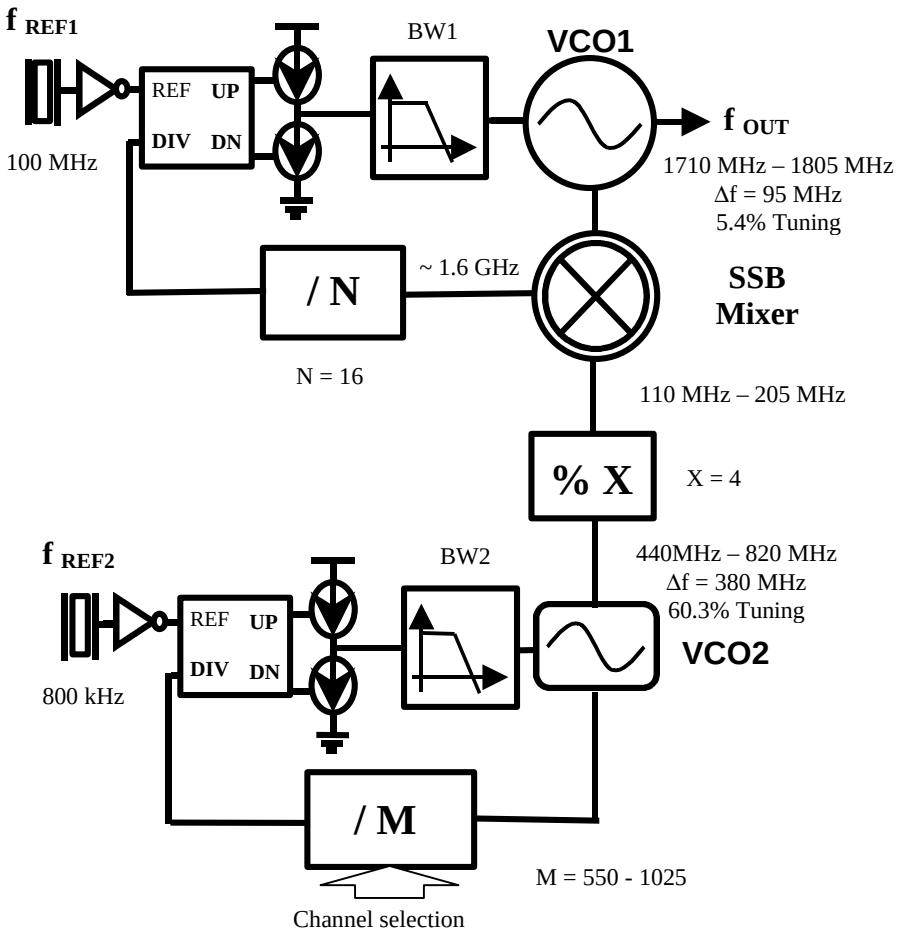


Figure 3.3 The block diagram of the dual-loop architecture

The upper loop provides a large offset frequency $f_{OFF} = N * f_{REF1}$ and hence it helps to reduce the division ratio in the programmable counter (M). The X counter between the two loops is used to release the phase noise requirements of the VCO2 with the expense of its wider tuning range. It also helps to increase the reference frequency (f_{REF2}) of the lower loop. Each divide-by-2 counter can provide 6 dB reduction of phase noise of its output carrier

comparing to its input and thus, the value of 4 in prescalar X can provide approximately 12-dB reduction of phase noise of the lower-loop output signal. Moreover, the prescalar X also attenuates the sidebands resulting from the reference source of the lower loop. The phase noise performance of VCO2 at the offset far from the carrier is further alleviated by the low-pass filter in the upper loop. The reference frequency (f_{REF1}) of the upper loop is 100 MHz and it is large enough to provide fast setting of the upper loop and enough suppression of the reference spurs by the upper loop filter. The settling time of the synthesizer mainly depends on the settling of the lower loop and thus the lower reference (f_{REF2}). With the frequency planning shown in Figure 3.3, the output frequency of the synthesizer can be tuned from 1710 MHz to 1805 MHz and the minimum required programmable value of counter M can change from 550 to 1025. The required tuning ability of VCO2 is as large as 60 % with a 630-MHz center carrier while that of VCO1 is only 5.4% with a 1757.5-MHz center carrier.

3.3 Loop Filter Topology

The loop filter is an important block in a synthesizer because it determines most of the PLL specifications such as phase noise performance, spur level and locking speed. Therefore, its design issue will be discussed in this section before further discussions of the loop behavior.

The schematic of dual-path loop filter used in the synthesizer is displayed in Figure 3.4 [2]. A fourth-order type-two PLL is obtained if the filter is driven by two charge pumps. The active configuration is used in order to keep voltages at the outputs of charge pumps to have a constant DC voltage. The virtual ground of the amplifier keeps the transistors of the charge pumps in desired saturation region effectively and therefore maintains the balance of the UP

and DN current sources in the charge pumps.

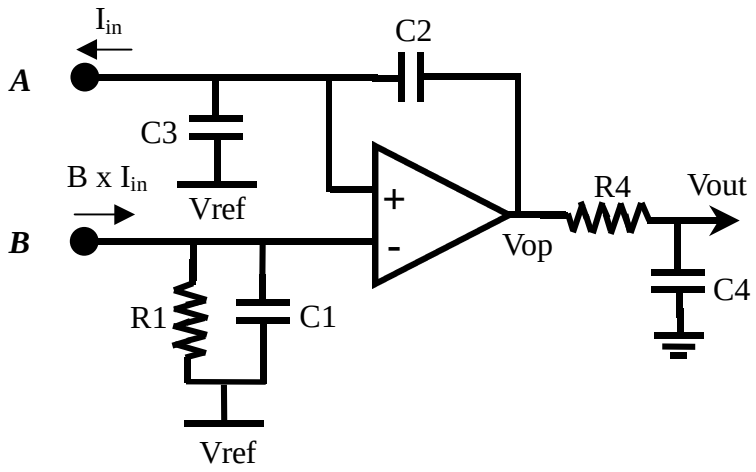


Figure 3.4 Dual-path filter implementation

This is good for the reduction of reference spur. Moreover, the large output voltage swing of the operation amplifier (Opamp) can provide wide enough tuning voltage for the VCO control.

In this filter, dual-path architecture is employed and the dual-path operation principle is shown in Figure 3.5.

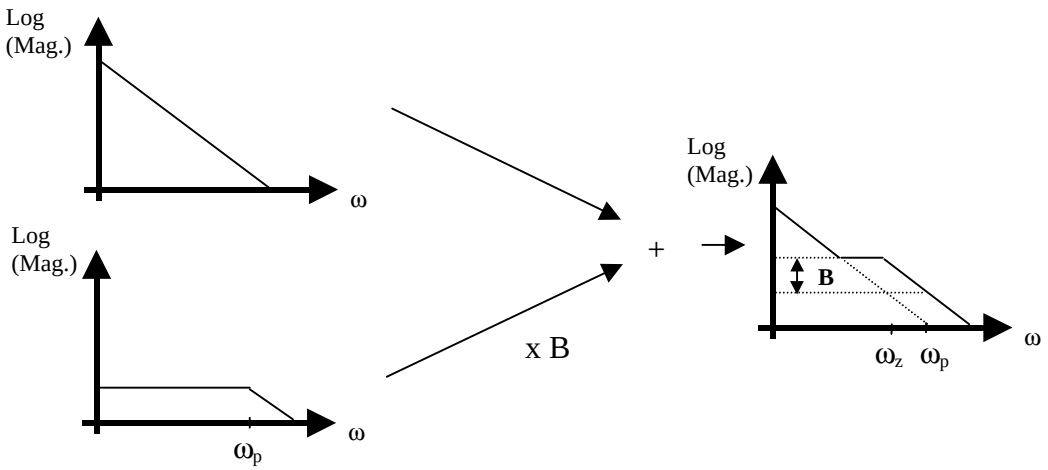


Figure 3.5 Dual-path loop filter principle

The filter is driven by two charge pumps with different current output levels I_{in} and (B x I_{in}), respectively and different directions of current flow. The transfer function from point A to Opamp output is shown as follows:

$$H_I(s) = \frac{V_{out}(s)}{I_{in}(s)} = (\frac{1}{sC_3} \left\| \frac{1}{sC_2}) = \frac{1}{s(C_2 + C_3)} \approx (\frac{1}{sC_2}) \qquad (3.3)$$

This is an integrator according to Eq. 3.3. In the circuit, C_3 is actually parasitic of the Opamp and thus it is much smaller than C_2 and C_1. So it will be neglected in following calculations. The transfer function from point B to Opamp output is calculated as follows:

$$H_L(s) = \frac{V_{out}(s)}{I_{in}(s)} = B \cdot (1 + \frac{C_3}{C_2}) \cdot (\frac{1}{sC_1} \left\| R_1) \approx (\frac{B \cdot R_1}{1 + sC_1R_1}) \right. \qquad (3.4)$$

This signal path has a low-pass function with a scaling factor B. The fourth pole is added by the combination of R_4 and C_4 to further attenuate the noise and the magnitude of the reference spurs at high frequency offsets from the carrier. This low-pass function is given by:

$$H_4(s) = \frac{Vout(s)}{Vop(s)} = \frac{1}{1 + sC_4R_4} \qquad (3.5)$$

The signal from the integrator and the signal passing through the passive network formed by C_1 and R_1 are now added by the Opamp and pass through $H_4(s)$ to form the overall loop filter function:

$$\begin{aligned} G(s) = \frac{V_{out}(s)}{I_{in}(s)} &= (H_I(s) + H_L(s)) \cdot H_4(s) \\ &= \frac{1 + s(C_1 + B \cdot C_2) \cdot R_1}{sC_2 \cdot (1 + sC_1R_1)} \cdot \frac{1}{1 + sC_4R_4} \\ &= \frac{1}{sC_2} \cdot \frac{1 + st_Z}{1 + st_p} \cdot \frac{1}{1 + st_4} \end{aligned} \qquad (3.6)$$

$$with \quad t_Z = R_1(C_1 + B \cdot C_2), t_p = C_1R_1 \quad and \quad t_4 = C_4R_4$$

As shown in Eq. 3.6, a large time constant is realized for the filter zero without the requirement for a large capacitor due to the multiplication by the factor B. Moreover, the DC operating voltages of both current inputs are positioned at a constant DC reference V_{ref}. When the loop is locked, the input B sets to V_{ref} because no current flows through R_1 and virtual ground property of the Opamp keeps the same constant DC voltage in the input of the integrating path.

3.4 Loop Gain of the loop

With the loop filter impedance calculated in Eq. 3.6, the open loop gain of the loop equals

$$A(s) = \frac{Iqp \cdot K_{VCO}}{2\pi \cdot N} \cdot \frac{1}{s^2 C_2} \cdot \frac{(1+st_Z)}{(1+st_p)\cdot(1+st_4)} \qquad (3.7)$$

The crossover frequency ω_{co} can be approximated as

$$\omega_{co} \approx \frac{Iqp \cdot K_{VCO} \cdot R_1}{2\pi \cdot N} \cdot \frac{C_1 + B \cdot C_2}{C_2} \approx \frac{Iqp \cdot K_{VCO} \cdot B \cdot R_1}{2\pi \cdot N} \qquad (3.8)$$

where Iqp is the current flow of the charge pump at filter input A. In Eq. 3.8, C_1 is assumed that it can be neglected with respect to BxC_2 and it is generally true in this design. In this equation, K_{PD} is assumed to be Iqp/(2π), which defines as current per radian change and is true in the case of high-impedance tri-state PFD used.

The zero $\omega_z=1/\tau_z$ will be designed at a frequency a factor of α below the loop bandwidth and the high-frequency pole $\omega_p=1/\tau_p$ will be placed at a frequency a factor β above ω_c. In order to maintain the loop stability, the parameters α and β should be chosen to preserve

enough phase margin for the loop. For phase margin of approximately 60^o, β is set to 6 and α is equal to 4 in the case of fourth-order type-two loop. The forth pole $\omega_4=1/\tau_4$ coincides with ω_p in order to obtain the best results for noise and spur suppression outside the loop bandwidth with the large enough phase margin. The resister R4 is defined as a factor γ smaller than R_1 and thus C_4 must larger than C_1 by the same amount.

The passive element values can be calculated as follows:

$$
\begin{aligned}
R_1 &= \frac{1}{B}\cdot\frac{2\pi\cdot N}{I_{qp}\cdot K_{VCO}}\cdot\omega_c \\
C_1 &= \frac{1}{B}\cdot\frac{1}{R_1\cdot\omega_c} \qquad R_4 = \frac{R_1}{\gamma} \\
C_2 &= \frac{\alpha}{\beta}\cdot\frac{1}{R_1\cdot\omega_c} \qquad C_4 = \gamma\cdot C_1
\end{aligned}
\tag{3.9}
$$

In a monolithic frequency synthesizer, the passive element values should be chosen as smaller as possible under the constraint of noise specifications, especially the values of the capacitors, because the larger the values are, the larger the chip area required. In the design of low-noise synthesizer, the capacitor values are generally as large as several tens of nano-F, which is not desirable for monolithic design. From the above equations, we can found that the factor B helps to reduce the values of R_1 and C_1. Thus, the noise generated from R_1 is smaller than the conventional design and at the same time, the active area of the filter can be decreased with the expense of the filter complexity. The crossover frequency also has effect on the element values. The smaller this frequency is, the larger the values of the capacitor. With the dual-loop architecture, the loop bandwidth of PLL can be increased. It not only increases the locking speed of the synthesizer but also reduces the filter chip area. Moreover, from Eq. 3.9, its is found that the element values can further be lowered by reducing the charge pump current I_{qp} and the K_{VCO} of the VCO.

3.5 Phase Noise Contribution

In order to meet the stringent phase noise specifications shown in Table 3.1, the phase noise of the VCO as well as that of others components should be considered very carefully. In this section, we will estimate the noise contributions from the filter, the charge pump and the Opamp to the output spectrum. With the assumption of a good quality crystal reference, the close-in phase noise of the output spectrum is mainly dominated by the noise of resistors, the active element and the charge pump in the VCO control signal path.

The charge pumps will generate current noise, which is proportional to its current level. The noise transfer function from the first noisy charge pump at input A is given by [2]:

$$\frac{\mathsf{f}_{out}(s)}{di_{nqp1}(s)} = \frac{H_I(s)\cdot H_4(s)\cdot K_{VCO}}{s + \dfrac{K_{PD}\cdot K_{VCO}\cdot G(s)}{N}} \qquad (3.10)$$

and that of the second charge pump equals

$$\frac{\mathsf{f}_{out}(s)}{di_{nqp2}(s)} = \frac{\dfrac{H_L(s)}{B}\cdot H_4(s)\cdot K_{VCO}}{s + \dfrac{K_{PD}\cdot K_{VCO}\cdot G(s)}{N}} \qquad (3.11)$$

The noise current magnitudes generated from the charge pumps can be estimated by

$$\begin{aligned} di_{nqp1}{}^2 &= 2\mathsf{l}_{on}\cdot 4kT\cdot g_{m,qp1}\cdot df \\ di_{nqp2}{}^2 &= 2\mathsf{l}_{on}\cdot 4kT\cdot B\cdot g_{m,qp1}\cdot df \\ \textit{where} \quad g_{m,qp1} &\approx \frac{2I_{qp}}{V_{gs}-V_t} \end{aligned} \qquad (3.12)$$

and λ_{on} is the on factor of the charge pump. The noise contribution is reduced by this factor because the noise sources are on only for a small duration over a reference period. The current noise of the charge pump at input terminal B is a factor of B larger than that at terminal A

because of the different current levels used. The equations point out that the larger the g_m, the more current noise is produced from the charge pump output. Therefore, in order to lower the noise, a larger V_{gs}-V_t value is wanted of the transistors in the design of charge pump current source.

The total noise contribution can be obtained by putting Eq. 3.12 into the noise transfer function of each charge pump input and then adding the results quadratically. The single sided spectral phase noise at $\Delta\omega$ offset from the carrier becomes

$$L_{qp}\{\Delta w\} = \frac{1}{2}\frac{\frac{(H_L(s))^2}{B} + H_I{}^2(s)}{\left(s + \frac{K_{PD}\cdot K_{VCO}\cdot G(s)}{N}\right)^2}\cdot H_4{}^2(s)\cdot K^2{}_{VCO}\cdot 8\mathrm{l}_{on}\cdot kT\cdot g_{m,qp1} \quad (3.13)$$

From the above equation, it is found that this filter reduces the phase noise contributions from the charge pumps approximately a factor B compared to the conventional 4^{th}-order loop filter design with the same total charge pump output current level, which is (B+1) x I_{qp}.

In the loop filter, the thermal noise generated by the passive resistors will also contribute to the output phase noise. The phase noise contributed from R_1 can be calculated as follows:

$$L_{R1}\{\Delta w\} = \frac{1}{2(1+sC_1R_1)^2}\frac{H_4{}^2(s)\cdot K^2{}_{VCO}}{\left(s + \frac{K_{PD}\cdot K_{VCO}\cdot G(s)}{N}\right)^2}\cdot 4\cdot kT\cdot R_1 \quad (3.14)$$

This equation shows that the noise generated from R_1 is filtered by the low-pass function formed by R_1 and C_1. Similarly, the phase noise generated by R_4 can be given by

$$L_{R4}\{\Delta w\} = \frac{1}{2}\frac{H_4{}^2(s)\cdot K^2{}_{VCO}}{\left(s + \frac{K_{PD}\cdot K_{VCO}\cdot G(s)}{N}\right)^2}\cdot 4\cdot kT\cdot R_4 \quad (3.15)$$

Finally, we should consider the noise produced by the Opamp in the filter because it is also placed at the sensitive control path of the VCO. The phase noise contributed by Opamp to the output can be given by

$$L_{OP}\{\Delta w\} = \frac{1}{2}\frac{{H_4}^2(s)\cdot {K^2}_{VCO}}{\left(s+\frac{K_{PD}\cdot K_{VCO}\cdot G(s)}{N}\right)^2}\cdot {i^2}_{op} \qquad (3.16)$$

where i^2_{op} is the input-refer current noise of the Opamp in unit of A^2/Hz. In order to minimize the noise from the Opamp, the circuit needs to burn a lot of power. This is one of the disadvantages for the active loop filters.

From the noise transfer functions shown, it can be found that the close-in phase noise contribution of each noise source is enlarged by the division ratio *N* [2]. Moreover, the power of noise is also increased by a factor of K_{VCO}^2. Therefore, for larger value of *N* or K_{VCO}, larger capacitance values are required to achieve the same phase noise specification compared to the case of small *N* or K_{VCO}.

3.6 Optimization of the Parameters

As discussed previously, an optimal choice of parameters such as the phase margin of the loop, the charge pump current, the current factor B, the factor γ and the passive element values of the filter requires very careful consideration for the stability, the phase noise performance and the dynamic of the loop. This cannot be represented by a simple formula and thus this was done using MATLAB and a behavioral linear model for the PLL, which is implemented in HSpice.

In order to obtain approximate 60° phase margin for stable loop behavior, β and α are set to 6 and 4, respectively. The predicted VCO constants K_{VCO} of the upper loop and lower loop are 200 MHz/V and 500 MHz/V, respectively. The fixed division ratio of the upper loop is 16 and the maximum division ratio of the lower loop is 1025. The remaining loop parameters such as ω_c, I_{qp} and B are incorporated into the optimization. The goal is to achieve the phase noise specification of DCS-1800 with a minimized chip area. We started with setting the current of the charge pumps as small as possible because it will give smallest capacitor values according to Eq. 3.9. However, it cannot be set to very low current because the output phase noise increases and the charge injection of the transistor switch in the pump enlarges the magnitudes of the reference spurs. With this minimum pump current, other parameters are designed so that the close-in and out-of-band phase noise specifications can be met. A few iterations of this process may be required to obtain the optimal parameters. The phase noise plots, which is based on the equations stated in previous section, using MATLAB are shown in Figure 3.6 and Figure 3.7.

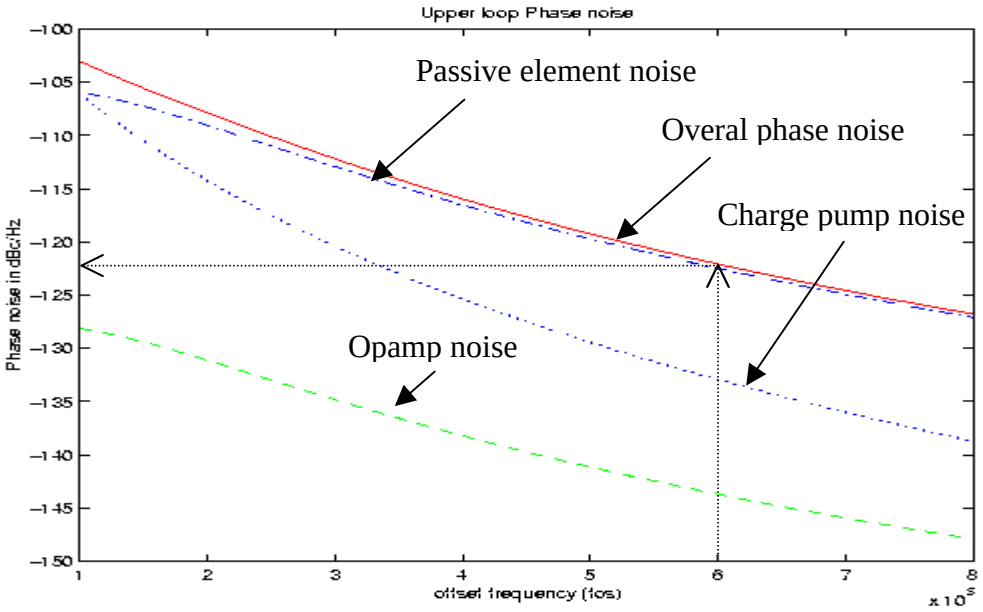


Figure 3.6 The phase noise plot of the upper loop

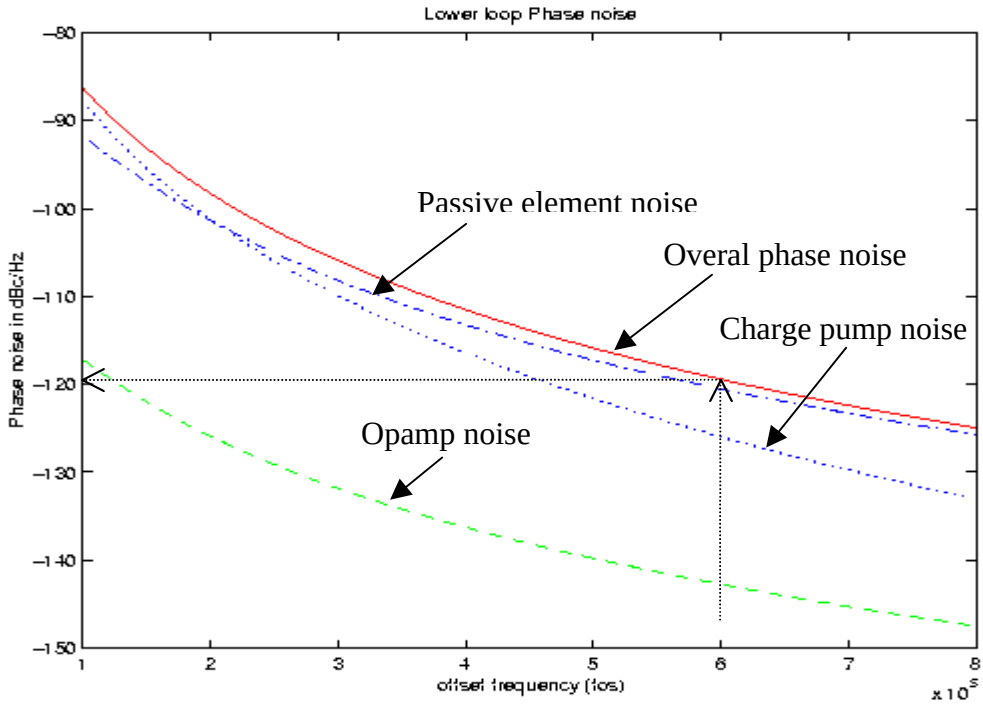


Figure 3.7 The phase noise plot of the lower loop

The final loop parameters and phase noise performance are summarized in Table 3.2. A charge pump of 1 μA is used, and the loop bandwidth of the upper loop and lower loop are 120 kHz and 42 kHz, respectively. The loop bandwidth should be large enough for the required settling time. The total phase noise of the lower loop is –119.4 dBc/Hz, which is small enough as the noise will be further reduced by the prescalar X and the upper-loop filter. The overall phase noise of the upper loop is –122.8 dBc/Hz with 3-dB margin from the desired -119 dBc/Hz requirement of DCS-1800. Moreover, the division ratios and K_{VCO} have been set to the values in the worst-case situation of phase noise performance. The total capacitance is in the order of 1000 pF because it is necessary in order to achieve the required low phase noise.

Parameters		**Upper loop**	**Lower Loop**
Reference Frequency	f_{ref}	100 MHz	800 kHz
Loop bandwidth	ω_c	120 kHz	42 kHz
Charge pump current	I_{qp}	1 μA	1 μA
Zero frequency	f_z	30 kHz	10.5 kHz
Pole frequency	f_p	720 kHz	252 kHz
Pump current ratio	B	120	350
Fourth pole ratio	γ	1	2
Passive elements	R_1	502 Ω	2.26 kΩ
	C_1	439.8 pF	279 pF
	C_2	87.95 pF	19.16 pF
	R_4	502 Ω	1.13 kΩ
	C_4	429.8 pF	558 pF
Phase noise @ 600 kHz offset			
Charge pump	L_{QP}	- 132.94 dBc/Hz	- 126 dBc/Hz
Resistor R_1	L_{R1}	- 126.79 dBc/Hz	- 126.9 dBc/Hz
Resistor R_4	L_{R4}	- 124.5 dBc/Hz	- 121.69 dBc/Hz
Total passive elements	L_{RS}	- 122.48 dBc/Hz	- 120.5 dBc/Hz
Opamp	L_{OP}	- 142.8 dBc/Hz	- 142.8 dBc/Hz
Total	L_{TOTAL}	- 122.08 dBc/Hz	- 119.4 dBc/Hz

Table 3.2 The final PLL parameters

After the parameters are fixed, Spice behavioral model is used to check the open-loop transfer function and obtain the requirements of some building blocks such as the charge pump and the Opamp. The simulation time of this model is much faster than the transient simulation.

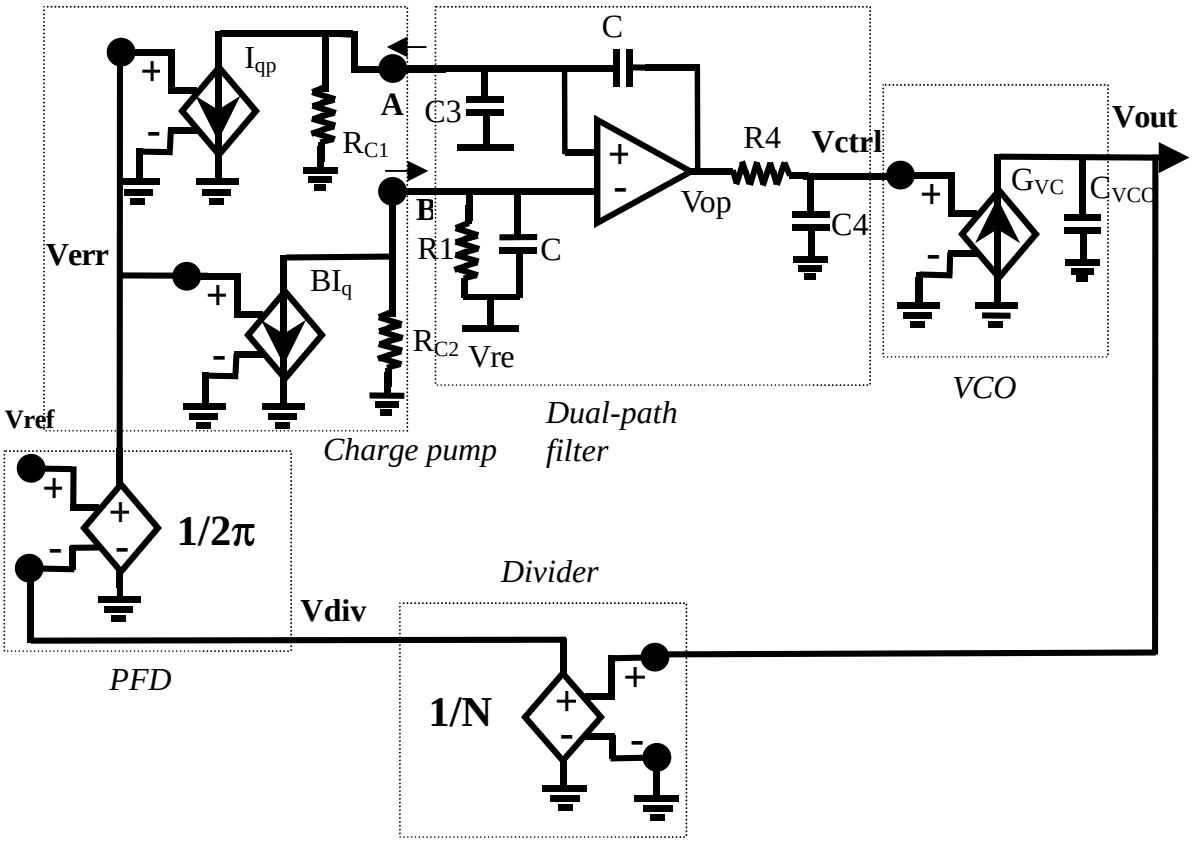


Figure 3.8 HSpice behavioral voltage model

The small-signal behavioral model of the loop is shown in Figure 3.8. In the model, the phases are represented by the voltages. The phase detector and the frequency divider can be modeled by the voltage-controlled voltage source with the scalar 1/2π and 1/N, respectively. The charge pumps are made using two voltage-controlled current sources. To implement the VCO transfer characteristic, a voltage-controlled current source G_{VCO} with a capacitance load C_{VCO} is used. The K_{VCO} is equal to G_{VCO}/C_{VCO}. The resistor R_{C1} and R_{C2} are added to model the finite output resistance of the pump. In the filter, the Opamp is replaced by a voltage-controlled voltage source with finite gain and bandwidth. Using the model shown in Figure 3.9, the open-loop responses can be found by breaking the loop at the output node Vdiv of the divider. In the simulation, the Opamp used has voltage gain of 60 dB, one zero located at 1 MHz, and two poles located at 10 MHz and 1k Hz, respectively. The charge pumps have 10

MΩ output resistance. The plots of the open-loop gain and phase are shown in Figure 3.9 and Figure 3.10. The simulation results show that the desired positions of the poles and zeros maintain. The phase margins of the upper and lower loop are 55^{o} and 60^{o},respectively.

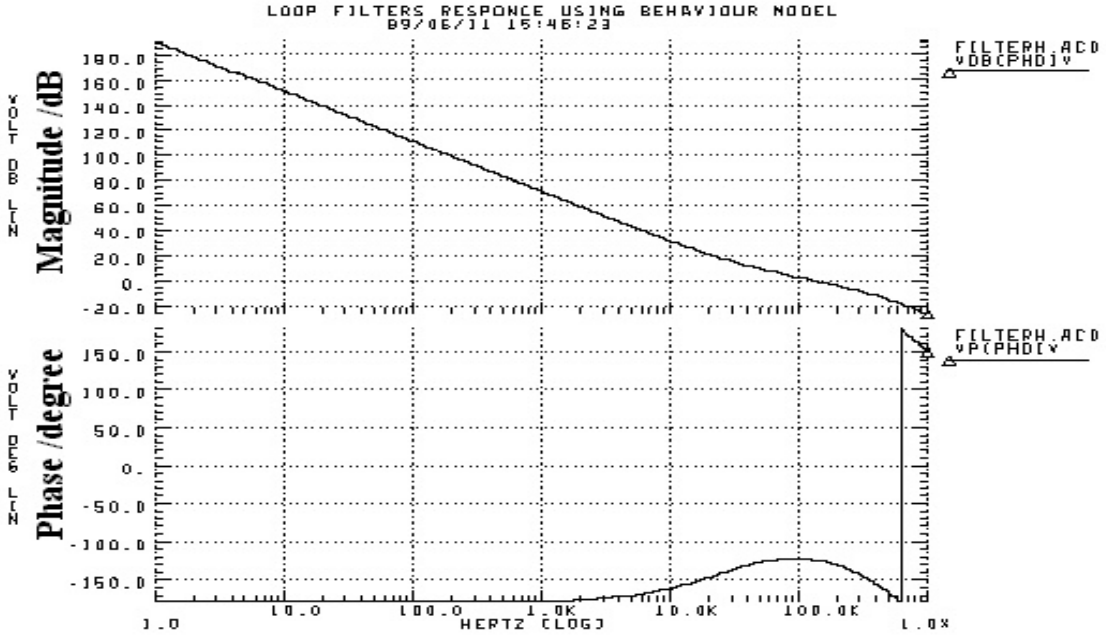


Figure 3.9 Open-loop response of the upper loop

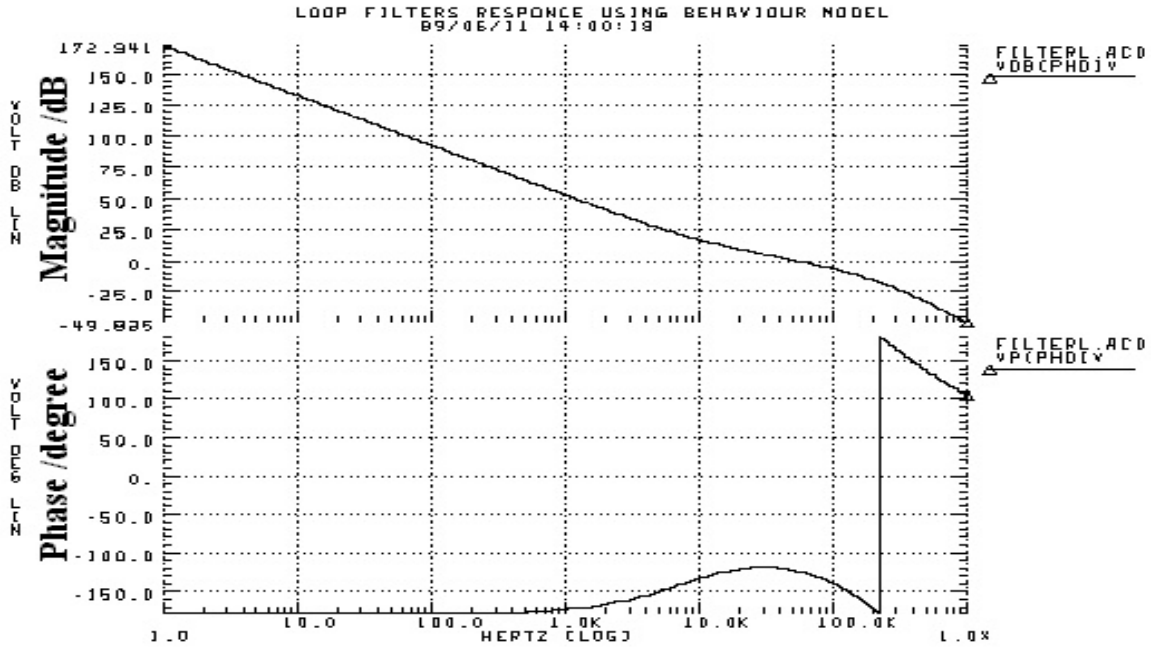


Figure 3.10 Open-loop response of the lower loop

Figure 3.11 and Figure 3.12 further show the designed closed-loop responses of upper and lower loops.

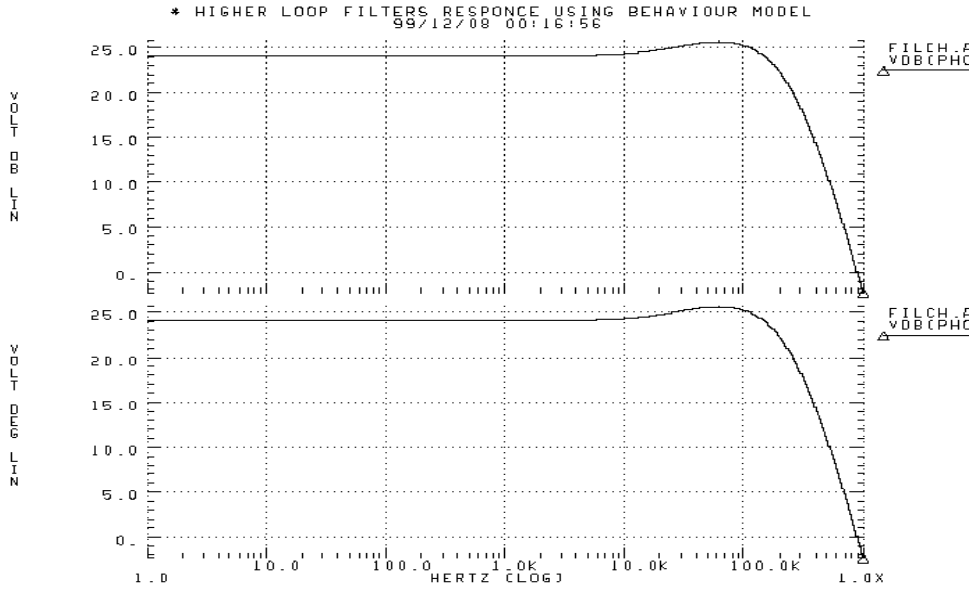


Figure 3.11 Close-loop response of the upper loop

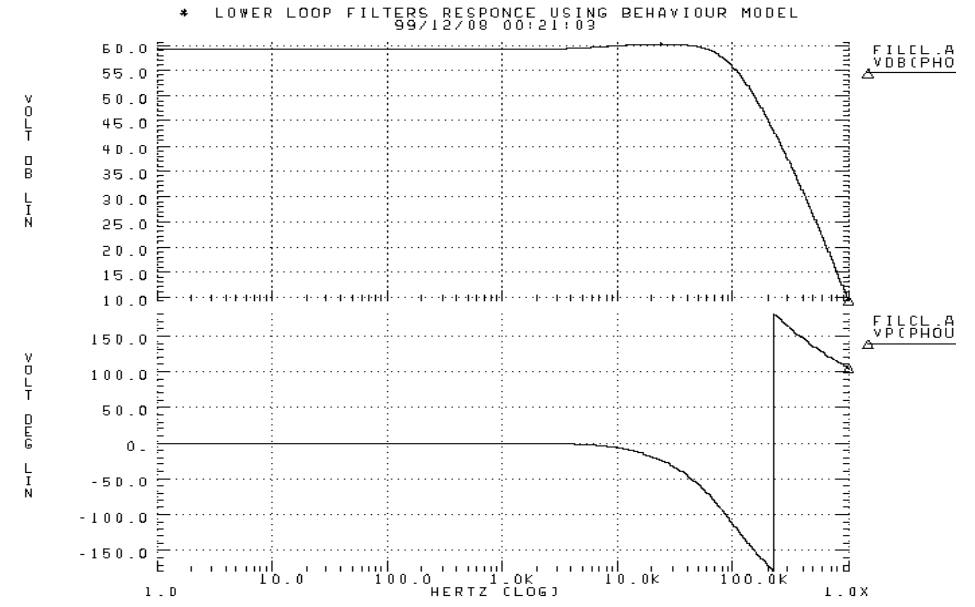


Figure 3.12 Close-loop response of lower loop

References

[1] J. Crols and M. Steyaert, ”CMOS Wireless Transceiver Design”, Kluwer Academic Publishers, 1997

[2] J. Craninckx and M. Steyaert, “A Fully Integrated CMOS DCS-1800 Frequency Synthesizer”, *IEEE Journal of Solid-State Circuit*, Vol. 33, No. 12, Dec. 1998.

[3] T.Aytur and John Khoury, “Advantages of Dual-loop Frequency Synthesizers for GSM Applications”, *IEEE International Symposium on Circuits and Systems*, June 9-12, 1997.

[4] Behzad Razavi, “Challenges in Design of Frequency Synthesizers for Wireless Applications” ”, *Proc. of the IEEE 1997 Custom Integrated Circuits*, pp.395-402, 1997.

Chapter 4 Building Block Design

In this session, the design of each building block will be discussed. The block diagram of the synthesizer is shown again in Figure 4.1 for reference.

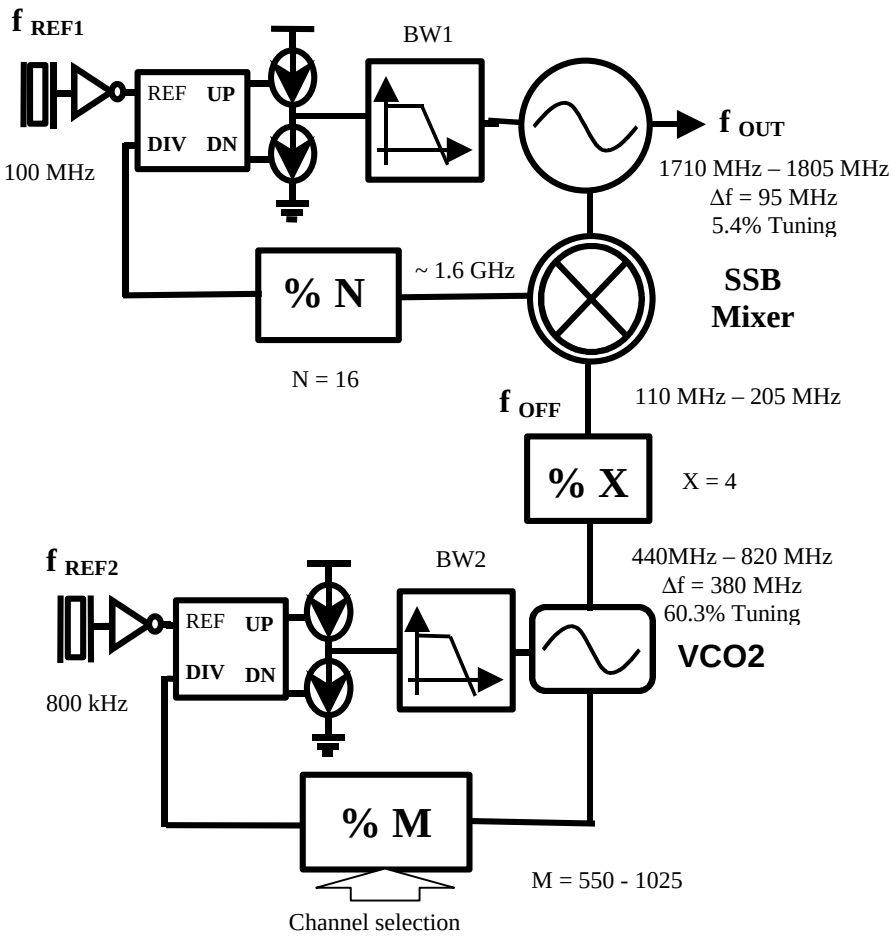


Figure 4.1 Block diagram of the synthesizer

4.1 LC Oscillator

In order to achieve the phase noise specification for the synthesizer, the high-frequency oscillator at the synthesizer output should have a very good phase noise performance. As long as the tuning range required is not too wide, this can be done by using a good quality LC-type oscillator. The design issues on a 1.8-GHz CMOS LC-Oscillator with quadrature outputs will be presented in this section. We will firstly consider the passive elements in the LC-tank and then discuss the design of the oscillator. Finally, the phase noise estimation will be given.

4.1.1 Optimization of Passive components

The basic operation principle of the LC-tank-type oscillator is using a negative transconductance cell to compensate the resistive loss in the LC-tank in order to start and sustain oscillation. Therefore, to design a low phase noise LC VCO, it is a must to have a good quality LC-tank. Unfortunately, we cannot easily obtain good quality inductors and varactors in existing standard CMOS processes, especially for the case of inductors. In most cases, the performance of an LC-tank will be determined by the quality and the parasitic of the inductor. In this section, the optimization on the passive components is discussed in detail. Before further discussion, a general definition of the parallel LCR-tank quality factor Q is given here:

$$Q_{LCR}(\omega_o) = 2\pi \cdot \frac{\textit{Peak energy stored}}{\textit{Energy loss per cycle}} = 2\pi \cdot \frac{\frac{C \cdot V^2}{2}}{\frac{\pi \cdot V^2}{\omega_o \cdot R_{eqp}}}$$

$$= R_{eqp} \cdot \omega_o C \qquad (4.1)$$

$$= R_{eqp} \cdot \sqrt{\frac{C}{L}}$$

The quality factors for a single inductor, a capacitor and a basic LC-tank oscillator configuration are estimated as

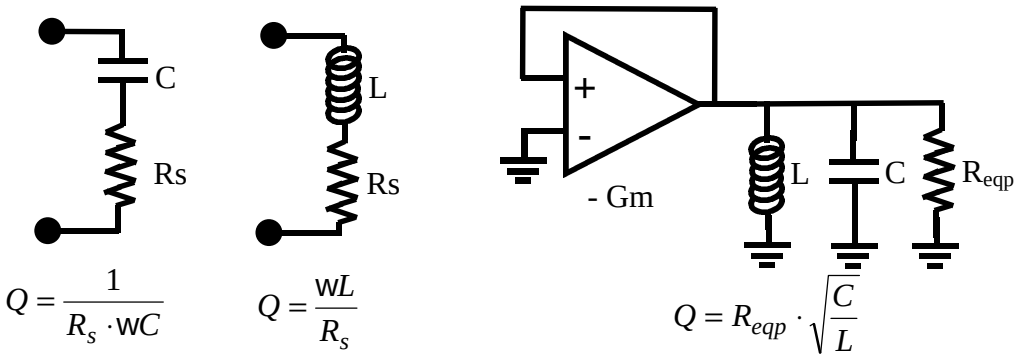


Figure 4.2 Quality factors for the passive elements

4.1.1.1 Inductor Design

The important requirements of a monolithic inductor include low cost, large inductance with predictable value, small series resistance, low substrate loss, small area and high self-resonance frequency. In standard CMOS processes, on-chip inductors are mostly realized by spiral-shaped planar metal coils. On-chip spiral inductors can offer low cost and small variations in the inductance, and no post-processing step required. However, they suffer from a lot of parasitic, which limit their quality factor at high frequencies. Extensive calculation of the inductance of the spiral inductors is based on Greenhouse formula [1]. Figure 4.3 shows a monolithic planar inductor on a CMOS substrate and its simple π model.

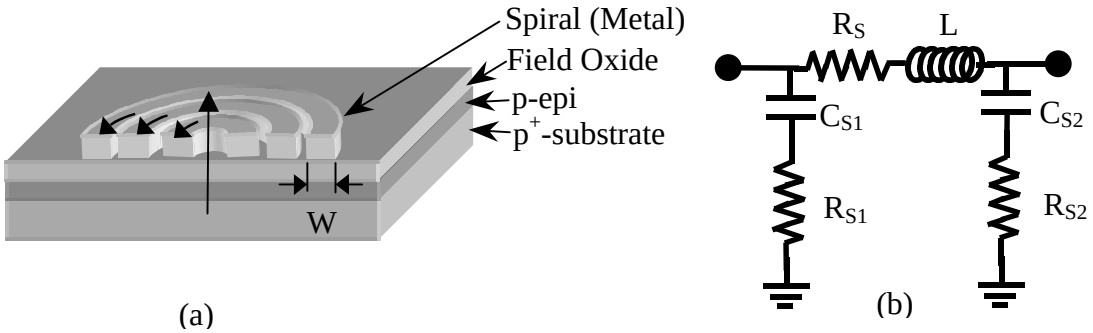


Figure 4.3 (a) the monolithic planar inductor (b) the simple π model.

In this project, HP 0.5-μm CMOS process is used, which has a p-epi layer above a high-conductive p^+ substrate and three aluminum metal layers for interconnection. In the π model, the loss of inductors is modeled by a series resistor R_S and two resistors R_{S1} and R_{S2}. The capacitors C_{S1} and C_{S2} are added as the parasitic coupling capacitors from the inductor to the substrate. The inductor and the its parasitic capacitors of the spiral form a LC-tank, which determines its self-resonant frequency and governs its maximum usable frequency range.

The Q-factor of monolithic high-frequency planar inductors in CMOS processes mainly suffers from four sources of loss. First, it corresponds to the low frequency resistance loss of the metal track of the inductor. The resistance value can be calculated by the sheet resistance and the number of squares of the track. Making the track wider and connecting several layers in parallel can reduce this kind of loss. A second and important effect is the high-frequency skin effect loss. At high frequency, the current flow in the inductor is non-uniform and crowds at the edge of the conductor. The loss is inversely proportional to the skin depth at that particular frequency. At 1.8 GHz, the skin depth for aluminum is around 1.92 μm. Therefore, at high frequencies, the conductance of the metal is limited by the skin effect and cannot improve even if the track width is increased. Thirdly, the induced eddy currents in the heavily doped substrate degrade the overall quality factor of the inductor. The induced current flow is generated to oppose the magnetic field created by the inductor. The magnitude of eddy currents is proportional to the change in magnetic field with respect to time and hence it becomes more and more serious with increasing of the frequency. The eddy currents cause extra resistive losses and decrease in inductance value of the coil. As the inductor area increases, more current induces in the substrate and the loss is further increased. Therefore, the inductor size should be limited to a small enough value to limit such kind of loss. The eddy currents are also induced in the metal track itself. The effect is more obvious at the inner

turn of the coil. The high-frequency effective resistance of the inner turns is much larger than that of the outer side and hence hollow coil should be used. Figure 4.4 illustrates the eddy current effect in the high conductive substrate and in the innermost turn of the planar inductor. The skin effect and the magnetic effects become increasingly serious with the frequency and limit the obtainable Q-factor of the planar inductor. Finally, the lossy capacitive coupling to the substrate further degrades the Q-factor of the inductor.

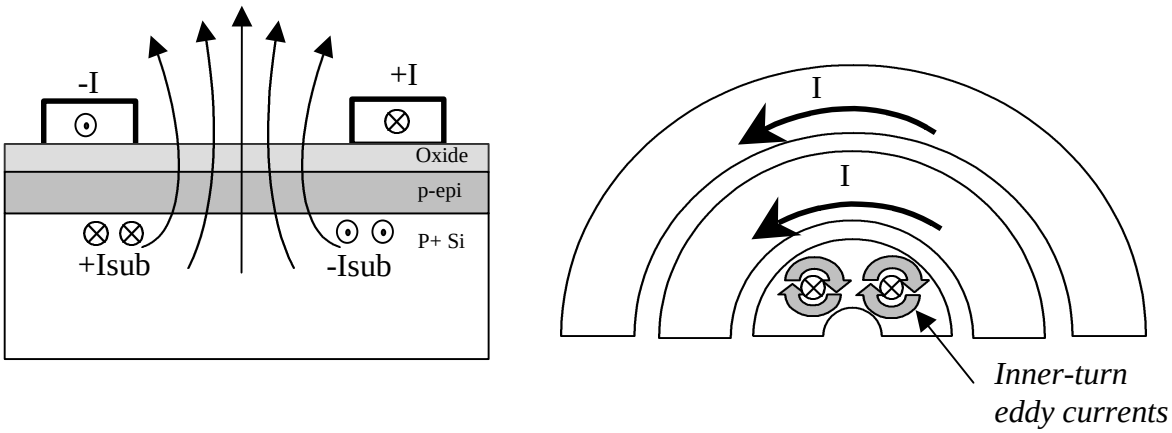


Figure 4.4 eddy current (a) at the substrate and (b) at the inner turn

A smaller resistive loss and lower substrate loss improve the Q-factor of the inductors and hence the noise performance of the LC-type VCO. One of the important goals of the inductor design is minimizing the total effective resistance resulted from the dc and ac resistive losses. The width of the track is set until the skin effect becomes non-negligible. A custom CAD tool *ASITIC* [2] is used to do the optimization. The program calculates the inductance using Greenhouse formula and considers almost all the mentioned loss mechanisms but the eddy current loss in the substrate

In the HP-0.5μm CMOS process, metal layer one and two have resistance of 0.07 Ω / and metal layer three has resistance of 0.05 Ω / . The inductor is in the shape of circular to reduce the corner resistance of the rectangular-shape design. The circular shape also gives

smaller resistance for a particular inductance because the circle is the shape with the smallest perimeter for a given area. The spacing between tracks is set to the minimum possible value according to the design rule so that mutual inductance can be maximized. In order to limit the substrate loss due to eddy current, the inductor is limited to the radius not larger than 95 μm [3]. A small area of the inductor can also lower the cost of the design. In order to decrease the series resistance and enhance the inductance, the planar inductor is made by top two layers of metal. In multi-layer planar inductor, the dc resistance is proportional to the number of turn n while the inductance is proportional to n^2 and hence the Q-factor can be increased. Moreover, the smaller area of the multiple layer inductor compared to single layer design with the same inductance value can improve the loss to substrate [4]. However, more parasitic capacitance is resulted when two-layer inductor is used. The final parameters of the inductor is shown as follows:

Design parameters	Metal two	Metal three	Model parameters	
Radius (R)	90 mm	95 μm	L	3.070 nH
Width (W)	22.2 μm	17.4 μm	R_S	4.837 Ω
Spacing (SP)	1.5 μm	1.2 μm	C_{S1}	0.190 pF
Turns (T)	1.7	2.4	R_{S1}	0.156 Ω
inductance	2.825 nH	1.1251 nH	C_{S2}	0.263 pF
			R_{S2}	1.179 Ω
			Q (1.8GHz)	6.632

Table 4.1 Parameters of the two-layer inductor

4.1.1.2 Varactor Design

Although the overall Q-factor of the LC-tank is dominated by the inductor, a good quality varactor is important to avoid further degrading the tank quality. In other words, the series resistance of the variable capacitor should be small. While P-N junction varactors are

widely used, accumulation-mode varactors offer a better average Q-factor over different biasing conditions with a larger tunable capacitance [5]. Figure 4.5 shows the cross-section, the simplified model and the actual layout of accumulation mode varactor.

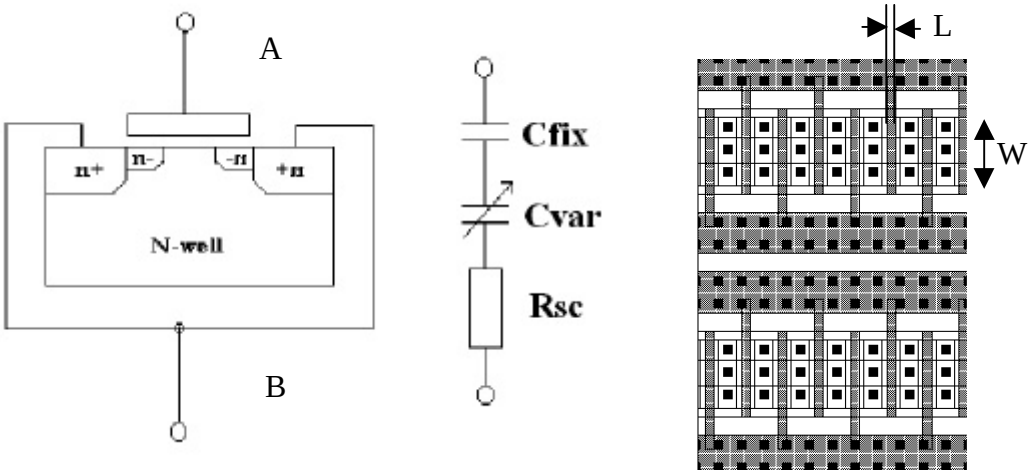


Figure 4.5 The cross-section, the simplified model and the actual layout of accumulation-mode varactor.

The structure is similar to an N-channel MOSFET transistor with the exception of being fabricated on an n-well instead of the p-substrate because of the higher mobility of n-carriers. The drain and source terminals are doped with n+ in order to reduce the parasitic pn-junction capacitance and thus to obtain larger variation of the capacitance. The basic operation of the device is similar to a standard MOS structure and the large capacitance variation from accumulation mode to flat-band region is utilized to obtain the varactor function. By applying a gate voltage much larger than the flat-band voltage, electrons are accumulated in the surface and the overall capacitance is simply the oxide capacitance. When the voltage is decreased towards the flat-band voltage, there is a depleted layer between the oxide and the n-well. The resulted capacitance is approximately the depletion capacitor and the oxide capacitor in series. The Q-factor of the varactor is increased by decreasing the channel length (L), reducing the width (W) and increasing the number of the gate fingers (N).

4.1.2 Design of The Oscillator

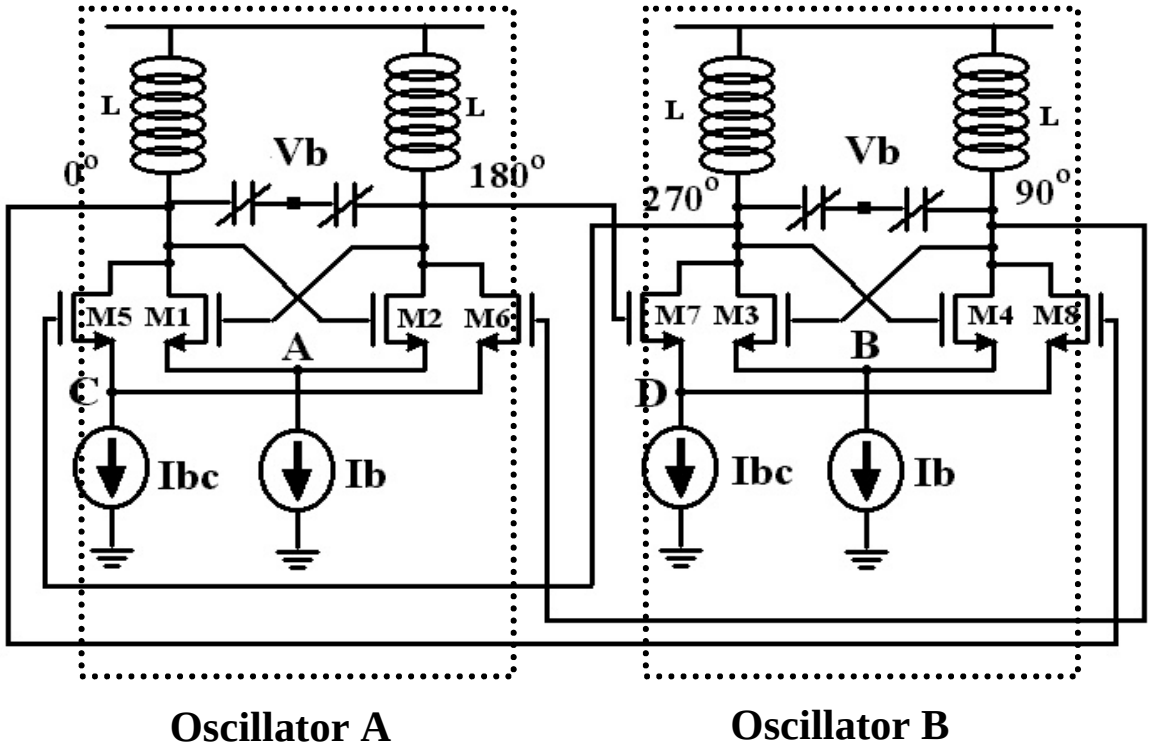


Figure 4.6 Schematic of the quadrature LC-oscillator

The schematic of a 1.8-GHz LC-oscillator is shown in

Figure 4.6 [6]. The oscillator consists of two individual oscillators, which are forced to have quadrature oscillation by the direct-coupling transistors (M7 and M8) and the crossed-coupling transistors (M5 and M6). Each transistor in the coupling stages can provide 90^o phase shift to the input signal. The quadrature outputs are required to drive the SSB mixer in order to obtain the image rejection function of SSB mixing. The transistors M1, M2 M3 and M4 of the negative transconductance pairs are used to compensate the loss in the LC-tank in order to obtain oscillation. The oscillation frequency is according to the following equation:

$$fo \approx \frac{1}{2\pi\sqrt{LC}} \cdot \sqrt{1-\frac{R_{SL}{}^2 C}{L}} \approx \frac{1}{2\pi\sqrt{LC}} \cdot A_{loss} \qquad (4.2)$$

where it is assumed that the Q-factor of the inductance dominates the overall Q and the equivalent series resistance of the inductor is R_{SL}. We can see that the Q-factor not only affects the noise performance of the oscillator, but also shifts down the oscillation frequency of the oscillator if the Q value is too small. The oscillation frequency reduction factor A_{loss} is around 0.88 with the estimated R_{SL}. The total capacitance C of the node can be given by

$$C \approx (C_{\text{var}} + C_{fv}) + C_A + C_{coup} + C_L \qquad (4.3)$$

where C_{var} is the variable capacitance provided by the varactor, C_{fv} is the fixed part of varactor's capacitance, C_A is the parasitic capacitance of the negative Gm cells, C_{coup} is the parasitic capacitance of the coupling transistors and C_L is the loading of the subsequent stage. Thus, the total capacitance consists of the fixed parasitic capacitance and a variable capacitance part provided by the varactor. The larger the inductance used, the smaller the capacitance required and lower power consumption can be obtained. However, in order to have large enough tuning range, the resulted C cannot be set to too small value. In this design, L is fixed to 3nH and C is roughly 2 pF. The value of (C_{fv} + C_{var}) is around 0.5pF. The overall effective single-ended series resistance [7] of the LC tank can be calculated as follows:

$$R_{eff} = R_{SL} + R_{SCV} + \frac{1}{R_A(2\pi f_o C)^2} \qquad (4.4)$$

where R_{SCV} is the effective series resistance of the varactor and R_A is the impedance of the gm cells. In the calculation, the value of R_{SL} is taken to be double the value of Rs obtained by *ASITIC* as show in Table 4.1 in order to take the high-frequency substrate loss into account. The Q-factor of the varactor is assumed to have around 25 and equivalently it is equal to R_{SCV} of 7 Ω for a varactor's capacitance is 0.5 pF. In this design, the resulted R_{eff} is approximately equal to 17 Ω.

The negative transconductance g_m required can be calculated as follows:

$$g_m = 2R_{eff}\left(\omega_o \frac{C}{2}\right)^2 = \frac{2R_{eff}}{(\omega_o 2L)^2} \qquad (4.5)$$

where C is the total single-ended capacitance and L is the single ended inductance of the LC tank. The required g_m is around 7.8 mS but in order to ensure proper start-up of the oscillation, the transconductance value used (G_m) is double of this required value. The bias current I_b and the W/L ratio of the transistors in the negative g_m pairs are given by

$$\left(\frac{W}{L}\right)_{M1} = \frac{G_m}{2\mu C_{ox}\cdot(V_{gs}-V_t)_{M1}}$$

$$I_b = 2\times\frac{G_m\cdot(V_{gs}-V_t)_{M1}}{2} \qquad (4.6)$$

In order to obtain larger tuning range by utilizing the high-gain region of the varactor's C-V characteristic and a proper common-mode biasing to the subsequent stage, a common-mode voltage of 1.3V is more preferable than 2V. This can be done by connecting a PMOS transistor, which acts as a resistor, to the common node between the two inductors in the two oscillators. However, the imperfect virtual ground at this common node for large signal operation will contribute to extra-lossy resistance to the inductors and degrade the quality of the LC tank. Therefore, a 1.3-V supply is used instead of a normal 2-V supply in this oscillator. It also allows larger oscillation amplitude without putting the transistors in the linear region. Spice simulation shows that the oscillator can tuned from 1.767 GHz to 1.875 GHz and 5.9 % tuning ability is obtained. The tuning is larger than the value required so that it can compensate the unpredicted center frequency shift after fabrication. The single-ended output amplitude is around 0.85 Vp.

Finally, the expected phase noise at 600-kHz offset can be estimated by

$$L\{600kHz\} = \frac{kT(2R_{eff}) \cdot (1+A) \cdot \left(\frac{\omega_o}{\Delta\omega}\right)^2}{V_A{}^2/2}$$
$$= \frac{(0.0259 \times 1.6 \times 10^{-19}) \cdot (2 \times 17) \cdot (1+2) \cdot \left(\frac{1.8G}{600k}\right)^2}{(1.7)^2/2} \qquad (4.7)$$
$$= -119\ dBc/Hz$$

where A is the noise-amplifying factor of the amplifier and V_A is the differential output amplitude. The factor A is roughly governed by the additional current used for the proper start-up of the oscillation and it is around 2 in this design. Eq. 4.7 shows that the phase noise is increased with the square of the center frequency and decreased with the square of the oscillation amplitude.

4.2 Ring-type Oscillator

The requirements of the lower-loop oscillator are having the center frequency of 630MHz and a tuning range around 400 MHz with tuning voltage vary from 0 to 2V. The phase noise should be smaller than –108 dBc/Hz at 600kHz offset from the carrier. In order to obtain such a large tuning range, a ring oscillator is used instead of a LC-tank oscillator, which has a typical frequency-tuning range limited to around 10-20%. The feasibility of low-noise CMOS ring oscillator that can be comparable with the performance of monolithic LC oscillators has been proven [10]. In this section, we present the design of a ring oscillator using negative delay path with normal delay path to achieve low-phase noise performance. The delay cell is designed to have large tuning ability and to achieve constant phase noise as well as constant output signal amplitude throughout the tuning range.

4.1.3 Circuit Design of The Oscillator

The oscillator is similar to the conventional four-stage ring oscillator with the exception of a negative delay path. Negative skewed delay path is employed with the normal delay path to obtain higher frequency operation and enhance the tuning range.

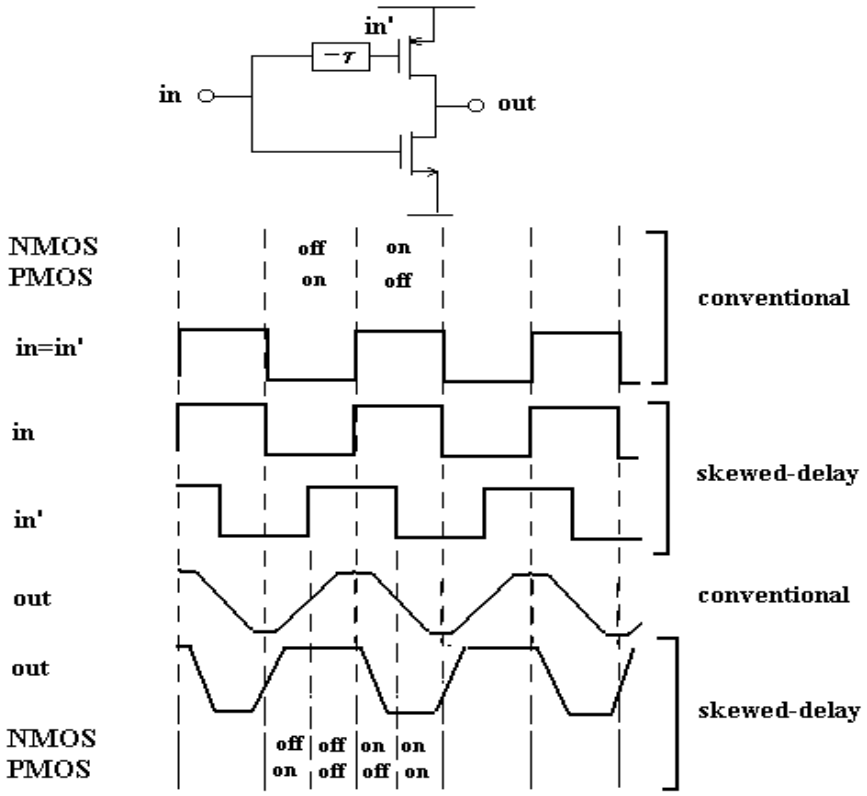


Figure 4.7 The ideal of negative skew

The simplified conceptual diagram of the negative delay skew idea is exhibited in Figure 4.7 [11]. As shown in Figure 4.7, unlike conventional delay cell, the negative-skewed cell turns on the PMOS before low-to-high output transition and turns off the PMOS before the high-to-low output transition. It speeds up the transitions and offers higher maximum achievable oscillation [11]. Moreover, It compensates the poor performance of PMOS in CMOS technology comparing with NMOS transistors. The improved performance is obtained with the larger power consumption due to the time overlap when both transistors are on.

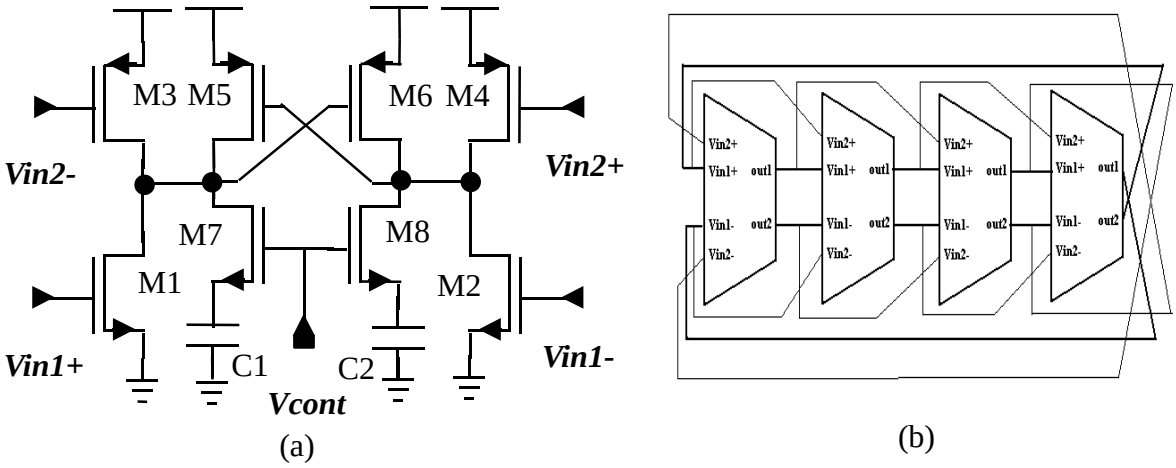


Figure 4.8 The schematics of (a) the differential delay cell and (b) the ring oscillator.

The block diagram of the ring oscillator and the schematic of the delay cell are shown in Figure 4.8. The oscillator has a normal delay path as other conventional differential ring oscillators and also has a negative-skewed delay path. The negative-skewed path is obtained by connecting the outputs of each delay cell to the PMOS inputs of the next delay cell. The differential structure of the delay cells is to attenuate the effect of power supply injected phase noise. Linear ring-shaped NMOS transistors, M7 and M8, in series with a fixed value capacitor are used to tune the RC product of the delay cells. When the controlled voltage *Vcont* is low, the delay is short, which is governed by the parasitic capacitance at output node and the resistance as well as the transconductance of the transistors, M2 and M4 (or M3 and M1). The ring-shaped transistors are to reduce the parasitic capacitance at the output nodes. Thus, it increases the tuning range of the oscillator and maximizes the highest operation frequency of the design. The large variation of resistance under different biasing voltages can provide large enough tuning capability for the design within the supply limit. Moreover, this tuning method can maintain the constant power consumption and constant output signal magnitude. In the delay cell, M5 and M6 form a PMOS latch with the same strength

throughout the tuning range. It helps the delay cell to maintain sharp transition edges with a full switching capability. Because of the short rise and fall times as well as large voltage swing of the output signal, it improves the phase noise performance [12]. Moreover, the latch makes the design oscillating differentially without problems with start-up or common-mode oscillation.

The impulse sensitivity function (ISF) of the oscillator at 970MHz is plotted in Figure 4.9, which is obtained by the simulated output waveform of the oscillator using the method provided from [12].

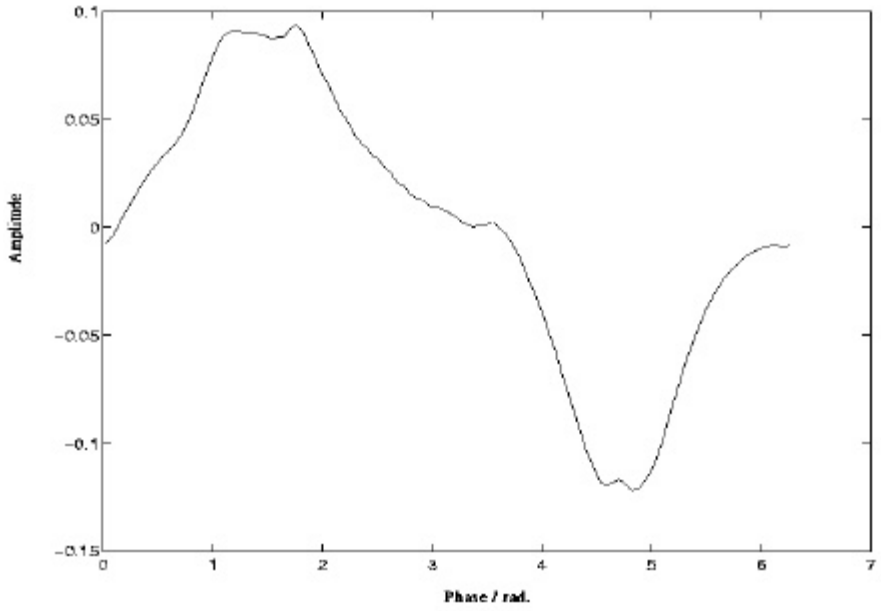


Figure 4.9 The simulated ISF plot of the single node in the ring oscillator using HSPICE.

In a conventional differential ring oscillator, the oscillation frequency is limited by the number of delay cells and the unit delay time of a delay cell. The oscillation frequency can be approximated as $1/(2N\tau)$, where N is the number of stages and τ is the delay of the unit delay cell. To increase the operation frequency, the negative skewed delay path is used. With the

negative skewed delay path, the operation frequency of the oscillator is almost double the value of $1/(2N\tau)$ [11]. Thus, operation frequency of the oscillator can be estimated as $1/(N\tau)$. This means the resulting design has the same total capacitance at the output nodes as the conventional oscillator operating at half of its frequency. Comparing with the oscillators operating at the same frequency without the negative skewed delay path, it therefore can provide better phase noise performance [12]. The maximum amplitude of the ISF is an order smaller than that of the conventional 4-stages ring oscillator [13]. This indicates the improvement of the noise performance in the design comparing to the conventional one.

Furthermore, the skewed delay cell turns on the PMOS before the low-to-high output transition. It compensates the poor performance of PMOS in CMOS technology comparing with NMOS transistors [11]. This makes the signal waveform more symmetrical and therefore diminishes the up-conversion of 1/f noise [13]. Moreover, this ring oscillator can be classified as a saturated-type ring oscillator, which allows the full switching operation of some devices. Thus, it can be modeled as switching on and off on the thermal noise current sources of the MOS devices in different portions of a whole oscillation period, which further reduces the phase noise [11].

The total capacitance at the output nodes (C_{tot}) and the maximum charge accumulated at the node (q_{max}) are modeled as following:

$$\begin{aligned} C_{tot} &\approx C_{gs\_pmos} + C_{gs\_latch} + C_{gs\_nmos} + C_{dsp} + C_{dsn} \\ q_{\max} &\approx C_{tot} \times \Delta V_{swing\_\max} \end{aligned} \qquad (4.8)$$

The average noise contributed to the circuit from the switching thermal noise current sources of the MOS devices is approximated as proportional to the factor (t_{on} / T), where t_{on} is the on

time of the transistors and T is the oscillation period. In this design, we assume this factor is equal to 1/2 due to turning off of NMOS and PMOS devices half of the whole period. Because the ring-shaped NMOS is totally off at its maximum operation frequency, the noise contributed from this transistor is neglected. We further assume the worst case noise performance is at the highest operation frequency due to the trade-off between phase noise and carrier frequency. The size of the latch is only half of the other device's size. Also, the g_m of the NMOS transistors, M1 and M2, and that of the PMOS transistors, M3 and M4, are adjusted to be the same. And the total average noise can be written as following:

$$\frac{in^2}{\Delta f} = \frac{ton}{T} \times \frac{in^2(nmos)}{\Delta f} + \frac{ton}{T} \times \frac{in^2(pmos)}{\Delta f} + \frac{in^2(latch)}{\Delta f}$$
$$where \quad \frac{in^2(nmos)}{\Delta f} = \frac{in^2(pmos)}{\Delta f} = 2 \times \frac{in^2(latch)}{\Delta f} \qquad (4.9)$$
$$and \quad \frac{in^2(tran)}{\Delta f} = 4kT\gamma\, gm$$

The noise is then calculated by assume γ= 2.5 for short-channel devices. Integrating the ISF over 2π, we have Γrms^2 = 6.7223e-2, which is much smaller than the approximate value $\Gamma rms^2 = 3/N^{1.5}$ in [7] for the conventional ring oscillators. Finally, the phase noise in dBc/Hz at $\Delta\omega$ offset from the carrier can be calculated by [7]

$$L(\Delta w) = 10 \times \log_{10}\left(\frac{2N}{2} \times \frac{in^2/\Delta f}{q\max^2} \times \frac{\Gamma rms^2}{2 \times \Delta v^2}\right) \qquad (4.10)$$

The 2N term is due to 2N nodes and thus 2N noise sources in the oscillator. The differential operation contributes the factor of 2 in the denominator. Using Eq. 4.10, the phase noise predicted to be –96.8 dBc/Hz at 100kHz and –112.4 dBc/Hz at 600kHz offset from the

carrier. From the HSPICE simulation with BSIM3V3 models, the oscillation is from 414.9MHz to 930MHz. The differential output amplitude is from 1.92V to 1.97V. A constant power of 30.16mW is dissipated from a single 2-V supply.

4.3 High-frequency Dividers

Depending on the frequency and the amplitude of the input signals, different types of single-ended or differential structures for frequency dividers can be chosen. Figure 4.1 shows the block diagram of the divide-by-16 N-prescalar as well as the divide-by-4 X-prescalar and their locations in the synthesizer. In this section, different types of divider circuits, which are used in high-frequency fixed dividers, will be discussed.

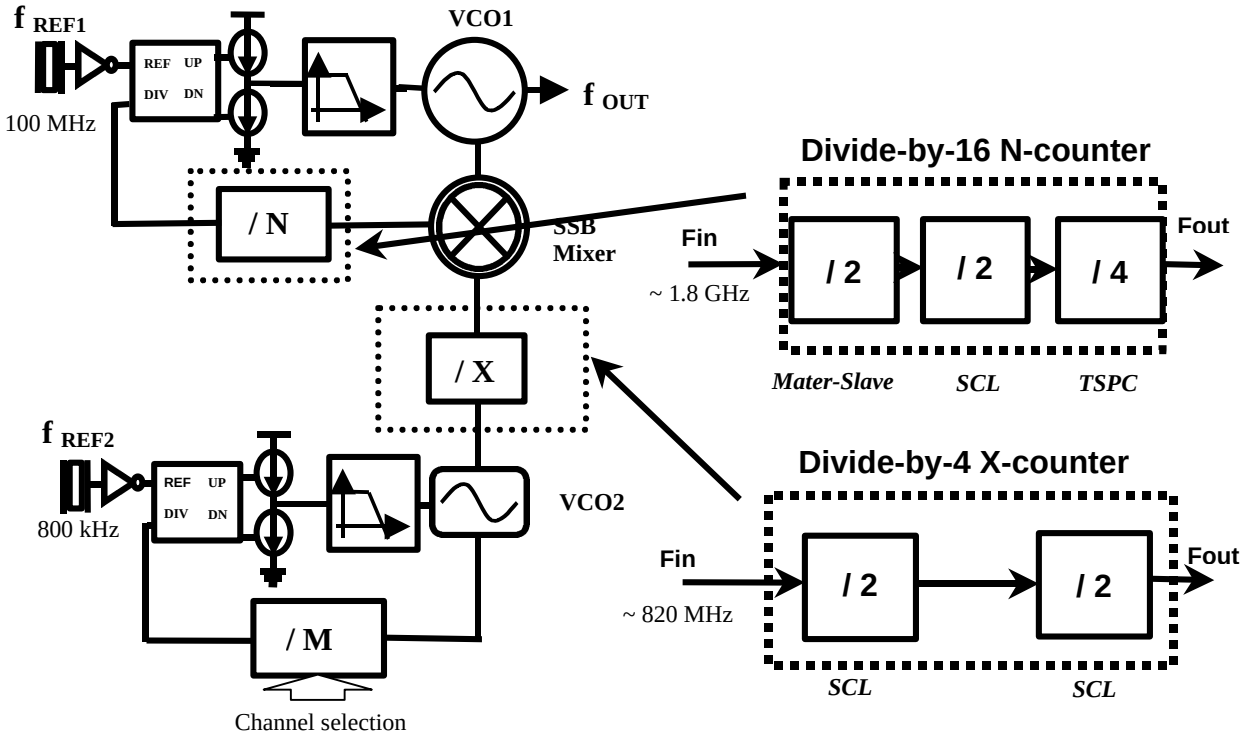


Figure 4.10 Block diagram of the fixed-value frequency prescalars

4.1.4 True Single Phase Clock (TSPC) Circuit

The first example of design is based on the dynamic True Single-Phase Circuit (TSPC) technique [15][16]. A TSPC divide-by-2, shown in Figure 4.11, is used as the basic building block of the TSPC frequency divider.

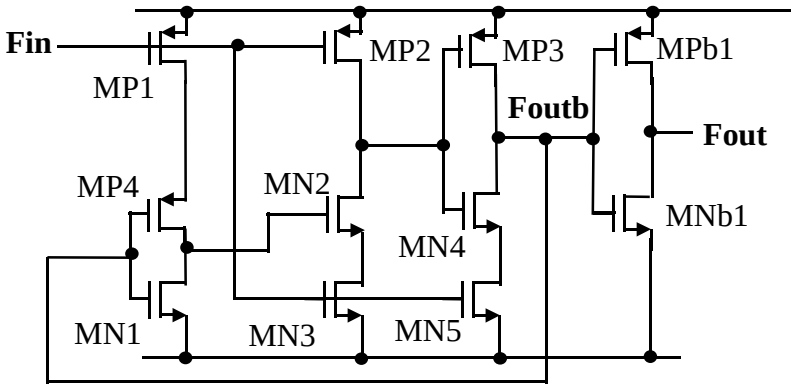


Figure 4.11 Circuit schematic of TSPC divide-by-2.

The circuit consists of three parts. The first part is a gated inverter that consists of MP1, MP4 and MN1, which passes the compliment of the divider output to the following stage when F_{in} goes low. The second part is a latch stage that consists of MP2, MP3, MN2, MN3, MN4 and MN5. This circuit will be activated and store the output of the gated inverter when F_{in} is high. The final part is an inverter to obtain a non-inverting output signal. The PMOS transistors MP1 and MP2 are used to pre-charge the internal nodes to increase the speed of the circuit. The output of the flip-flop is directly connected back to the D-input to obtain the divide-by-2 function because the TSPC circuit can completely isolate the sense and latch stage at different phases of the clock signal. The static power of the circuit is zero because no direct path from supply to ground and it only consumes dynamic power. One of the advantages of the TSPC divider is its simplicity. The circuit consists of only nine transistors excluding the output inverter. However, the circuit requires large amplitude of the input signal, and it is very sensitive to the slope of the signal. [16] Therefore, a high-frequency

input buffer may need to insert in front of the TSPC divider. The speed of the circuit greatly depends on the voltage supply. The circuit will be slow if low-voltage supply is used. In order to operate at higher frequency, larger sizes of the transistors are needed to increase the g_m and thus make a faster operation. However, increasing the size also increases loading for previous stage and thus the trade-off should be considered during design. Moreover, using larger transistor sizes will increase the degree of charge leakage and charge sharing at the output nodes and thus will affect the minimum operation frequency of the circuit. Due to the required large amplitude of the input signal, the TSPC divider is used as the second divide-by-4 inside the N-prescalar after the high frequency divide-by-4 as shown in Figure 4.10.

4.1.5 Source-coupled Logic (SCL)

The SCL divide-by-2 circuit is based on a standard Master/Slave ECL D-flip-flop and has a fully differential structure. As shown in Figure 4.12(a), the half-speed SCL latch circuit consists of two main pairs. The first one is the sensing circuit, which is formed by M1, M3 and M4. It is used to sense the differential signal at the D-input when the clock is high. The result will be stored to the subsequent latch stage, which consists of M2, M5 and M6, when the clock is low. The current source in conventional SCL logic at the common source terminal shared by M1 and M2 is omitted in order to operate at a low-voltage supply. However, omitting the current source requires a larger input signal swing to drive the input transistors, which is not a problem for the ring oscillator output as it is already maximized for low-phase noise. Due to the limited output swing, a higher speed of the divider can be obtained compared to the TSPC divider. Moreover, the fully differential structure helps to avoid serious polluting of the substrate, which is a serious problem of TSPC logic. The circuit is used in the second divide-by-2 stages in the X-counter and N-counter.

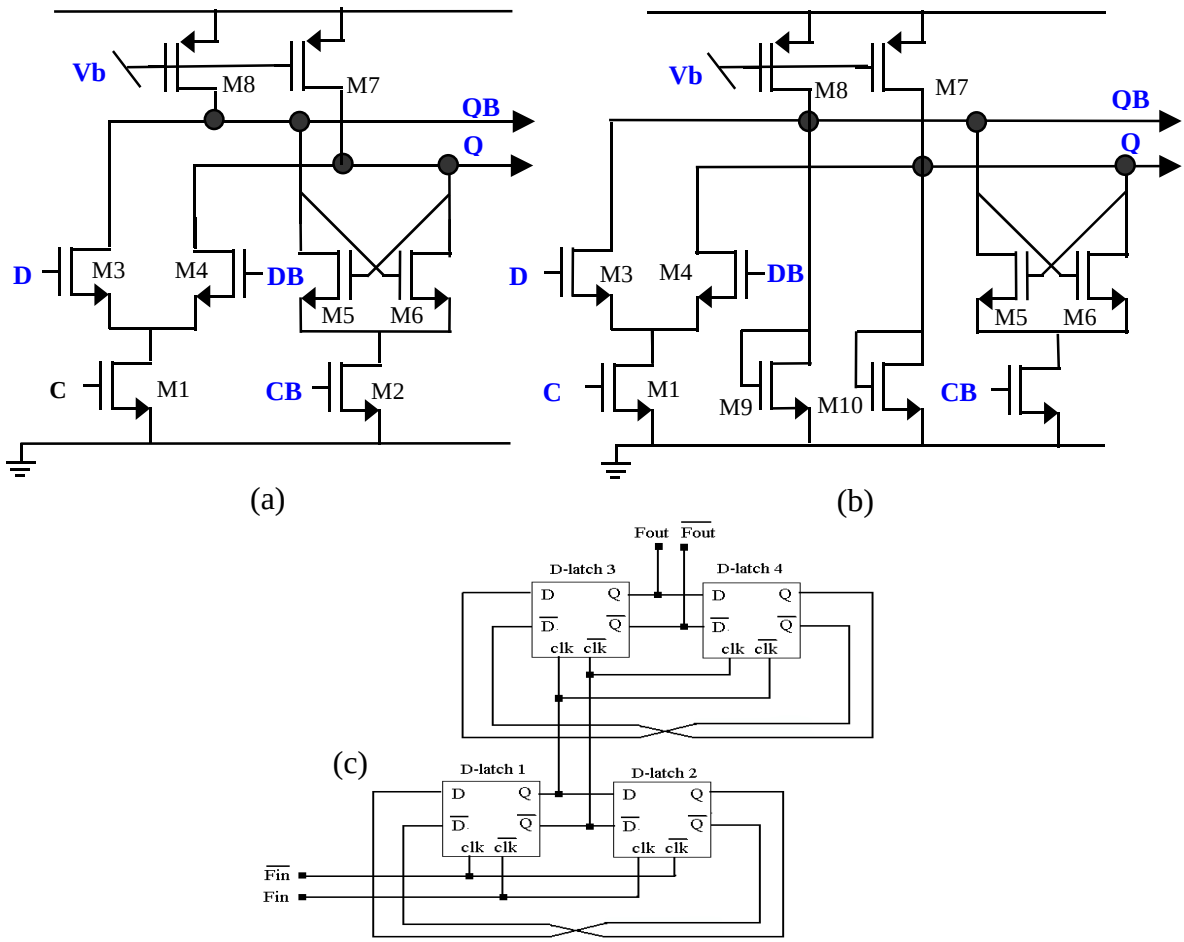


Figure 4.12 (a) Half-speed SCL latch (b) full-speed SCL latch and (c) Divide-by-4 circuit

The full-speed SCL latch is also shown in Figure 4.12(b) [7]. The only difference between the half-speed and the full-speed design is an additional pair of diode-connected transistors, M9 and M10. The transistors help to adjust the output common-mode voltage, to allow lower supply voltage and most importantly, to limit the output swing of the latch. By further limiting the output swing, reduction of the time required to switch from a low level to a high level is reduced and hence the speed of the circuit further increased. The circuit is used in the first divide-by-2 stage in the X-counter, which have maximum operation frequency around 1 GHz. The SCL latch cannot be fed back as the TSPC logic, and only a latch function is obtained because the sensing result directly appears at the output. Two SCL latches is cascaded to form the divide-by-2 circuit and the divide-by-4 circuit is obtained by cascading

two divide-by-2 circuits as illustrated in Figure 4.12(c).

Owing to the high-speed and small amplitude of the SSB mixer output signal, the divider-by-2 circuit shown in Figure 4.13 is used for the first stage of the 1.6-GHz N-counter [17].

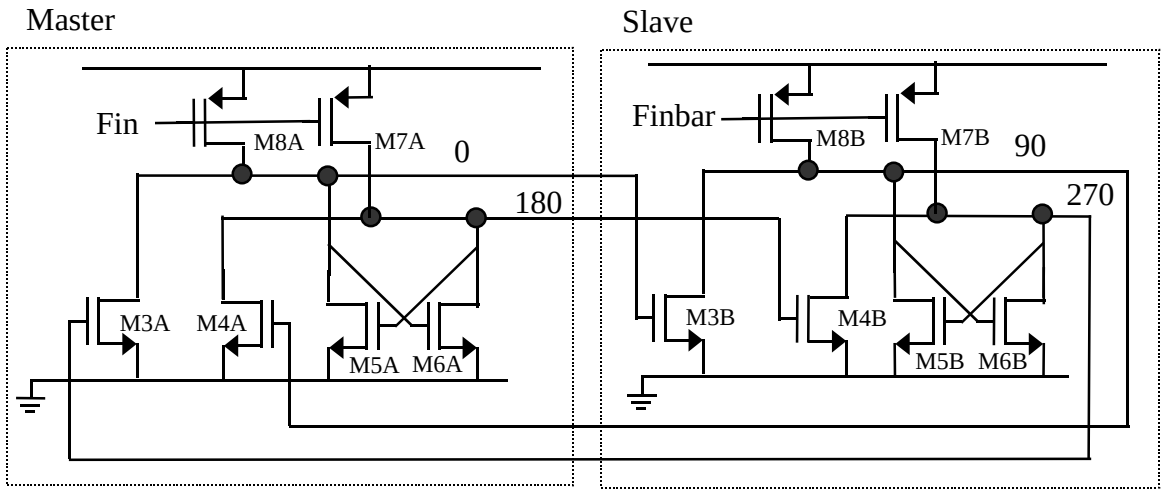


Figure 4.13 The 1.6-GHz divide-by-2 prescalar

The structure is essentially a Johmson Master and Slave counter that achieves high-speed operation by avoiding the stacking of the NMOS or PMOS transistor. The latch operates by using PMOS devices to drive current into its output nodes according to the clock signal, and the NMOS devices, M3 and M4, to selectively discharge the nodes according to signal levels of the other latch. When signal *Fin* is high, the master is in sense mode, while the slave is in store mode. When *Fin* goes low, the reverse occurs. The circuit can accept input signal as small as 250m Vp according to the simulation results, while the divider oscillates if the input signal magnitude is too small. However, the divider is sensitive to the common mode voltage of the input and therefore an AC coupling stage is used at the divider input and proper DC bias can be applied through two resistors. Intensive simulations have been done to ensure proper operation of the dividers for different temperature with different input signal

magnitudes and frequencies. Also, the process variation of the devices should be considered.

4.4 Programmable Counter

Other than the fixed frequency scalars, there is a programmable multi-modulus counter in the low-frequency loop in order to adjust the desired channel in the synthesizer.

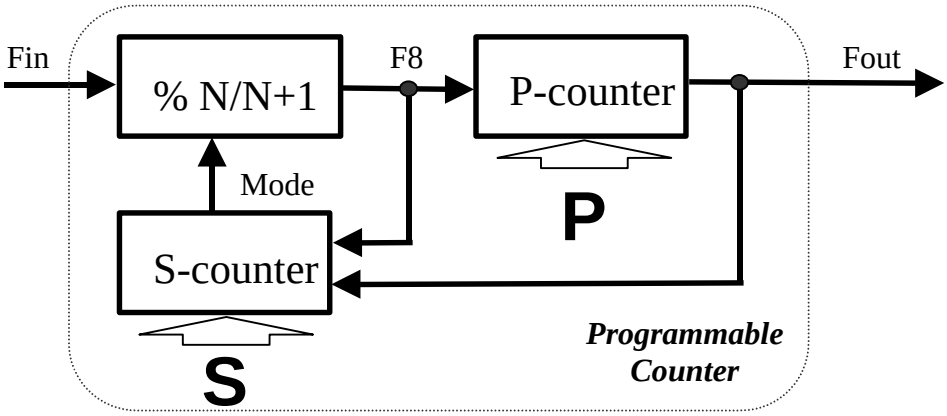


Figure 4.14 Block diagram of the programmable counter.

. The counter employs the conventional design, which consists of a dual-modulus prescalar (DMP), a pulse (P) and a swallow (S) counter. The block diagram is shown in Figure 4.14. The DMP initially divides the high-frequency input by N+1 with the *Mode* signal being high. After the S-counter counts S output pulses from the DMP, it changes the *Mode* signal to low, and the DMP starts to count by N. The output from the DMP is also counted by the P-counter simultaneously, and the P-counter resets the S-counter and itself after counting P output pulses. Therefore, the total counting number M is given by

$$M = P \times \left[(N+1) \times \frac{S}{P} + N \times \frac{P-S}{P} \right] = P \cdot N + S \qquad (4.11)$$

In order to have a proper function of the counter, S should be smaller than P. The numbers of N, P and S should be chosen carefully according to the maximum limitation of the

allowable input frequency of the counters. In this design, N is 8 and hence the input frequency to the S-counter as well as P-counter is lower than 150 MHz. In the design, the P-counter has 7 bit binary inputs, and the S-counter has 4 bit inputs. Therefore, the maximum counting number of the frequency counter is 2070.

The dual-modulus divide-by-8/9 prescalar is shown in Figure 4.15. It is a critical building block of the programmable counter because it input is required to operate at a full speed of the input. When the *Mode* signal is low, the second stage of the asynchronous divide-by-2/3 is disabled and the dual-modulus divider counts a number of eight. When the *Mode* signal goes high, the second stage of the synchronous divide-by-2/3 circuit is enabled on the every fourth count of the divide-by-4 stage and hence the counting number becomes nine instead of eight. In order to obtain faster operation of the full speed divide-by-2/3, a NAND gate is embedded into the TSPC D-flip-flop, which is shown in Figure 4.16.

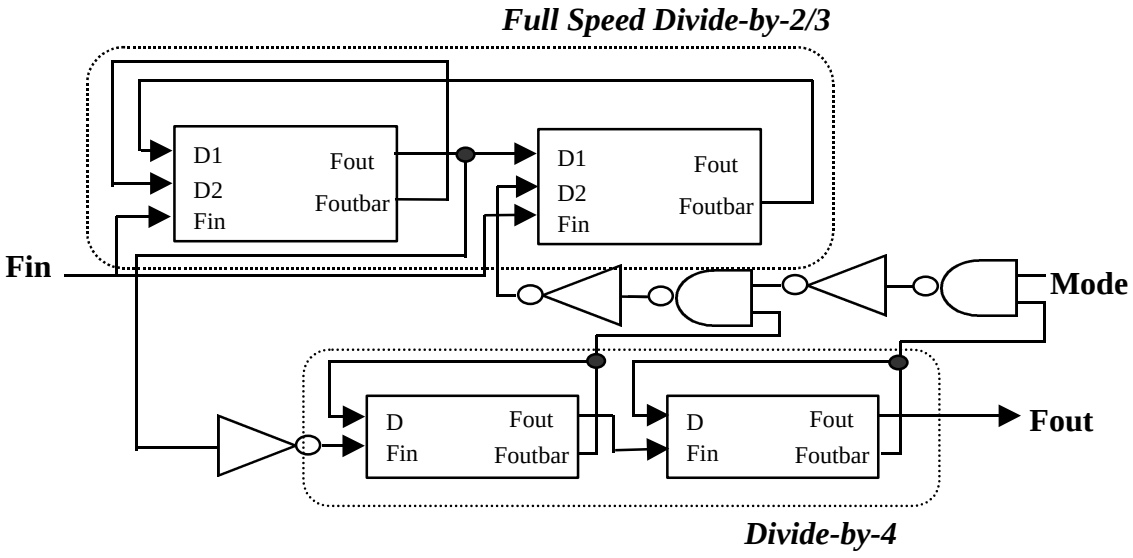


Figure 4.15 The block diagram of the dual-modulus divide-by-8/9 prescalar

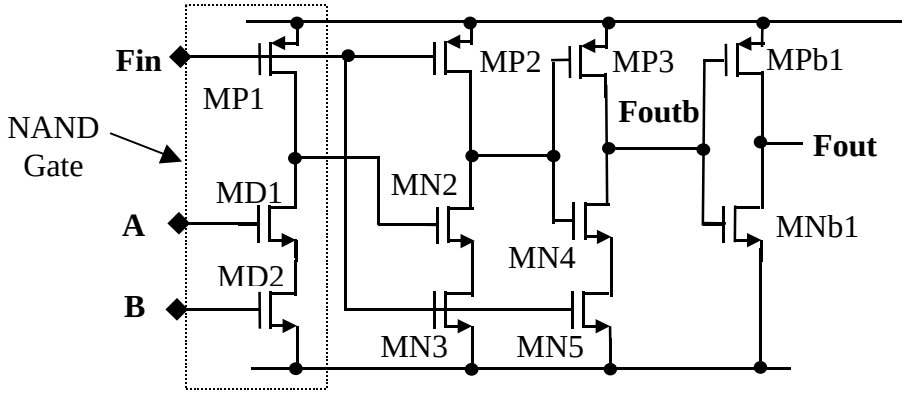


Figure 4.16 The D flip-flop with embedded NAND gate

The asynchronous S-counter and P-counter are shown in Figure 4.17 and Figure 4.18, respectively. In both counters, a chain of TSPC flip-flops is used as the internal asynchronous ripple counters. The output bits of the ripple counter are then compared with the input bits by the comparator. In the S-counter, a T-flip-flop after the comparator is used to obtain the "*STOP*" signal and "*MODE*" signal after *S* count of the input signal *F8*, which is obtained from the DMP output. The ripple counter in the S-counter will stop its counting when signal *STOP* goes high until the *Reset* signal comes from the P-counter after *P* count of the input signal. The output signal of the P-counter is actually the output of the overall M-counter and resets both P-counter and S-counter when it goes high.

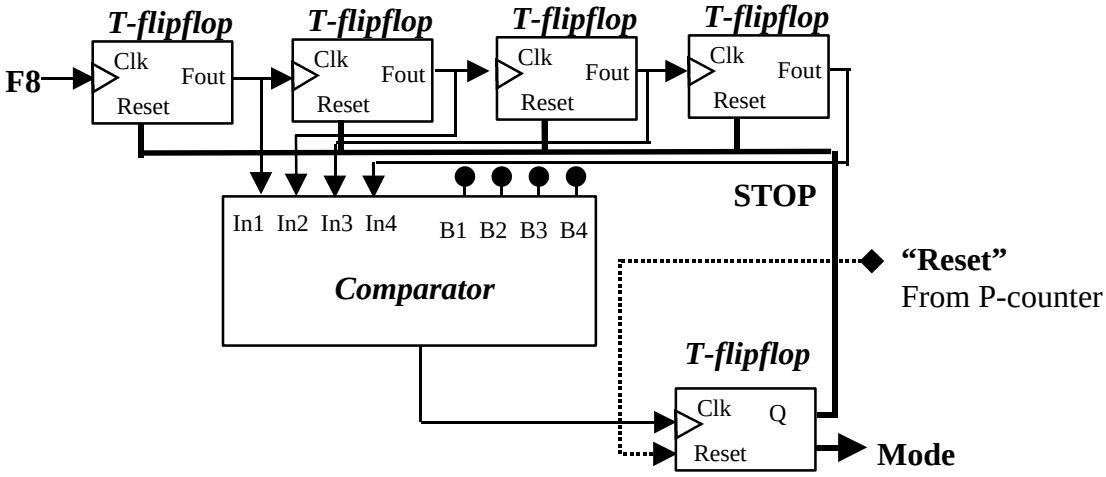


Figure 4.17 Block diagram of the 4 bits S-counter

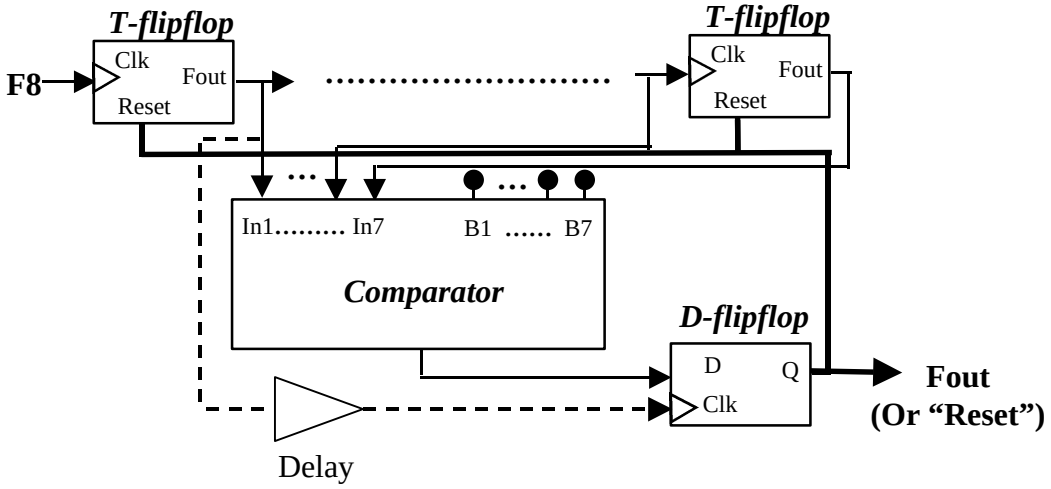


Figure 4.18 Block diagram of the 7 bits P-counter

4.5 Phase-Frequency Detector (PFD)

The phase detectors used in both low and high PLLs act as comparators, which provide an output signal having DC component proportional to the phase difference between two input signals. The conventional tri-state PFD is used because it is simple, has linear phase-detecting range of +/-2π radians, is duty-cycle insensitive and can act both as a phase detector and as a frequency detector [17]. The block diagram is shown in Figure 4.19(a).

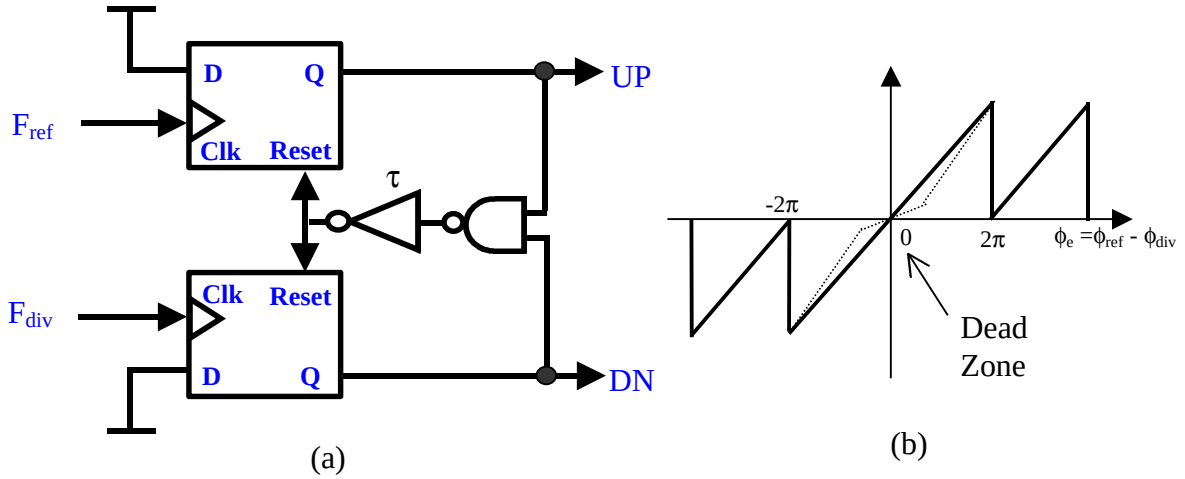


Figure 4.19 (a) Block diagram of the PFD (b) Phase detection characteristic curve

The frequency detection action of the PFD operates as follows: For $F_{ref} > F_{div}$, phase error ϕ_e increases with time and thus the *UP* signal is activated most of the time. For $F_{ref} < F_{div}$, ϕ_e decreases with time and thus the *DN* signal is dominant. This action greatly aids to the acquiring lock of the loop when the frequency of the reference source and that of the divider output signal are different. The circuit is input edge sensitive. When the frequencies of the input signals are the same, the circuit produces an output signal according to their phase difference and its phase detection characteristic curve is shown in Figure 4.19(b). The corresponding PD characteristic grows linearly over a range of 4π radians. The non-ideal PD characteristic is drawn by a dotted line in Figure 4.19(b). A nonlinear gain flattening is found when the phase differential is small because of the difference in the rise times between the *UP* and *DN* signal paths. Such a gain variation of the detector will seriously affect the loop behavior. Therefore, a finite delay (τ) is added to reduce this dead-zone problem of the detector. The delay time should be chosen to improve the dead-zone as much as possible but it cannot be too long because it increases the power of reference sidebands when the loop is in lock.

Two PFDs employed in the dual-loop synthesizer use the same architecture as shown in Figure 4.19(a). However, due to their different operation speed requirements, the D-flip-flops in the PFDs used in the high-frequency loop are realized by TSPC logic while those in the low-frequency loop CMOS logic.

After the comparison of the phase difference, the resulted *UP* and *DN* signals are combined by a charge pump, where schematic is shown in Figure 4.20 [7]. The *UP* and *DN* current sources remain on all the time, but their currents are diverted into either a reference voltage V_{ref} during the off-state or to the output node ding the on-state.

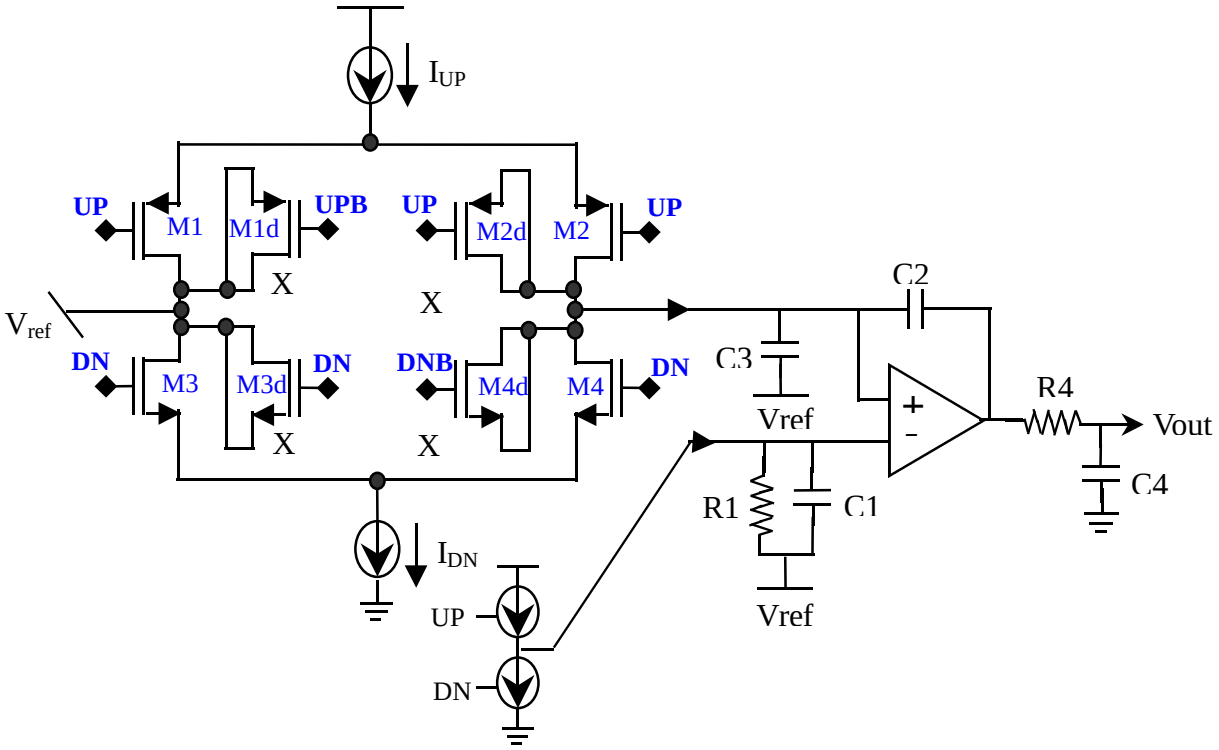


Figure 4.20 Schematic of the charge pump with the active loop filter

One of the advantages of this charge-pump configuration is that the response to the *UP* and *DN* signals is immediate, the start-up time for the current sources is short. Theoretically, a charge pump does not suffer from the reference clock feedthrough problem because once the loop in lock, both *UP* and *DN* current source are turned off. However, since a delay is added to the delay path of the PFD, the reference spurs are created if there is any unbalance between the *UP* and *DN* signal paths and any spike at the charge pump output. Half-sized dummy switches are added to help reduce the error due to charge injection of the switches and hence to reduce the spurs levels. The charge-sharing problem of the charge pump is diminished by the use of an active filter, which provides a DC reference voltage to the charge pump output.

4.6 Single-sideband (SSB) Mixer

In the upper-loop, a SSB mixer is needed to obtain the desired sideband for the high-frequency prescalar output. The design is based on the conventional Gilbert cell mixer and the circuit diagram is shown in Figure 4.21.

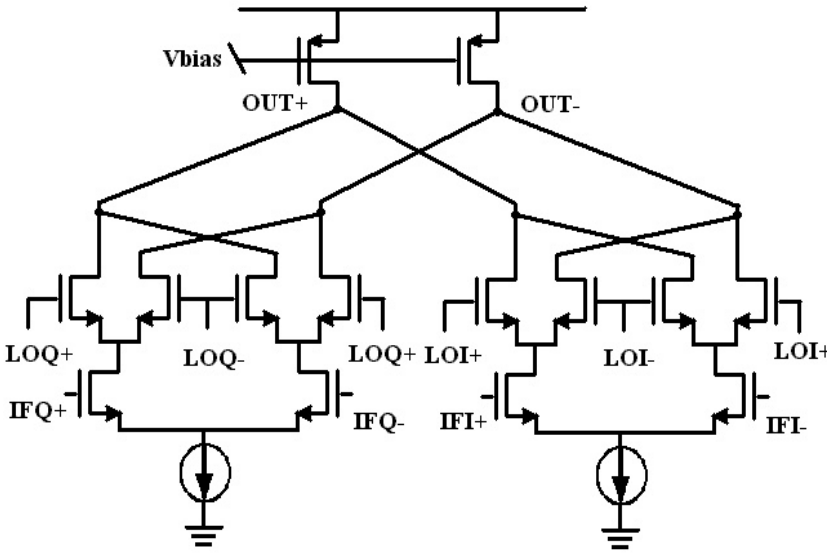


Figure 4.21 Circuit schematic of the SSB mixer

The LO terminals of the mixer are driven by the I and Q outputs of the ring oscillator and the IF terminals are connected to the I and Q outputs of LC oscillator. The resulting mixing currents are added together in the output nodes and convert to voltage by two linear transistors. In order to ensure a correct locking of the loop, the mixer should have small gain and phase mismatch and it is done by having symmetrical layout carefully of both individual mixers. The linearity is not so important in this design because there is only a single dominant tone at the LC oscillator output.

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Chapter 5 Layout

5.1 Floor Planning

The synthesizer is basically laid out as the same as the signal flow in the schematic as shown in Figure 5.2. Each block is placed as close to the previous block as possible in order to shorten the path of the signal passing through. It is extremely important for the high-frequency signal paths. The die photo is shown in Figure 5.2 and the active area of the chip is around 2000μm x 1000μm with a actual die size of 2310μm x 2000μm. Some internal testing pads are added to examine the function of the building blocks. The power supplies of the circuits are separated so that individual blocks can be tested and there is less influence among the building blocks. In order to reduce the substrate noise coupling from the dividers and the ring oscillator to other circuits, guard rings are placed around these noisy circuits. Some large guard rings are placed surrounding the inductors because it can absorb some amount of the eddy current induced under the inductors. In order to achieve better isolation of the noise, the ground of the guard rings is connected to a separated bonding pad. In the layout, the grounds of the loop filters, LC-oscillator, Ring-oscillator and other digital circuits are connected to separated pads to minimize the problem of ground bounce. The digital ground and the analog ground are also connected to the different dc bonding pads. Testing structures of the passive

components included planar inductor, linear capacitor and accumulation-mode varactor are included for high-frequency measurements and characterization.

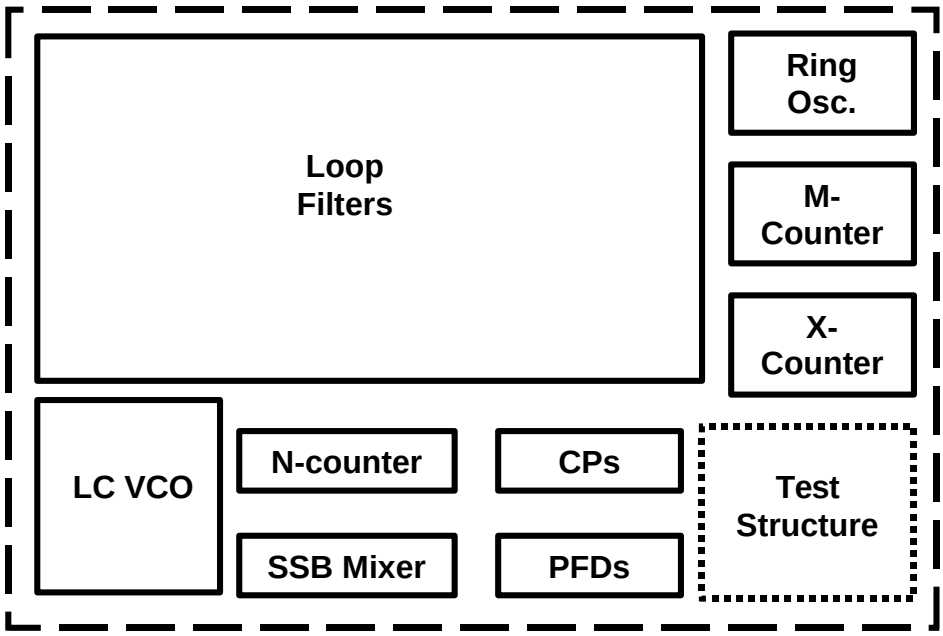

Figure 5. 1 Floorplan of the synthesizer layout

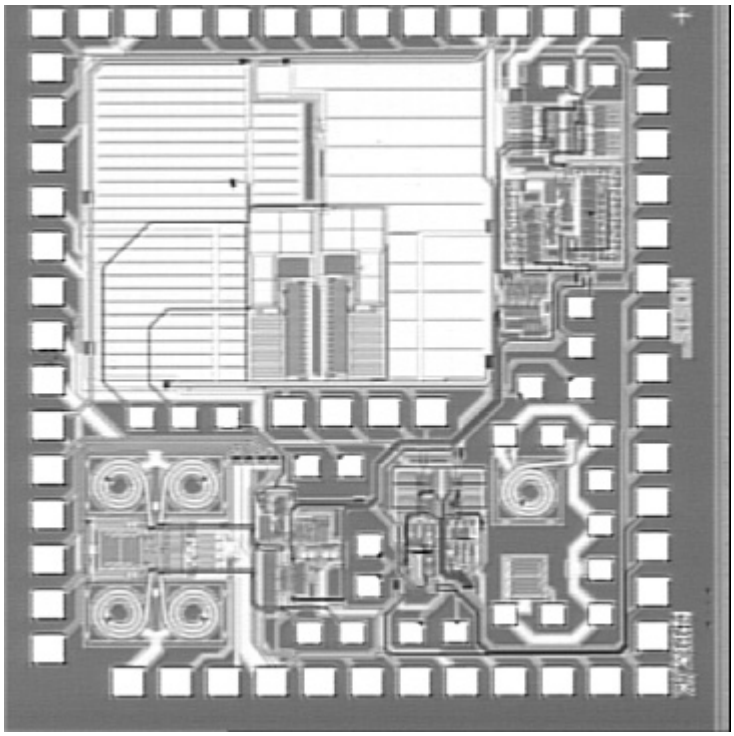

Figure 5.2 The die photo of the synthesizer

Chapter 6 Measurement

6.1 Introduction

The prototype of the frequency synthesizer has been fabricated using HP-0.5μm N-well CMOS process with linear capacitor option through MOSIS, and its chip area is 2310 x 2001 μm^2. The measurement results will be presented in this chapter. Firstly, the testing results of passive components will be given. Secondly, the measurements of the building blocks will be presented. Finally, the whole synthesizer testing will be and discussed.

6.2 Passive components Testing

The impedance of the passive components is extracted using the network analyzer (HP 8510C) with S-parameter test set (HP 8517B) and a high-speed ground-signal-ground (GSG) picoprobe. Before the extraction of S11 parameters, the calibration is done with the GSG probe calibration kit and an open GSG pad in the system chip.

6.2.1 Planar Inductor

The measured Q-factor of the two-layer planar inductor with designed value of 3nH is plotted versus frequency in Figure 6.1.

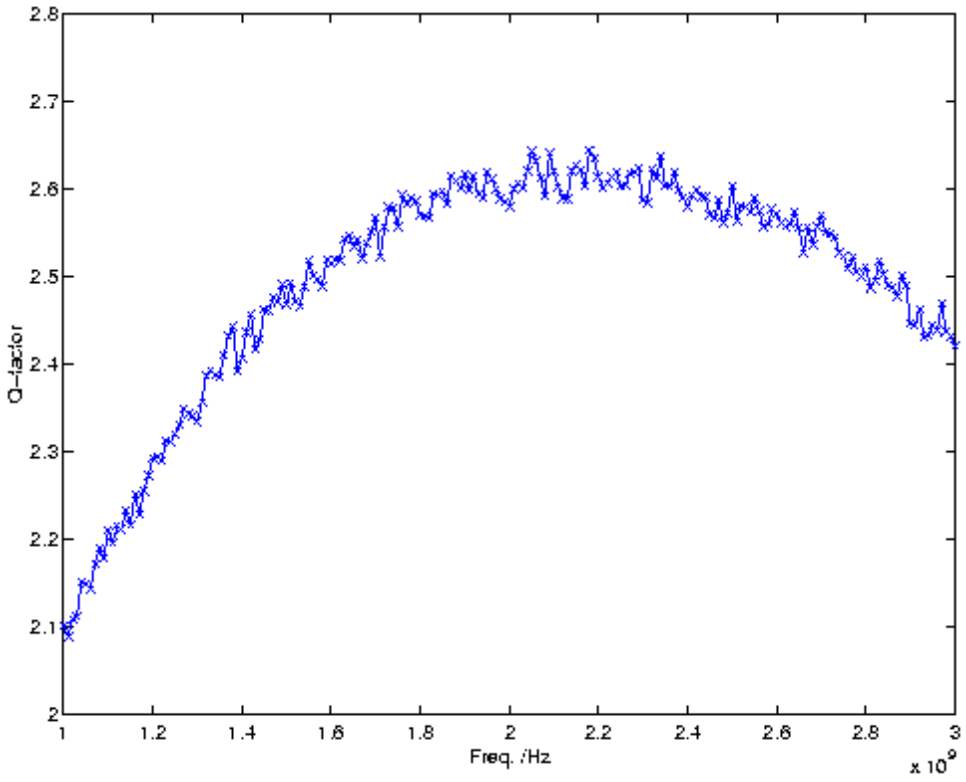

Figure 6.1 The plot of inductor Q-factor versus frequency.

In the design of the LC-Oscillator, the value of inductor Q is taken to be half the value of that obtained by *ASITIC* to take the high-frequency substrate loss into account. However, the measured Q-value is only around 2.6 at 1.8 GHz, which is even smaller than the estimated value of 3.316. The maximum Q value is 2.63 at around 2.2 GHz. The self-resonance frequency is larger than 3 GHz as expected, which is the upper frequency limit of the network analyzer used. The single-port inductor is modeled with the lossy lumped network [1] [2] as shown in Figure 6.2.

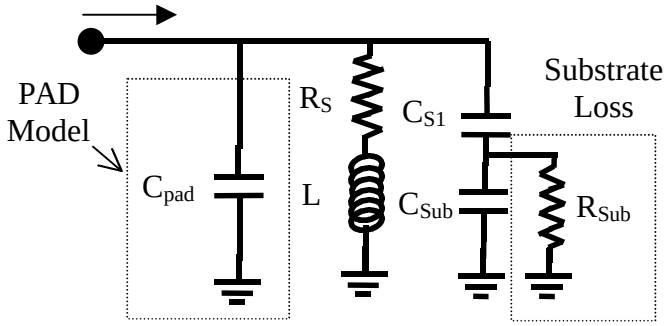

Figure 6.2 Lumped single-port physical model of the inductor

A 56.3-fF capacitor is added in parallel to model the input-probing pad. A capacitor (C_{sub}) represents the variation of substrate impedance as a function of frequency and a resistor (R_{sub}) is the substrate coupling resistor, which models the loss of the highly doped substrate in high operation frequency [1]. By fitting the value of the components in the model, the real part and the imaginary part of Z11 can match to the measurement data as displayed in Figure 6.1.

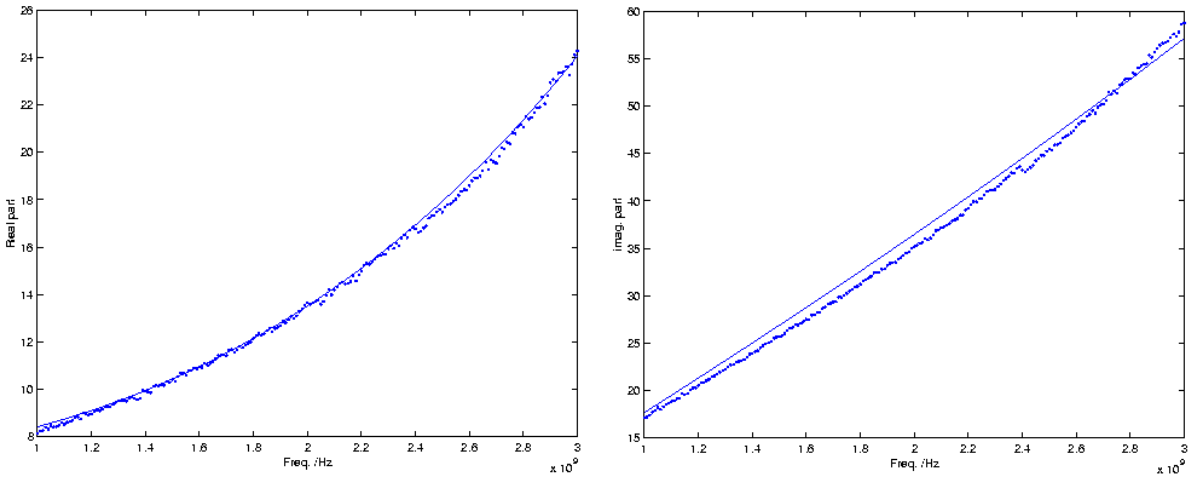

Figure 6.3 Real part and imaginary part and of inductor Z11 from measurement.

In Figure 6.3, the points indicate the measured data points and the solid line is the approximation line of the model. By adding the extra-components to the simple π inductor model used in design phase, the model can work in a wider frequency range from 1 GHz to 2.5GHz, which is far below the self-oscillation frequency. The following table summarizes the values used in the design and the measured results.

Parameters used for the design from ASITIC		Measured parameters of the simple π model @ 1.8GHz		Measured parameters of the wideband model	
L	3.070 nH	L	2.65 nH	L	2.8 nH
R_S	9 Ω	R_S	11 Ω	R_S	7 Ω
C_{S1}	0.190 pF	C_{S1}	0.10 pF	C_{S1}	0.10 pF
R_{S1}	0.156 Ω	R_{S1}	0.19 Ω	R_{S1}	\
C_{sub}	\	C_{sub}	\	C_{sub}	0.9 pF
R_{sub}	\	R_{sub}	\	R_{sub}	200 Ω
Q (1.8GHz)	3.316	Q (1.8GHz)	2.6	Q (1.8GHz)	2.6

Table 6.1 Modeled parameters of the two-layer inductor

The measured values demonstrate a large degradation of the Q-factor due to extra-substrate loss, which is neglected by *ASITIC*. The inductance value is almost 10% smaller due to accuracy of the program and the further loss of the conducting substrate. The other parameters are close to the *ASITIC* results.

6.2.2 Accumulation-Mode Varactor

A simple model of a lossy capacitor is used to model the accumulation-mode varactor as displayed in Figure 6.4. The resistor (R_S) is used to model the loss of the capacitor. The total capacitor (C) consists of a fixed capacitance part and a variable part, which depends on the voltage bias applied through the DC biasing network of the network analyzer.

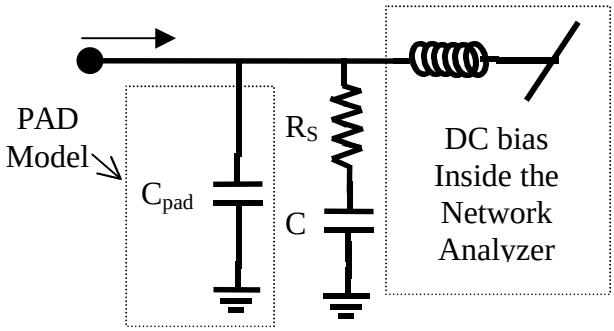

Figure 6.4 Model of the accumulation-mode varator

In the design phase, the value of C is expected to be from 0.5 pF to 0.628 pF, which is predicted by the information of C_{OX} value, the channel doping and the WL product value. The Q-value of the varactor is expected to be around 25, and in order to ensure such high Q, each varactor is separated into 64 small parts, each part of which has minimum device feature size of 0.6um. The measurement results are plotted as follows:

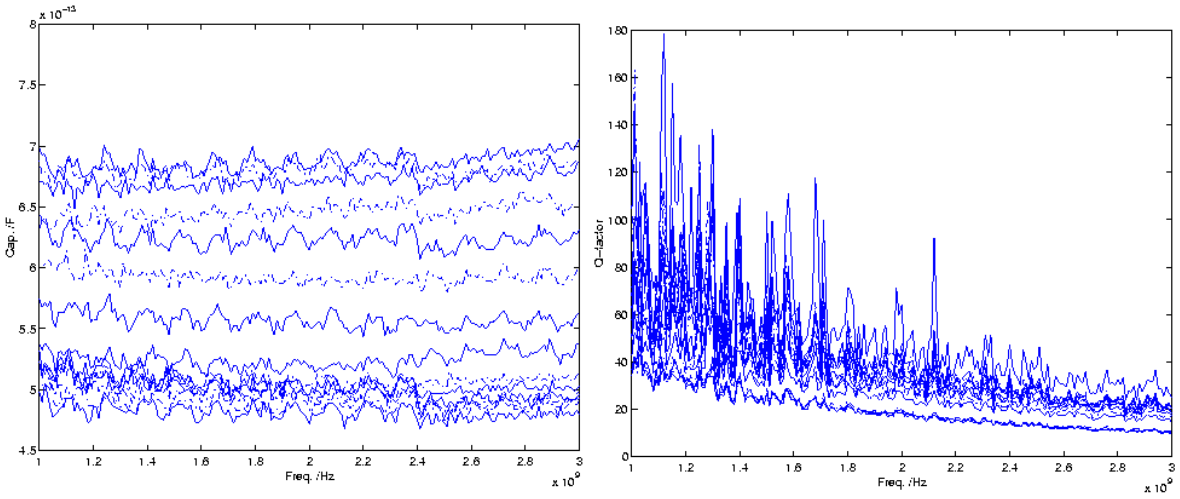

Figure 6.5 The plot of capacitance and the Q-factor with different bias voltages versus frequency.

In Figure 6.5, each line represents the capacitance and Q-factor versus frequency with a given biasing voltage. The figure illustrates the capacitance with a given biasing voltage is almost constant over frequency range from 1 GHz to 2 GHz. On the other hand, the Q-value drops as the frequency increases and it is greatly dependent on bias. Figure 6.6 illustrates the variations of capacitance and Q value with the function of biasing voltage at 1.8 GHz.

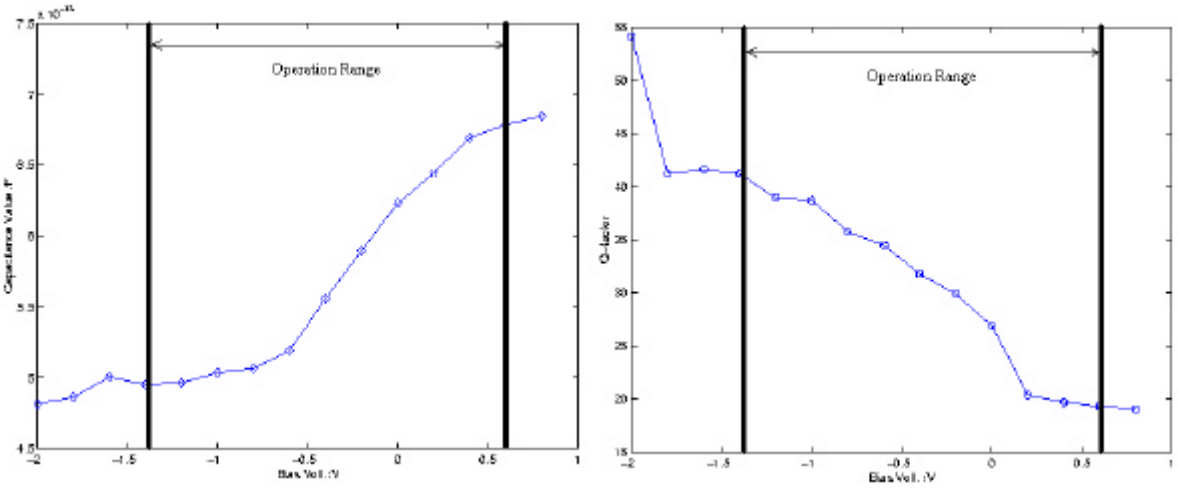

Figure 6.6 The plot of capacitance and the Q-factor at 1.8 GHz versus bias voltage.

As shown in Figure 6.6, the Q value varies from 19 to 40 in the desired operation range and the capacitance changes from 0.68 pF down to 0.48 pF with the bias voltages varying from 0.7 V to –1.3 V. From the indication of the flatband region position, the threshold voltage of this accumulation-mode device is smaller than that of normal PMOS devices. The Q-value degrade towards positive gate bias is due to an increase in accumulation-layer resistance [3].

6.2.3 Linear Capacitor

The linear capacitor being tested is used as a unit capacitor in the loop filter of the high-frequency loop. Each capacitor should have a value of 4 pF with the size of 41 x 41 μm^2. The structure of the linear capacitor is similar to the MOS transistor but the active layer is replaced by a highly doped capacitor well. The model used is the same as the varactor without external DC biasing. Figure 6.7 exhibits the measured capacitance and the Q-factor versus frequency.

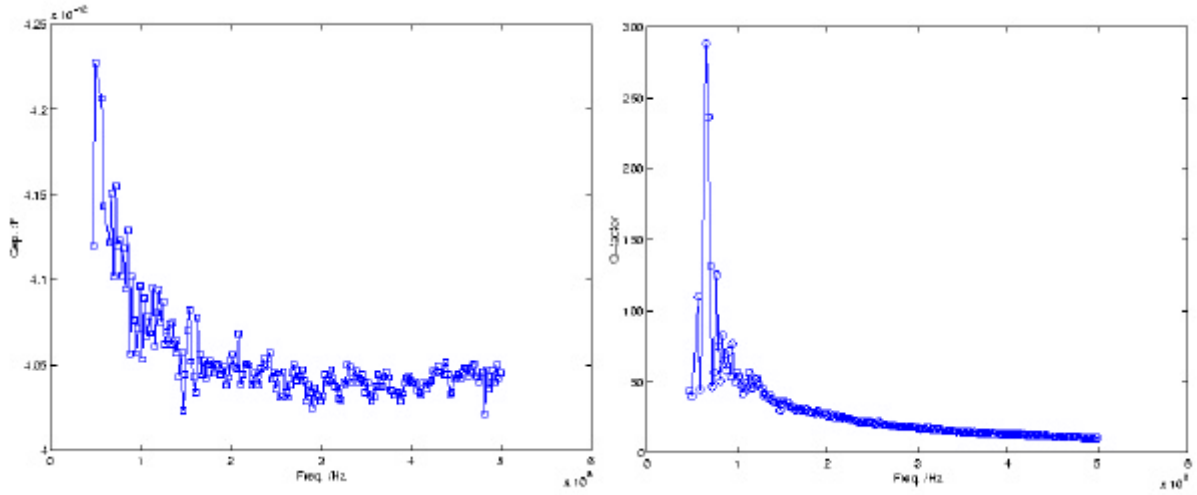

Figure 6.7 Capacitance and the Q-factor of linear capacitor versus frequency.

The large fluctuations in lower frequencies are due to the Q value of the device under test being too large and the measured frequency being too close to the lowest operation limit of the network analyzer. The capacitance value is approximately the same in the valid measurement range as expected. Its Q-value at 100 MHz is as large as 50 and it is even as large as several hundreds at lower frequency.

6.3 Individual building blocks

After the discussion of the passive components testing, the functional testing of some important building blocks will be given in this session. Since the building blocks are in the system chip, the optimal bias condition can be found and the performance of the building blocks can directly indicate the performance of the whole synthesizer.

The detailed schematic is shown again in Figure 6.8 for reference purpose.

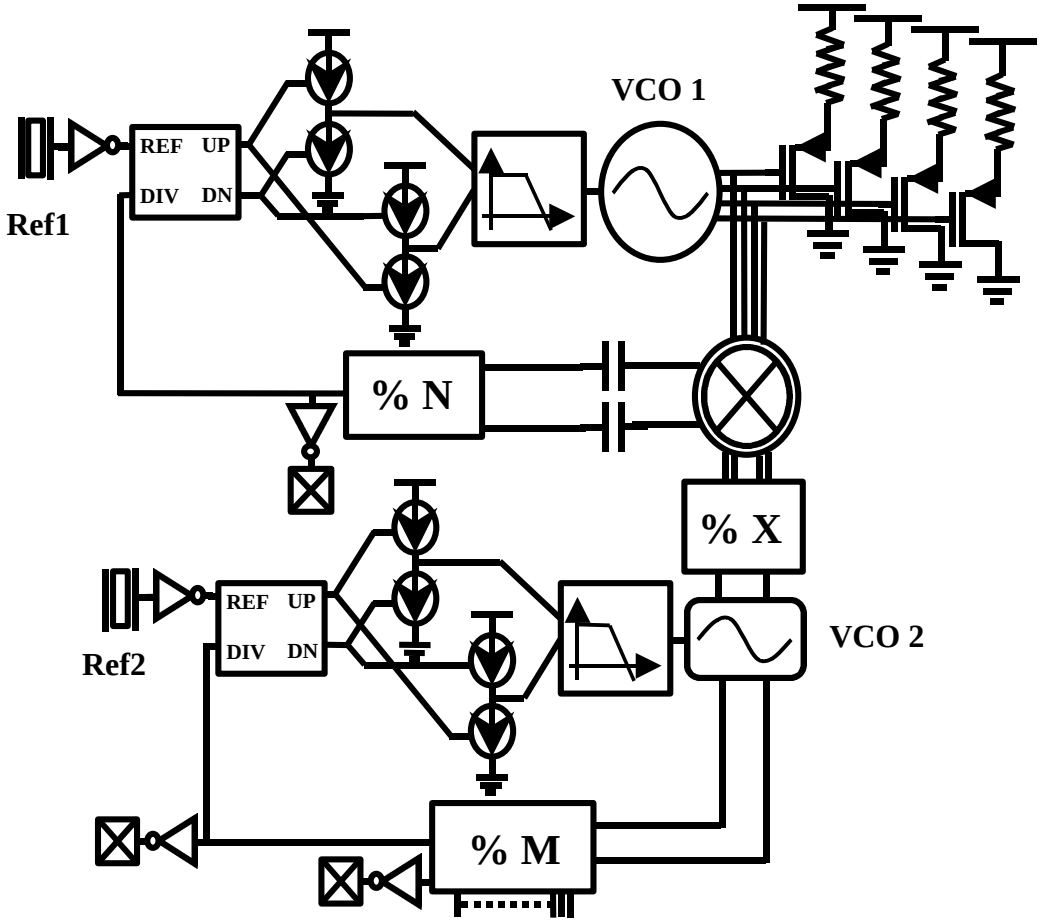

Figure 6.8 The detailed schematic of the synthesizer

6.3.1 LC-Oscillator

The quadrature LC-Oscillator consists of four planar inductors and four accumulation-mode varators, which are characterized and described in the previous sessions. The nominal bias condition of the oscillator is with a 1.3-V voltage supply and with a bias current of 8 mA. In this nominal bias condition, the LC-oscillator can be tuned from 1.874 GHz to 1.928 GHz with tuning voltage changing from 0 V to 2 V, and the power consumption is 20.8mW. The tuning characteristic curves with different bias conditions are plotted in Figure 6.9.

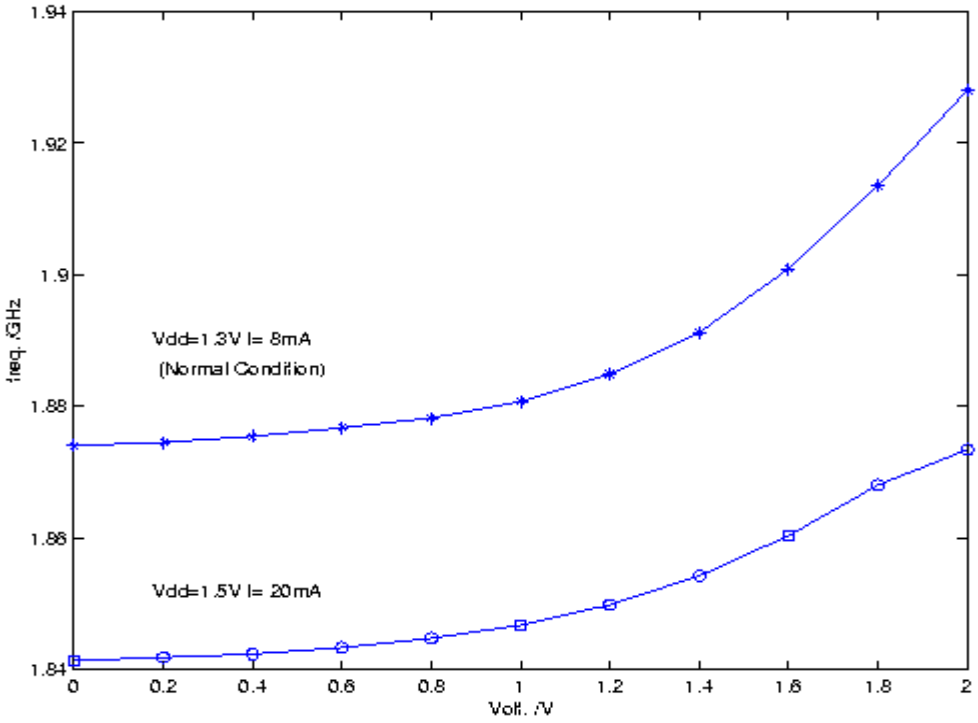

Figure 6.9 Tuning characteristic curve of the LC-oscillator

The operation frequency is higher than predicted range from 1.767 GHz to 1.875 GHz due to the unexpected 10 % decrease of the inductor value. At the nominal bias condition, the measured tuning range is 54 MHz, which is smaller than the expected value of 108 MHz or even the system required value of 95MHz. It is due an under-estimation of the parasitic capacitance at the oscillator output node. The tuning curve with supply voltage of 1.5V and bias current of 20mA is also shown in Figure 6.9 as illustration. It indicates that both the oscillation frequency and tuning range decrease due to increase of the parasitic of the g_m cells and coupling transistors, while the output amplitude increases with bias current.

The single-ended output power spectrums of the LC-oscillator is obtained by directly connecting the buffered output to the spectrum analyzer (HP8594E). As illustration, the output spectrum at 1.88GHz is shown in Figure 6.10.

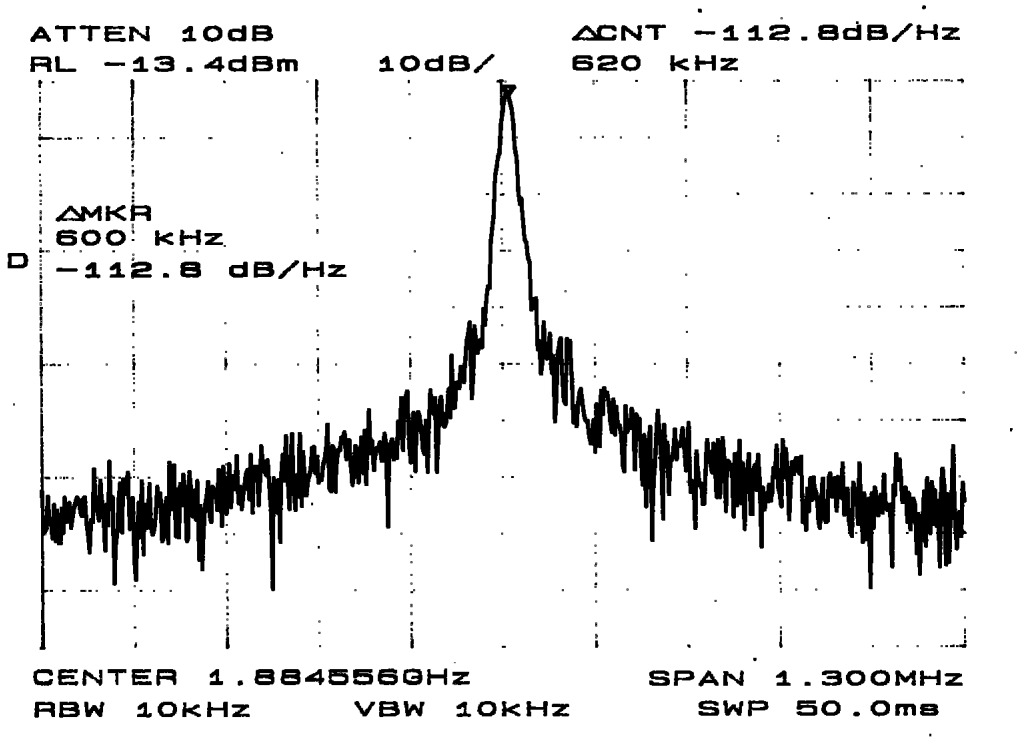

Figure 6.10 The output spectrum of the free-running LC-Oscillator at 1.88GHz

The output differential amplitude of the oscillator is 1.12 Vp and the differential phase noise performances are –99.4 dBc at 100-kHz offset and –115 dBc at 600kHz offset from a 1.88-GHz carrier. The amplitude is smaller than the expected value of 1.71 Vp due to the reduction of the inductor Q factor. From Eq. 4.7, the reduction of the inductor Q-value and of the output oscillation amplitude lead to 4.15-dB degradation of the phase noise compared to the designed value, which matches well with the measurement.

6.3.2 Ring-Oscillator

One of the critical building blocks in the synthesizer is a ring-type VCO with a wide frequency tuning range as large as 60.9% with a low phase noise. Therefore, the ring oscillator was fabricated twice. The first prototype was sent two months before the tape-out of the system die. The measurement of the first prototype and the second one on the system die will be discussed.

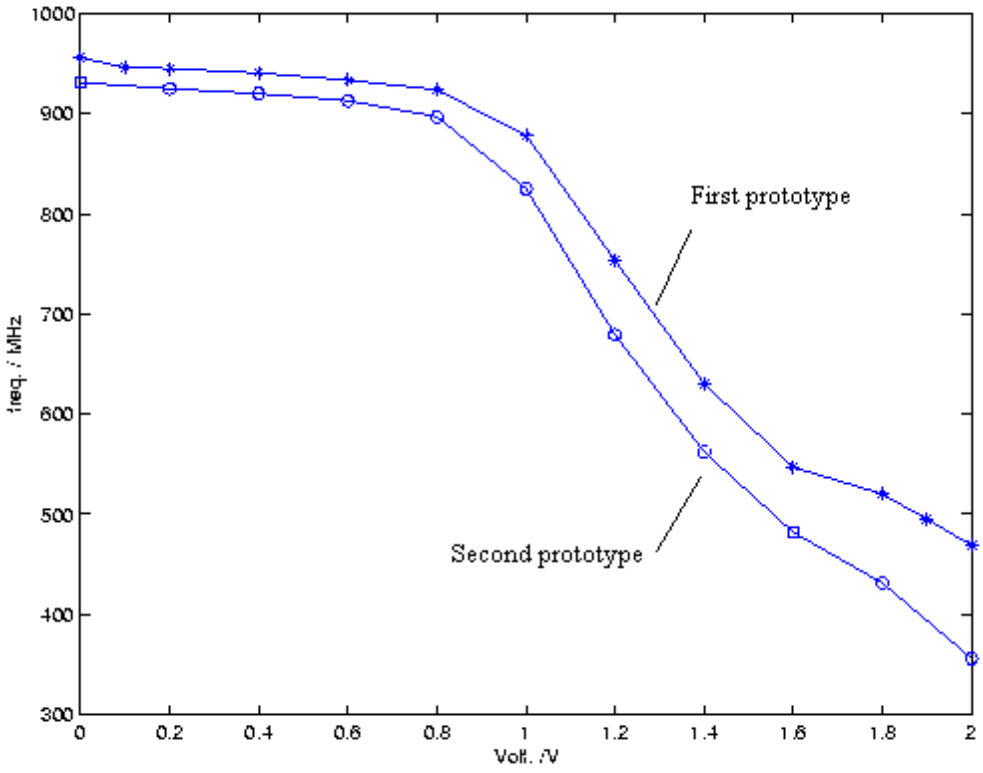

Figure 6.11 The tuning characteristic curve of the VCO

The tuning characteristic curves of two prototypes are plotted in Figure 6.11. The measured tuning ranges of two prototypes are from 460 MHz to 970 MHz and from 356 MHz to 931 MHz, respectively, with a constant 15-mA current drawn from a single 2-V supply in both prototypes. The higher operation frequency of the first prototype than the simulated value is due to the over-estimation of the parasitic in the design phase. In the second prototype, the capacitance values are adjusted so that the operation frequency range is wider and the operation frequency is close to the designed one. However, the skew rate of the delay cell is reduced with the adjustment and the deviation from the predicted phase noise performance is expected. The effective tuning ranges of two prototypes are 71.32% with center oscillation frequency at 715MHz and 89.36% with center frequency at 643.5 MHz.

In the linear ranges of the curves between 0.9V and 1.6V, the VCO gains of two prototypes are around 500 MHz/V. Figure 6.12 and Figure 6.13 show the single-ended output power spectrums of two prototypes, respectively, which are obtained by probing single-ended output of the oscillator with a high impedance probe that has a 26-dB attenuation.

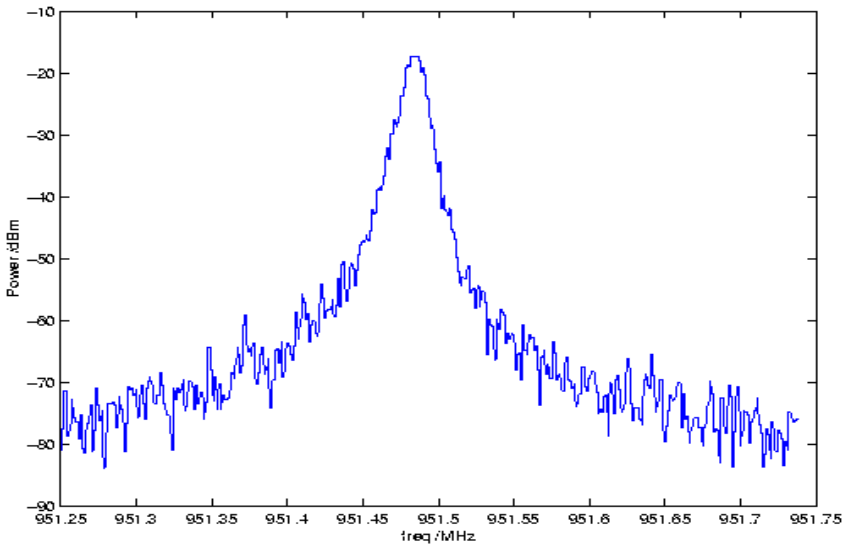

Figure 6.12 The output power spectrum of first prototype with 951.48-MHz output frequency resolution bandwidth of 10 kHz.

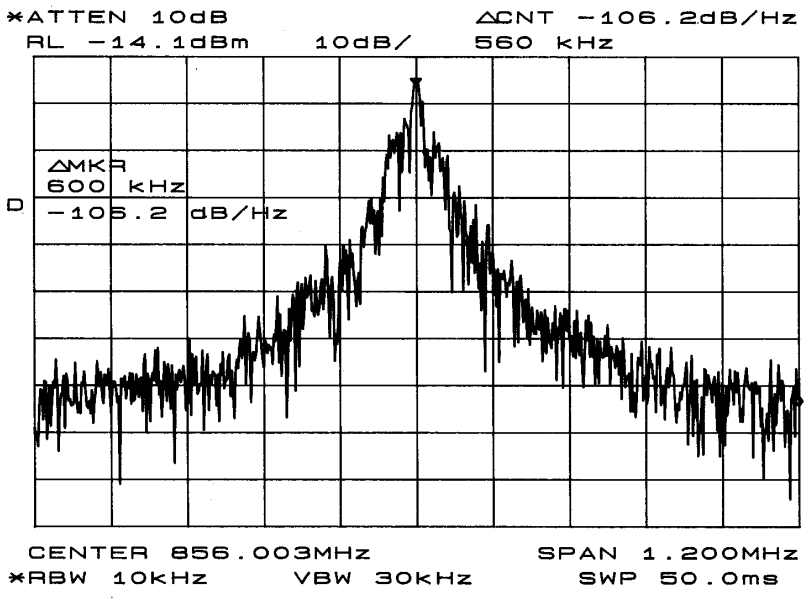

Figure 6.13 The output power spectrum of second prototype with oscillation frequency equal to 856MHz and resolution bandwidth of 30 kHz.

The measured differential output amplitudes of two prototypes are 1.92 Vp and 1.85 Vp, respectively. In the first prototype, the measured phase noise at 100kHz offset from the carrier is –96 dBc/Hz and that at 600kHz offset is –112 dBc/Hz The measured differential phase noise performance of the first prototype agrees very well with the theoretically expected value. The output power had variation less than 1 dBm and the phase noise varies less than 1.5 dBm throughout the whole frequency-tuning range. The phase noise and output signal power versus its operating frequency is shown in Figure 6.14.

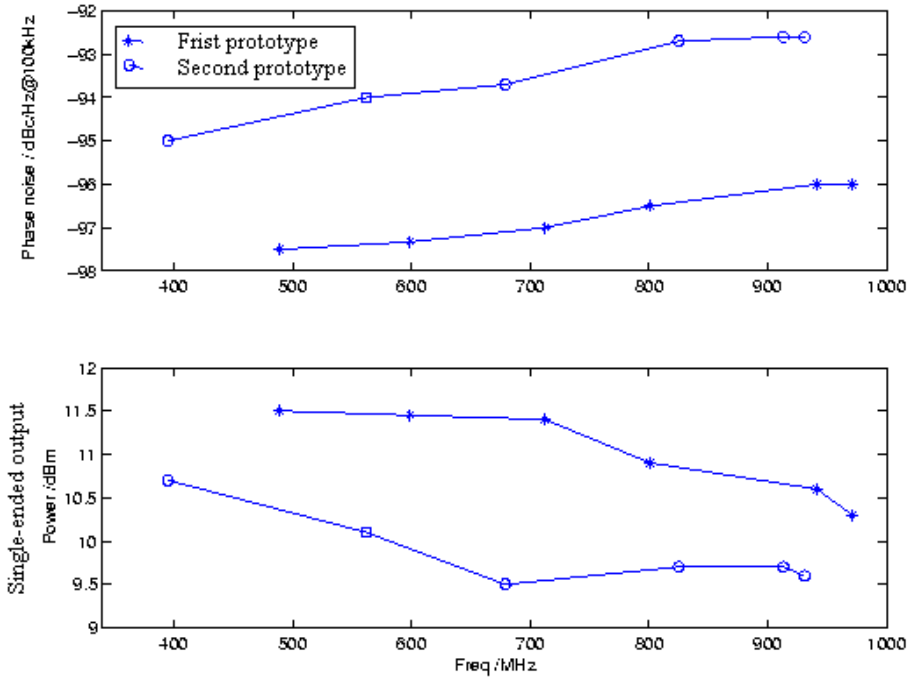

Figure 6.14 Phase noise and output signal power versus operating frequency

Owing to the reduction of the output signal amplitude and the degradation of the skew rate in the delay cells, the phase noise of the second prototype is increased. The measured phase noise of the second prototype is –92.7 dBc/Hz at 100kHz offset and –108.2dBc/Hz at 600kHz offset. The phase noise performance is degraded but it still meets the minimum requirement of the system. As shown in Figure 6.14, the output power had variation less than 1.2 dBm and the phase noise varies around 3.4 dBm throughout the whole frequency-tuning

range. The I-Q mismatch was also measured. There is 2.5 ps mismatch between I output signal and Q output signal when the oscillation period is 1030 ps. The phase mismatch is thus 0.87 degrees. The gain mismatch is 0.42 dB. It gives rise to around 32-dB image suppression theoretically.

6.3.3 X-counter

Figure 6.15 illustrates the input and output waveform of the divide-by-4 X-counter operating at 930 MHz.

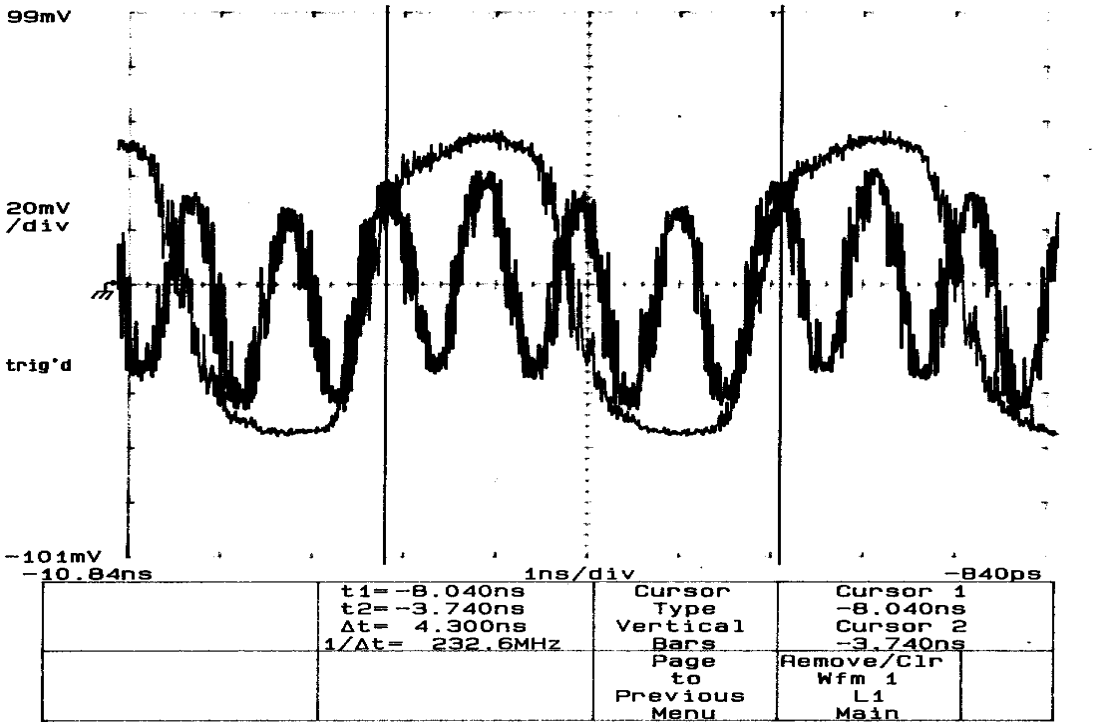

Figure 6.15 Output waveforms of the divide-by-4 X-counter

The plot is obtained by a digital oscilloscope (HP 54522A) with a high-impedance probe. In Figure 6.15, the correct function of divide-by-4 is demonstrated. It consumes 2 mW from a 2-V supply.

6.3.4 Programmable M-Counter

Figure 6.16 shows the input and output waveform of the programmable M-counter operating at 952.2 MHz.

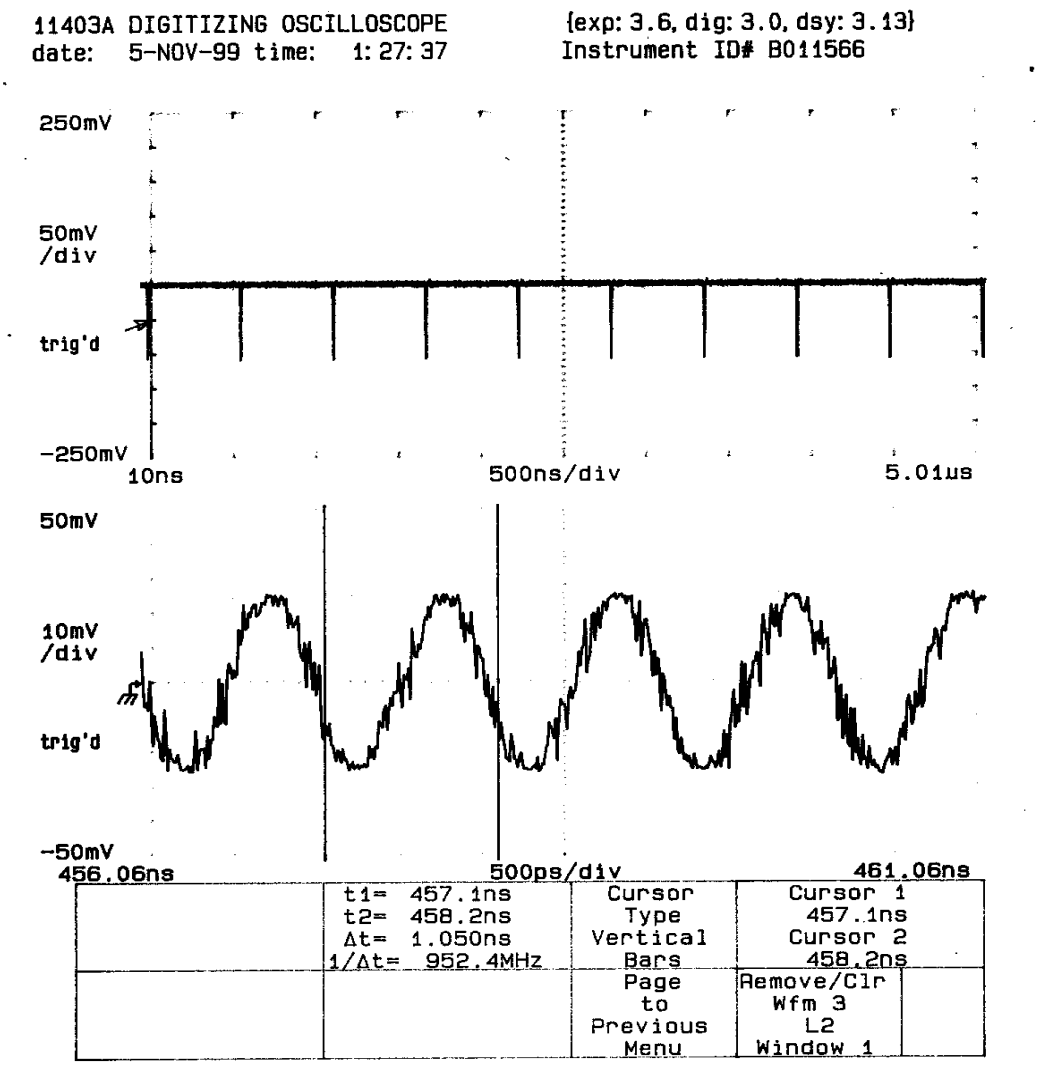

Figure 6.16 Output waveforms of the programmable counter with M = 529

In the figure, the upper waveform is the output of an inverter, which is connected directly to the M-counter output, and the lower one is the output waveform of the free-running ring oscillator. The ring oscillator acts as the input signal source of the M-counter. The M-value of counter can be changed up to 2070 according to the bits of the digital controls as expected.

6.3.5 Divide-by-16 N-counter

The single-ended output spectrum of the N-counter with a 1.76-GHz input signal is shown in Figure 6.17.

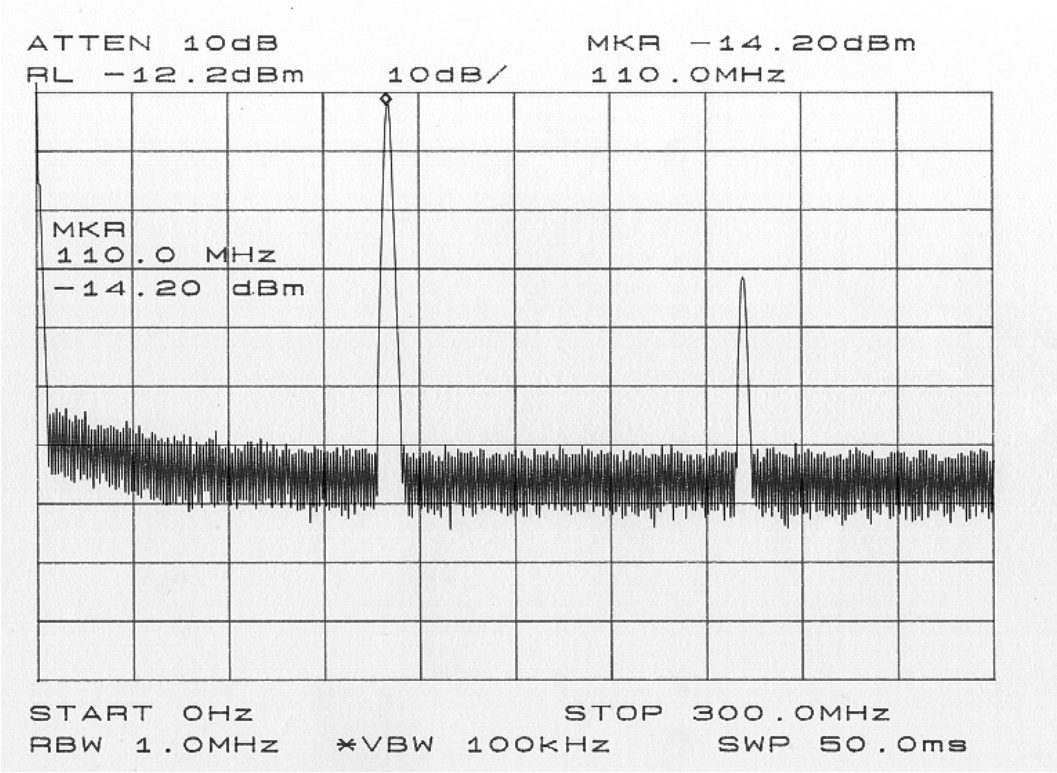

Figure 6.17 The single-ended output spectrum of the N-counter

The minimum detectable signal is 252 mVp differentially as the value obtained from simulation with a 1.8-GHz input signal. With the minimum acceptable input signal level, the prescalar can count correctly with an input signal from 824 MHz to 1.8 GHz. It consumes 5mW from a single 2-V supply.

6.3.6 Loop filters

The passive components of the filters are measured by a precision LCR meter (HP 4284A) with the loops being opened. The results are summarized as follows:

Parameters		**Upper loop filter**		**Lower Loop filter**	
		Designed	**Measured**	**Designed**	**Measured**
Passive elements	R_1	502 Ω	508.732 Ω	2.26 kΩ	2.35 kΩ
	C_1	439.8 pF	439.8 pF	279 pF	297 pF
	C_2	87.95 pF	100 pF	19.16 pF	22.1 pF
	R_4	502 Ω	642 Ω	1.13 kΩ	1.337 kΩ
	C_4	429.8 pF	497.1 pF	558 pF	609.37 pF

Table 6.2 Passive component value of the loop filters

The value of the capacitor is larger than the designed due to the parasitic of the wiring, of the linear capacitor and of the subsequent stage. The variations of the resistors are larger than that of capacitor as expected in CMOS process. Smaller value resistors have larger variation because their values are easier to be altered by the wiring and even the contacts between the layers. Using the behavior model with the measured values, the open-loop responses of two loops can be obtained as shown in Figure 6.18 and Figure 6.19. The simulation results show that the locations of the crossover frequencies are maintained as designed values, and the phase margins of the loops are degraded only by 2 degrees.

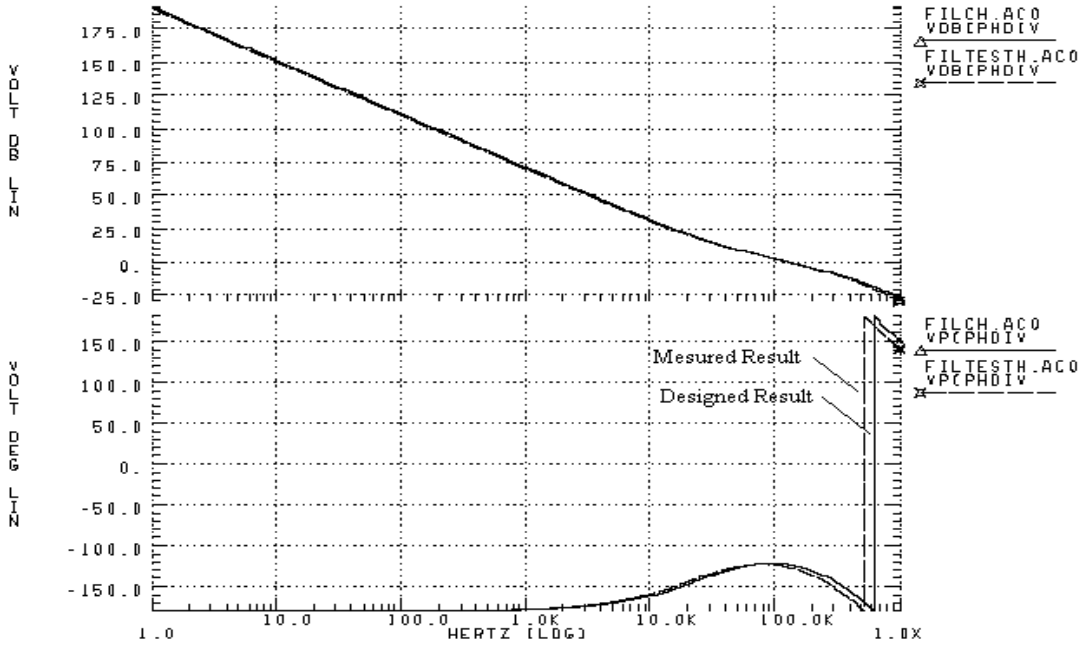

Figure 6.18 Open-loop response of the measured upper loop filter

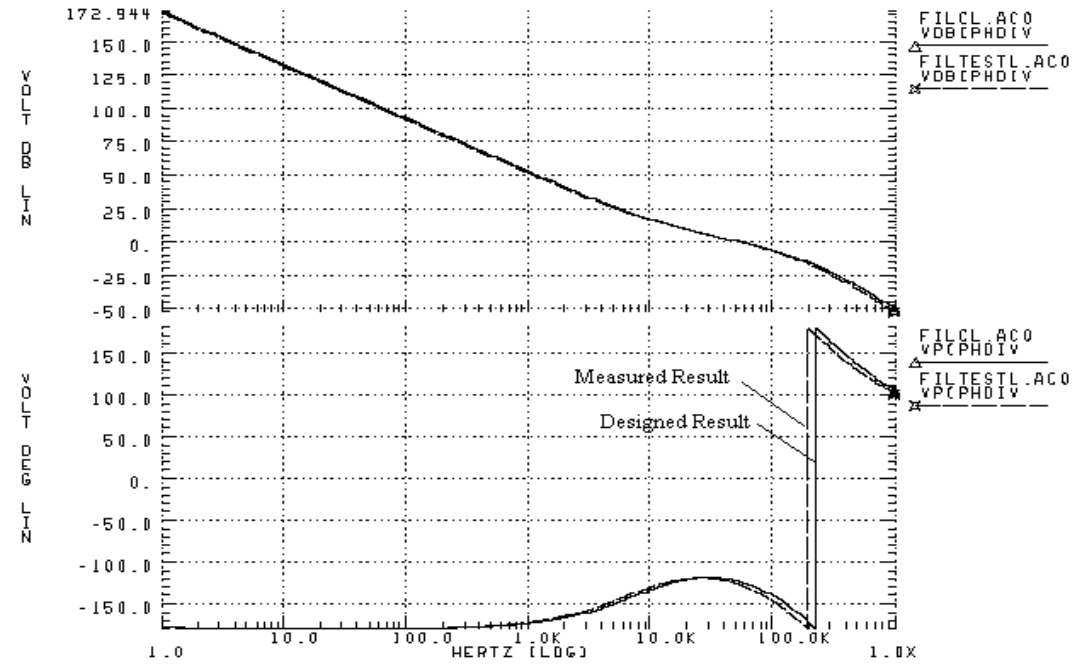

Figure 6.19 Open-loop response of the measured lower loop filter

6.4 Synthesizer Testing

The synthesizer is tested by applying the optimal bias condition, which is obtained from the individual testing of each building block. The 100-MHz frequency reference source is generated by a signal generator (HP E4422B) and the 800-kHz reference is synthesized by another signal generator (Marconi 2052).

6.4.1 Lower loop

The output spectrum of the ring oscillator is shown in Figure 6.20 with a reference frequency of 800 kHz and an M value of 1079.

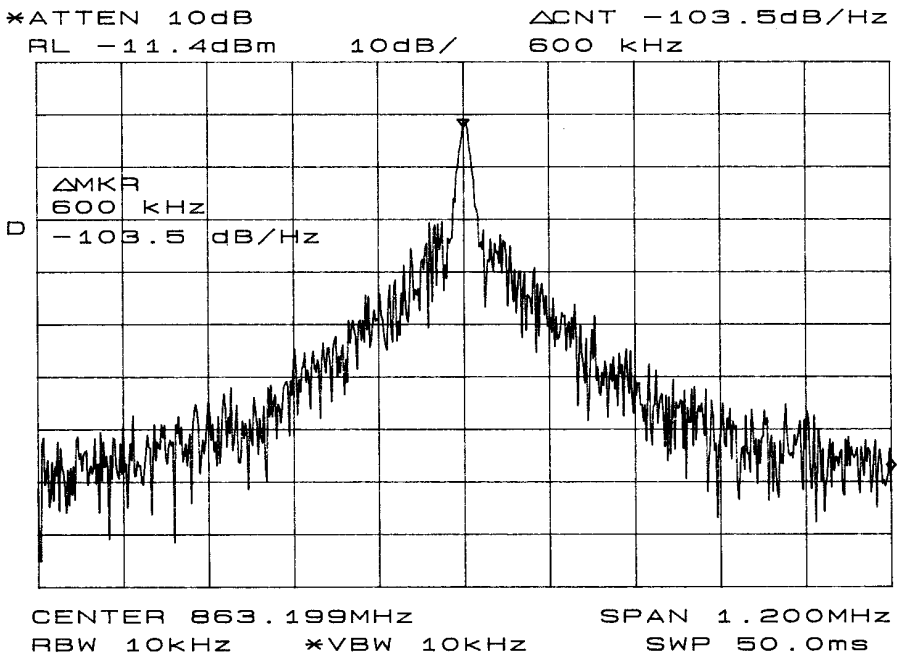

Figure 6.20 Single-ended output spectrum of lower PLL with frequency span of 1.2 MHz

The lower loop is locked to the expected value of 863.2 MHz. The differential phase noise is – 106.5 dBc/Hz at 600k-Hz offset. The degradation of the phase noise performance is mainly due to the larger phase noise of the free running ring oscillator and additional 2-dB

more noise coming from the other circuits, such as charge pump and PFD in the loop. Figure 6.21 and Figure 6. 22 show the plots of the output spectrum with larger frequency spans.

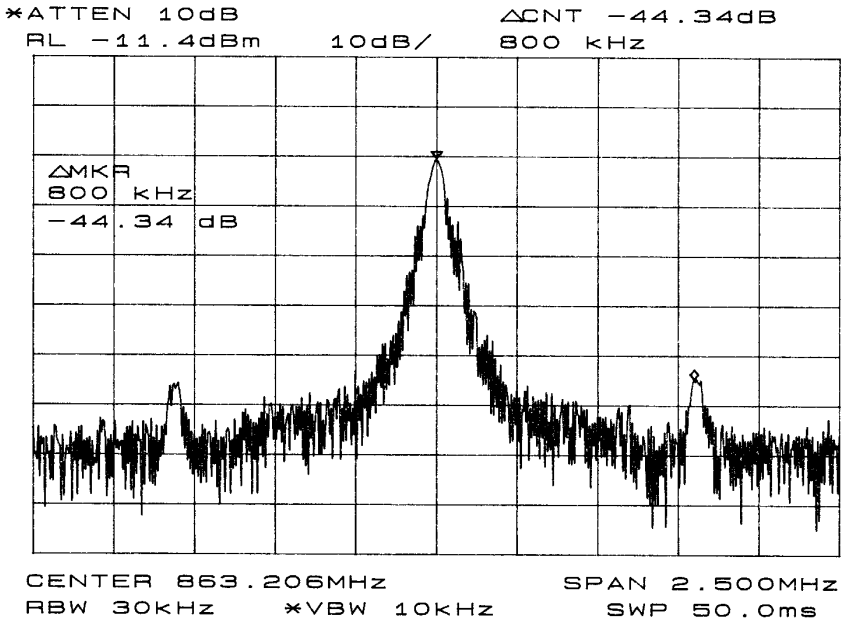

Figure 6.21 Output spectrum of lower PLL with frequency span of 2.5 MHz

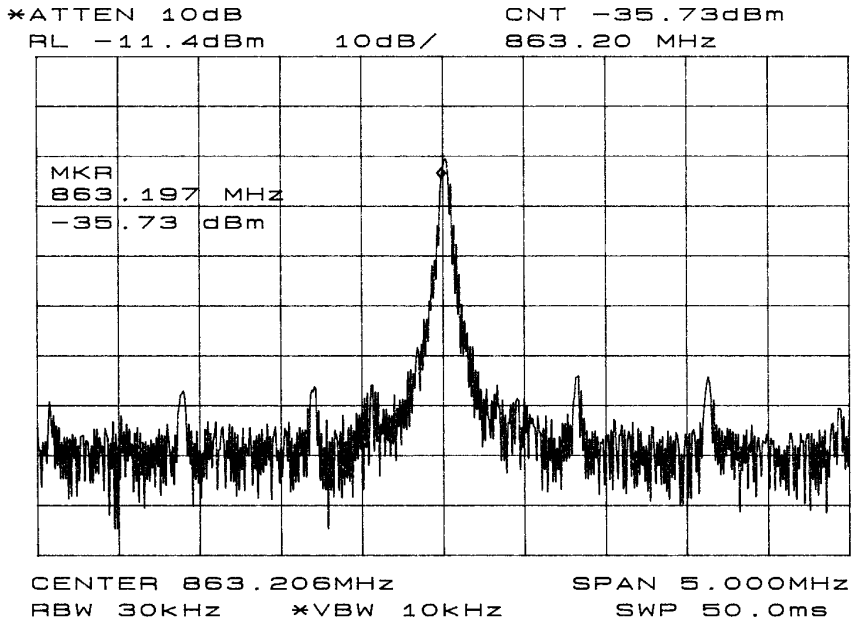

Figure 6. 22 Output spectrum of lower PLL with frequency span of 5 MHz

The figures above illustrate the spur response of the loop. The unwanted sidebands appear at frequency offsets of 800 kHz and multiple from the carrier with a magnitude of

- 44.3 dBc. The reason of large value of the spurs is due to the unexpected substrate coupling to the control line of the VCO. It causes FM modulation at the oscillator. The large K_V of the ring oscillator makes the design very sensitive to the fluctuation of the substrate. In order to verify this fact, the PFD, loop filter and the charge pump is turned off and the ring oscillator is operating with the M-counter. The output spectrum of the ring oscillator in this condition is shown in Figure 6.23.

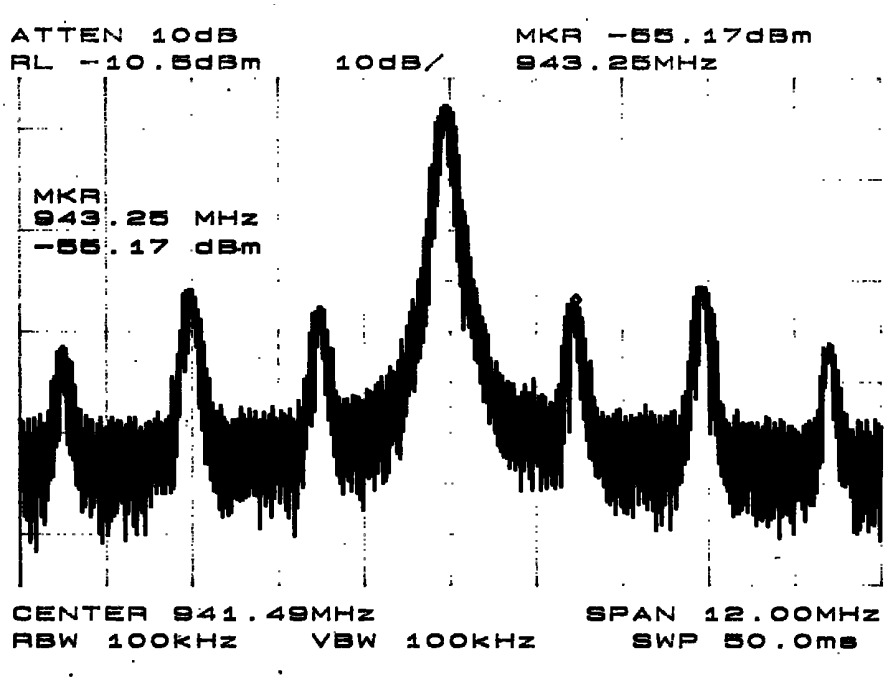

Figure 6.23 The plot of substrate coupling to the oscillator output

From Figure 6.23, the sidebands have large magnitude of around –40dBc at the offset frequencies as the operation frequencies of the intermediate stages in the M-counter. When the loop is in lock, the sidebands can be attenuated a bit due to the feedback action but it still cannot be significantly reduced. By tuning on and off of the reference, it is found that the substrate noise coupling to the VCO is mainly from the signals in the programmable counter but not from the reference source. After passing through the X-counter, the spur levels are reduced by approximately 2-dB as shown in Figure 6.24.

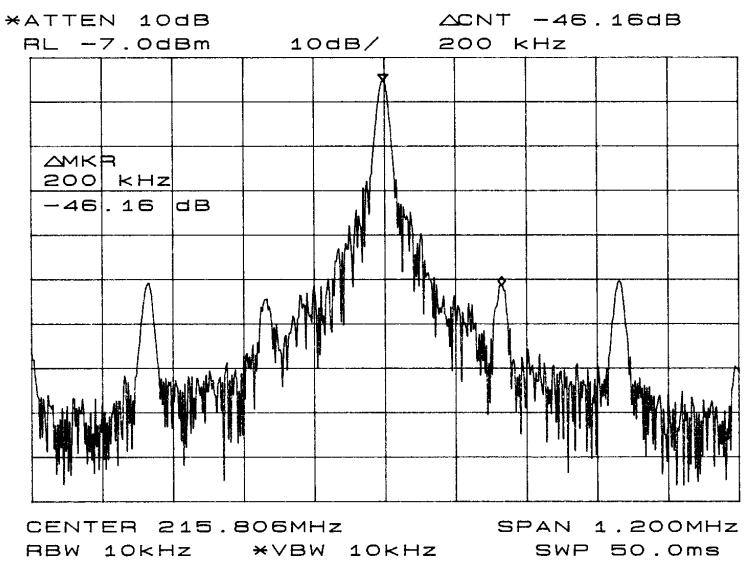

Figure 6.24 The output spectrum of X-counter.

The plot of the control voltage of the ring VCO when the channel is changed from 400 MHz to 863.2 MHz is shown in Figure 6.25. The plot is obtained by a digitizing oscilloscope (Tektronix 11403A) with a dc probe.

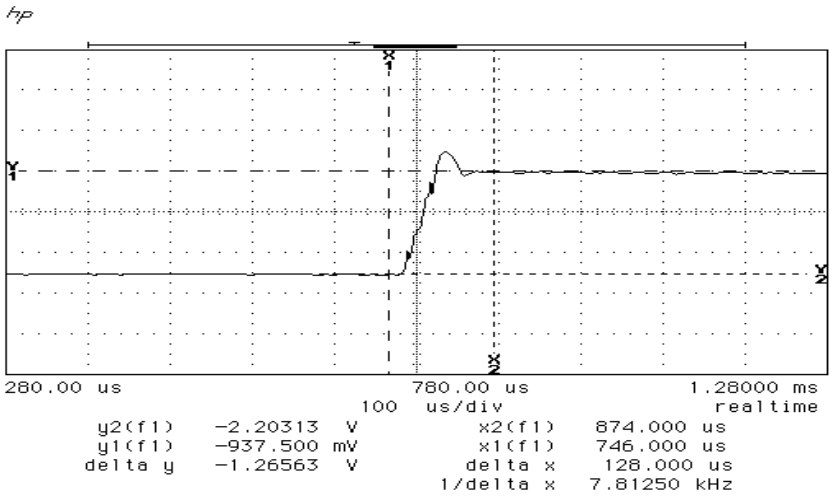

Figure 6.25 The control voltage of the Ring VCO.

The measured settling time of the loop is around 128 μs, which is close to the estimated value of 125 μs.

6.4.2 N-Counter

It is found that signal path from the mixer to the prescalar output has some problem. With the upper loop being open and the operation frequencies of the LC-oscillator and the ring oscillator being changed, the output frequency of the N-counter remains fixed at around 27MHz as shown in Figure 6.26. One of the possible problems is that high-frequency prescalar right after the SSB mixer is self-oscillating, which would happen if the amplitude of the prescalar input signal is too small. Unfortunately, probing pad has not been put to the SSB mixer output due to the high sensitivity of this high-frequency output node and the output of the mixer cannot be probed for verification in the chip. However, this can be confirmed by the individual testing of VCO that shows a reduction of its output amplitude and would result in a smaller amplitude at the mixer output.

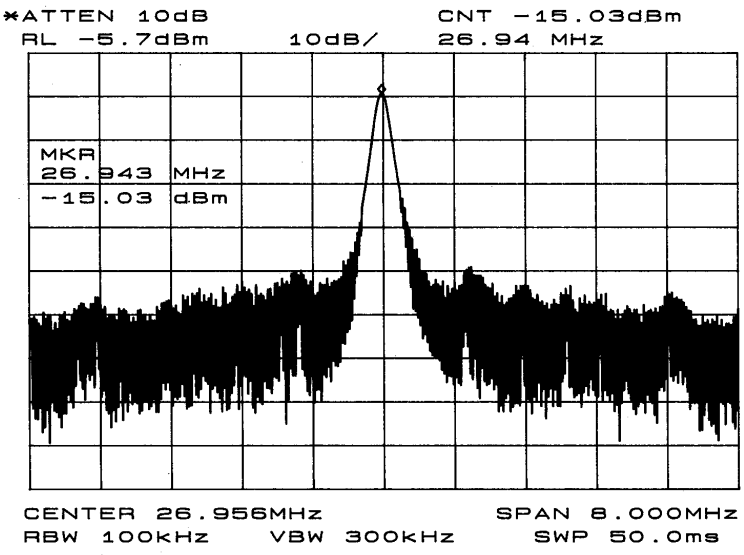

Figure 6.26 Self-oscillating N-counter output.

In order to increase the input signal amplitude of the prescalar, the supply voltage and bias current of the LC oscillator are increased to 1.5 V and 25mA, respectively. The output amplitude of the LC-oscillator is increased to 2.2 Vpp and the phase noise is –112.5 dBc/Hz at

600kHz in this bias condition. The larger oscillation amplitude is obtained from the sacrifice of the power and the tuning range of the oscillator as shown in Figure 6.9. With this new bias condition, the output spectrum when f_{LC} = 1.784 GHz and $f_{X\text{-counter}}$ =215.8 MHz is shown in Figure 6.27. It shows that the output frequency of the N-counter becomes 98 MHz for N being 16 and thus the counter can function correctly.

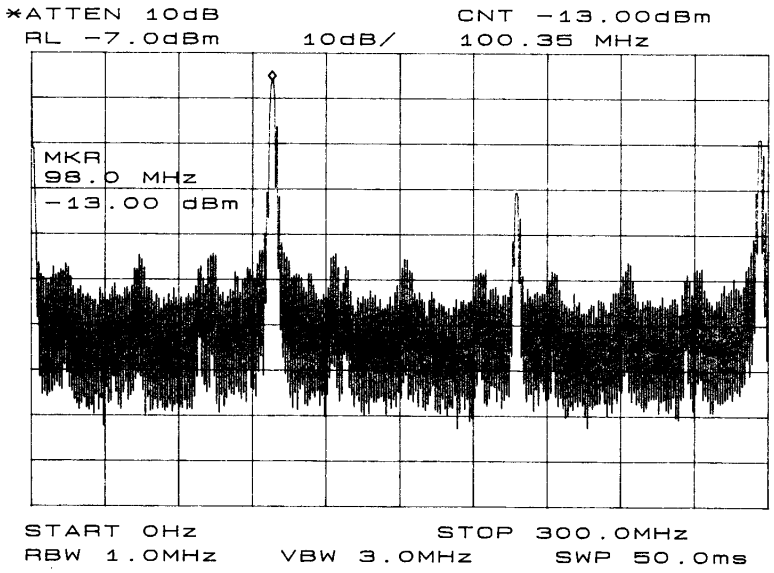

Figure 6.27 Output spectrum of open-loop high-frequency N-counter with new bias condition of the LC VCOs

6.4.3 The Whole Synthesizer

The measured output spectrum of the whole synthesizer is shown in Figure 6.28 when M is equal to 1300. The measured differential phase noise is –111 dBc/Hz at 600kHz offset from a 1.86-GHz carrier. The increase of phase noise is due to larger LC-oscillator free-runing noise, the non-neglected noise contribution from the N-prescalar and the substrate noise coupling. The synthesizer can be tuned from 1.8698 GHz to 1.8492 GHz and therefore the measured tuning range is around 20.6 MHz. The zoom-out plot of the synthesizer output is

shown in Figure 6. 29. The unwanted spur levels are much larger than that expected due to serious substrate coupling of the signals in the programmable couter.

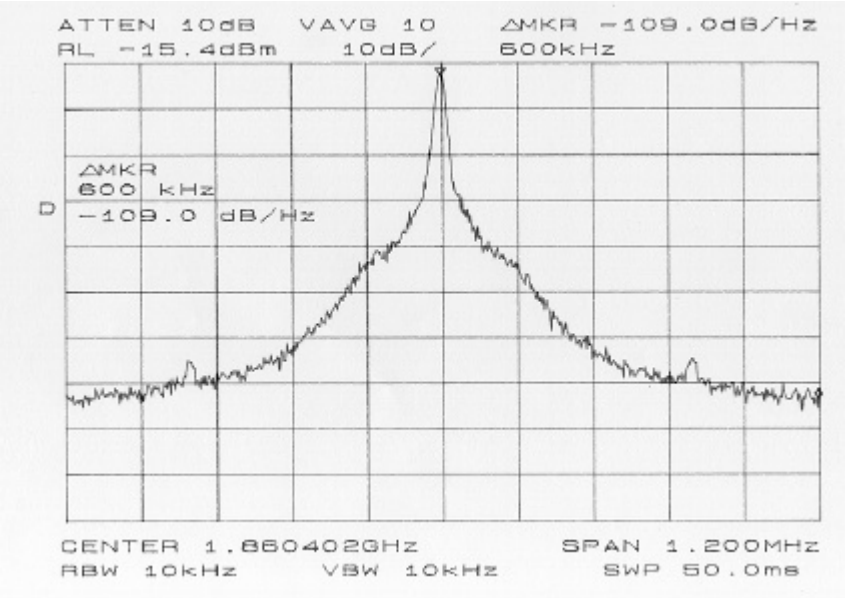

Figure 6.28 Single-ended output spectrum of the whole synthesizer

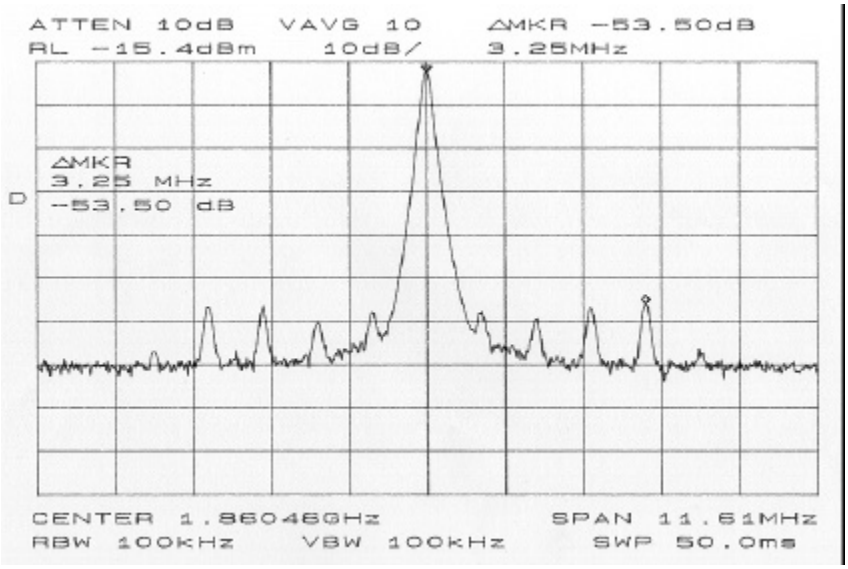

Figure 6. 29 Output spectrum of the whole synthesizer with 11.6-MHz span

The testing results are summarized as follows:

Blocks	Designed	Measured
LC-Oscillator	Fc = 1.82 GHz to 1.923 GHz Phase noise -119 dBc/Hz@ 600 kHz consumes 10.4 mW	Fc = 1.874 GHz to 1.928 GHz Phase noise -115 dBc/Hz @ 600kHz consumes 32.5 mW
Ring-Oscillator	Fc = 414 MHz to 930 MHz Phase noise -112 dBc/Hz @ 600 kHz consumes 30 mW	*1st prototype* Fc = 460MHz to 970 MHz Phase noise -112 dBc/Hz @ 600kHz *2nd prototype* Fc = 356MHz to 931 MHz Phase noise -108 dBc/Hz @ 600kHz consumes 30 mW
N-Counter	N = 16 with power of 5mW	N = 16 with power of 5mW
X-Counter	X = 4 with power of 2mW	X =4 with power of 2mW
M-Counter	M_{max} = 2070 consumes 3mW	M_{max} = 2070 consumes 3.5mW
Low-Frequency Loop	Fc = 400 MHz to 900 MHz Phase noise -108 dBc/Hz @ 600 kHz Settling time Ts = 125 μs	Fc = 400 MHz to 900 MHz Phase noise -106.5 dBc/Hz @ 600 kHz Settling time Ts = ~128 μs
The Synthesizer	Fc = 1.82 GHz to 1.923 GHz With 103-MHz tuning range Phase noise -119 dBc/Hz @ 600kHz consumes 75 mW	Fc=1.8698GHz to 1.8492GHz With 20.6-MHz tuning range Phase noise -111 dBc/Hz @ 600kHz consumes 95 mW

6.5 Verification

In order to check why the amplitude of the mixer output becomes unexpectedly smaller, the mixer is simulated with *HSPICE* for three different cases. In case I, the mixer is simulated with its nominal designed condition using the BSIM3 model of the run that was used in the design phase. In case II, the model of the actual run for the system fabrication is used with the measured amplitude of the LC-oscillator in nominal bias condition. Finally, the bias condition of LC-oscillator is changed according to the testing (Vdd = 1.5 and I_B = 20mA).

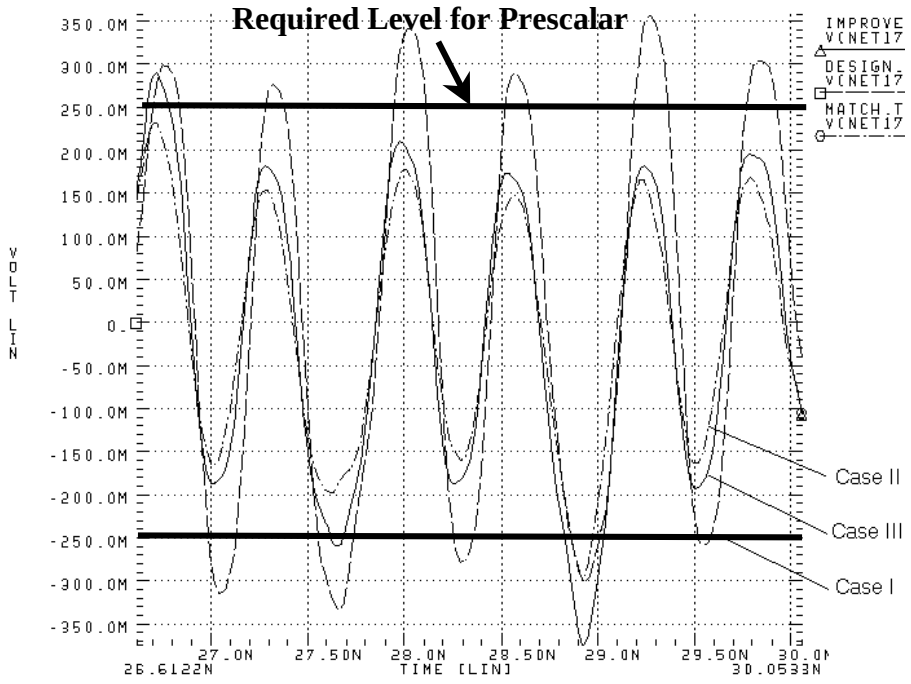

Figure 6.30 Waveforms in high-frequency prescalar input

The input signal waveforms at the mixer output for the three cases are shown in Figure 6.30. As shown in the Figure 6.30, the amplitude of the mixer output signal is reduced if the actual model is used.

The small signal gains of the mixer as conditions of the case I and of the case III are obtained by SPICE simulation and shown in Figure 6.31. The smaller loading resistance, smaller input g_m and larger parasitic capacitance at the output nodes contribute to the reduction of dc gain and output bandwidth of the mixer and thus make a reduction of its gain at the designed IF. The voltage gain at the designed output frequency (1.6 GHz) is reduced by approximately 0.6. The reduction of both LC-oscillator output signal and the gain of the mixer make the input signal of the prescalar smaller than the measured minimum value of 252 mVp. The increase of the LC-oscillator amplitude by pumping more current and increasing its supply voltage can make the signal amplitude larger, but the amplitude still cannot increase to the original design level. Thus, the insufficient large input signal of the prescalar accounts for the much smaller tuning range of the prescalar and thus the synthesizer

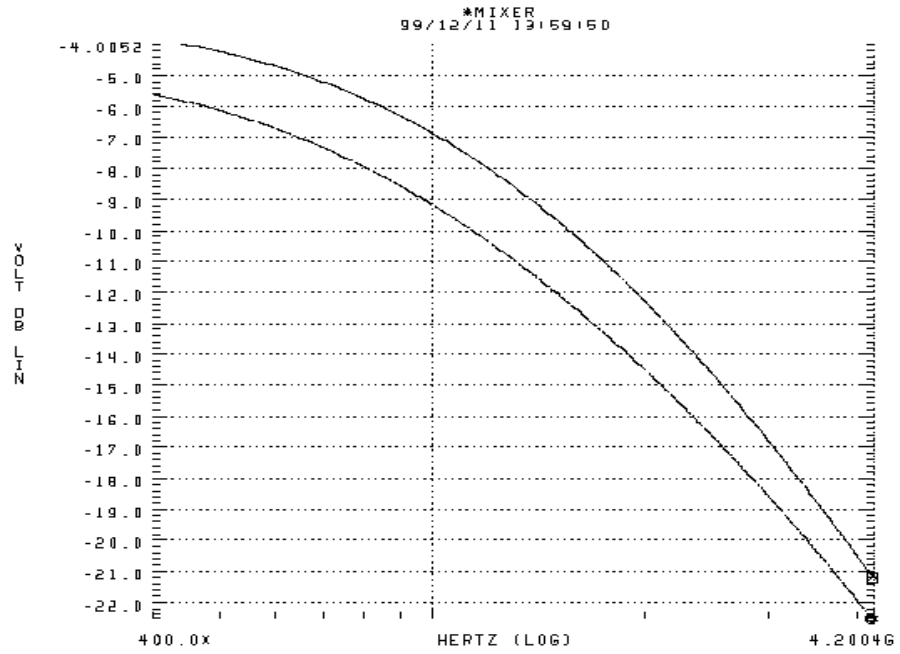

Figure 6.31 The small signal gains of the mixer in case I and in case III

Reference

[4] K. B. Ashby, W.C. Finley, J.J. Bastek, S. Moinian, and I. A. Koullias, "High Q inductors for wireless applications in a complementary silicon bipolar process", in *Proc. Bipolar and BiCMOS Circuits and Technol. Meet*, pp179 - 182, 1994.

[5] Ali M. Niknejad, "Analysis, Design, and Optimization of Spiral Inductors and Transformers for SI RF ICs", *M. Phil. Thesis*, University of California, Berkeley, 1997.

[6] Theerachet Soorapanth, C. Patrick Yue, Derek K. Shaeffer, Thomas H. Lee, S. Simon Wong, "Analysis and Optimization of Accumulation-Mode Varactor for RF ICs", *Symposium on VLSI Circuits Digest of Technical Papers*, 1998.

Chapter 7 Conclusion

7.1 Further Improvement

The dual-loop CMOS synthesizer using HP0.5-μm N-well CMOS process is designed and measured. Most building blocks have the designed performance except the high-frequency SSB mixer with smaller output amplitude, which limits the tuning ability of the synthesizer. Actually, the SSB mixer requires very stringent high-frequency performance, which includes output frequency of 1.6 GHz with both input frequencies of around 100 MHz and 1.8 GHz. One of the possible solutions to release such tough requirements is putting a high-frequency prescalar between the SSB mixer and the LC-oscillator. The prescalar can reduce the input frequency of the mixer RF input. However, the trade-off of this proposed architecture is the reduction of the low-frequency loop reference frequency due to the required channel spacing. Thus, in order to maintain the designed large loop bandwidths, a larger modulus number of the X-counter may be required to compensate the change and at the same time, the tuning capacity of the VCO in low-frequency loop should be increased but it is already very large.

7.2 Performance Comparison

Table 7.1 summarizes the performance of different monolithic frequency synthesizers published in recent years for comparison purpose.

Designs	Work in [1]	Work in [2]	Work in [3]	This work
Carrier Frequency	1.8 GHz	1.6 GHz	900 MHz	1.8 GHz
Channel Spacing	200 kHz	600 kHz	200 kHz	200 kHz
No. of Channel	124	N.A.	124	103
Process	0.4-μm CMOS	0.6-μm CMOS	0.5-μm CMOS	0.5-μm CMOS
Architecture	Fractional-N	Fractional-N	Dual-loop	Dual-loop
Supply Voltage	3 V	3 V	2 V	2 V
Reference Frequency	26.6 MHz	61.5 MHz	1.6 MHz 205 MHz	800 kHz 100 MHz
Chip Area	3.23 mm^2	1.6 mm^2	2.64 mm^2	2 mm^2
Loop Filter	On-chip	On-chip	On-chip	On-chip
Loop Bandwidth	45 kHz	200 kHz	40 kHz 27 kHz	120 kHz 42 kHz
Phase Noise at 600-kHz offset	-121 dBc/Hz	-115 dBc/Hz	-121.8 dBc/Hz	-111 dBc/Hz
Power Consumption	51 mW	90 mW	34 mW	95 mW

7.3 Conclusion

In this thesis, the design of a 2-V 1.8-GHz fully integrated CMOS frequency synthesizer is presented. The dual-loop architecture to obtain more optimal trade-off among phase noise,

channel spacing, reference frequency and settling time compared to the conventional integer-N phase-locked loop architecture is discussed. The synthesizer prototype is fabricated using a standard HP 0.5-um N-well CMOS process without any external component.

A ring-type voltage-controlled oscillator with a 89% frequency tuning range with a 643-MHz carrier is designed with a constant 15-mA current consumed from a single 2-V supply. The first prototype achieves a measured low phase noise of -112 dBc/Hz at 600-KHz, while the second one have phase noise of -108 dBc/Hz at 600-KHz offset. The measured differential output amplitude is as large as 1.85 V. The phase noise and the output amplitude vary less than 1.2 dB throughout the range. The VCO has low-phase noise comparable to the performance of LC based integrated oscillators with reasonable power. At the same time, it provides a large amplitude output signal, which usually is limited in integrated CMOS LC, oscillators to prevent devices from operating in linear region. The high-frequency LC-oscillator is realized using double-layer inductors and accumulation-mode varactors and achieves a measured free-running phase noise of -115 dBc/Hz at 600kHz offset with a 1.88-GHz carrier.

The synthesizer employs a dual-path active loop filter to minimize its chip area. The measured phase noise of the low-frequency loop is -108.5 dBc/Hz at 600 kHz offset with a carrier at 863.2MHz and the settling time is 128 μs The measured phase noise of the whole synthesizer is -111 dBc/Hz at 600-kHz offset from a 1.87-GHz carrier. With an active chip area of 2000 x 1000 μm^2, the test chip consumes 95mW.

Reference

[1] J. Craninckx and M. Steyaert, "A Fully Integrated CMOS DCS-1800 Frequency Synthesizer", *IEEE Journal of Solid-State Circuit*, Vol. 33, No. 12, Dec. 1998.

[2] J. F. Parker, and D. Ray, "A 1.6-GHz CMOS PLL with On-chip Loop Filter", *IEEE Journal of Solid-State Circuit*, Vol. 33, No. 3, Mar. 1998.

[3] Yan Shing Tak, "A 2-V 900-MHz Monolithic CMOS Dual-loop Frequency Synthesizer for GSM Receivers", *Master Thesis*, Hong Kong University of Science and Technology, Nov. 1999.