A Monolithic 900-MHz CMOS Wireless Transceiver

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by

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A Monolithic 900-MHz CMOS Wireless Transceiver

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for the Degree of

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ABSTRACT

This dissertation demonstrates a monolithic 900-MHz CMOS wireless transceiver. Single-conversion architecture with a high-IF of 70 MHz is chosen for the receiver and direct modulation architecture is chosen for the transmitter to save components, to maximize the image rejection, and to minimize the chip area.

The transceiver integrates all building blocks on-chip, including a low-noise amplifier with an input-matching network, an image-rejection RF filter with a notch filter, a fully-integrated fractional-N frequency synthesizer with sigma-delta modulation, image-rejection mixers, phase shifters, a high-Q channel-selection IF filter, a variable-gain amplifier with continuous-time offset cancellation, a band-pass sigma-delta analog-to-digital converter and a class-E power amplifier.

The proposed transceiver has been designed and fabricated with 0.5μm CMOS process. The measurement of the whole transceiver has been completed. The image rejection, noise figure and linearity of the receiver are high enough to achieve a sensitivity of -90 dBm.

This research confirms that a standard CMOS process can be used to implement a fully monolithic transceiver for short-distance wireless communications.

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TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

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Chapter 1

INTRODUCTION

The explosive growth of wireless applications has resulted in an increasing demand for wireless transceivers with low cost, low power consumption and small form factors. In order to meet the demand, much work has been focused on and recently demonstrated in realizing fully-integrated single-chip receivers in a low-cost CMOS process [1]-[4]. Unfortunately, all these transceivers still require some special post-processing [2] or some off-chip components, including off-chip or bondwire inductors, [1][4], input matching network [3], filters [4], or VCOs [1][2][4], which inevitably increases the cost of the whole transceiver.

This dissertation demonstrates a monolithic CMOS wireless transceiver for short-distance wireless communication with an extremely high level of integration, without off-chip components. The transceiver integrates all building blocks on-chip, including a low-noise amplifier (LNA) with an input-matching network, an image-rejection RF filter (IRF) with a notch filter, a fully-integrated fractional-N frequency synthesizer with sigma-delta modulation, image-rejection mixers, phase shifters, a channel-selection IF filter, a variable-gain amplifier (VGA), a band-pass sigma-delta analog-to-digital converter (BPSD), and a class-E power amplifier.

Single-conversion architecture with high IF (70 MHz) is chosen for the receiver to save components, to maximize the image rejection, and to minimize the chip area. All building blocks are fully differential to minimize the substrate coupling and to maximize the

linearity at a cost of larger power consumption. The receiver does not use any off-chip component and achieves a total image rejection of 79 dB. Direct-modulation with the sigma-delta modulated fractional-N frequency synthesizer, which is shared by the receiver as well, is chosen for the transmitter to save power and reduce the chip area.

The dissertation is organized into 11 chapters. Transceiver fundamentals is briefly discussed in Chapter 2 to prepare the reader for the material in the following chapters. System specification is discussed in Chapter 3. Pros and cons of different architectures for receivers and transmitters and the architecture of the proposed transceiver are also presented in this chapter. The passive components used in the transceiver are discussed in Chapter 4. The circuit implementations of the building blocks, including the low noise amplifier, the synthesizer and the variable gain amplifier, are described in Chapter 5, Chapter 6 and Chapter 7. In Chapter 8, the other building blocks including the mixers, the IF filter, the ADC and the power amplifier are briefly described. Chapter 9 discusses the effect of the IF frequency on the system performance including the image rejection, noise figure, linearity and power consumption. Chapter 10 presents the layout consideration and the experimental results of the transceiver. Finally, the conclusion and the possible improvements of the transceiver are presented in Chapter 11.

Chapter 2

TRANSCEIVER FUNDAMENTALS

In this chapter, some fundamental issues about transceiver front-ends are discussed, e.g. nonlinearity, noise figure, image rejection and phase noise.

Wireless products, e.g. mobile phones, pagers, wireless local-area-network (LAN) etc., usually consists of several basic blocks including transceiver front-ends and base-band back-ends. A transceiver front-end is a combination of a receiver front-end and a transmitter front-end. A receiver front-end converts a received radio frequency (RF) signal from an antenna into a baseband signal and a transmitter front-end converts a baseband signal into an RF signal and sends it to an antenna. The conversion is done by a few of frequency domain operation including downconversion, upconversion, filtering and amplification. The frequency domain operation is realized in physical building blocks including LNA, image-rejection filter, mixers, synthesizer, IF filter and amplifiers. Those building blocks are not perfect. Besides the wanted frequency domain operation, unwanted operations are also performed. Those unwanted operations include adding noise to the signal and distorting the signal. Therefore the performance of a transceiver is limited.

The performance transceivers is defined as the output signal-to-unwanted-signal ration (SUSR). For the transmitter, this ratio is taken at the antenna, for the receiver, this ratio is taken at its output, before demodulation and after analog-to-digital (A/D) conversion.

2.1 Linearity

Many RF and analog circuits can be approximated with a linear model to obtain their response to small signals. Nonlinearity often leads to interesting and important phenomena. For simplicity, a nonlinear system can modeled as follows:

$$y(t) \approx \alpha_1 x(t) + \alpha_2 x^2(t) + \alpha_3 x^3(t) \tag{2.1}$$

Higher orders are assumed to have much smaller gain and are therefore ignored.

Nonlinearity of analog circuits will cause problems of harmonics, gain compression, desensitization, intermodulation, etc. [5]. Intermodulation is commonly used as a measure of linearity of a circuit. Two-tone test is usually used to measure the intermodulation of a circuit. As shown in Fig. 2.1, the amplitude of the input signal is swept from small power to large power. The output signals are measured at both the fundamental frequency, ω_1 or ω_2, and the IM3 frequency, $2\omega_1 - \omega_2$ or $2\omega_2 - \omega_1$. Two curves can be plotted in log-scale based on the measured amplitude of both fundamental and IM3 components. There is an intersection point if the two lines are extrapolated. This point is called third interception point (IP_3). Input referred IP_3 (IIP_3) is often used to specify the linearity of a system.

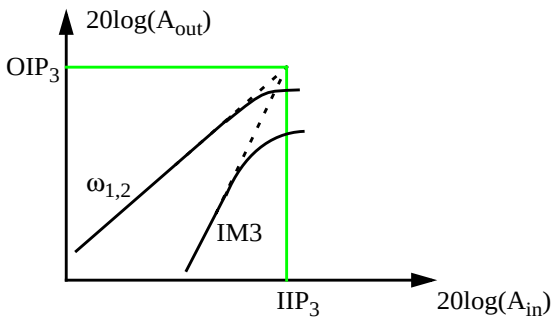


Fig. 2.1 Two-tone Test of a Nonlinear System

In a system with cascading of several stages, the IIP3 of the system, A^2_{IP3}, can be expressed as:

$$\frac{1}{A^2_{IP3}} = \frac{1}{A^2_{IP3,1}} + \frac{\alpha_1^2}{A^2_{IP3,2}} + \frac{\alpha_1^2\beta_1^2}{A^2_{IP3,3}} + \ldots \quad (2.2)$$

where $A^2_{IP3,i}$ is the IIP3 of i^{th} stage and α^2_1, β^2_1,... are gain of each stage.

2.2 Noise Figure

RF circuits always suffer from a noise problem. Noise can be defined as random interference unrelated to the desired signal. It is a kind of unwanted signal. But unlike harmonics and intermodulation, it is not a deterministic signal. For RF circuits built on CMOS technology, there are a few types of noise, e.g. thermal noise, shot noise, flicker noise, need to be considered.

In analog circuit design, signal-to-noise ratio (SNR) and noise figure (NF) are commonly used to specify the noise performance of a system. SNR is defined as a ratio of signal power over noise power. NF is defined as a ratio of SNR at the input of a system over SNR at the output of the system. i.e. $SNR=P_{signal}/P_{noise}$, $NF=SNR_{in}/SNR_{out}$

Assume in a system, matched to 50-Ω impedance, has power gain of A^2, and internal input referred noise of P_o and it is connected to a source with source noise of $P_{n,s}$. Then the NF is:

$$\begin{aligned} NF &= SNR_{in}/SNR_{out} \\ &= (P_{s,in}/P_{n,s}) / (P_{s,out}/P_{n,out}) \\ &= (P_{s,in}/P_{n,s}) / [P_{s,in} * A^2/(P_{n,s} * A^2 + P_o * A^2] \\ &= 1 + P_o/P_{n,s} \end{aligned} \quad (2.3)$$

The source noise, $P_{n,s}$, is referred to the thermal noise from a 50 Ω resistor, i.e. $V^2_{n,s}=4kTR_s\Delta f$, where k is Boltzmann's constant ($1.38*10^{-23}$ JK^{-1}), T is the temperature in

Kelvins, and R_s is the source resistance (50 Ω), and Δf is the bandwidth of interests. At room temperature, T=300^{o}K, a 50 Ω resistor has a noise power of:

$$P_{n,s}/\Delta f = 10*\log_{10}(kT/1mW) = 10*\log_{10}(1.38*10^{-23}*300/0.001) = -174 \text{ dBm / Hz.}$$

Or in a bandwidth of 200kHz,

$$P_{n,s}= 10*\log_{10}(kT*\Delta f/1mW) = 10*\log_{10}(1.38*10^{-23}*300*200*10^3/0.001) = -121 \text{ dBm}$$

In a system with a few stages in cascade,

$$NF=NF_1 + (NF_2-1)/A^2_1+(NF_3-1)/(A^2_1A^2_2)+(NF_4-1)/(A^2_1A^2_2A^2_3) +... \quad (2.4)$$

where NF_i is the NF of i^{th} stage and A^2_i is the gain of i^{th} stage. From Eq. (2.4), an important observation can be made. NF of the first stage is directly added to the NF of the whole system. The NF of each of other stages is scaled down by the total gain of stages in front of it when referred to the overall NF. Therefore, to achieve a smaller NF of the whole system, NF_1 should be as small as possible. At the same time, the gain of this stage, A^2_1, should be as high as possible so that noise contribution from following stages can be reduced.

2.3 Image Rejection

Image signal is a problem related to frequency conversion. A mixer is usually used in a receiver to downconvert the signal from RF frequency to IF frequency, as shown in Fig. 2.2. For example, if the RF signal is $A_{RF}\cos\omega_{RF}t$ and the local-oscillator (LO) signal is $\cos\omega_{LO}t$, then the output of the mixer is:

$$A_{RF}\cos\omega_{RF}t\times\cos\omega_{LO}t=1/2A_{RF}(\cos(\omega_{RF}-\omega_{LO})t+\cos(\omega_{RF}+\omega_{LO})t). \quad (2.5)$$

The component at frequency $(\omega_{RF}+\omega_{LO})$ is filtered out by the IF filter. The component at frequency $(\omega_{RF}-\omega_{LO})$ is the desired signal, and IF frequency $\omega_{IF} = (\omega_{RF}-\omega_{LO})$. The

amplitude of this signal is proportional to amplitude of RF signal and the conversion gain of the mixer, G_{mix}. That means the final IF signal is:

$$A_{RF}G_{mix}\cos(\omega_{RF}-\omega_{LO})t = A_{RF}G_{mix}\cos\omega_{IF}t \quad (2.6)$$

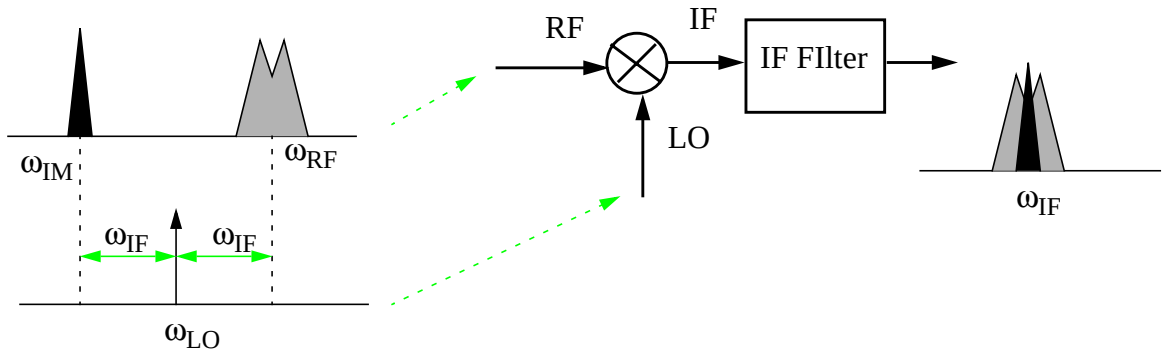


Fig. 2.2 Problem of Image Signal

However, if there is a signal at frequency $\omega_{IM}=(\omega_{LO}-\omega_{IF})$, it will be converted to IF frequency as well. This signal is called the image signal. The output of the mixer due to this signal is:

$$A_{IM}G_{mix}\cos(\omega_{LO}-\omega_{IM})t = A_{IM}G_{mix}\cos\omega_{IF}t$$

After downconversion the image signal is located at the same frequency as the wanted signal. Therefore the SUSR is decreased greatly. To maintain high SUSR of the receiver, it is necessary to remove the image signal from the wanted signal. Image-rejection (IR) filters or I-Q downconverters are often used to solve the image signal problem.

As shown in Fig. 2.3, an IR filter is adopted before the mixer. The image signal is suppressed after the IR filter. Therefore, at the output of the mixer, the power of the image signal is much lower than the wanted signal.

As shown in Fig. 2.4, I-Q downconverters can also be used to remove the image signal from the wanted signal. At node 'A', the signals are:

$$A_{RF}G_{mix}\sin(\omega_{LO}-\omega_{RF}-90^{o})t + A_{IM}G_{mix}\sin(\omega_{LO}-\omega_{IM}-90^{o})t$$

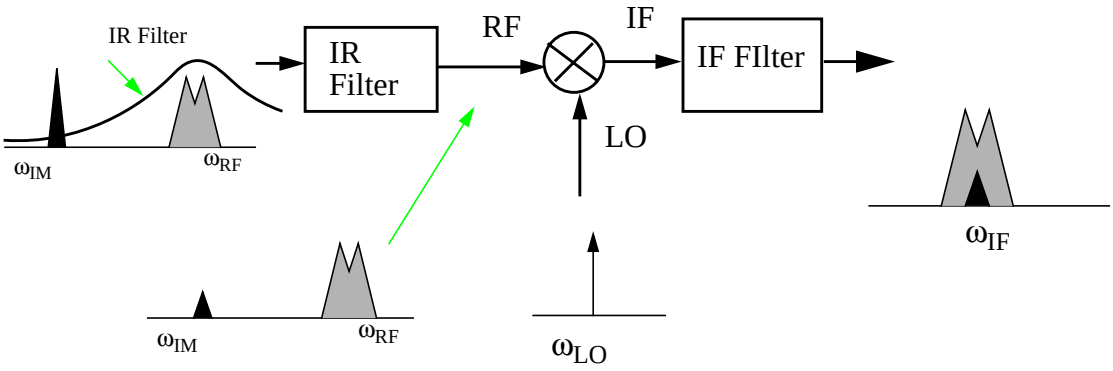


Fig. 2.3 Image Rejection Filter to Remove Image Signal

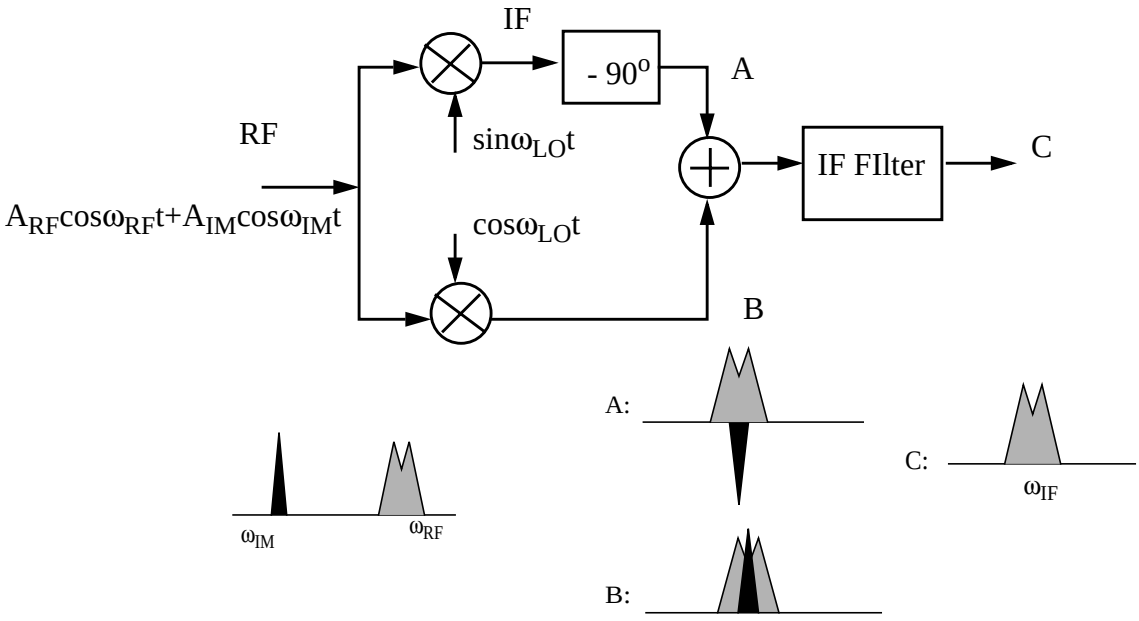


Fig. 2.4 I-Q Downconverter to Remove Image Signal

$$= A_{RF}G_{mix}\cos(\omega_{RF}-\omega_{LO})t - A_{IM}G_{mix}\cos(\omega_{LO}-\omega_{IM})t$$

At node ‘B’, the signals are:

$$A_{RF}G_{mix}\cos(\omega_{RF}-\omega_{LO})t + A_{IM}G_{mix}\cos(\omega_{LO}-\omega_{IM})t$$

Between node ‘A’ and node ‘B’, the wanted IF signals are in the same phase and same amplitude, but the image signals are in the same amplitude but with a 180^o phase difference. After summing together the two signals, the node ‘C’ consists of the wanted IF signal only.

The image signal is cancelled completely. However, in reality, the cancellation of the image signal is not complete due to the amplitude and phase mismatch between I and Q channels. A 30-dB image rejection is achievable with 0.1-dB amplitude mismatch and 1^o phase mismatch.

2.4 Phase Noise of LO Signal

In practice, the local oscillator (LO) signal is not a pure sinusoid signal. It consists of some noise at frequencies close to ω_{LO}. This is called phase noise. The phase noise (PN) of the LO signal is defined as the ratio between the noise power in 1-Hz bandwidth at a certain offset, Δf, and the carrier power, as shown in Fig. 2.5:

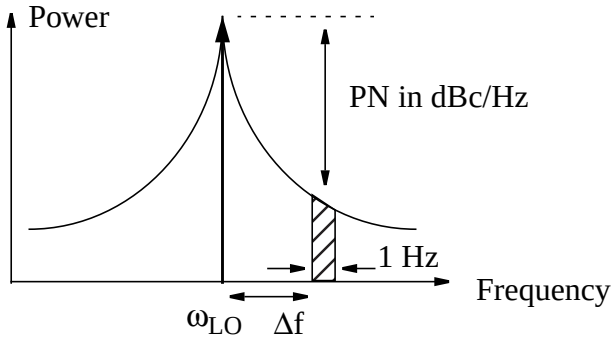


Fig. 2.5 Phase Noise of LO Signal

$$PN=10\log_{10}[(\text{noise power in 1-Hz bandwidth})/(\text{Carrier power})] \quad (2.7)$$

Because of the phase noise, the interference close to the RF frequency will generate some noise located in the signal frequency band, as shown in Fig. 2.6. Assume the signal has a bandwidth of BW and the power is P_s, and there is an interference at Δf with a power of P_i. Assume the conversion gain is one, after downconversion, the interference has a similar spectrum as LO signal. The power of the noise that located within the signal bandwidth is:

$$P_{n\_dB}=P_{i\_dB} + PN + 10\log_{10}(BW) \quad (2.8)$$

$$\text{and } SUSR=P_{s\_dB} - P_{n\_dB} =P_{s\_dB} - P_{i\_dB} - PN - 10\log_{10}(BW).$$

To achieve enough SUSR, the PN of the LO signal should be as large as possible, and the minimum requirement is:

$$PN = P_{s\_dB} - P_{i\_dB} - 10\log_{10}(BW) - SUSR. \quad (2.9)$$

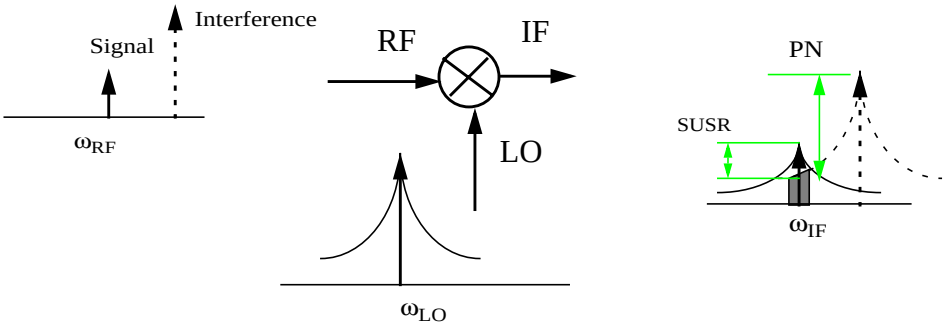


Fig. 2.6 SNR Degradation due to Phase Noise of the LO Signal

Chapter 3

SYSTEM DESIGN AND ARCHITECTURE

The system level design of the transceiver is discussed in this chapter. It starts with the discussion of the system specification. Specification of the receiver and each building block is then derived. Optimization of the system performance is also included.

3.1 System Specification

The proposed transceiver is intended for GSM-like short distance wireless application. Most of the specifications are derived based on GSM specifications. However, the sensitivity of the receiver is -90 dBm instead of -102 dBm.

3.1.1 Receiving Band

The receiving band of the system is 935 MHz to 960 MHz, as shown in Fig. 3.1. It is divided into 124 channels with a channel spacing of 200 kHz. Since two guard bands of 100 kHz are provided at both the upper end and lower end of the receiving band, only 124 channels are implemented, which is called the Absolute Radio Frequency Channel (ARFC). The center frequency of each channel, which is also called downlink (receiving) frequency, Fd, can be obtained from Eq. (3.1):

$$F_d = 935.2 + 0.2(N - 1) \text{ MHz} \quad (3.1)$$

where N=1,2,....., 124.

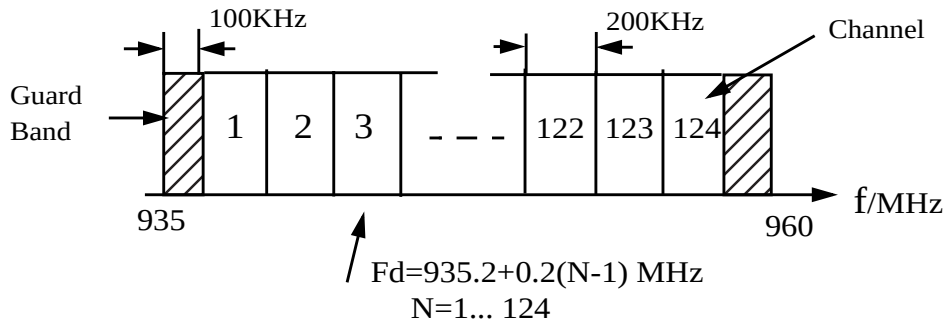


Fig. 3.1 Receiving Band

3.1.2 Sensitivity

The sensitivity is a measure of receiver performance. Although the performance of a wireless communication system is often specified in terms of the bit error rate (BER), the frame error rate (FER) and the residual bit error rate (RBER), those specifications are very impractical for the receiver front-end design. As a receiver front-end can only be evaluated by adding unwanted signals, such as noise, image signals and intermodulation signals, to the wanted signal, the performance can therefore be translated into the specification of signal-to-unwanted-signal ratio (SUSR), which can also be called as signal-to-noise ratio (SNR), if all unwanted signals are treated as kinds of noise. An approximate value for this SUSR can be found by means of BER simulations. For the GSM system, the required SUSR, which meets the BER, FER and RBER specifications, is 9 dB [5], which is also used in the proposed transceiver. The sensitivity of a receiver is defined as the minimum signal power at the input of the receiver when a minimum SUSR of 9 dB is achieved at the output of the receiver. In the proposed application, a sensitivity of -90 dBm is required.

3.1.3 Cochannel and Adjacent Channel Interferences

The interference performance is also specified by BER, FER and RBER specifications, but again an equivalent SUSR of 9 dB is assumed as the specification. The cochannel and adjacent channel interferences are defined as follows:

i) an interference signal in the same channel as the wanted signal (cochannel interference) with a power of 9 dB below the wanted signal level, as shown in Fig. 3.2;

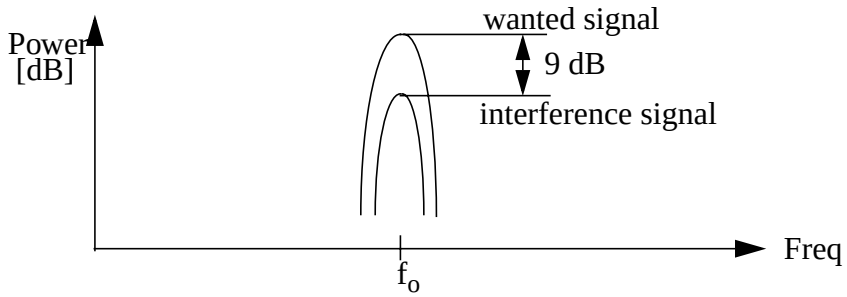


Fig. 3.2 Cochannel Interferences

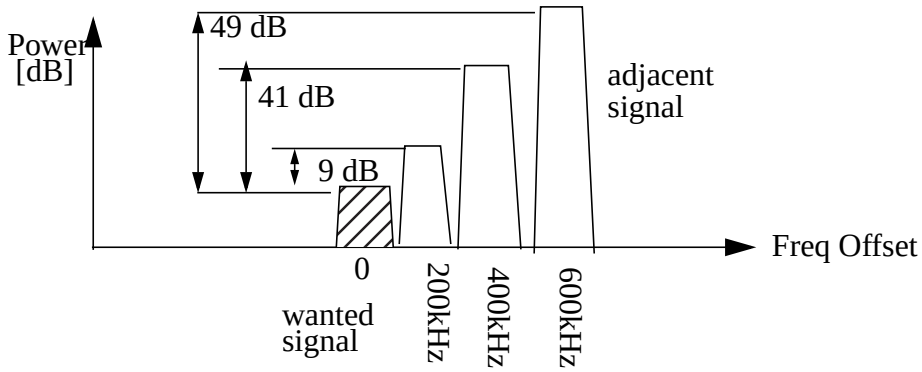


Fig. 3.3 Adjacent Channel Interference

ii) an interference signal in the channel directly adjacent to the channel of the wanted signal (at +200 KHz or -200KHz offset) with a power of 9 dB above the wanted signal, as shown in Fig. 3.3;

iii) an interference signal in the adjacent channel at +/- 400 kHz offset, with a power of 41 dB above the wanted signal, as shown in Fig. 3.3;

iv) an interference signal in the adjacent channel at +/ 600 kHz offset, with a power of 49 dB above the wanted signal;

An SUSR of 9 dB must be achieved when one of these interference signals is presented together with the minimum wanted signal.

3.1.4 Blocking Signals

The effects of interference signals at the frequency offset more than 600 kHz away from the wanted signal are specified as the blocking signal specifications. The reference sensitivity must be met when the wanted signal a accompanied by an interference signal with power level as listed in Table 3.1, which is also visualized in Fig. 3.4.

Table 3.1 The In-Band and the Out-of-Band Blocking Signal Levels

Frequency	**Power Level of Blocking Signal**
In-Band	
600 KHz <= |f-fo| <= 1.6 MHz [a]	-43 dBm
1.6 MHz < |f-fo| < 3 MHz	- 33 dBm
960 MHz < f < fo+3 MHz or 935 MHz < f < fo-3 MHz	-23 dBm
Out-of-Band	
835 MHz < f < 915 MHz	0 dBm
980 MHz < f < 1000 MHz	0 dBm
100 kHz < f < 835 MHz	-23 dBm
fo+3 MHz < f < 980 MHz or 915 MHz < f < fo-3 MHz	-23 dBm
1000 MHz < f < 12.75 MHz	-23 dBm

a. f is the frequency of the interference signal, f_o is a frequency of the wanted signal.

3.1.5 Intermodulation

As the impact of the third-order intermodulation products is most critical in a fully differential system, two 3rd order intermodulation signals are used to characterizes the nonlinearity of the receiver. The sensitivity performance is required when the following wanted signal and the interference signals are applied to the receiver.

i.) a wanted signal of -90 dBm at a frequency f_o;

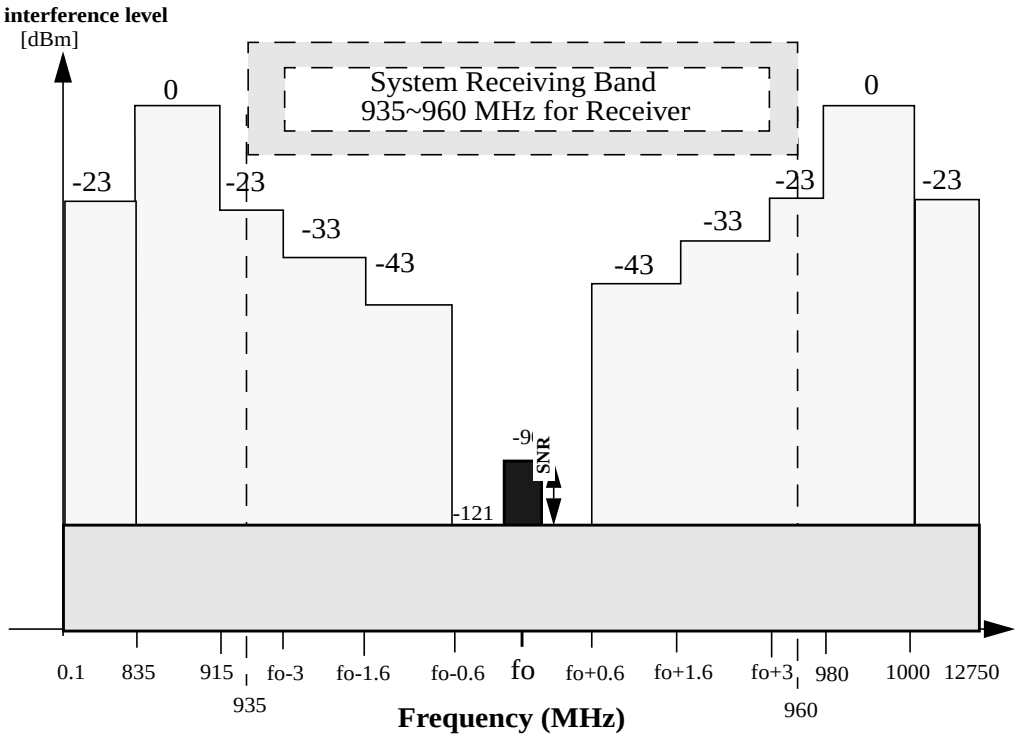


Fig. 3.4 Specifications of Blocking Signals

ii) two pseudo-random modulated signals of -50 dBm at a frequency f_1;

The frequencies of interference signals, f_1 and f_2, must be placed at 800 kHz from each other and the frequency of the 3rd order intermodulation product ($2f_1$-f_2) must be at the frequency f_o, as shown in Fig. 3.5.

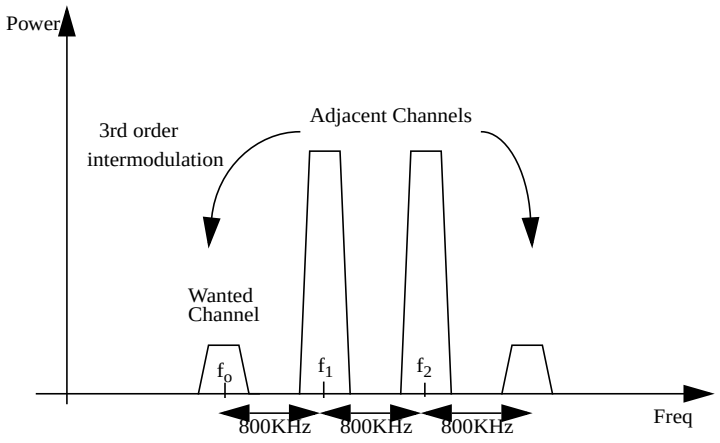


Fig. 3.5 Degradation of the receiver performance due to intermodulation

3.1.6 Output RF Power Spectrum

To avoid interfering of output RF signals to the adjacent channels, the output RF power spectrum of the transmitted signal, due to modulation, should be under the profile as shown in Fig. 3.6.

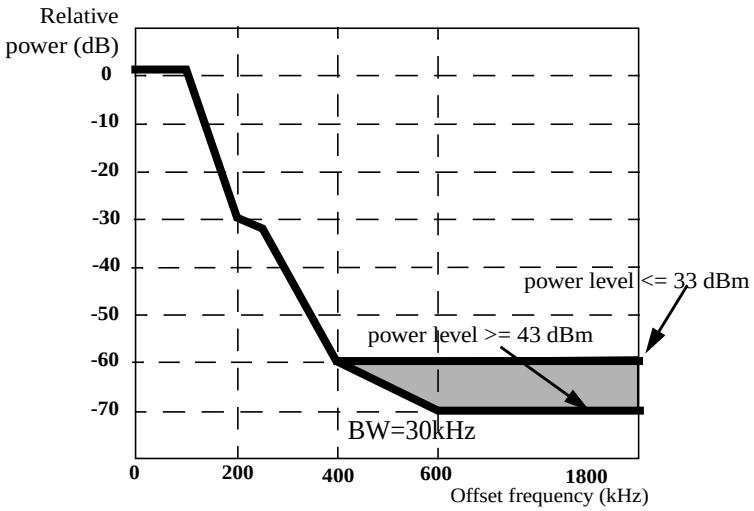


Fig. 3.6 Spectrum due to Modulation

3.2 TRANSCEIVER ARCHITECTURE

3.2.1 Receiver Architecture

Different architectures can be used to implement a receiver, e.g. high-IF, low-IF, very-low-IF and zero-IF. Selection of receiver architecture is a compromise of some tradeoffs, e.g. image rejection, noise, DC offset and power.

High-IF Architecture [1] can achieve high image rejection and use small passive components. However, there are disadvantages. Firstly, it needs RF and high-Q IF channel selection filter, which are usually off-chip. Secondly, the high-Q IF channel selection filter can introduce more noise. Low-IF architecture [3] needs only low-Q IF channel selection filter. However, the disadvantage is that it can not achieve high image rejection. Zero-IF architecture [2] doesn’t have the problem of image signal, but it suffers problems from DC offset and flicker noise.

3.2.2 Transmitter Architecture

The transmitter architectures can be grouped into two basic types, transmitters with mixers and transmitters without mixers (also called direct-modulation transmitter). The former type includes direct-conversion transmitters and two-step transmitters. The later type uses a frequency synthesizer to directly modulate the base-band signal to the RF frequency.

In a direct-modulation transmitter [6], as shown in Fig. 3.7, the baseband digital signal is first filtered by a Gaussian filter to reduce the side-lobe of the output spectrum. The filtered signal is used to control a fractional-N synthesizer. The output of the synthesizer is a modulated signal and RF frequency. This signal is then used to drive a power amplifier. There is no mixer and filters used in the transmitter. Therefore, chip area and power consumption can be reduced. Gaussian filter is usually implemented with DSP circuits.

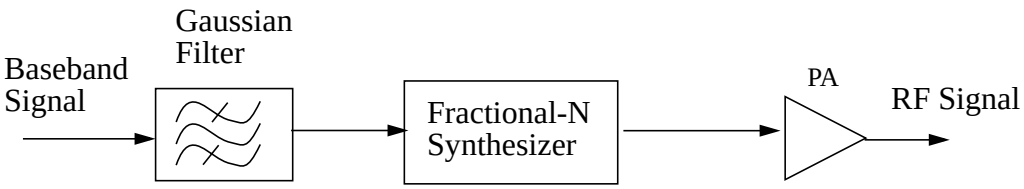


Fig. 3.7 Direct-Modulation Transmitter

3.2.3 Architecture of the Proposed Transceiver

The architecture of the whole proposed transceiver is shown in Fig. 3.8. The upper part is the receiver, which has a single high-IF architecture with I-Q mixers. An IF frequency of 70 MHz is used to enable the use of the image-rejection filter, which is a 4^{th} order IRF with a 3^{rd} order notch-filter. As such, a total image-rejection of 79 dB can be achieved. A frequency synthesizer with I and Q outputs is used to drive the I and Q mixers. A 6^{th} order channel-selection IF filter with a high Q of 350 is used to filter out interferences. A VGA with 78 dB gain control range is used to amplify the signal and reduce the signal dynamic range. A band-pass sigma-delta (BPSD) ADC with a sampling frequency of 280 MHz is used to

convert the 70 MHz signal to the digital domain. The details of each building block will be discussed in the following chapters

Single-IF architecture is chosen so that the signal is only downconverted once and only one IF filter is needed, which can save power, area and reduce the noise contribution. High-IF is chosen so that high image rejection can be achieved, which is required by the system specification. The capacitors' value can be reduced in IF circuits with high IF frequency. I-Q downconversion is chosen to improve the image rejection. The signals are added together before the IF filter so that only one IF chain, including IF filter, AGC and ADC, is needed to save power and chip area.

The proposed direct-modulation transmitter is realized with a fractional-N synthesizer with sigma-delta modulation to save power and chip area. The synthesizer is shared by both the receiver and transmitter. A Gaussian filter is used to filtered the digital signal to obtain GMSK modulation. Since it is usually implemented with DSP circuits, it is not included in this design.

The output of the Gaussian filter controls the sigma-delta modulator and further controls the division value of the divider. Therefore, the output of the VCO, which is proportional to division value, is controlled by the baseband signal. The function of the synthesizer on the controlling signal of the divider is a low-pass function with a bandwidth same as the loop bandwidth of the synthesizer. Therefore, the loop bandwidth should be large enough, 200kHz.

The advantage of the direct-modulation transmitter is that it can save power and reduce chip area because the upconversion mixers are removed and the fractional-N synthesizer can be shared with the receiver.

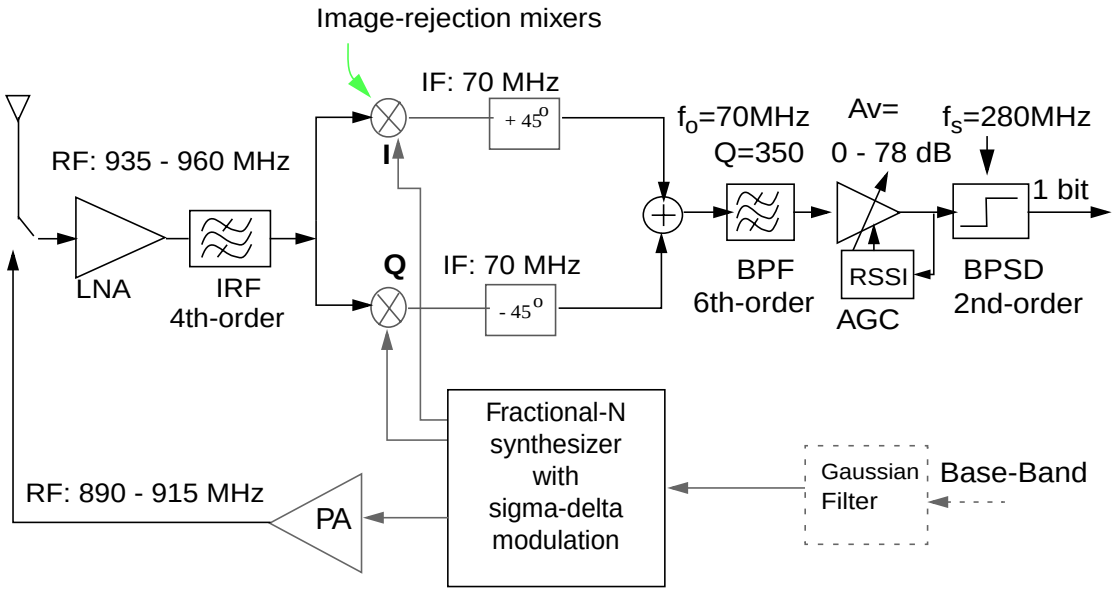


Fig. 3.8 Proposed Transceiver

3.3 Specification of the Transceiver

According to the system specifications described above, such as the sensitivity, the intermodulation signals and the blocking signals, the specification of the proposed receiver, including image rejection, noise figure and linearity, will be derived in the following paragraphs.

3.3.1 Image Rejection

Because the IF frequency of the proposed receiver is 70 MHz, and the lower-side-band downconversion is used, the image signal is located at 140 MHz lower than the receiving band. This frequency is between 795 ~ 820 MHz, as shown in Fig. 3.9. The image signal is actually a blocking signal with power of -23 dBm. According to the system specification, an SUSR of 9 dB must also be obtained after the downconversion. Therefore, the total input-referred unwanted signal level must be 9 dB lower than the minimum wanted signal, -90dBm. According to these requirements, the image signal rejection, IR, is derived as:

IR=

- 23 dBm [the largest possible image signal before mixing]

- (- 90 dBm -9) [the allowed largest possible image signal after rejection]

= 76 dB

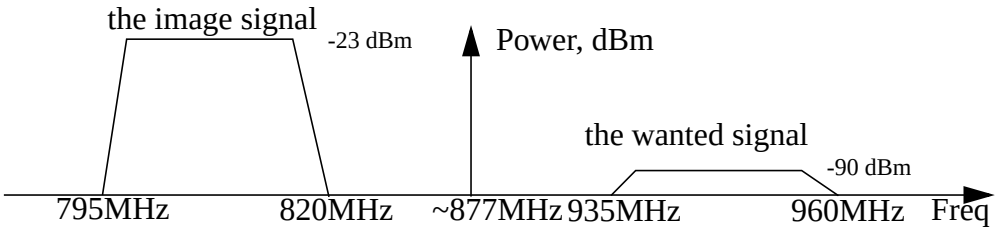


Fig. 3.9 The Image Signal and the Desired Signal

The image rejection is realized by two building blocks, the LNA with image rejection filter (IRF) and the I & Q down-conversion mixers.

3.3.2 Noise Figure

Because of the internal noise of the receiver, the SNR at the output is degraded. The noise figure (NF) is used to specify how much the SNR is degraded. It is defined as the ratio between the SNR at input, SNR_{in}, and the SNR at the output, SNR_{out}. In log-scale, NF equals SNR_{in}-SNR_{out} and SNR_{out}=9 dB is required to satisfy the requirement of BER. When the receiver is matched to a source resistor of 50 Ω, the source noise power is

$$N_s/\Delta f=V^2_{ns}/4R_s=4KTR_s/4R_s = KT = 1.38x10^{-23}x300=4.14x10^{-21}W/Hz=-174\ dBm/Hz,$$

and within the bandwidth of 200kHz,

$$N_s= - 174 + 10\log_{10}(200k) = -174 + 53 = -121\ dBm.$$

For a sensitivity requirement of P_s=- 90 dBm, the required NF is

$NF = SNR_{in} - SNR_{out} = P_s - N_s - SNR_{out} =$

- 90 dBm [the smallest possible wanted signal power]

- (-121) dBm [the input thermal noise power in 200 KHz]

- (9 dB) [the required SNR on the smallest possible wanted signal]

= 22 dB

The input-referred noise floor of the receiver is

$N_{in}=P_s-SNR_{out}= -90 - 9 =-99$ dBm.

3.3.3 Linearity

The required sensitivity should be achieved when the interference signals of -50 dBm are applied at 800 kHz and 1600 kHz away from the desired signal channel [8]. To achieve the required sensitivity, the input referred IM3 signal must be 9 dB lower than the smallest possible wanted signal, - 90 dBm, and the input intercept point (IIP3) is equal to [10]:

$$IIP_3= P_{in} + (P_{in}-IM3)/2$$

$$\text{or} \qquad IM3=3\times P_{in}-2\times IP3$$

where P_{in} is the input power of an interference to the receiver in dBm. The IM3 should be lower than the input-referred noise floor of the system, N_{in}=-99 dBm.

$$IM3 \leq N_{in}$$

$$3\times P_{in}-2\times IP3 \leq N_{in}$$

Therefore,

$$IP3 \geq (3\times P_{in}-N_{in})/2$$

$$=(-50\times 3+99)/2$$

$$=-25.5 \text{ dBm}$$

3.3.4 Direct Modulation in the Transmitter

A direct-modulation transmitter with GMSK (BT=0.3) modulation is implemented in the system. The transmitting band is 890 MHz to 915 MHz. It consists of 124 channels with a channel spacing of 200 kHz. Two guard bands of 100 kHz each are provided at the lower and upper end of the transmitting band. The data rate of the transmitter is 270 kbps, which corresponds a bandwidth of about 200 kHz after the Gaussian filter.

The modulation is realized by a fractional-N synthesizer with Sigma-Delta modulation. The baseband signal after the Gaussian filter is used to control the Sigma-Delta modulator and further control the output frequency of the synthesizer. Therefore, the loop bandwidth of the fractional-N synthesizer is required to be 200 kHz.

3.4 Specification of Each Building Block

The specification of each building block is derived based on the specifications of the receiver.

3.4.1 LNA and Image Rejection Filter

The LNA is used to amplify the received signal without degrading the linearity of the system. For noise consideration, the gain of the LNA should be as high as possible. However, for linearity consideration, the gain is limited by the worst linearity in the proceeding stages. After iterations, the linearity of the IF filter is found to be the limitation of the linearity of the system. To avoid the linearity degradation due to IF filter, the gain of the LNA is set to 23 dB.

The noise figure contribution of each stage is set at 3 dB lower than the NF requirement of the whole receiver to guarantee the receiver performance. As the noise of the LNA is directly added to the received signal without any reduction, the NF of the LNA must be as low as possible. For the sensitivity of -90 dBm, the required NF of the LNA is

$$NF_{lna}=NF_{sys} - 3 = 22 - 3 = 19 \text{ dB}.$$

Since the LNA is the first block in the receiver, the IIP3 of the LNA directly limits the IIP3 of the receiver. Leaving 3 dB to guarantee safety, the required IIP3 of the LNA should be $IIP3_{lna} = IIP3_{sys} + 3 = -25.5 + 3 = -22.5$ dBm for the sensitivity of -90 dBm, or $IIP3_{lna} = -19.5 + 3 = -16.5$ dBm for the sensitivity of -102 dBm.

The image-rejection filter is used to achieve high image rejection. Due to the amplitude and phase mismatch, the I-Q downconverters can only achieve an image rejection of about 30 dB. Therefore, an image-rejection filter is required to provide the other 46-dB rejection for the sensitivity of -90 dBm.

3.4.2 Mixer

Because the mixer is the second stage in the receiver after the LNA, the noise contribution from the mixer is directly scaled down by the gain of the LNA. Consequently, the NF requirement of the downconverter is relaxed to be approximately $F_{mix}=F_{sys}\times A^2_{lna}+1$. For $F>>1$, $F_{mix}\approx F_{sys}\times A^2_{lna}$, or $NF_{mix}\approx NF_{sys}+A^2_{lna\_dB}= 22dB + 23 dB = 45$ dB. Consider 3 dB margin, it is $NF_{mix}= 45 dB+3 dB = 42$ dB.

The noise figure of an I-Q mixers is 3 dB higher than the noise figure of its individual mixer [5]. Therefore, the required NF for each individual mixer is $NF_{mix}= 39$ dB. $NF_{mix}=30$ dB is finally used as the NF requirement of the mixers. The conversion gain of the mixers is set to be 0 dB.

According to Eq. (2.2) in Chapter 2, the IIP3 of the system due to that of the mixer is

$$\frac{1}{A^2_{IP3}} = \frac{A^2_{lna}}{A^2_{IP3,mix}}$$

In log-scale, $IIP3_{sys}=IIP3_{mix} - Gain_{lna}$, or $IIP3_{mix}=IIP3_{sys}+Gain_{lna}$, which is $-25.5 + 23 = -2.5$ dBm. If 3 dB is left to guarantee the safety, the IIP3 requirement of the mixer is 0.5 dBm.

3.4.3 Frequency Synthesizer

The key specification of the synthesizer is the phase noise requirement, which is specified as a spectral density in dBc/Hz at a certain frequency offset and can be determined by the unwanted downconversion of the adjacent channel interferences.

In the second adjacent channel (at 400 kHz offset), the power of interference signal is 41 dB larger than the wanted signal. According to Eq. (2.9) in Chapter 2, the required phase noise is

$PN = P_{s\_dB} - P_{i\_dB} - 10\log_{10}(BW) - SUSR =$

- 41 dB [the adjacent signal at 400 KHz to wanted signal ratio]

- 53.0 dB [200 KHz bandwidth]

- 9 dB [the required SNR on smallest possible wanted signal]

= -103 dBc/Hz @400 KHz

In the third adjacent channel (at 600 kHz offset), there is a blocking signal with power level of 43 dBm. Therefore, the required phase noise is $PN = P_{s\_dB} - P_{i\_dB} - 10\log_{10}(BW) - SUSR$. For sensitivity of P_s = -90 dBm, the required PN is

$PN = P_{s\_dB} - P_{i\_dB} - 10\log_{10}(BW) - SUSR =$

- 90 dBm [the smallest possible wanted signal]

- (- 43 dBm) [the blocking signal at 600 KHz]

- 53.0 dB [200 KHz bandwidth]

- 9 dB [the required SNR on smallest possible wanted signal]

= -109 dBc/Hz @600 KHz

Since only a 30-dB image rejection is required in the I-Q structure, the phase mismatch is required to be less than 1^o and the amplitude mismatch is required to be less than 0.1 dB.

3.4.4 IF Filter

After the amplifying by the LNA and downconverting by the mixer, the power of interferences at receiver input, -23 dBm (f = fo+3MHz), -33 dBm (f = fo+1.6 MHz), - 43 dBm (f = fo+0.8 MHz) and -90 dBm ($f=f_o$), are amplified to 0 dBm (f = fo+3MHz), -10 dBm (f = fo+1.6 MHz), -20 dBm (f = fo+0.8 MHz) and -67 dBm (f=fo), respectively. The wanted signal can now be selected by the IF channel selection filter and the interference signals can be suppressed.

To achieve sufficient suppression, a 6^{th} order bandpass filter is required. Since the center frequency is 70 MHz and the signal bandwidth is about 200 kHz, the Q of the filter is required to be 70MHz / 200 kHz = 350.

To achieve the NF requirement of the whole receiver, the NF of the IF filter is required to be: $F_{filter}=F_{sys} \times Gain_{lna} \times Gain_{mix} + 1$. For F>>1, it is approximately $F_{filter} \approx F_{sys} \times Gain_{lna} \times Gain_{mix}$. In log-scale, $NF_{filter} \approx NF_{sys} + Gain_{lna} + Gain_{mix} = 45$ dB. Consider 3 dB margin, the NF of the filter is required to be 42 dB.

Since the IF filter is implemented with a three-stage Gm-C filter, each stage contributes some noise to the system. To reduce the noise contribution from the second and third stage, the first stage is designed to have a gain higher than that of second and third stage, i.e. 14 dB in the first stage, 3 dB in the second stage, 3 dB in the third stage and 20 dB total.

The IIP3 requirement of the IF filter is more restricted because of the gain in the previous stages. According to Eq. (2.2) in Chapter 2, the IIP3 of the system due the IF filter is:

$$\frac{1}{A^2_{IP3}} = \frac{A^2_{lna}A^2_{mix}}{A^2_{IP3,filter}} \tag{3.2}$$

In log-scale, $IIP3_{sys}=IIP3_{filter} - Gain_{lna} - Gain_{mix}$, and $IIP3_{filter}=IIP3_{sys} + Gain_{lna} + Gain_{mix}$. For the sensitivity of -90 dBm, the IIP3 requirement of the filter is $IIP3_{filter}=-25.5 + 23 = -2.5$ dBm. For the sensitivity of - 102 dBm, $IIP3_{filter}=-19.5 + 23 = 3.5$ dBm

3.4.5 Variable Gain Amplifier

The variable gain amplifier (VGA) is used to amplify the signal further and reduce the signal dynamic range. For the sensitivity of -90 dBm, the dynamic range of the wanted signal is -12 dBm - (-90 dBm) = 78 dB.

Because of gain in previous stages, the NF requirement of the VGA is relaxed. Assume F>>1,

$$NF_{vga} \approx NF_{sys} + Gain_{lna} + Gain_{mix} + Gain_{filter} - 3$$

$$= 22 + 23 + 0 + 20 - 3 = 62 \text{ dB}.$$

The IIP3 requirement of the VGA is also more relaxed because the interference signals are suppressed by the IF filter. Because the gain of the VGA is varying, the IIP3 of the VGA is varying too. Therefore, the linearity of the VGA is defined in output-referred IP3 (OIP3), which is 5 dBm in this design.

3.4.6 A/D Converter

Sigma-delta A/D conversion is a popular technique for high-resolution A/D converters. Although, there are several types of Sigma-Delta modulators used in A/D converters, the bandpass Sigma-Delta modulator can utilize the major advantages of conventional Sigma-Delta converters at higher frequencies [11]. Because the IF signal is typically a small fraction of the carrier frequency, the use of a wide-band Nyquist-rate converter does not result in an optimum solution for converting the IF signal. An optimum

solution for converting the IF signal is a converter that provides high resolution in a narrow bandwidth and is capable of handling large out-of-band signals. Because of their oversampling and noise shaping nature, bandpass Sigma-Delta converters provide the most optimum solution. In the proposed system, an A/D converter with 6 bit resolution is enough to maintain the required SNR at output.

3.4.7 Power Amplifier

A class-E power amplifier with an output power of 100 mW and a power added efficiency (PAE) of 20% is required to amplify the output RF signal and drive the antenna.

3.5 Summary of Specifications

Table 3.2 summarizes the specifications of the receiver system and each building block, which will be used as a target in the design of each building block.

Table 3.2 Specifications of Receiver and Building Blocks

Building block	**Specification**	**Derived Value for the proposed system**	**Derived value for the GSM system**
Receiver Front-end	Sensitivity	- 90 dBm	-102 dBm
	SNR	9 dB	
	NF	22 dB	10 dB
	Input IP3	- 25.5 dBm	- 19.5 dBm
	Image rejection	76 dB	85 dB
LNA	Noise Figure	19 dB	7 dB
and IRF	Gain	0 dB or 23 dB, switchable	
	Input IP3	-22.5 dBm	- 16.5 dBm
	Passband	935 - 960 MHz	
	Image Rejection	46 dB	55 dB
Downconversion mixers	IF frequency	70 MHz	
	Input bandwidth	1 GHz	
	Noise Figure	39 dB	27 dB
	Conversion gain	0 dB	

Table 3.2 Specifications of Receiver and Building Blocks

Building block	**Specification**	**Derived Value for the proposed system**	**Derived value for the GSM system**
	Input IP3	0.5 dBm	6.5 dBm
Synthesizer	Frequency tuning range	935 MHz ~ 960 MHz for RX 890 MHz ~ 915 MHz for TX	
	Phase noise	-109 dBc/Hz @ 600 kHz	-121 dBc/Hz@600kHz
	Loop Bandwidth	200 kHz	
	Phase mismatch	$< 1^{o}$	
	Amplitude mismatch	< 0.1 dB	
IF bandpass filter	Centre frequency	70 MHz	
	Bandwidth	200 KHz	
	NF	42 dB	30 dB
	IIP3	- 2.5 dBm	3.5 dBm
VGA	Gain Control Range	78 dB	90 dB
A/D converters	Centre frequency	70 MHz	
	Input bandwidth	200 KHz	
	Dynamic range	6 bit	

Chapter 4

PASSIVE COMPONENTS

Passive components used in the proposed transceiver, including on-chip inductors, switched-capacitor arrays and varactors, will be discussed in this chapter. Design considerations and simulated performance of those components will be presented.

4.1 On-Chip Inductor [12][13]

One of the critical limitations when integrating RF circuits on-chip is a lack of high-Q on-chip inductors. Unlike resistors and capacitors, whose values are well estimated except for the process variations (around 10%), on-chip inductors are still not well optimized in terms of shape, metal width, metal spacing, quality factor and inductance value. Modern CMOS processes usually consists of a heavily doped epi layer which is highly conductive. The eddy current induced by the magnetic field of the inductor onto the substrate directly decreases the quality factor (Q) of the inductor.

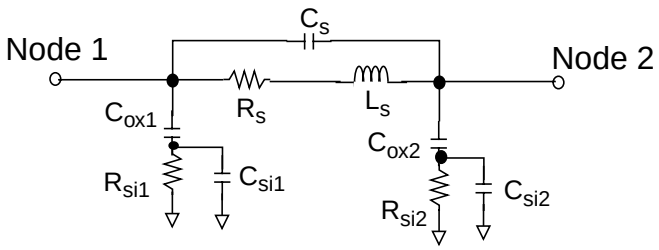


Fig. 4.1 A complete inductor model

A widely used inductor model [14] is depicted in Fig. 4.1, where R_s is the series resistance of the inductor L_s, C_s represents the capacitance between each turn of the inductor, C_{ox} is the capacitance between the inductor and the substrate, R_{si} and C_{si} model the lossy silicon substrate.

The loss of the on-chip inductors is usually caused not only by the resistance loss of the metal layer but also by the loss in the silicon substrate. At low frequencies, the impedance of C_{ox} is very high, and the inductor is isolated from the lossy substrate. Thus, the loss is mainly introduced by the metal layer. As the frequency of interests increases, the impedance of C_{ox} decreases, and the resistive loss due to the lossy substrate becomes important. At a high frequency, C_{ox} is virtually shorted and the substrate loss dominates. As a result, the loss of the on-chip inductor increases with the frequency, instead of remaining constant.

The inductance value of a single metal layer is well estimated by the Greenhouse's formula [15]. A simple estimate of the inductance can also be found to be [16],

$$L = \mu_0 n^2 r, \tag{4.1}$$

where μ_0 is the permeability of the free space, n is the number of turns, and r is the radius of the inductor. To have a more accurate estimation of the inductance value, the inductor structure can be analyzed with a 3-D electromagnetic simulator like SONNET EM [17]. However, it is usually time-consuming especially when the structure needs to be optimized in terms of metal spacing, metal width and total area.

As a compromise, another program, ASITIC [18], which runs much faster, is employed in this design to optimize the inductor quality factor. An attractive advantage of using this program is that it runs much faster than E-M SONNET, and circular inductors can also be analyzed. However, one of the drawbacks of this program is that it does not include the effect of eddy current in the substrate for circular inductors, which is not serious in a

less-conductive BiCMOS substrate but quite important in lossy CMOS substrate. This accounts for the fact that the simulated Q's of inductor at high-frequency are much better than the measured one.

Some process information for the 0.5 μm single-poly, triple metal CMOS is illustrated in Fig. 4.2.

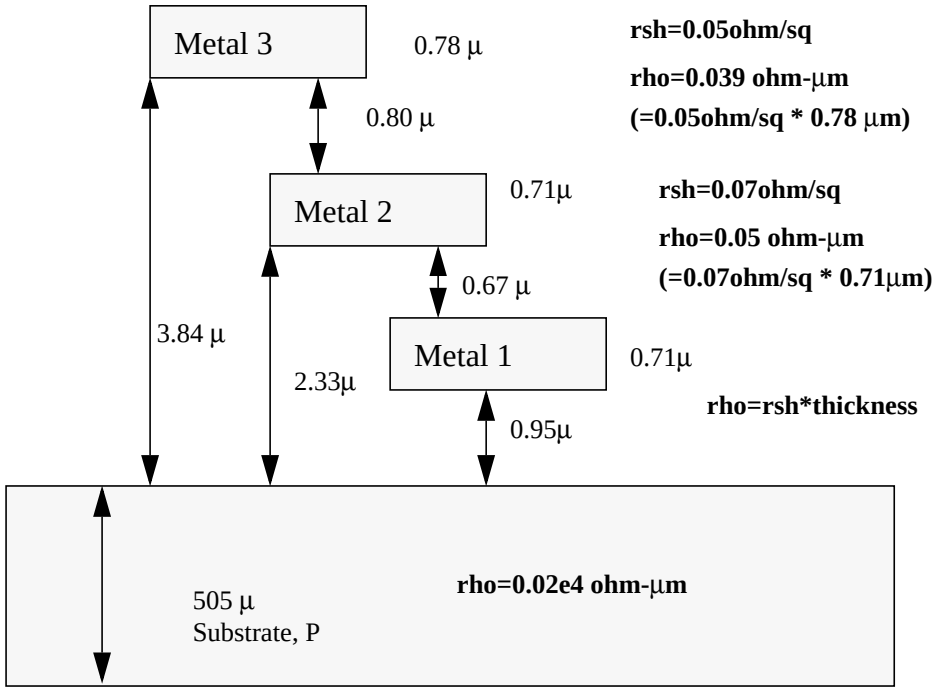


Fig. 4.2 Process information of a Typical 0.5μm CMOS

On-chip inductors are usually implemented using the topmost metal layer(s) (M3, in this case) as the sheet resistance is the smallest (50 mΩ/sq) and the separation between the topmost layer and the lossy substrate is the largest (3.84 μm), which results in the best Q of the inductor. In addition, circular inductors are known to have higher Q than the square inductors with the same metal width and spacing.

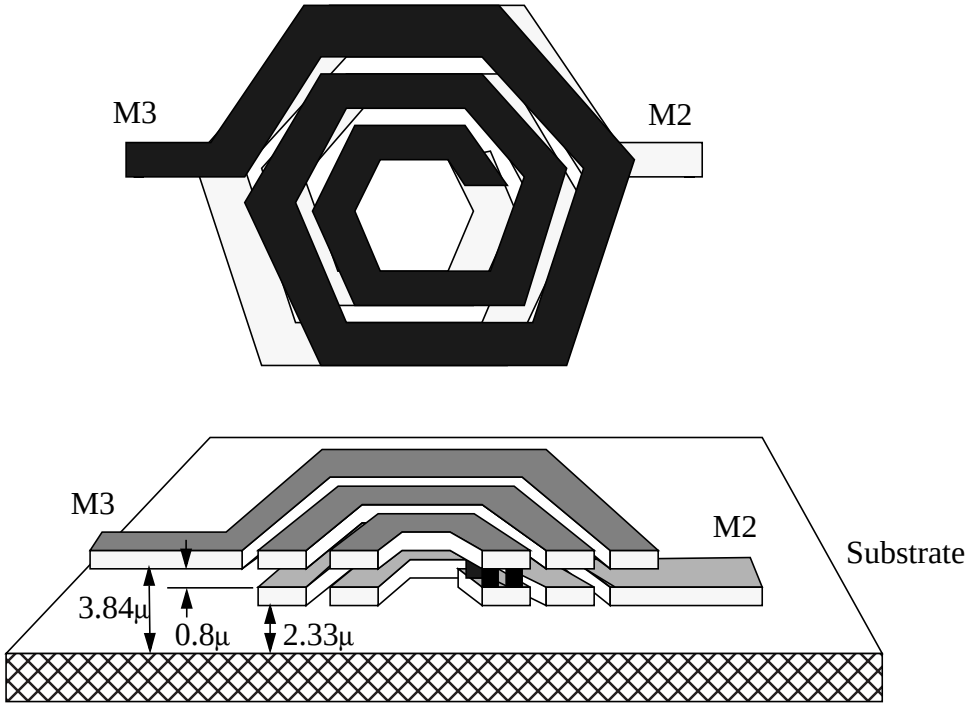


Fig. 4.3 Double-layer On-Chip Inductor

When the desired inductance is large, double layer (M2, M3) inductors, which are formed by a series connection of two single layer inductors, are used to improve the Q of the overall inductors, as shown in Fig. 4.3. With two layers used in the inductor design, the total area can be reduced by more than half because the mutual inductance between M2 and M3 also contributes to the total inductance. Although the parasitic capacitance per unit area from M2 to the substrate is a little bit larger than that from M3 to the substrate, the overall signal coupled to the substrate is still smaller.

However, the parasitic capacitance between the two metal layers reduces the self-resonant frequency of the inductor. For example, a double-layer spiral inductor with 4.3 nH in this process has a self-resonant frequency of 4.9 GHz, while each layer is simulated to have a self-resonant frequency of about 10 GHz. Fortunately, the self-resonant frequency is still much larger than the frequency of interest, which is 950-MHz in this design.

In the case where the inductor is used as a single-ended form, M3 should be connected to the signal node and M2 should be connected to the ground or Vdd so that a smaller parasitic capacitor is connected to the signal node.

With the double layer design, the inductor achieves a simulated Q of 3.6 with the inductance value of 4.3 nH. The geometry parameters and simulated performance of the inductors used in the LNA is summarized in Table 4.1.

Table 4.1 Simulation Results of On-Chip Inductors in LNA

	Gate Inductor	**Source Inductor**	**Output Inductor**
Metal Layers	M2/M3	M3	M2/M3
Sides of Each Turn	32	64	16
Metal Width, μm	14.25	14.25	18
Metal Spacing, μm	1.2	1.2	1.2
No. of Turns	4.75	2.25	2.25
Center-to-Edge Radius	135	80	100
Inductance (nH)	21.3	0.9	4.3
Q at 950 MHz	3.3	2	3.6
Self-Resonant Frequency GHz	1.5	21.7	4.9

4.2 Switched-Capacitor Array

Frequency tuning is traditionally realized with Miller capacitors [35]. However, extra noise is introduced by the Miller amplifier. In addition, the transistor in the amplifier degrades the overall linearity and consumes extra power. To avoid these problems, switched-capacitor arrays are used in LNA, Notch filter and VCO to tune the center frequencies of those building blocks.

The structure of switched-capacitor arrays (SCA) used in the LNA, the Notch filter and the VCO is shown in Fig. 4.4.

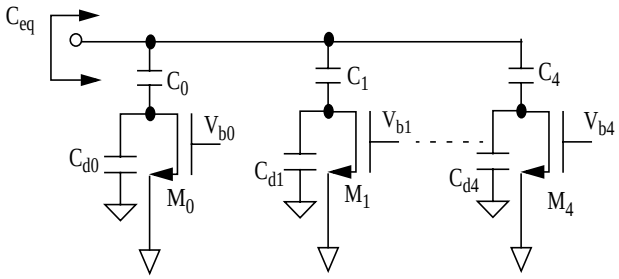


Fig. 4.4 Switched-Capacitor Array

To maximize the tuning range of the switched-capacitor arrays, donut transistors [37] are used in realizing the switches. Each switch is realized with a donut transistor, as shown in Fig. 4.5 (a). The equivalent channel width of the donut transistor is 11.6 μm, the channel length is 0.6 μm and the drain area is 5.76 μm^2. If a traditional transistor with two fingers is used as shown in Fig. 4.5 (b), the drain area would be 9.9 μm^2. Because the drain area of the donut transistor is shared by the gates in all four sides, the parasitic drain capacitance is reduced to minimum, and the capacitance tuning range is maximized.

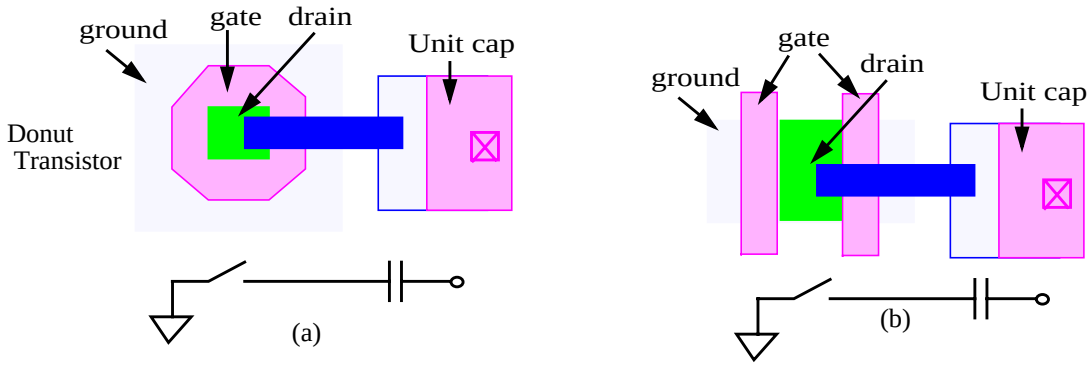


Fig. 4.5 (a) Donut Transistor and Unit-Cap, (b) Traditional Transistor and Unit-Cap

Assume the turn-on resistance of the switches is negligible, when some switches (M_i) are on and other switches (M_j) are off, the equivalent capacitance C_{eq} is:

$$C_{eq} = \sum_i C_i + \sum_j \frac{C_j \times C_{dj}}{C_j + C_{dj}} \tag{4.2}$$

where C_i are capacitors with the switches (M_i) on, C_j and C_{dj} are capacitors and parasitic capacitors with the switches (M_j) off. When switches are all turned on, the maximum equivalent capacitance is a sum of C_0 to C_4. When switches are all turned off, the minimum equivalent capacitance is a sum of C_0 in series with C_{d0} to C_n in series with C_{dn}. The value of C_{max}/C_{min} is a measure of the capacitance tuning ability.

The turn-on resistance of M_0 - M_4 limits the overall Q of the switched-capacitor arrays. A larger size for M_0 - M_4 is more desirable to reduce the turn-on resistance and maximize the Q. However, the capacitance tuning range will be reduced due to the larger parasitic drain capacitance. To balance between the Q and the capacitance tuning range, the size of transistors are properly set so that the overall capacitor can maintain a Q of 10, which is high enough to reduce the noise contribution of the switched-capacitor array to a negligible level.

The switched-capacitor array has a high linearity. When a switch is turned on, the signal that appears at the drain of the switch, $V_{d,}$ is:

$$|V_d| \approx \left| V_o \times \frac{R_{on}}{R_{on} + \frac{1}{j\omega C}} \right| < V_o \times \frac{R_{on}}{\frac{1}{\omega C}} = \frac{V_o}{Q} \tag{4.3}$$

where V_o is the signal appears at the capacitor output node, and R_{on} is the turn-on resistance of the switch. Therefore, V_d is at least Q times smaller than V_o. Because the signal at the drain of the switches is small, it doesn't affect the linearity of the amplifier. When a switch is turned off, it has no effect on the linearity.

Because the switches are connected in series with the capacitors, there is no DC current

passing through. Therefore, the switched-capacitor arrays consume no DC power.

4.3 Varactor

To achieve fine frequency tuning, two varactors based on parasitic PN junction diode of P+ active and N-well are used in the VCO, as well as the switched-capacitor arrays. They are divided into 18 and 186 unit PN junction diodes. As shown in Fig. 4.6, each unit diode has a capacitance of about 2.1fF at 1V reverse bias and the gain of capacitance varying is around 15% per volt. Each diode also has an Nwell-to-substrate parasitic capacitance of 1.5fF to ground, which reduces the tuning range of the varactor. The overall gain of the capacitance tuning is about 9% per volt, from 0.74pF to 0.8pF.

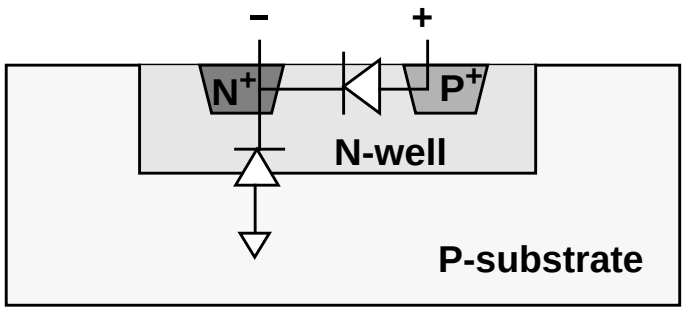


Fig. 4.6 Parasitic PN Junction Varactor

The parasitic PN junction varactors have a quality factor of around 30 by minimizing the size of unit diode in the array. Because the quality factor of the diode degrades greatly when the diode is forward-biased, the available biasing range of the diode is very limited. However, it is not a problem in this design because the diode is always 1V reverse-biased with a small variation of 0.1V.

4.4 Summary

Some passive components, the on-chip inductors used, the switched-capacitor arrays, the varactors, are discussed in this chapter. The physical structures and the performances of those components are described. These components will be used in some building blocks, such as LNA, VCO and IF filter.

Chapter 5

LOW NOISE AMPLIFIER

The design of the low noise amplifier (LNA) is discussed in this chapter. An on-chip input matching network is used in the LNA to achieve a 50-Ω input matching. Unbalanced negative Gm-cells are used to compensate the loss due to low-Q on-chip inductors. Switched-capacitor arrays are used to tune the center frequency of the LNA. A notch filter is used to improve the image rejection of the LNA. The noise analysis of the LNA core circuit is discussed at last.

5.1 General Considerations

Because the LNA is the first block in the receiver, the weak signal from the antenna is applied to the LNA directly. Therefore, the LNA is required to provide a high gain, otherwise the noise of subsequent stages, such as the mixer and the IF filter, will decrease the SNR at the receiver output. However, if the gain of the LNA is too high, the linearity requirement of the following stages will be too high. Because the noise from LNA is added to the weak signal directly without any reduction of previous gain stage, the noise figure of the LNA itself must be minimized.

The input impedance of the LNA must be matched to 50 Ω, so that the signal from the antenna won't be reflected and a maximum power transfer from antenna to LNA can be obtained. The image rejection is also a big issue. Since the image-rejection mixers can achieve an image rejection of 30 dB due to the amplitude and phase mismatch in I and Q channels, the LNA is required to provide a high image rejection of 46 dB. Otherwise an external

image-rejection filter must be adopted to satisfy the total image rejection of 76 dB. The specification of the LNA is summarized in Table 5.1.

Table 5.1 Specifications of LNA

Parameters	**Specifications**
Passband	935 - 960 MHz
Gain	23 dB
Noise Figure	7 dB
IIP3	- 16.5 dBm
Input Impedance	50 Ω

In conventional LNA design, the inductors are either off-chip or realized with bond-wires. However, the external inductors are bulky and prevent the LNA from being fully integrated. The bond-wire inductors are not well controlled. Therefore, the best choice is to build the inductors on-chip. However, the on-chip inductors usually have a low Q of around 2.5. Q compensation is then necessary to compensate the loss in on-chip inductors. Although the loss can be compensated, the noise from low-Q inductors inevitably degrades the noise performance of the LNA.

Due to the process variation, the parasitic capacitance of on-chip inductors and transistors can vary as much as 20%. Even the capacitance of linear capacitors varies as well. Besides variation in capacitance value, the inductance value of on-chip inductors are also not well modeled. As a result, the resonant frequency of LC tanks changes. Therefore a frequency tuning circuit must be adopted to compensate the process variation and tune the center frequency of the LNA to 947-MHz.

5.2 LNA Topology

The topology of the proposed LNA, which consists of two stages, is shown in Fig. 5.1. The first stage is a cascode differential pair with inductive input matching [26] and an LC

resonant tank as the output loading. Inductor degeneration is used to obtain the input matching because it can achieve better noise performance than $1/g_m$ or resistive termination. The C_{gs} of the input devices are made as small as possible to minimize the noise figure [32].

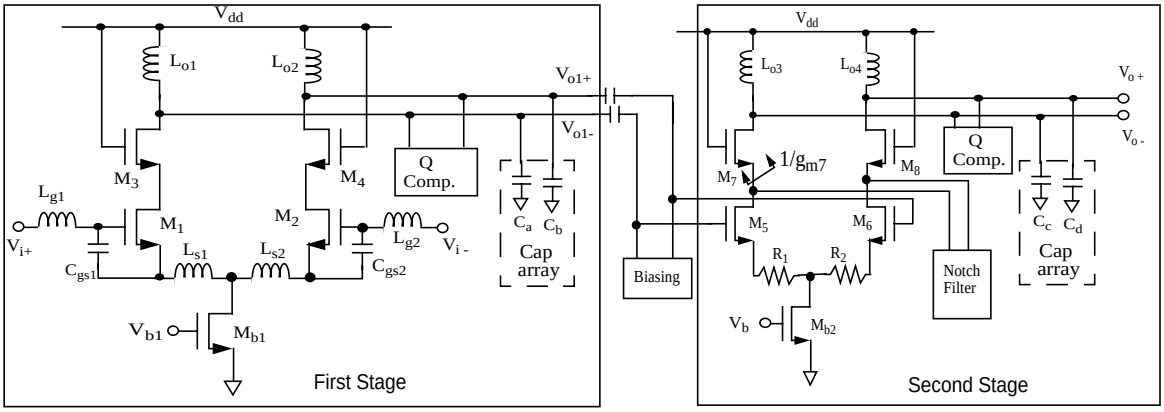


Fig. 5.1 Schematic of the Proposed LNA

To compensate for the low Q of the output spiral inductor, which is as low as 2.5, and to achieve the desired bandwidth of 25 MHz, a Q-compensation circuit with negative G_m is introduced.

The second stage of the LNA has basically the same architecture as that of the first stage but with resistive source degeneration to minimize the chip area. The noise from the resistors, R_1 and R_2, is negligible when referred to the input of the whole amplifier due to the high gain of the first stage. Capacitor coupling is used between the two stages to enable operation at a 2-V supply.

The two-stage combination yields a fourth-order bandpass function with a bandwidth of 25 MHz but can provide only 27-dB image rejection at 140 MHz offset. A notch filter is adopted in the second stage to achieve an overall image rejection of 50 dB. To minimize the overall noise figure, the gain of first stage is set to a high value of 22 dB, and that of second

stage is 0 dB. The center frequencies of the two stages are slightly deviated from each other to obtain maximum image rejection.

5.3 Input Matching

There are several topologies which could be used in the input matching of an LNA [69], 50-Ω resistor matching, $1/g_m$ matching, and inductive degeneration matching. Inductive source degeneration, as shown in Fig. 5.2, can achieve a better noise figure.

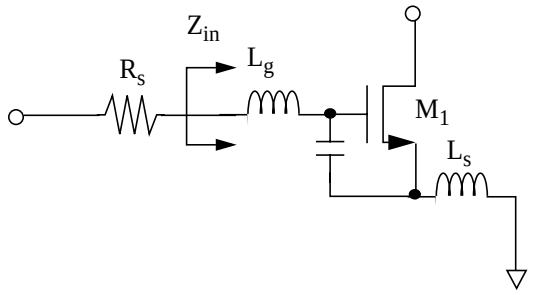


Fig. 5.2 Inductive Degeneration Used as Input Matching

The input impedance looking into the matching network, Z_{in} is

$$\begin{aligned} Z_{in}(j\omega) &= j\omega L_g + R_g + \frac{1}{j\omega C_{gs}} + \left(1 + \frac{g_m}{j\omega C_{gs}}\right)(j\omega L_s + R_l) \\ &= j\omega L_g + j\omega L_s + \frac{1}{j\omega C_{gs}} + \frac{\omega_T}{j\omega} R_l + \omega_T L_s + R_g + R_l \end{aligned} \tag{5.1}$$

where R_g and R_l represents the series resistance of the on-chip inductor L_g and L_s. The resonant frequency is

$$\begin{aligned} \omega_o &= \frac{1}{\sqrt{(L_g + L_s)\dfrac{C_{gs}\omega_T R_l}{C_{gs} + \omega_T R_l}}} \\ &\approx \frac{1}{\sqrt{(L_g + L_s)C_{gs}}} \quad . \end{aligned} \tag{5.2}$$

At resonant frequency, the impedance becomes a pure resistor,

$$Z_{in}(\omega_o) = \omega_T L_s + R_g + R_l \tag{5.3}$$

The input matching network works like a gain stage with the gain depending on the value of the capacitor C_{gs}. The smaller the capacitor gets, the larger the voltage V_{gs} is, and therefore, the larger the gain becomes. To reduce the noise contribution from the following stages including the input devices of the LNA, C_{gs} is to be minimized. However, to reduce the C_{gs}, the input transistors have to be small in size which results in small g_m and in turn degradation in the gain and noise performance of the whole LNA. In addition, to keep the same resonant frequency, larger inductors, (L_g + L_s), have to be used for the small C_{gs}, which have larger resistive loss, lower Q and larger noise contribution. Consequently, careful tradeoffs have to be made between the transistor size and the inductors to optimize the overall noise performance. In this design, the gate inductor L_g is set to 21.3 nH, and source inductor is set to 0.9 nH, and the Q of inductors is around 2.5. The size of input devices are W/L=21.3μ/0.9μ x 24.

The simulation results are shown in Fig. 5.3. S_{11} of -30 dB is achieved at 950 MHz.

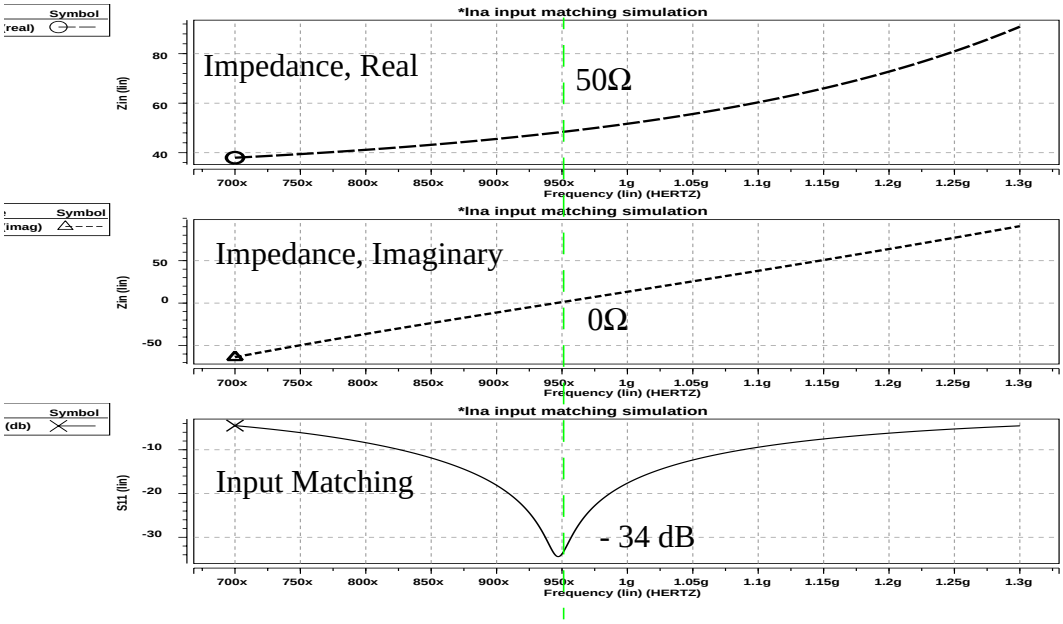


Fig. 5.3 Simulation Result of Input Matching, Single-Ended

5.4 Q-Compensation Circuit

Q-compensation circuits are usually to compensate the loss due the low-Q on-chip inductors in RF circuits [69]. A resonant tank formed by the output inductor and capacitor, as shown in Fig. 5.4 (a), is used as the output loading in the LNA. The low-Q inductor here is modeled by an ideal inductor with a series resistor.

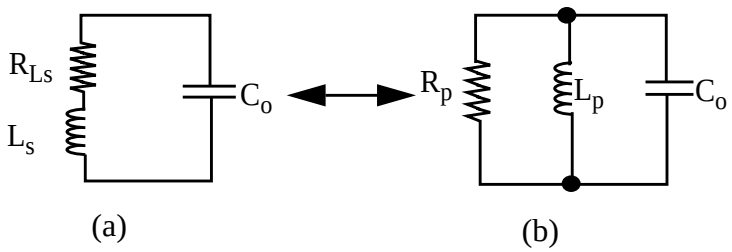


Fig. 5.4 Equivalent Parallel Resonant Circuit for the Output

(a) Inductor is Simplified to Be an Ideal Inductor in Series with a Resistor
(b) Equivalent Parallel Model

Low-Q on-chip inductors have small parallel resistors, which results in low gain and low image rejection achieved from the LNA. To increase the gain and image rejection, negative Gm cells are usually used to compensate the loss due to the on-chip inductors.

However, simple -Gm cells have poor linearity [69]. Unbalanced -Gm cells are used in this design to improve the linearity of the Q-compensation circuits. As shown in Fig. 5.5, the unbalanced -G_m-cell is similar with the simple -G_m-cell but the two transistors have different aspect ratios, W/L. Relatively constant -g_m is achieved within a large signal range in this Q-compensation circuit. The transistor size is summarized in Table 5.4.

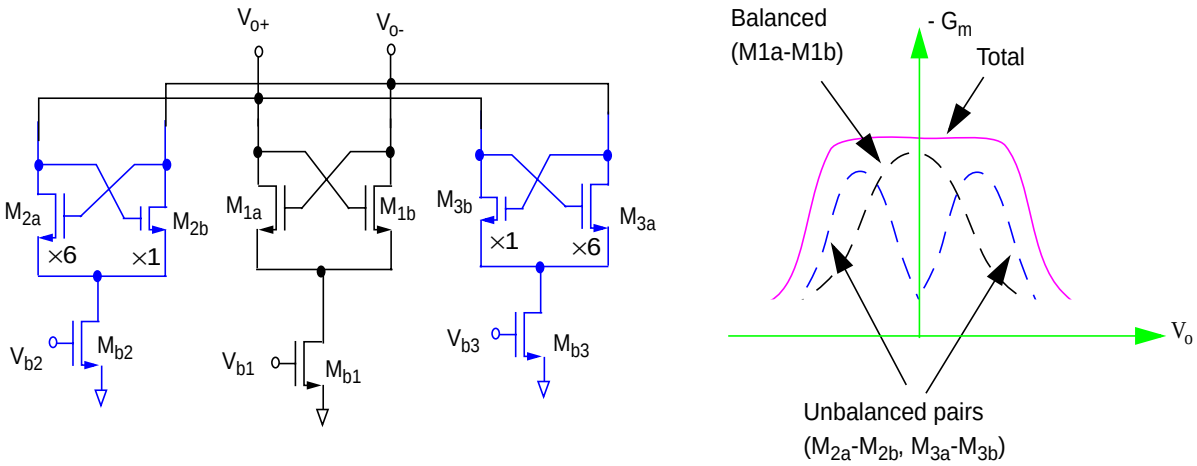


Fig. 5.5 Unbalanced -G_m of the Proposed Q-Compensation Circuit

The simulation result of -G_m provided by the proposed Q-compensation circuit is shown in Fig. 5.6. The resultant g_m remains constant within an input range of ±140 mV, which is much larger than that of the original simple balanced g_m-cells (±40 mV).

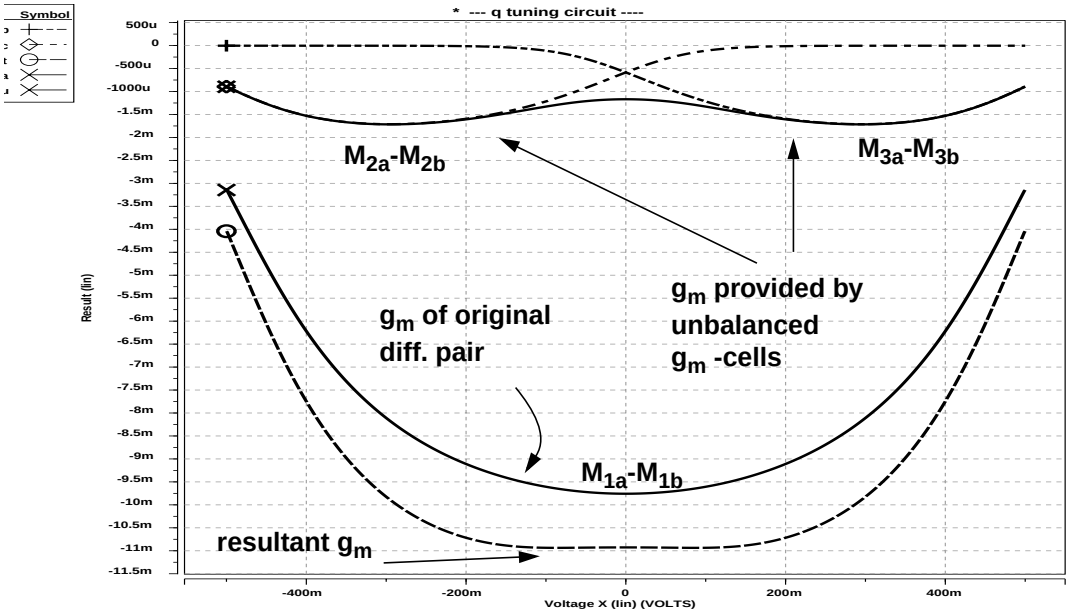


Fig. 5.6 -G_m Curves With and Without Unbalanced g_m-cells

5.5 Center-Frequency Tuning Circuit

In previous work [35], a Miller capacitor is used to tune the center frequency. However, extra noise is introduced from the Miller amplifier. In addition, the transistor in the amplifier degrades the overall linearity and consumes extra power.

To avoid these problems, a 5-bit binary-weighted switchable-capacitor array [37] is used in this design. The LSB, C_0 with switch M_0, is implemented with 3 unit-capacitors with 3 switches in parallel. The MSB, C_4 with switch M_4, is implemented with 48 ($=3*2^4$) unit-capacitors with 48 switches in parallel. C_{d0} - C_{d4} are parasitic capacitors which limit the capacitance tuning range. It can achieve a capacitance tuning range of 1.32pF to 3.46pF, C_{max}/C_{min}=2.6. The achieved capacitance tuning range is 62% which corresponds to a frequency tuning range of 160 MHz.

The simulation results of LNA frequency response with frequency tuning capability is shown in Fig. 5.7. The frequency tuning range is 160 MHz (870 MHz to 1030 MHz). As more capacitors are turned on, the center frequency is tuned to lower frequency. Although the Q of capacitors, ~10, is much higher than that of on-chip inductors, ~3, it is still lower than the required Q of the LNA response, 38. Therefore, when more capacitors are turned on, the overall Q of the LNA is lower and more $-G_m$ is needed to maintain the same Q. The frequency response with different capacitance and $-G_m$ is shown in Fig. 5.8.

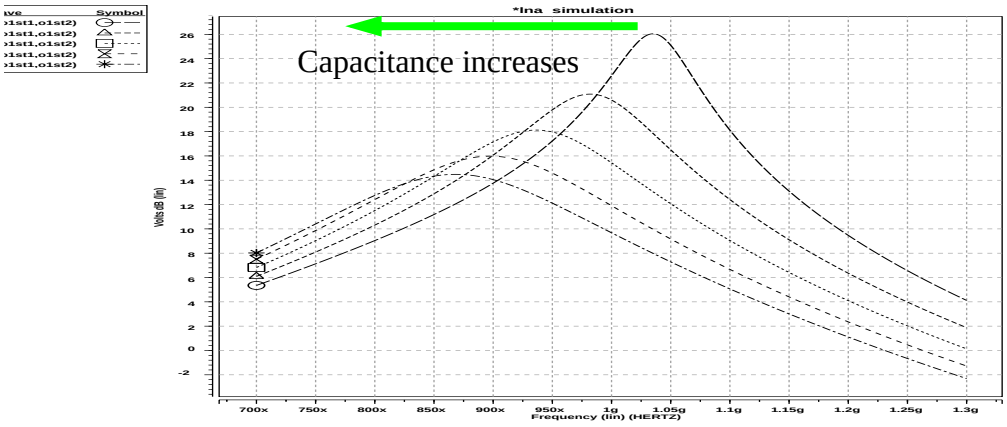


Fig. 5.7 Frequency Tuning Capability of LNA 1st Stage

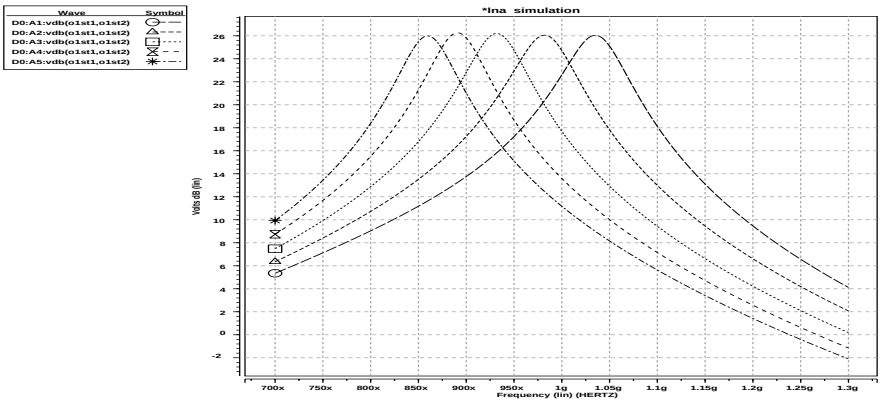


Fig. 5.8 Frequency Tuning Capability with Re-tuned Q

Each stage of the LNA has the same switchable-capacitor array to tune the frequency independently. To obtain the overall center frequency of 950-MHz, both stages can simply tune to the same center frequency, 950-MHz. However, if both of them have a bandwidth of 25-MHz, each of them would have 3 dB attenuation and the whole LNA including two stages would have 6 dB attenuation at 12.5-MHz offset. Therefore, the overall 3-dB bandwidth must be smaller than 25 MHz. To maintain a 3-dB bandwidth of 25 MHz for the whole LNA, each stage must have a bandwidth larger than 25 MHz. In this case, the Q of each stage would need to be smaller which would in turn result in lower image-rejection.

To avoid the degradation in the image rejection, the center frequencies of the two stages are slightly separated within the 25-MHz range. The bandwidth of the whole LNA is determined by both the Q of each stage and the difference in the center frequencies of the two stages. Because the center frequencies are slightly offset, the gain of the whole LNA is inevitably reduced. To maintain the same gain, the Q of each stage has to be increased. The larger Q helps to improve the image-rejection again but will not degrade the linearity because the gain remains the same. The overall image-rejection of the whole LNA is around 27 dB. A

3-dB improvement in image-rejection is achieved compared to the case where the center frequencies of both stages are the same.

5.6 NOTCH FILTER

A notch filter connected at the sources of the cascode devices in the second stage of the LNA is used to improve the image rejection of the whole LNA, as shown in Fig. 5.1.

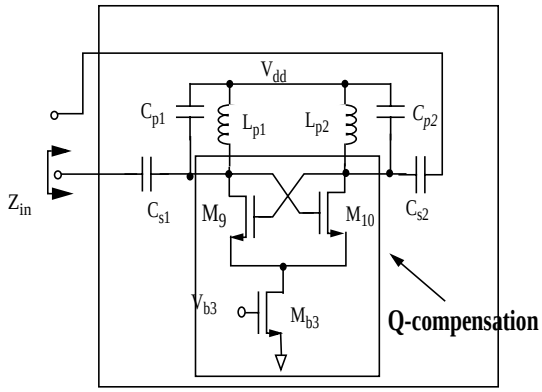


Fig. 5.9 Schematic of the Proposed Notch Filter

An image-rejection notch filter was first introduced in [39], in which a second-order notch filter is inserted between the input device and the cascode device. At the image frequency, image signals see a low impedance path to ground through the notch filter, and hence, are effectively attenuated. However, part of wanted signal may leak through the notch filter at the same time. This can be improved by using a high IF. Another modified version using a third-order notch filter [40] is adopted as shown in Fig. 5.9. The idea is the same as in [39] except a blocking capacitor is added to form a third-order notch filter. It also offers a control of the desired signal according to the following equation:

$$Z_{in}(s) = \frac{L_p(C_s + C_p) \cdot s^2 + 1}{C_s C_p L_p \cdot s^3 + C_s \cdot s} \tag{5.4}$$

By proper design of the values, the impedance, looking into the source of the cascode device ($1/g_{m7}$), is much higher than the impedance looking into the notch filter at image frequency.

Nevertheless, there are some limitations described in [40]. First, the noise contributed by the notch filter can be large as it is inserted in the LNA. Second, the transconductance g_m is typically high in LNA. Since the strength of the image rejection depends on the difference between ($1/g_m$) and the impedance looking into the notch filter at the image frequency, a large g_m limits the image rejection. The reported image rejection by the notch filter in [40] is only around 11 dB.

To further improve the image rejection, the adopted notch filter is moved to the second-stage bandpass amplifier as shown in Fig. 5.1. With the high-gain first-stage amplifier, the noise contribution due to the second-stage bandpass amplifier and the notch filter is negligible. A unity gain provided by the second-stage bandpass amplifier leads to a low transconductance g_{m7}. Given the same impedance looking into the notch filter, image rejection can be increased.

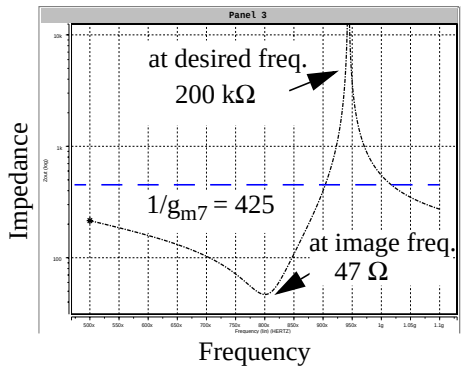


Fig. 5.10 Input Impedance of the Notch Filter

Fig. 5.10 shows the simulated impedance looking into the notch filter and the source of the cascode device for comparison. As shown, the impedance at the image frequency is

only 47 ohm, which is about ten times smaller than $1/g_{m7}$. On the other hand, the impedance at desired frequency is about 4000 times larger than the $1/g_{m7}$, which is high enough not to affect the wanted signal. Fig. 5.11 shows the frequency responses of the whole LNA with and without image-rejection notch filter for comparison.

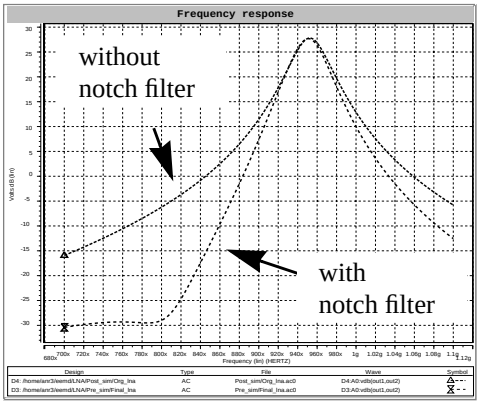


Fig. 5.11 Frequency Response of the LNA With and Without Notch Filter

5.7 Noise Analysis

The equivalent circuit of the LNA for noise analysis is shown in Fig. 5.12. R_s and $\overline{v}_s^2$ are the source resistance and thermal noise from source resistance. $\overline{v}_g^2$ are $\overline{v}_l^2$ are the thermal noise due to loss in the gate inductor and the source inductor in the matching network. $\overline{i}_{Rp}^2$ is the thermal noise due to the loss in the output inductor. $\overline{i}_{d1}^2$, $\overline{i}_{d2}^2$, $\overline{i}_{d3}^2$ and $\overline{i}_{d4}^2$ are the thermal noise from transistors M_1, M_2, M_3 and M_4. The noise from transistor M_{b2} is not included because it is a common mode noise.

The transconductance of the input stage of the LNA including the matching network is:

$$G_m(\omega) = \frac{g_m \frac{1}{sC_{gs}}}{sL_g + sL_s + \frac{1}{sC_{gs}} + \frac{\omega_T}{s}R_l + \omega_T L_s + R_g + R_l + R_s} \qquad (5.5)$$

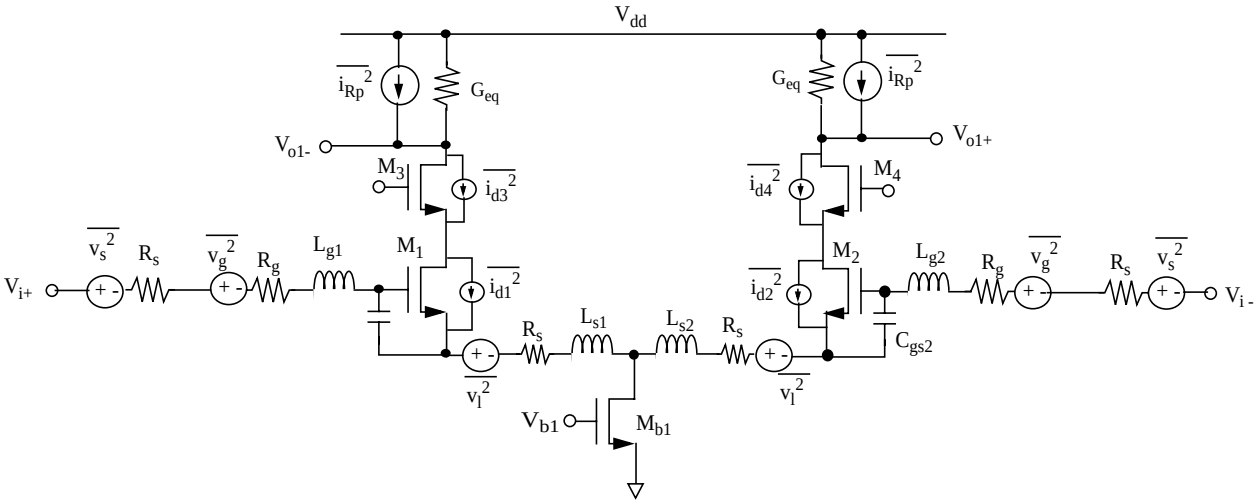


Fig. 5.12 Equivalent Circuit of LNA with Noise Sources

At the resonant frequency, the imaginary part vanishes and the real part equals $2R_S$. Therefore the Eq. (5.5) can be revised as:

$$G_m(\omega_0) = \frac{g_m \frac{1}{sC_{gs}}}{2R_s} = \frac{\omega_T}{2\omega_0 R_s} \tag{5.6}$$

The noise factor of the LNA is [69]:

$$F = 1 + 2\frac{R_g + R_l}{R_s} + 2\frac{\gamma g_{m1}}{R_s}(R_s + R_g)^2\left(\frac{\omega_o}{\omega_T}\right)^2 + 2\frac{R_s}{(1 + Q_{Lo}^2)R_{Lo}}4\left(\frac{\omega_o}{\omega_T}\right)^2 + 2\gamma g_{mq} R_s 4\left(\frac{\omega_o}{\omega_T}\right)^2 \tag{5.7}$$

From equation Eq. (5.6), the equivalent Gm of the LNA is independent from the gm of the input device, as long as the unit gain frequency, ω_T, of the device is fixed. From equation Eq. (5.7), the output noise due the source noise is also independent from the gm of the input devices for a fixed unit-gain frequency, ω_T. Therefore, the best method to improve the noise performance of the LNA, is to increase the unit-gain frequency, ω_T, of the input devices by increasing the bias current of the input devices or reducing the C_{gs} of input devices. However, a smaller C_{gs} needs a larger L_g to maintain the same resonant frequency, and a larger L_g will

have more loss and cause more noise. Therefore, a trade-off must be made between L_g and C_{gs} to optimize the NF of the LNA.

Typical values can be assumed to the constant parameters, e.g. R_s=50Ω, ω_o=950MHz, Q_{Lo}=3, R_{Lo}=7.7, g_{mq}=10ms, g_{m1}=26ms, γ=2/3. Because the gate inductor is relatively large, 17nH in this design, Q_g is relatively low. A typical number of Q_g is 2. According to these numbers, the calculated NF according to Eq. (5.7) is 5.67 dB, which is consistent with the simulation result of 5.63 dB. The simulated noise contribution of each component is summarized in Table 5.1. However, including the notch-filter, the NF increases to 6.2 dB. The NF as a function of frequency is plotted in Fig. 5.13.

Table 5.2 Noise Contribution of Each Component

Components	**Noise Voltage at Output**	**Percentage in Overall Noise**
Source resistor (50 Ω)	3.63e-16 V^2/Hz	27.2%
Gate inductors	1.13e-16	17%
Fist stage:		
Output inductors	6.89e-17	10.4%
Input transistors	3.78e-17	5.7%
Cascode transistors	1.07e-17	1.6%
Q-tuning circuits	1.55e-16	11.6%
Second stage:		
Output inductors	4.28e-17	6.5%
Input transistors	6.58e-18	1%
Cascode transistors	1.47e-18	0.2%
Q-tuning circuits	1.31e-16	9.9%
Total noise	1.33d-15	NF=5.63 dB

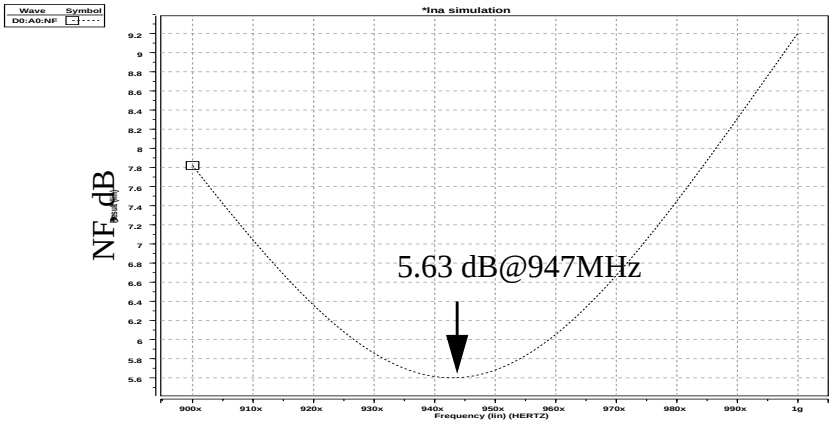


Fig. 5.13 NF of the LNA

Table 5.3 Transistors In LNA Core Circuit

Transistor	**Size W/L**	**Current (Vdd=2V)**
Mb1	48x18.15µm/0.6µm	7.4 mA
M1	24x21.3µm/0.9µm	3.7 mA
M2	24x21.3µm/0.9µm	3.7 mA
M3	24x15µm/0.9µm	3.7 mA
M4	24x15µm/0.9µm	3.7 mA
Mb2	10x9.45µm/0.6µm	734 uA
M5	6x9.3µm/0.9µm	367 uA
M6	6x9.3µm/0.9µm	367 uA
M7	6x7.8µm / 0.9µm	367 uA
M8	6x7.8µm / 0.9µm	367 uA
R1, R2	100 Ω	367 uA
Total		8.1mA

Table 5.4 Transistors In Q-tuning Circuit

Transistor	**Size W/L**	**Current (Vdd=2V)**
M1a	16x9.9µm/0.9µm	2.2 mA

Table 5.4 Transistors In Q-tuning Circuit

Transistor	Size W/L	Current (Vdd=2V)
M1b	16x9.9µm/0.9µm	2.2 mA
M2a	16x7.5µm/0.6µm	486 uA
M2b	4x7.5µm/0.9µm	20 uA
M3a	4x7.5µm/0.9µm	20 uA
M3b	16x7.5µm/0.6µm	486 uA
Mb1	20x36µm/1.2µm	4.4 mA
Mb2	4x30µm/1.2µm	506 uA
Mb3	4x30µm/1.2µm	506 uA
Total		5.4 mA

5.8 Summary

The LNA with a third-order notch filter to improve the image rejection is presented in this chapter. The LNA consists of two stages and each stage is a source-coupled pair with a cascode configuration. Inductive source degeneration with on-chip inductors is used in the first stage to achieve an on-chip 50-Ω matching. The parallel resonant tanks including the on-chip inductors and the SCAs are used as output loading. The unbalanced negative Gm-cells are used to compensated the loss due to on-chip inductors and maximize the linearity of the LNA. The third-notch filter is used in the second stage of the LNA to improved the image rejection.

According to the simulation results, with the notch filter, the image rejection is achieved to be 50 dB. The gain is simulated to be 23 dB. The desired bandwidth of 25 MHz is achieved by compensating the loss of the on-chip inductors using negative g_m-cells. The IIP3 is simulated to be -17 dBm. With the switchable-capacitor array, the frequency tuning range is more than 150 MHz. The noise figure of the amplifier is 6.2 dB. The amplifier consumes 25 mA current from a 2-V single supply.

Chapter 6

FRACTIONAL-N FREQUENCY SYNTHESIZER WITH SIGMA-DELTA MODULATION

Frequency synthesizers are usually used to provide LO frequencies in wireless transceivers, which require very high absolute accuracy in the LO frequencies and precise tuning steps. Phase noise, spurious tones and settling time are also important for the performance of a transceiver.

A fractional-N frequency synthesizer with sigma-delta modulation used in the proposed transceiver, including a switched-capacitor array used in the voltage-controlled oscillator (VCO), a sigma-delta modulator and a dual-path filter. The synthesizer can be used as a direct-modulation transmitter by controlling the division value of the divider.

The first prototype of the synthesizer is designed for the receiver with a loop bandwidth of 80 kHz, which is not high enough for the transmitter with a transmission bandwidth of 200 kHz. Therefore, the second prototype is design for the transceiver with and bandwidth of 200 kHz. With larger bandwidth, more in-band VCO noise is suppressed, but quantization noise outside the loop band is larger. However, the out-of-band phase noise meet the specification. The settling time, which is limited by the loop bandwidth, of the second prototype is further reduced. The chip area is also reduced by using smaller capacitors in the second prototype.

6.1 Block Diagram of the Synthesizer

The bock diagram of the proposed frequency synthesizer is shown in Fig. 6.1. It consists of a third-order sigma-delta modulator, a multi-modulus divider, a dual-path filter, and a VCO with two switched-capacitor arrays.

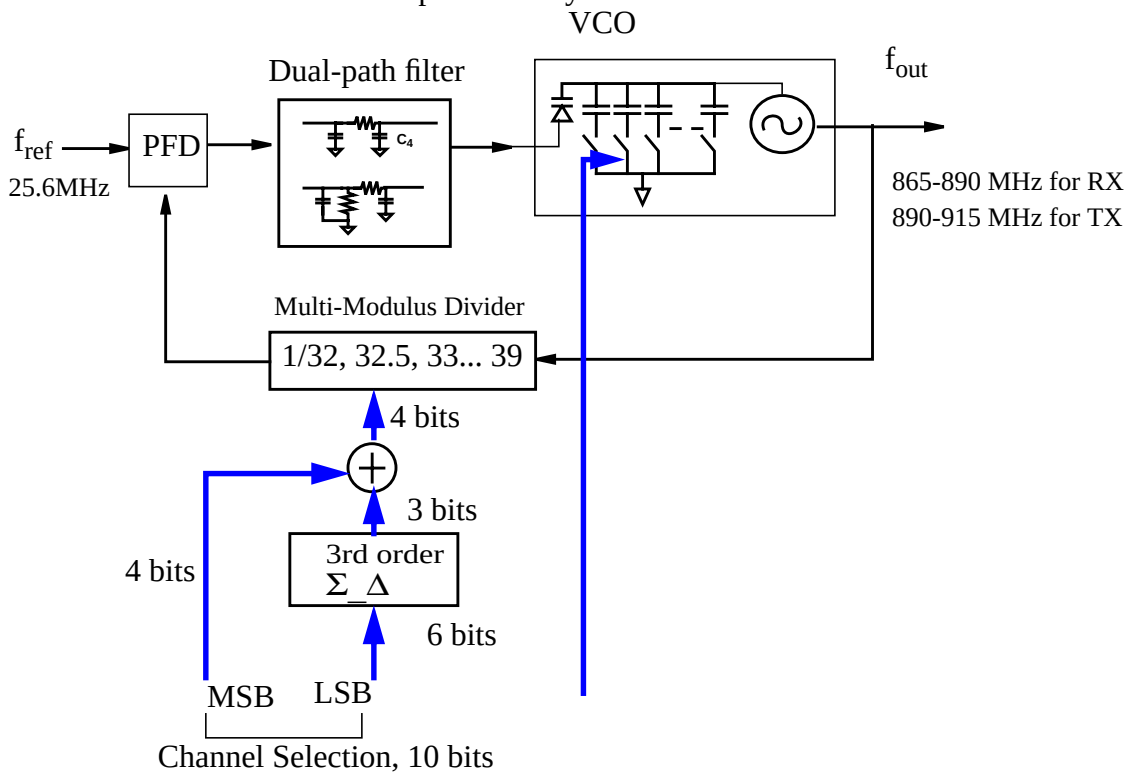


Fig. 6.1 Proposed Synthesizer with Sigma-Delta Modulation

A switched-capacitor array (SCA) is used in the VCO to improve the switching speed. in this design. The predicted capacitance of the VCO is directly added to the VCO by the SCA. Therefore, the output frequency of the synthesizer is tuned close to the output frequency directly without the loop response. As a result, the switching speed is improved.

With the SCAs, only a small tuning voltage is needed from the PLL loop to achieve fine tuning, which results in a constant bias condition and a constant gain of the varactor. Therefore a constant optimal loop bandwidth for settling time is obtained without any linearization techniques.

The capacitance value of the switched-capacitor array is insensitive to the substrate noise when the switches, which are NMOS transistors, are fully turned on or off. Because the varactor is very small, it has a small contribution to the VCO phase noise. Therefore, a better phase noise performance is achieved with the SCA. In addition, the SCA doesn't consume DC power.

The third-order sigma-delta modulator is used to continuously switch the prescaler between two values, e.g. N and N+1. The average division value is between N and N+1. The final frequency resolution of the fractional-N synthesizer depends on the resolution of the averaged division value, which is determined by the number of bits at the input of the sigma-delta modulator. Third-order sigma-delta modulator is chosen to trade off between loop bandwidth and phase noise [45].

One advantage of the fractional-N synthesizer is that the harmonics of the reference signal is outside the receiving band because the reference frequency can be much larger than the channel spacing. The other advantage is that the divider can be easily implemented because the division value can be lower. However, it suffers from a problem of pattern noise. The pattern noise is generated by the periodical changing of the division value, which controls the output of the synthesizer. This periodical signal can be located within the receiving band and corrupt the spurious performance. A dither, that can outputs a pseudo-random signal, is used to control the sigma-delta modulator to remove the pattern noise, when the synthesizer is working for the receiver. When the synthesizer is working for the transmitter, the input signal itself is a random signal. Therefore, no dither signal is needed and the dither is turned off.

6.2 Dual-Path Loop Filter

In a phase-locked loop with charge pumps in the loop filter (type-II PLL), a zero in the open loop transfer function is required to keep the loop stable. It can be implemented with an

active loop filter with resistors and capacitors. However, a large capacitor (C_z) of a few nF, is needed because of the large ratio between the C_z and C_p. A large capacitor will occupy a large chip area.

Dual-path filters [46] are used to implement the required zero with smaller capacitors. As shown Fig. 6.2, a zero is realized by adding the outputs of an integrator and a low-pass filter. Because the dependence between C_z and C_p is removed, both of them can have smaller capacitance values. The outputs of the two paths are used to control the bias voltages of the two varactors. Because both the two varactors contribute to the total capacitance of the VCO, $C_{tot}=C_1+C_2$, the output signals of the two paths are equivalently added together in capacitance domain [41].

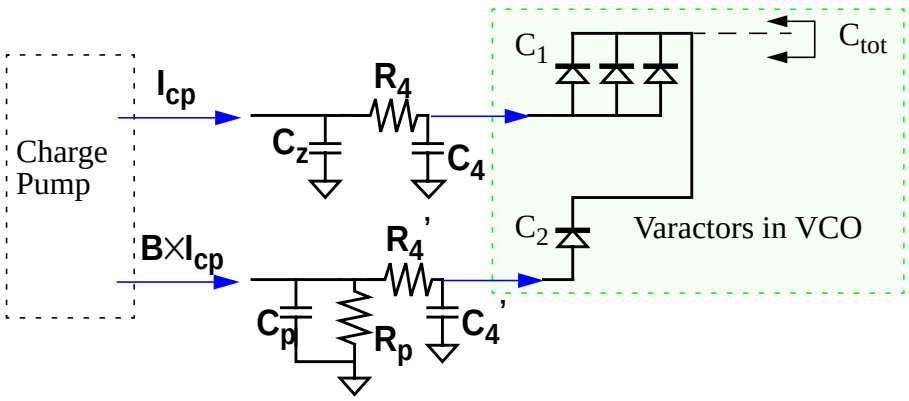


Fig. 6.2 Dual-Path Loop Filter with Signal Added in Capacitance Domain

6.3 Voltage-Controlled Oscillator

The voltage-controlled-oscillator (VCO) used in the frequency synthesizer is shown in Fig. 6.3. It consists of two L-C oscillators cross-coupled with four transistors to achieve quadrature outputs. By sharing bias current sources of both the oscillators and coupling transistors[47], better amplitude and phase matching is achieved [43]. Two switched-capacitor arrays (SCA) are used in the VCO to achieve fast switching. Two PN-junction varactors used

in each oscillator are connected to the outputs of the dual-path filter to provide fine frequency tuning. The gain of frequency controlling of the large varactor is 9 MHz/V, and that of the small varactor is 0.9 MHz/V.

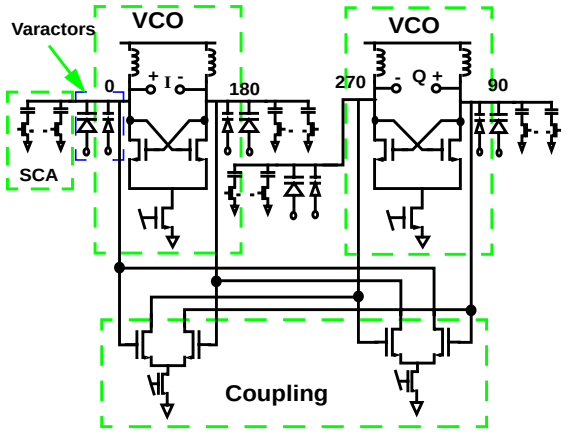


Fig. 6.3 VCO with Switched-Capacitor Array

6.4 Passive Components

To facilitate the analysis of the synthesizer loop, a behavior model of the proposed synthesizer is used, as shown in Fig. 6.4. K_{vco1} and K_{vco2} represent the VCO gain for the two varactors and K_{vco1}=9MHz/V, K_{vco2}=0.9MHz/V. I_{qp} and $B \cdot I_{qp}$ represent the charge pump current in the two paths. 1/N is the nominal division value of the divider. C_{vco}=1 is used to model the integration-function of the VCO. $1/2\pi$ is used to model the phase-frequency detector (PFD) which converts the phase difference to the control signal of the charge pumps. Let $K_{vco1}=K_{vco}$, then $K_{vco2}=K_{vco}/\rho$.

The loop filter, H(s), and the equations of passive components is derived in [51] and summarized in follows. One difference from [51] is that the VCO gain for one path with the low-pass filter is $1/\rho$ smaller than that of the path with the integrator. The smaller gain accounts for the smaller varactor used in this path, which results in smaller chip area, smaller noise coupling from the substrate and better phase noise of the output signal.

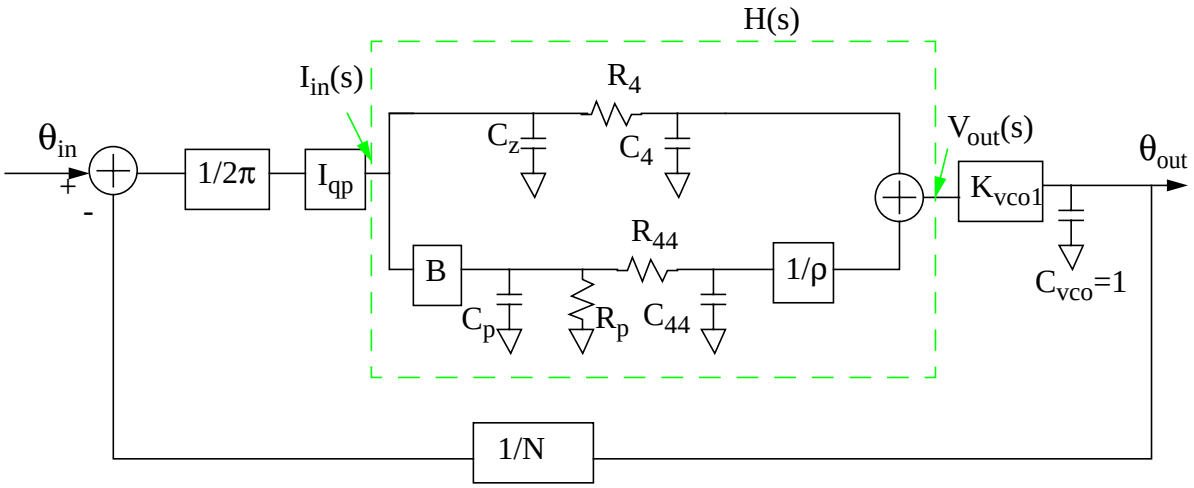


Fig. 6.4 Behavior Model of the Synthesizer

$$H(s) = \frac{V_{out}(s)}{I_{in}(s)} = \frac{1}{sC_z}\cdot\frac{1}{1+sC_4R_4} + \frac{B}{\rho}\cdot\frac{R_p}{1+sC_pR_p}\frac{1}{1+sC_{44}R_{44}}$$
$$= \frac{1}{sC_z}\cdot\frac{1}{1+s\tau_4} + \frac{B}{\rho}\cdot\frac{R_p}{1+s\tau_p}\cdot\frac{1}{1+s\tau_{44}} \qquad (6.1)$$

where $\tau_4=C_4R_4$, $\tau_p=C_pR_p$, $\tau_{44}=C_{44}R_{44}$.

$$\tau_4=\tau_p=\tau_{44} \text{ and } \omega_p=1/\tau_p=\beta\omega_c,\ \beta=6.$$

$$\omega_c = \frac{I_{qp}}{2\pi}\cdot\frac{K_{vco}}{N}\cdot\frac{R_p\left(C_p+\frac{B}{\rho}\cdot C_z\right)}{C_z}, \qquad (6.2)$$

$$\omega_z=1/\tau_z=\omega_c/\alpha, \qquad (6.3)$$

$$\alpha=4$$

$$\tau_z = R_pC_p + R_p\frac{B}{\rho}\cdot C_z \approx R_p\frac{B}{\rho}\cdot C_z\,. \qquad (6.4)$$

The open-loop function of the synthesizer is:

$$GH(s) = \frac{I_{qp}}{2\pi}\cdot\frac{K_{vco}}{sN}\cdot\frac{1}{sC_z}\cdot\frac{1+s\tau_z}{(1+s\tau_p)^2} \qquad (6.5)$$

The passive components used in the synthesizer can be derived as follows according to

$$R_p = \frac{2\pi N\rho}{I_{qp}K_{vco}B} \cdot \omega_c \tag{6.6}$$

$$C_p = \frac{1}{\beta R_p \omega_c} = \frac{I_{qp}K_{vco}B}{2\pi N\rho\beta\omega_c^2} \tag{6.7}$$

$$C_z = \frac{\alpha\rho}{R_p B\omega_c} \tag{6.8}$$

$$R_{44}=R_p/\gamma,\ C_{44}=\gamma C_p, \tag{6.9}$$

$$R_4=R_{44}/\rho,\ C_{44}=\rho C_4 \tag{6.10}$$

The values of passive components are summarized in Table 6.1. The synthesizer is firstly designed for the receiver with loop bandwidth of 80 kHz. In the second prototype, the synthesizer for transceiver with bandwidth of 200 kHz.

Table 6.1 Passive Components in Synthesizer Loop for Receiver and Transceiver

Component	**Receiver**	**Transceiver**	**Component**	**Receiver**	**Transceiver**
Iqp	2.9 μA	14 μA	C44	6.75 pF	5.18pF
Cz	54 pF	41.5pF	Cp	2.25 pF	1.73pF
R4	24.7 kΩ	5.1kΩ	Rp	740 kΩ	153.5kΩ
C4	67.5 pF	51.8pF	Kvco1	9 MHz/V	9MHz/V
R44	247 kΩ	51.2kΩ	Kvco2	0.9 MHz/V	0.9MHz/V

In the first prototype, the resistor, R_p, is very big, which has to be implemented with a transistor in linear region. Therefore, the linearity of the resistor is not high. In the second prototype, smaller resistors are used for larger bandwidth. As a result, they can all be implemented with poly resistors with high linearity.

The synthesizer loop is simulated with Hspice based on the behavior model, and the simulation result is shown in Fig. 6.5. A single-side bandwidth of 100 kHz or double-side

bandwidth of 200 kHz is achieved in second prototype, which is large enough for the bandwidth requirement in the direct-modulation transmitter.

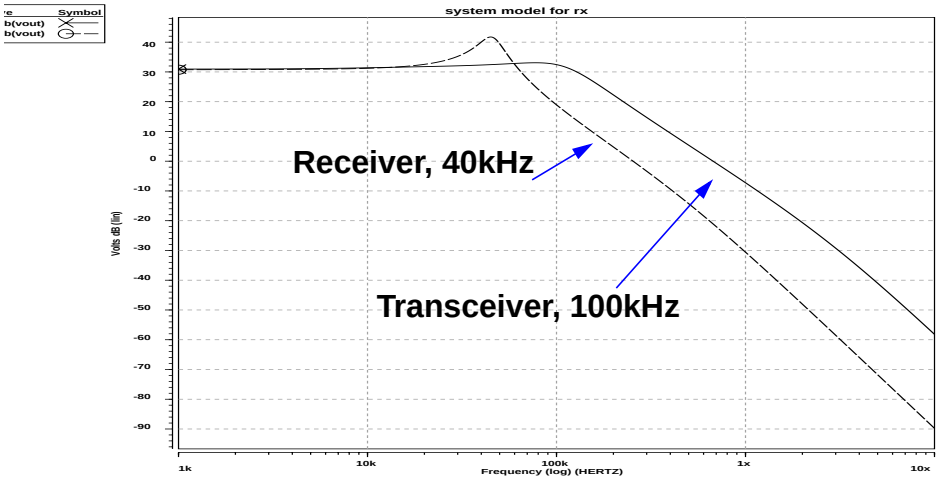


Fig. 6.5 Simulation Result Based on the Behavior Model

6.5 Noise Analysis of the Synthesizer

The noise contribution in the synthesizer can be analyzed according to the behavior model derived above. Including the noise sources, the synthesizer is modeled in Fig. 6.6, where $\bar{i}_{n1}^2$ and $\bar{i}_{n2}^2$ are noise sources of two charge pumps, $\overline{V}_{R4}^2$ is the noise from the resistor R_4, $\overline{V}_{R44}^2$ is the noise from the resistor R_{44}, $\bar{i}_{Rp}^2$ is the noise from the resistor R_p.

For the noise source i_{n1}^2,

$$\left[\left(\theta_{out}(s)\frac{1}{N}\frac{1}{2\pi}I_{qp} + i_{n1}(s)\right)\cdot H_i(s)H_4(s) - \theta_{out}(s)\frac{1}{N}\frac{1}{2\pi}I_{qp}\frac{B}{\rho}H_L(s)H_{44}(s)\right]\frac{K_{vco}}{s} = \theta_{out}(s) \quad (6.11)$$

where $H_i(s)=1/sC_z$, $H_4(s)=1/(1+sR_4C_4)$, $H_{44}(s)=1/(1+sR_{44}C_{44})$, $H_L(s)=R_p/(1+sR_pC_p)$,

and $H(s)=H_i(s)H_4(s) + H_L(s)H_{44}(s)$.

Therefore,

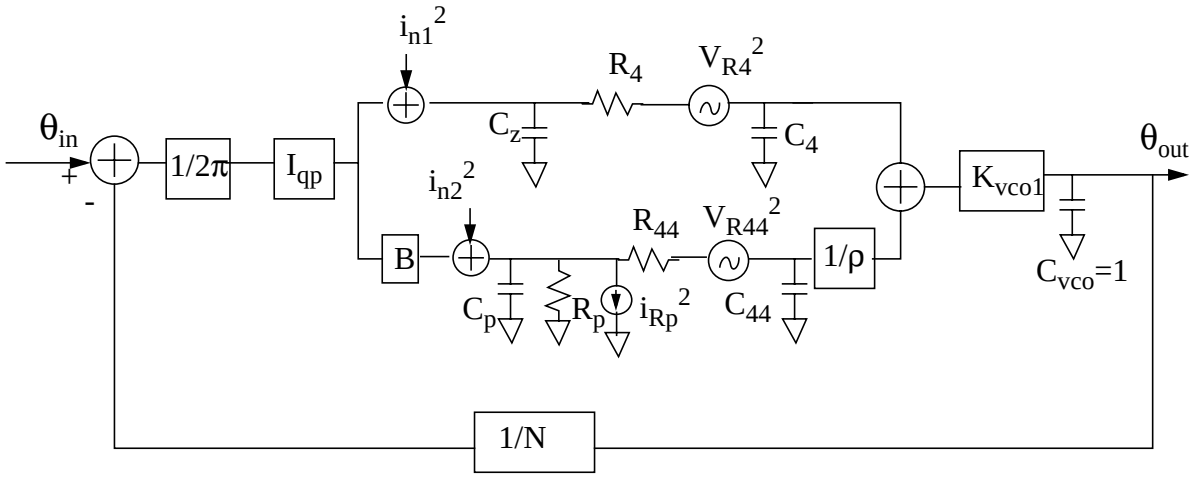


Fig. 6.6 Behavior Model with the Noise Sources

$$\frac{\theta_{out}(s)}{i_{n1}(s)} = \frac{H_i(s)H_4(s)K_{vco}}{s + \frac{K_{vco}I_{qp}}{N2\pi}H(s)} \tag{6.12}$$

Similarly, for the noise source i_{n2}^2,

$$\frac{\theta_{out}(s)}{i_{n2}(s)} = \frac{H_p(s)H_{44}(s)\frac{K_{vco}}{\rho}}{s + \frac{K_{vco}I_{qp}}{N2\pi}H(s)} \tag{6.13}$$

At frequencies larger than ω_p, Eq. (6.12) can be simplified as:

$$\begin{aligned}
\frac{\theta_{out}(s)}{i_{n1}(s)} &= \frac{H_i(s)H_4(s)K_{vco}}{s + \frac{K_{vco}I_{qp}}{N2\pi}H(s)} \\
&\approx \frac{H_i(s)H_4(s)(K_{vco}/s)}{1 + GH(s)} \\
&= H_i(s)H_4(s)(K_{vco}/s) \\
&= \frac{1}{sC_z}\frac{1}{1 + \frac{s}{\omega_p}}\frac{K_{vco}}{s} \\
&= \frac{\beta K_{vco}\omega_c}{C_z S^3} \\
&= \frac{2\pi N\beta}{I_{qp}\alpha}\left(\frac{\omega_c}{s}\right)^3
\end{aligned} \tag{6.14}$$

Similarly, Eq. (6.13) can be simplified as:

$$\begin{aligned}
\frac{\theta_{out}(s)}{i_{n2}(s)} &= \frac{H_p(s)H_{44}(s)\frac{K_{vco}}{\rho s}}{1 + GH(s)} \\
&= H_p(s)H_{44}(s)(K_{vco}/(\rho s)) \\
&= \frac{1}{sC_z}\frac{1}{1 + \frac{s}{\omega_p}}\frac{K_{vco}}{s} \\
&= \frac{\beta K_{vco}R_p\omega_c^3}{\rho S^3} \\
&= \frac{2\pi N\beta^2}{I_{qp}B}\left(\frac{\omega_c}{s}\right)^3
\end{aligned} \tag{6.15}$$

Therefore, the phase noise due to charge pump noise is:

$$
\begin{aligned}
L_{qp}(\Delta\omega) &= \frac{1}{2}\left[\left|\frac{Q_{out}(\Delta\omega)}{i_{n1}(\Delta\omega)}\right|^2 \cdot di_{n1}^2 + \left|\frac{Q_{out}(\Delta\omega)}{i_{n2}(\Delta\omega)}\right|^2 \cdot di_{n2}^2\right] \\
&= \frac{1}{2}\left[\left|\frac{2\pi N\beta}{I_{qp}\alpha}\left(\frac{\omega_c}{\Delta\omega}\right)^3\right|^2 4kT2\alpha_{qp}g_{m1} + \left|\frac{2\pi N\beta^2}{I_{qp}B}\left(\frac{\omega_c}{\Delta\omega}\right)^3\right|^2 4kT2\alpha_{qp}g_{m2}\right] \\
&= \frac{1}{2}\left[\left(\frac{2\pi N\beta}{I_{qp}\alpha}\right)^2\left(\frac{1}{\alpha^2} + \frac{\beta^2}{B}\right)4kT2\alpha_{qp}g_{m1}\left(\frac{\omega_c}{\Delta\omega}\right)^6\right]
\end{aligned} \tag{6.16}
$$

The noise from the resistors in the synthesizer loop can be analyzed as:

$$
\begin{aligned}
\frac{\theta_{out}(s)}{i_{RP}(s)} &= \frac{H_p(s)H_{44}(s)\dfrac{K_{vco}}{\rho s}}{1 + \dfrac{K_{vco}I_{qp}}{2\pi N s}H(s)} \\
&= H_p(s)H_{44}(s)(K_{vco}/(\rho s)) \\
&= \frac{1}{sC_z}\frac{1}{1 + \dfrac{s}{\omega_p}}\frac{K_{vco}}{s} \\
&= \frac{\beta K_{vco}R_p\omega_c^3}{\rho S^3} \\
&= \frac{2\pi N\beta^2}{I_{qp}B}\left(\frac{\omega_c}{s}\right)^3
\end{aligned} \tag{6.17}
$$

$$
\begin{aligned}
\frac{\theta_{out}(s)}{V_{R4}(s)} &= \frac{H_4(s)\dfrac{K_{vco}}{s}}{1 + GH(s)} \\
&= \frac{\beta K_{vco}\omega_c}{S^2}
\end{aligned} \tag{6.18}
$$

$$\frac{\theta_{out}(s)}{V_{R44}(s)} = \frac{H_{44}(s)\frac{K_{vco}}{\rho s}}{1 + GH(s)}$$

$$= \frac{\beta K_{vco}\omega_c}{\rho S^2} \tag{6.19}$$

The phase noise due to quantization noise of the sigma-delta modulator is:

$$S_{\Phi q}(f) = \frac{1}{T}\left(\frac{(2\pi)^2}{12}(2\pi fT)^{2(n-1)}\right)|TG(f)|^2 \tag{6.20}$$

For the bandwidth of 200kHz, the phase noise contribution of each noise source is plotted in Fig. 6.7. A phase noise of -118 dBc/Hz @600kHz is obtain when Iqp=14μA and the passive components are Cz=41.48pF, C4=51.85pF, C44=5.18pF, Cp=1.73pF, R4=5.1kW, Rp=153.5kW, R44=51.16k, and Kvco1=9MHz/V, Kvco2=0.9MHz/V.

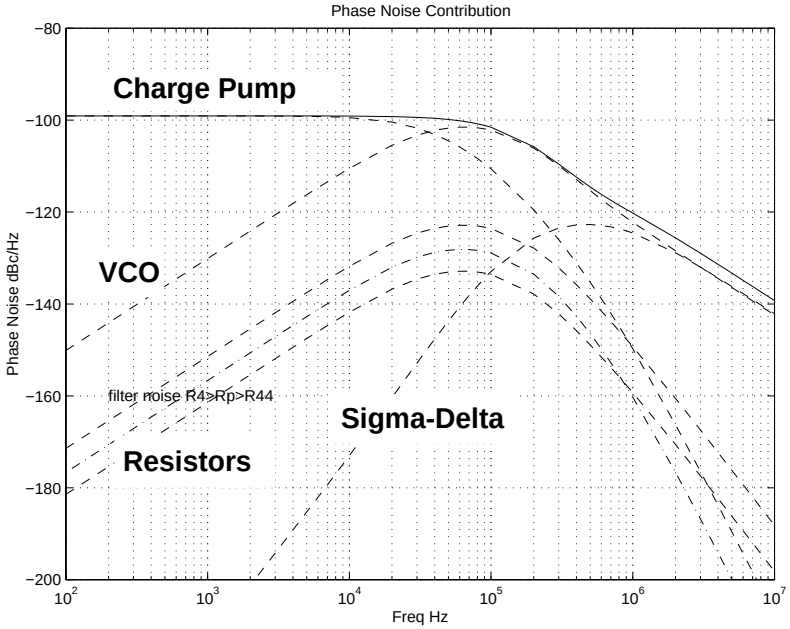


Fig. 6.7 Phase Noise Contribution of Each Noise Source

As required by transmitter, the loop bandwidth is designed to be 200 kHz by transmission band, by properly set the loop gain and loop filter. The noise contribution from the resistors in the loop filter is negligible compared with other noise source. The charge pump

current is set to an optimum value so that the in-band noise power has same noise floor as VCO noise at 100kHz offset. The phase noise outside the bandwidth is limited by both VCO noise and quantization noise from sigma-delta modulator. A PN of -118 dBc/Hz at 600 kHz is achieved.

6.6 Direct-Modulation

The direct-modulation transmitter is realized by modulate the division value of the fractional-N frequency synthesizer as shown in Fig. 6.8. A Gaussian filter with BT=0.3 is used to filter the input digital signal so that GMSK modulation can be realized. Since the Gaussian filtered is usually implemented with DSP circuits, it is not included in the proposed transceiver. However, a MATLAB program is used to simulate the Gaussian filter and generate the filtered data as the input signal for the transmitter [72]. The input signal has a bit rate of 270kbps. It is filtered and then digitalized with 10-bit resolution and 2.7-MHz sampling frequency. With 10-bit resolution and 10-times oversampling, the SNR of the input base-band signal itself due to the quantization noise is suppressed to SNR=6x10+10=-70 dB/270kHz=124 dBc/Hz, which is good enough to meet the output spectrum requirement (70dB/30kHz). One more sigma-delta modulator is used to convert the 10-bit-resolution 10-times oversampled baseband signal to a 3-bit oversampled signal, so that it can achieve better frequency resolution. The VCO frequency is modulated by the filtered input signal.

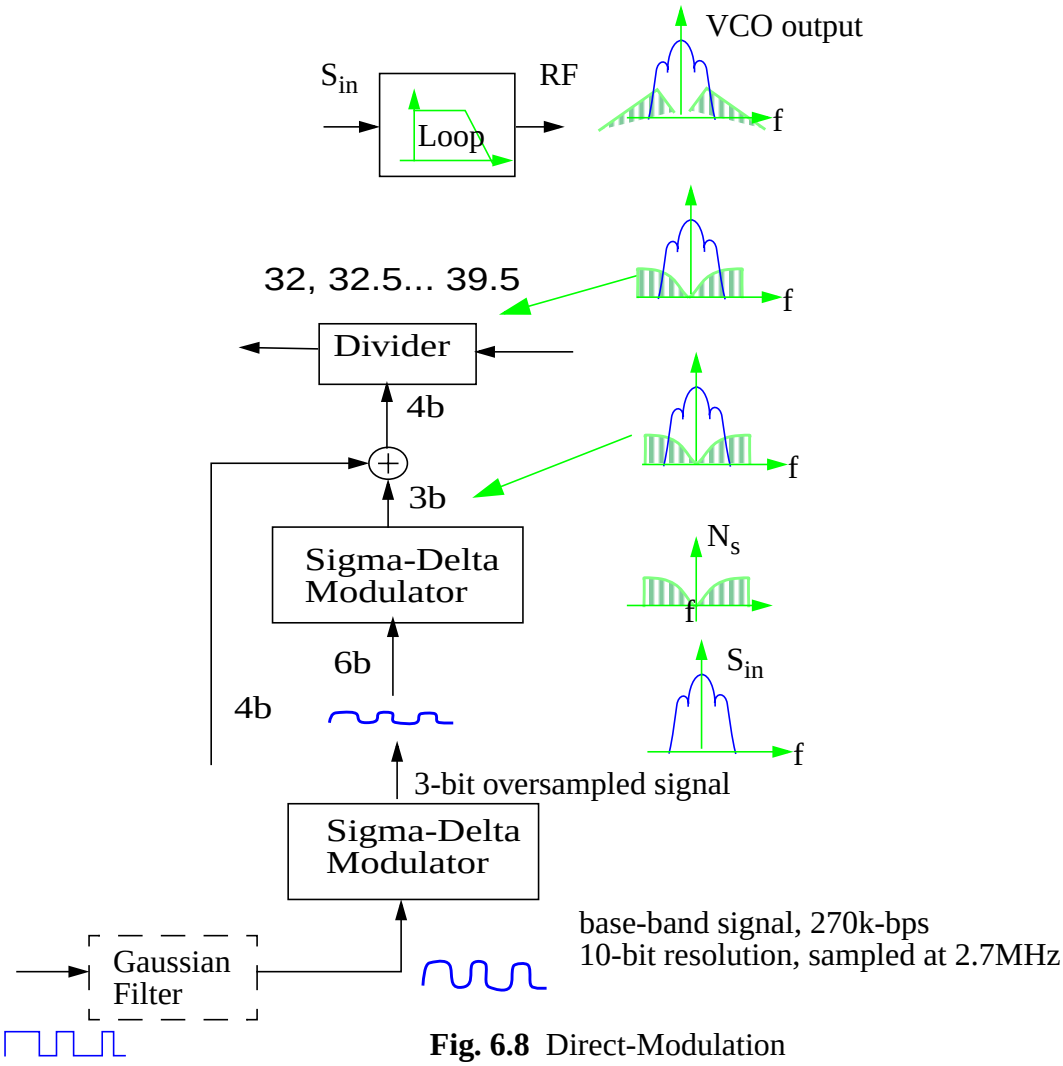


Fig. 6.8 Direct-Modulation

6.7 Summary

The design of the frequency synthesizer is briefly described in this chapter. The equations to design the loop parameters and component values are also discussed. The loop is designed to obtain 200kHz bandwidth. The synthesizer can work as a direct-modulation transmitter with 200kHz signal bandwidth.

Chapter 7

VARIABLE GAIN AMPLIFIER

A variable gain amplifier (VGA) working at 70 MHz is discussed in this chapter. An offset cancellation circuit is adopted in the VGA to suppress the DC offset at the VGA output. A simple received-signal-strength-indicator (RSSI) is built to demonstrate the automatic-gain-control (AGC) operation.

7.1 General Considerations

The dynamic range of the received signal at the receiver input is up to 78 dB. This dynamic range is much larger than the maximum achievable input dynamic range of the ADC. Therefore, a VGA is needed before the ADC to provide an appropriate signal dynamic range. With the 23-dB switchable gain LNA, the VGA is required to provide the other gain control range of 55 dB. As such, the input signal to the ADC is fixed at an optimum level so that the SNR of the ADC output is maximum.

Because of the filtering function of the IF channel selection filter, the input signal of the VGA is almost free of out-of-channel interferences. Therefore, the linearity requirement of the VGA is much relaxed. In addition, the effect of the VGA's noise figure (NF) on the system NF is scaled down by the total gain of the previous blocks in the system [52], including LNA, mixer and IFBP. As a result, the required noise figure is also much relaxed. For the proposed receiver, the target IIP3 and NF for the VGA are - 40 dBm and 20 dB, respectively.

Because of the process variations, any high-gain CMOS amplifier will suffer from a problem with offset voltage. In order to prevent the VGA from being saturated by its offset voltage, an offset cancellation technique is employed, which enables the VGA to tolerate an offset voltage of more than 50 mV.

7.2 Gain Varying Techniques

7.2.1 Problems with Existing Techniques of Gain Varying

There are several ways to vary the gain of an amplifier. As shown in Fig. 7.1, the gain of a simple differential amplifier can be controlled by its bias or loading. By tuning the loading R_{L1} and R_{L2}, the gain at low frequencies is varied, but its common mode output voltage is also changed and affects the bias for the next stage. Alternatively, the gain can be varied by tuning the bias I_b [58]. However, when the signal is large, the bias should be set to a smaller value to get a smaller gain, in which case, the dynamic range of the input devices is also reduced. This is opposite to the requirement of a VGA [59]. In addition, the common-mode output also depends on the gain, and this technique also entails a lot of power dissipation to obtain gain variation [60].

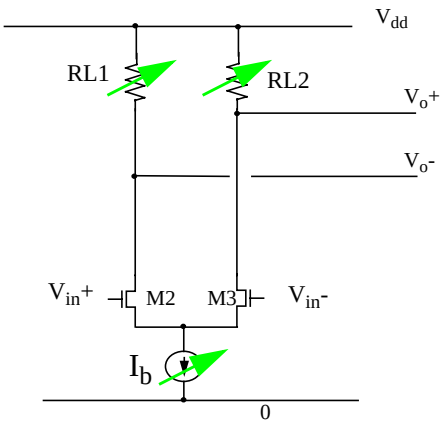


Fig. 7.1 Existing Gain Varying Techniques

7.2.2 Proposed Technique of Gain Varying

The proposed VGA is realized with 3 identical cells, A_1, A_2, and A_3, as shown in Fig. 7.2. The gain of each cell can be varied independently from 0 dB to 23 dB by adjusting its own control voltage V_c. To achieve a minimum NF, the gain of the first stage should be as high as possible [57]. In other words, when the signal is large, the gain of the second and third stage should be reduced before the gain of first stages is reduced. However, for large input signals, the noise requirement of the VGA is actually relaxed. Therefore, for simplicity, the control voltage of all three cells are connected together, and their gain is varied at same time.

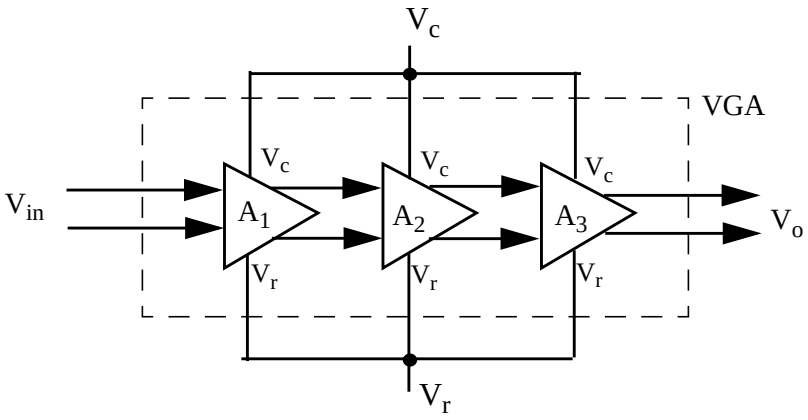


Fig. 7.2 Block Diagram of the VGA

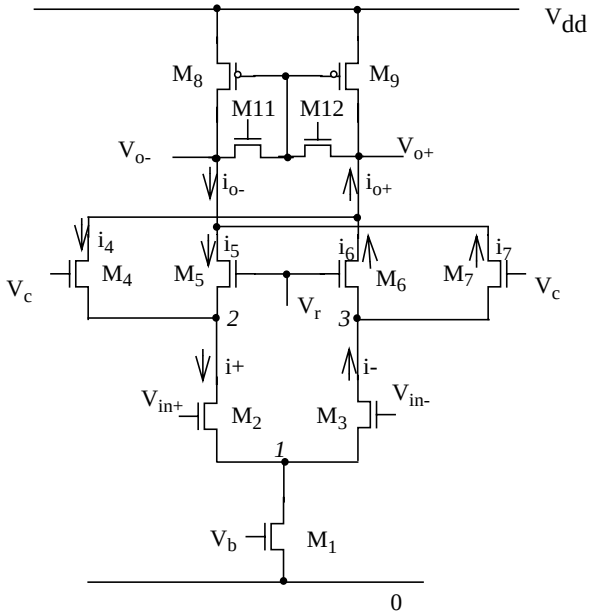


Fig. 7.3 Proposed VGA Schematic

As shown in Fig. 7.3, each proposed VGA cell comprises a differential pair with a common-mode feedback and four cross-coupled control transistors, M_4 - M_7. M_1 is the bias transistor, and M_2 and M_3 are input devices. M_8 and M_9 are PMOS transistors in saturation region working as active loading. M_{11} and M_{12} form a common-mode feedback circuitry. V_r is a reference voltage, and V_c is used to control the cross coupling between the two differential ends, which in turn controls the gain. When V_r = 2.1 V and V_c = 0 V, the cross coupling is turned off, and the gain is maximum. When $V_r = V_c$ = 2.1 V, the cross coupling is maximum, and the gain is 0.

Let α be the fraction of the current in M_2 that flows in M_4, i.e.

$$i_4 = \alpha \times i_+ \tag{7.1}$$

With g_{ma} being the transconductance of M_2 and M_3, it is easy to show that

$$\begin{aligned} V_o &= (i_{o+} + i_{o-})\, R_L \\ &= (2\alpha\text{-}1)\, g_{ma} \times R_L \times V_i \\ &= K \times g_{ma} \times R_L \times V_i \end{aligned} \tag{7.2}$$

So the gain A is

$$A = K \times g_{ma} \times R_L, \tag{7.3}$$

where $K = 2\alpha - 1$.

When V_r is 2.1 V and V_c is 0 V, M_5, M_6 are turned off, and α = 1, K = 1. So the maximum gain A_{max} is

$$A_{max} = g_{ma} \times R_L. \tag{7.4}$$

At 70 MHz, since the maximum gain of each cell is larger than 23 dB, the maximum gain of the whole VGA with the three cells is around 70 dB.

On the other hand, when $V_c = V_r = 2.1$ V, $\alpha = 0.5$ and K = 0, so the gain A is 0. However, this case is never needed in this application.

The simulated frequency response of the VGA with the gain set at 63 dB at 70 MHz is shown Fig. 7.4. The simulated gain-control range is shown in Fig. 7.5. The gain is simulated at 70 MHz and the maximum gain is 69 dB. The minimum gain can be infinity in ideal case.

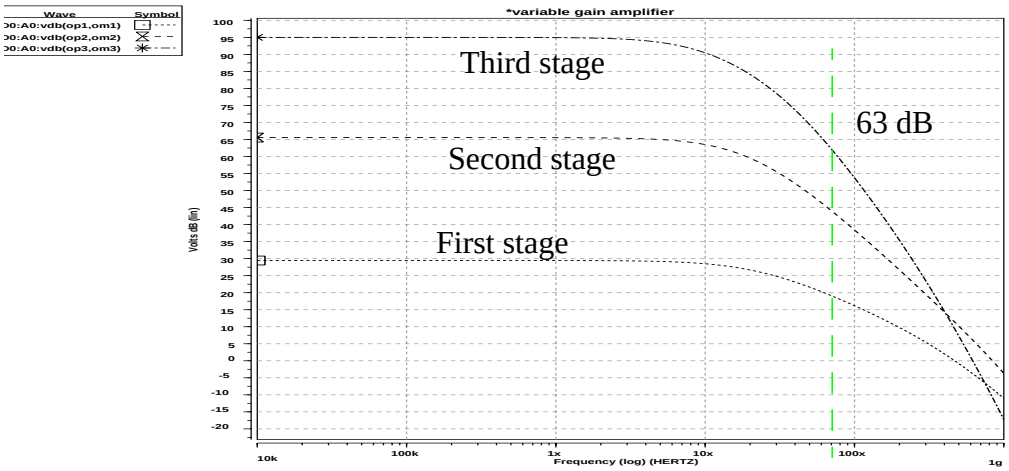


Fig. 7.4 Simulated VGA Frequency Response

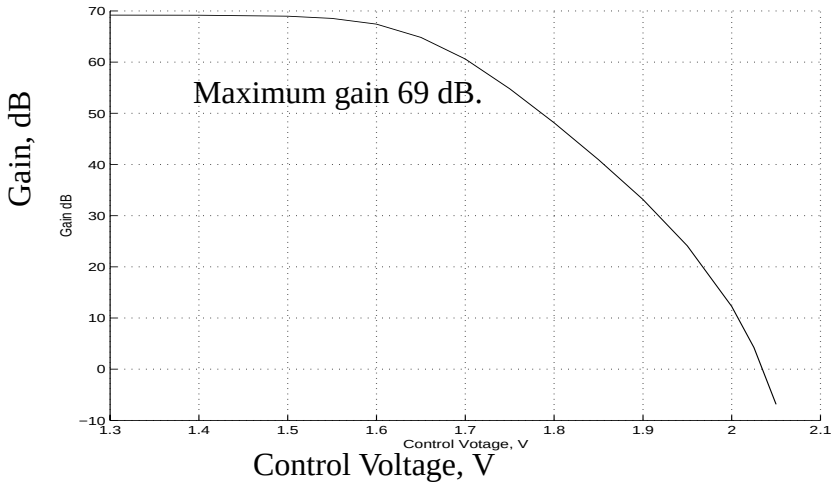


Fig. 7.5 Simulated VGA Gain-Control Range

7.3 Offset Cancellation Techniques

7.3.1 Problem of Offset Voltage and Existing Offset Cancellation Techniques

High input-referred offset voltage is one the most important drawbacks of MOS analog circuits when compared to their BJT and BiCMOS counterparts. Typically the offset voltage can be as high as 20 mV, which can easily saturate the amplifier output stage when the DC gain is high enough. This problem is even worse in low-supply applications.

Traditional offset cancellation techniques [61][62] usually utilize sampling circuit and memory components to sample, store and cancel the offset voltage. As shown in Fig. 7.6, the offset voltage is sensed and stored in a capacitor during the calibration period, and feeding it back to signal after the calibration.The main problem with these methods is that they require a clock signal and a calibration period. A clock signal would cause problems with clock feedthrough and charge injection, which make cancellation inaccurate. A calibration period would reduce the overall speed and prevent the amplifier to operate continuously.

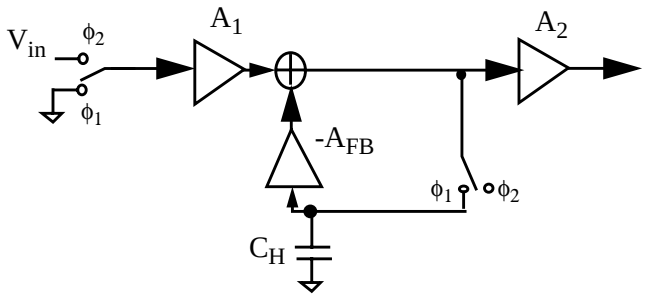


Fig. 7.6 Existing Offset Cancellation [61]

To achieve automatic offset cancellation, some techniques [63][64] also use some logic circuits to control the amplifier and the tuning circuitry. However the controlling and tuning circuitry will introduce large noise, consume more power and occupy more chip area. They still have the problems of clock feedthrough and charge injection and cannot operate continuously.

7.3.2 Proposed Offset Cancellation Technique

As described earlier, the proposed VGA consists of three identical cells. Each cell has its own offset voltage, which is typically as large as 20 mV. Without offset cancellation, each cell would have almost same gain of 30 dB at DC. Therefore, the offset voltage in each cell would be amplified to about 0.632 V, which would be large enough to saturate the cell. As a result, each cell should have its own offset cancellation circuitry.

The VGA is used to amplify the signal at an IF frequency 70 MHz while the gain at DC is not useful. Considering this characteristic, a negative feedback with a lowpass filter is designed to cancel the DC offset in each VGA cell. As shown in Fig. 7.7, Part 2, M_{15} and M_{16} are working in triode region as two resistors. These two resistors together with C_1 and C_2 form two low-pass filters to block the IF signal in the feedback path to guarantee that the IF gain is not affected. M_{13} and M_{14} are used to convert the voltage feedback signal to current, which is added to the input signal in current domain at Nodes 2 and 3. The VGA and the offset cancellation circuitry use two independent bias sources to avoid the possible current allocation problem caused in the presence of mismatch between the common mode voltages of the input and the feedback signals.

Because the unit-gain frequency of the VGA is much larger than the IF (70 MHz), the VGA without offset cancellation can be simply modelled by a single-pole low-pass function *A(jω)*.

$$A(j\omega) = \frac{g_{ma}R_L}{1 + \dfrac{j\omega}{\omega_{-3dB,\,VGA}}} \tag{7.5}$$

The feedback path can also modelled by a low-pass function *B(jω)* with DC gain of one.

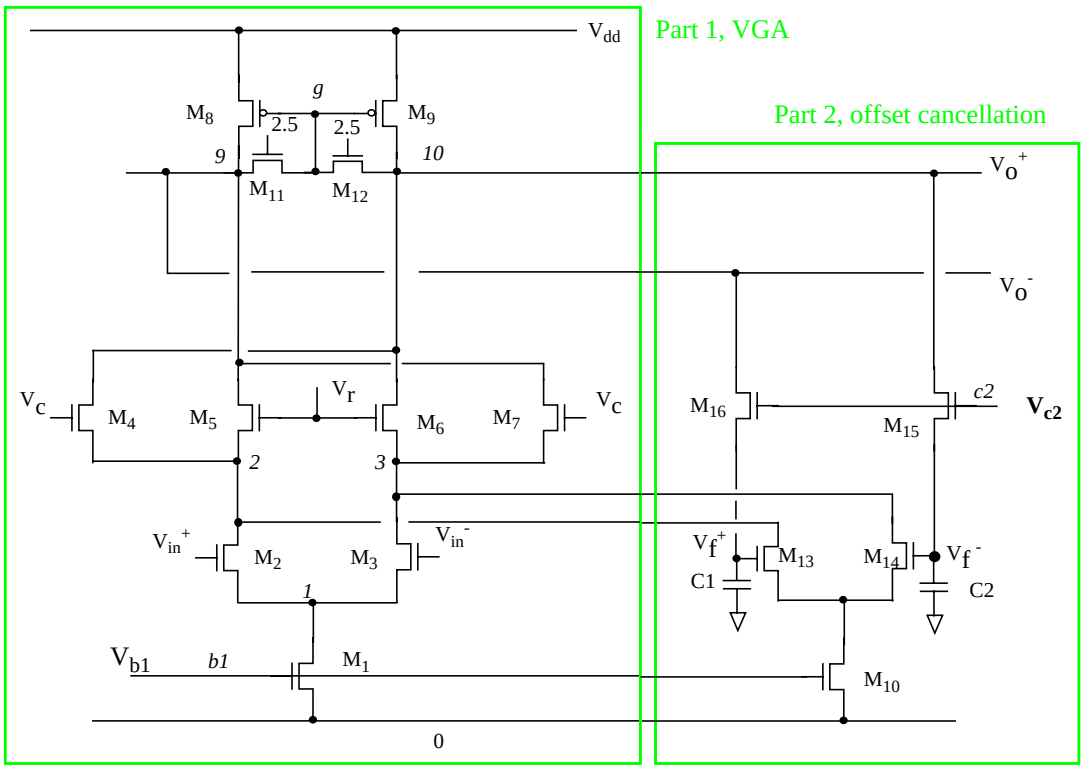


Fig. 7.7 Proposed VGA with offset cancellation

$$B(j\omega) = \frac{1}{1 + \dfrac{j\omega}{\omega_{-3dB,\,f}}} \tag{7.6}$$

where $\omega_{-3dB,VGA}$ and $\omega_{-3dB,f}$ are the -3 dB frequencies of the main amplifier and the feedback path, respectively, and g_{ma} is transconductance of M_2 and M_3. With the offset cancellation, the close-loop overall transfer function of the VGA can be derived to be

$$H(\omega) = \frac{g_{ma}R_L}{1 + g_{mb}R_L} \cdot \frac{1 + \dfrac{j\omega}{\omega_{-3dB,\,f}}}{1 + \dfrac{j\omega}{\omega_o Q} + \dfrac{(j\omega)^2}{\omega_o^2}} \tag{7.7}$$

$$\omega_o = \sqrt{(1 + g_{mb}R_L) \cdot \omega_{-3dB,\,VGA}\omega_{-3dB,\,f}} \approx \sqrt{\omega_T \omega_{-3dB,\,f}} \tag{7.8}$$

$$Q = \frac{\sqrt{(1 + g_{mb}R_L) \cdot \omega_{-3dB,\,VGA}\omega_{-3dB,\,f}}}{\omega_{-3dB,\,VGA} + \omega_{-3dB,\,f}} \tag{7.9}$$

where ω_T is the unit-gain frequency of the main amplifier, and g_{mb} is transconductance of M_{13} and M_{14}. It is clear from Eq. 7.7 that the closed-loop VGA is a band-pass system with a center frequency at ω_o.

From Eq. 7.8, ω_T should be as high possible to achieve high gain at IF. However with a given power and current, ω_T is limited to around 700 MHz by the loading and parasitic capacitance at the output node. To amplify the signal at IF frequency without amplifying the interference at other frequencies, ω_o should be set to the same frequency as IF, in which case the -3 dB frequency of the feedback $\omega_{-3dB,f}$ becomes

$$\omega_{-3\text{dB, f}} = \omega_{\text{IF}}^2 / \omega_{\text{T}} \tag{7.10}$$

which is about 7 MHz in this design application.

Because the offset voltage is a DC signal, the output-referred offset voltage can be minimized by minimizing the DC gain, which is given from Eq. 7.7 as

$$H(j\omega = 0) = \frac{g_{ma}R_L}{1 + g_{mb}R_L} \tag{7.11}$$

To trade off among power, area, noise and output offset, g_{mb} is set to be the same as g_{ma}. As such, the closed-loop DC gain is approximately 0 dB, and the offset voltage would not be amplified. As a consequence, the VGA can tolerate more process mismatch and a larger input offset voltage while the IF gain and the linearity remain unaffected. The effective input-referred offset voltage is reduced by the IF gain. If g_{mb} is larger, the DC gain would be smaller and the offset voltage would be reduced further, but it would cost more power and more area, and the input-referred noise due to M_{13} and M_{14} would also be larger.

Since the DC gain is around 0 dB, low-frequency noise will not be amplified either, and the VGA can achieve a better noise performance at low frequencies. Because the offset

cancellation is automatic and continuous, any variation of offset voltage as a function of time and temperature will be effectively and instantaneously compensated. Therefore, this offset cancellation method is also temperature stable.

The simulated frequency response of the VGA with offset cancellation is shown Fig. 7.8. The gain at low frequency is suppressed, but at 70MHz, the gain is improved to 70 dB, which is 63 dB in the original VGA without offset cancellation.

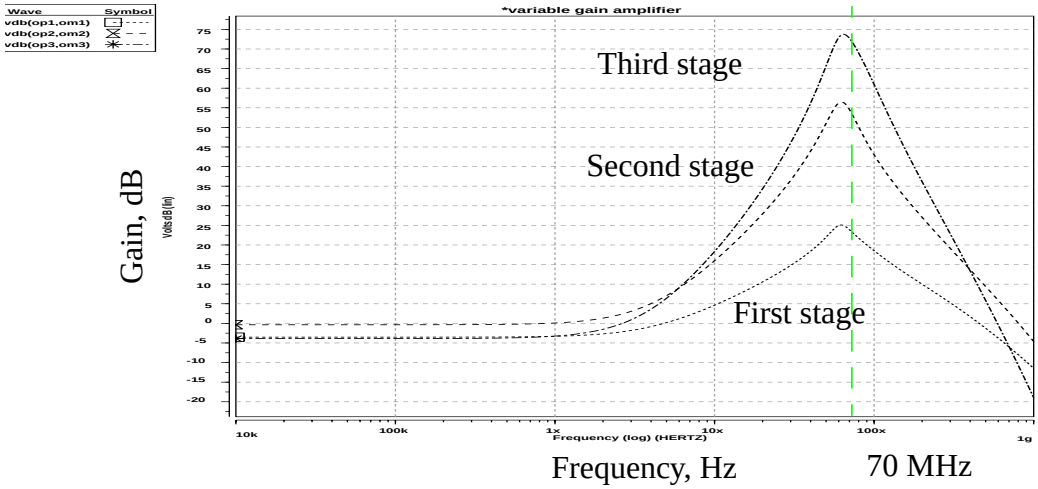


Fig. 7.8 The Simulated Frequency Response of The VGA with Offset Cancellation

7.4 NF and IIP3 as a Function of Gain Setting Among Three stages

The VGA consists of a cascade of 3 identical stages. Each stage has an independent gain control. Different gain distributions give different NF and IIP3 of the whole VGA.

Assume A_1, A_2, A_3 are gain of first, second, third stage. F_1, F_2, F_3 are noise factors. A_{IP31}, A_{IP32}, A_{IP33} are input referred interception points. The noise factor of the whole VGA, F, is then:

$$F = F_1 + \frac{F_2 - 1}{A^2_1} + \frac{F_3 - 1}{A^2_1 A^2_2} \quad . \tag{7.12}$$

And the IIP3 of the VGA is:

$$\frac{1}{A^2_{IP3}} = \frac{1}{A^2_{IP31}} + \frac{A^2_1}{A^2_{IP32}} + \frac{A^2_1 A^2_2}{A^2_{IP33}} \tag{7.13}$$

When all stages are set to maximum gain, the noise figure of the whole VGA is minimized, however the IP3 is degraded to minimum value as well. For a large input signal, the total gain of the VGA will be decreased to a smaller value. Since the signal power is large, the noise contribution from the VGA is not important any more, the gain of all stages can decrease at the same time. The IIP3 of the whole amplifier can also be improved when the gain in the first and second stage decreases.

7.5 RSSI in the AGC Loop

A received-signal-strength-indicator (RSSI) is used in the AGC loop to measure the amplitude of the signal at VGA output. The input to the RSSI is a sine wave, the output of the RSSI is a DC signal indicating the amplitude of the input signal. In the proposed AGC, an open-loop current-mode rectification structure [65] is used as the RSSI. The conceptual circuit diagram is shown in Fig. 7.9 (a). When the input current I_{in} flows into or out from the rectifier, it switches devices M_{rp} and M_{rn} ON and OFF respectively. A half-wave rectified current I_{out} is therefore established at output. A full-wave rectification can be obtained by utilizing two identical paths in parallel, which are driven by a pair of differential input currents.

Two additional circuit techniques, namely, nMOS substitute and pre-bias techniques, are used in order to obtain a better precision during fast switching. The former replaces the pMOS device M_{rp} of current sink to ground with an nMOS diode. This modification improves the speed performance due to less parasitic capacitance of the nMOS device. The other technique used is the pre-bias method. The voltage V_{bs} biases two switches at the nearly-on condition. Consequently, only a small amount of change of input current makes the switch

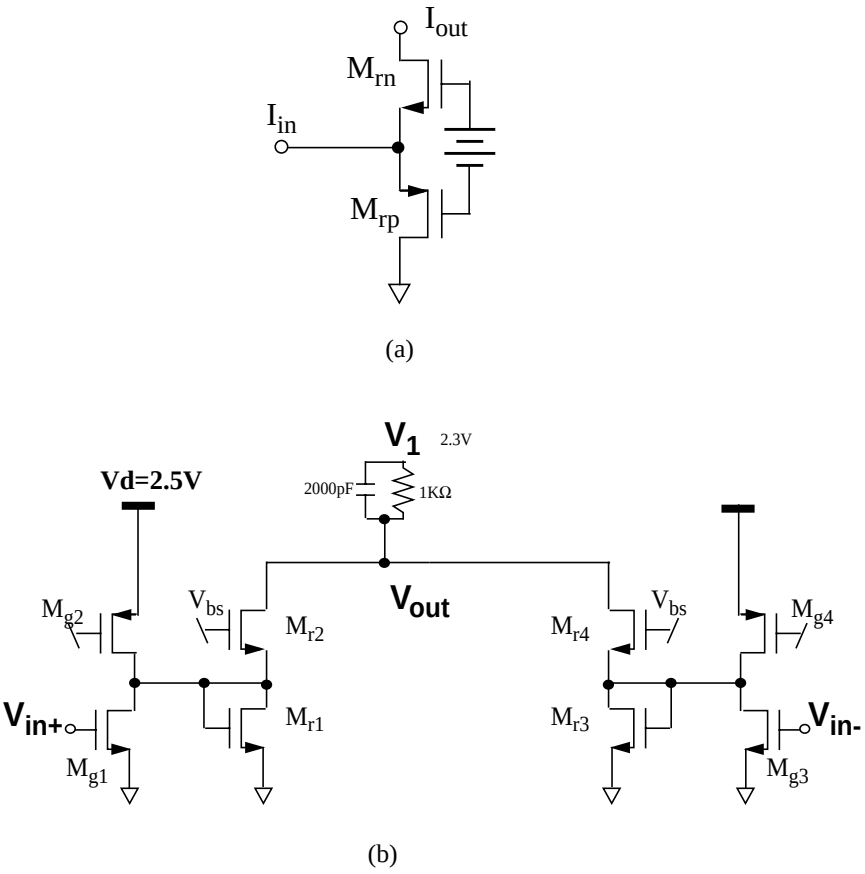


Fig. 7.9 RSSI in the AGC Loop

fully ON or OFF. This reduces the error caused by extra current when one switch is ON while the other is not completely OFF, which can be significant for high-speed under low-voltage operation.

The final circuit of RSSI is shown in Fig. 7.9 (b). Devices M_{g1} - M_{g4} form transconductance stage that convert the input voltage to current. The devices M_{r1} - M_{r4} form a current mode full-wave-rectifier (FWR). The output current is summed and filtered by an R-C low pass filter at cut-off frequency 700 kHz. A larger bandwidth helps to suppress more fast variation in the signal power, but it may cause stability problem.

The AGC Loop is shown in Fig. 7.10. The output signal from the last stage is fed into the RSSI and the output of the RSSI is used to control the gain of each stage at the same time.

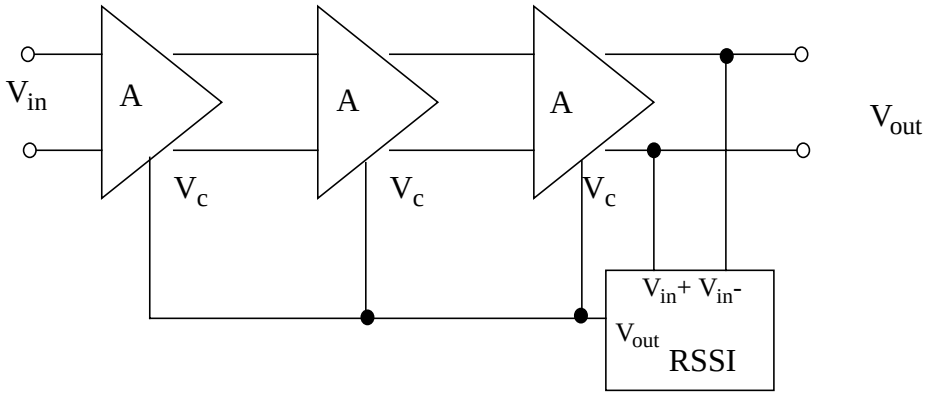


Fig. 7.10 Block Diagram of the AGC Loop

The transient simulation of the AGC loop is shown in Fig. 7.11. With the AGC loop, the variation of the output signal amplitude is reduced by 12 dB and a relatively constant signal amplitude is achieved. The settling time of the AGC loop is about 3µs. It consumes 4mA current from a 2.5 V supply.

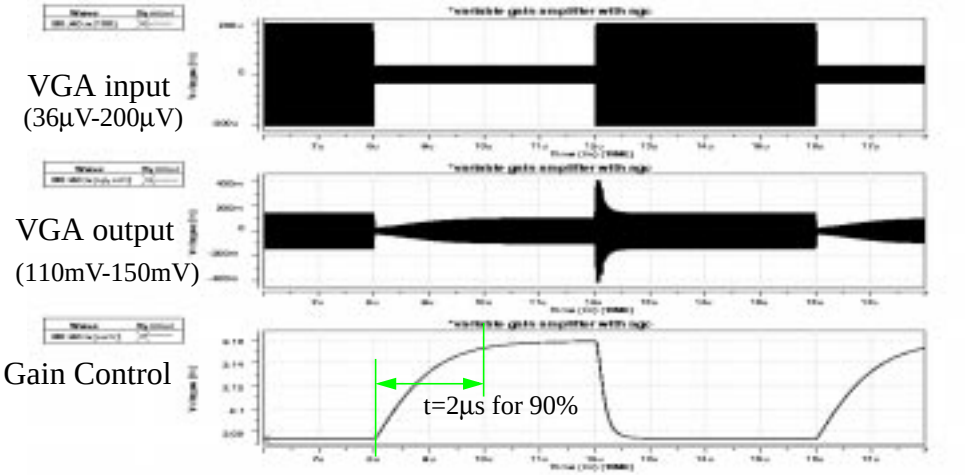


Fig. 7.11 Transient Simulation of the AGC Loop

The transistors, capacitors and bias voltages of the VGA and the RSSI are summarized in Table 7.1 and Table 7.2, respectively.

Table 7.1 Components in Each Stage of the VGA

Transistor	Size	Transistor	Size
M1	20*14.4μ/0.9μ	M11	1.2μ/8.1μ
M2	16x8.1μ/0.6μ	M12	1.2μ/8.1μ
M3	16x8.1μ/0.6μ	M13	16x8.1μ/0.6μ
M4	8x7.2μ/0.9μ	M14	16x8.1μ/0.6μ
M5	8x7.2μ/0.9μ	M15	2.1μ/3.6μ
M6	8x7.2μ/0.9μ	M16	2.1μ/3.6μ
M7	8x7.2μ/0.9μ	C1	1 pF
M8	16x13.5μ/0.9μ	C2	1 pF
M9	16x13.5μ/0.9μ	Vdd	2.5 V
M10	20*14.4μ/0.9μ	Ivdd	2 mA

Table 7.2 Components in RSSI

Components	**Value**
Mg1, Mg3	5x21.9μ/1.2μ
Mg2, Mg4	5x75μ/1.2μ
Mr1, Mr3	5x21.9μ/1.2μ
Mr2, Mr4	5x21.9μ/1.2μ
C	2000 pF
R	1kΩ
Total Current	4.4 mA, Vdd=2.5V

7.6 Summary

The variable gain amplifier used to amplify the signal at the 70-MHz IF frequency and to improve the signal dynamic range has been discussed. To prevent the VGA from being saturated by the offset voltage, a continuous-time automatic offset cancellation technique with a low-pass filter in the feedback path has been included. The gain varying of the VGA is realized by tuning the ratio of cross coupling which results in a stable common mode output voltage independent of the gain varying. The simulation results show that the VGA has a continuous tuning range of 69 dB for the gain. Implemented in a 0.5-μm CMOS process, the

VGA consumes a power of 15 mW from a 2.5-V supply. A simple RSSI circuit have also been implemented to demonstrate the AGC function.

Chapter 8

OTHER BUILDING BLOCKS

The proposed transceiver consists of many building blocks. Some of them, the image-rejection mixers, the phase shifters, the IF filter, the ADC and the power amplifier, are briefly described in this chapter. Readers can refer to the corresponding references if they are interested in more details for those building blocks.

8.1 Image-Rejection Mixers

The image-rejection mixers used in the receiver consists of two identical double-balanced mixers to achieve I-Q downconversion. The design of each mixer, as shown in Fig. 8.1, is similar to that of the Gilbert cell but uses two source-followers as current modulators rather than common-source input stages in order to support low-voltage operation and to improve the linearity [53]. In order to maximize the conversion gain with a fixed LO amplitude, the transistors in the cross-coupling pair are biased at the edge of the saturation region.

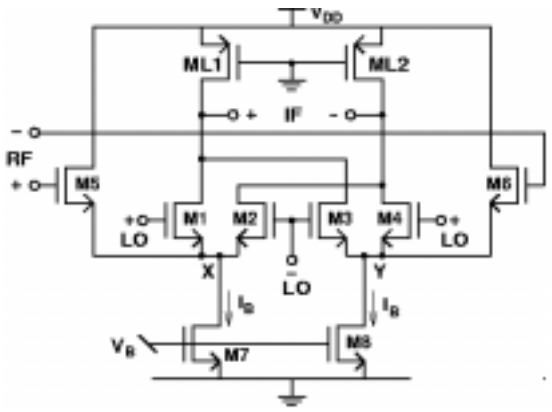


Fig. 8.1 Circuit schematic of the mixer

Each mixer consumes a current of 2 mA from a 2-V single supply. It can achieve a conversion gain of -2 dB with an IIP3 of 7 dBm and a NF of 27 dB.

8.2 The Phase Shifters

Four simple R-C phase shifters are used to achieve 45^o and -45^o phase shifting, as shown in Eq. (8.2).

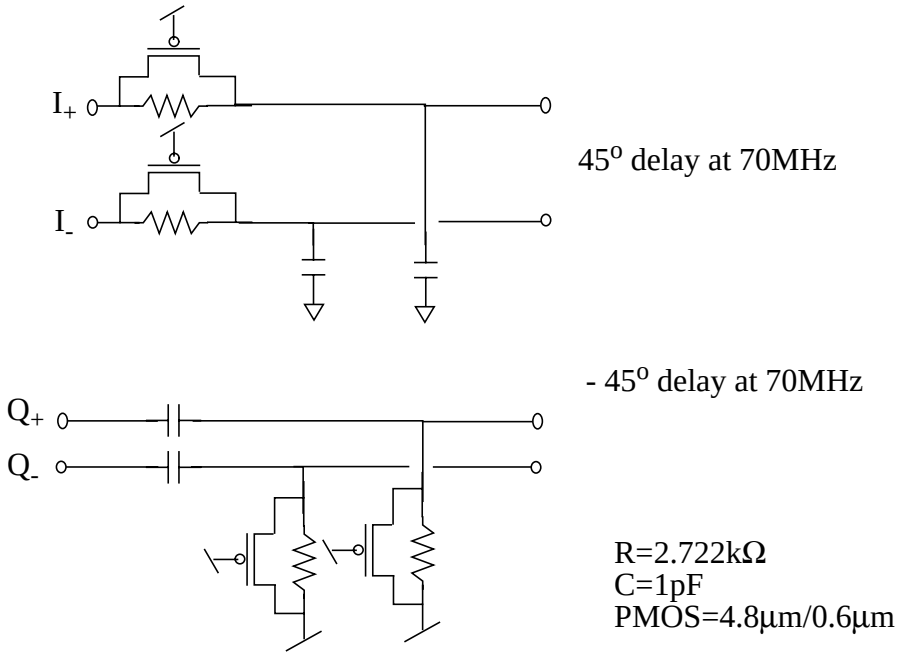


Fig. 8.2 The Phase Shifters

Before the phase shifter, the signals in the I channel are:

$$A_I=-A_{RF}\sin(\omega_{RF}-\omega_{LO})t + A_{im}\sin(\omega_{LO}-\omega_{im})t \tag{8.1}$$

and the signals in the Q channel are:

$$A_Q=A_{RF}\cos(\omega_{RF}-\omega_{LO})t + A_{im}\cos(\omega_{LO}-\omega_{im})t. \tag{8.2}$$

where the IF signal is $A_{RF}\cos(\omega_{RF}-\omega_{LO})t$ and the image signal is $A_{im}\cos(\omega_{LO}-\omega_{im})t$. After the 45^o and -45^o phase shifters, the signals in the I channel are:

$$A_I=-A_{RF}\sin[(\omega_{RF}-\omega_{LO})t - 45]+A_{im}\sin[(\omega_{LO}-\omega_{im})t - 45]$$

$$=A_{RF}\cos[(\omega_{RF}-\omega_{LO})t+45] - A_{im}\cos[(\omega_{LO}-\omega_{im})t +45], \quad (8.3)$$

and the signals in the Q channel are:

$$A_Q=A_{RF}[\cos(\omega_{RF}-\omega_{LO})t+45] + A_{im}\cos[(\omega_{LO}-\omega_{im})t+45]. \quad (8.4)$$

From Eq. (8.3) and Eq. (8.4), the IF signals in the I and Q channels are in the same phase and the image signals in the I and Q channels are 180^o out of phase. After adding the signals from the I and Q channels together, the image signal is cancelled by itself and only the IF signal is left.

The phase shifters are realized by using simple R-C and C-R networks, as shown Fig. 8.2. Since the output of each channel is a differential signal, two R-C networks are used for each channel. Each resistor is realized by a resistor in parallel with a P-MOS transistor working in the linear region to achieve variable resistance and compensate the process variations.

8.3 70-MHz High-Q Channel-Selection IF Filter

The 70-MHz channel-selection IF filter is constructed with three G_m-C biquads in cascade as shown in Fig. 8.3 [54]. Optimization of the noise, linearity, and power consumption of the whole filter is done, not only by designing highly-linearized G_m cells for the gyrators, but also by distributing proper gain and power consumption among the three stages.

Active biasing is used to linearize the G_m cells as shown in Fig. 8.3. Differential active loads with polysilicon resistors as feedback are employed to achieve high output impedance with good linearity and high output swing. Q-compensation circuits using negative-G_m cells are connected in parallel at the outputs to boost up the output impedance to achieve high and

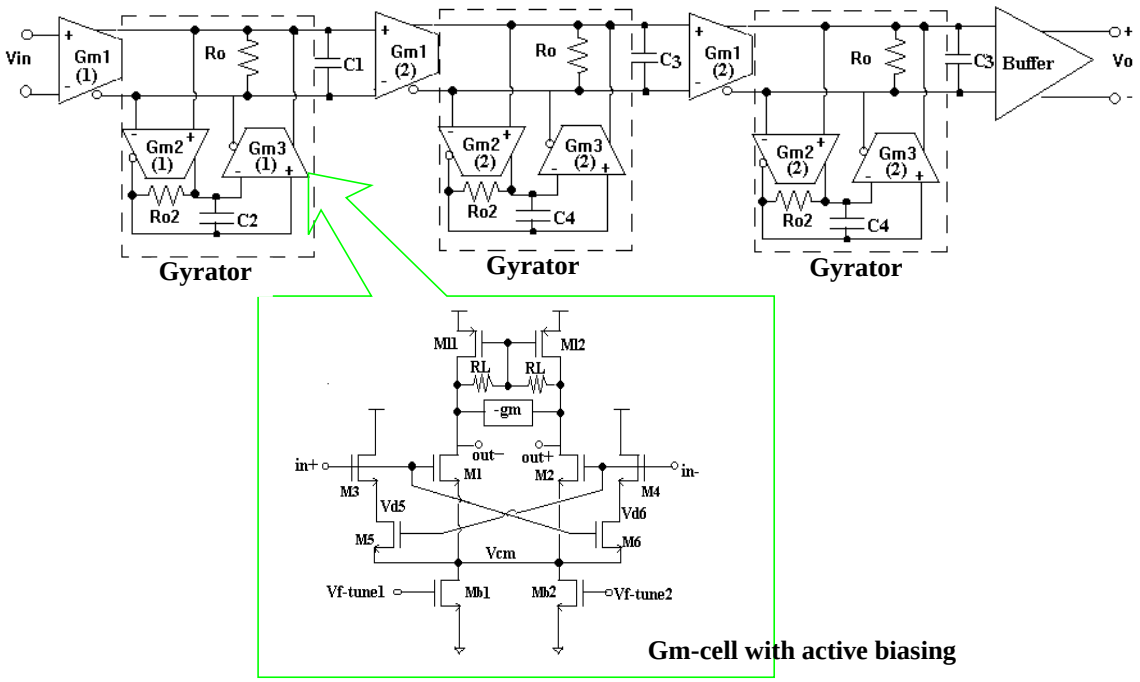


Fig. 8.3 Circuit implementation of the channel-selection IF filter

tunable Q. The design of these negative-G_m cells is similar to that of the G_m cells for the gyrators except that the outputs are cross-coupled back to the inputs. Because interferers are suppressed by the filtering effect of the first stage, the linearity requirement of the last two stages is more relaxed. As a result, the gains of the three stages are purposely set to be 14dB, 3dB, and 3dB, respectively. For the same reason, approximately 50% of the power consumption is allocated to the first stage, and the size of the gyrator in the first stage is designed to be double of that in the second and third stages.

The total input-referred noise power of a biquad is mainly contributed by the noise sources in the gyrators as shown in Fig. 8.4 and can be estimated to be:

$$V_n^2/\text{Hz} = \frac{8\gamma KTg_{mg}}{3G_{mi}}\left(\frac{Q}{G_{mg}}\right)^2 \tag{8.5}$$

where g_{mg} is the transconductance of the input transistors of the G_{mg} cells. From the equation, the biquad noise strongly depends on its quality factor Q. For a given Q, the noise can be

reduced by either increasing G_{mg}, which would burn more power, or increasing G_{mi}, which would degrade the linearity.

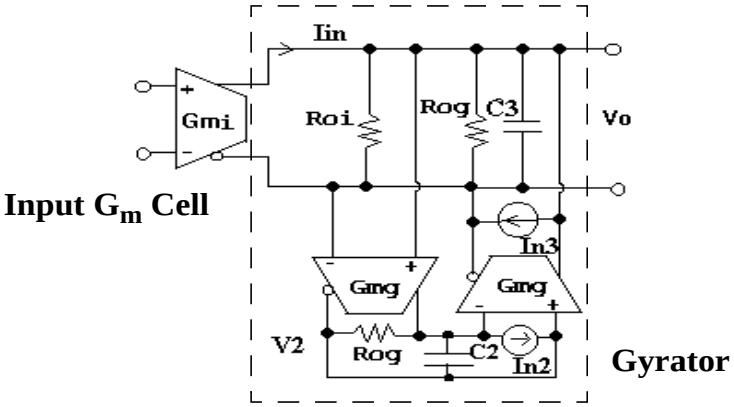


Fig. 8.4 Noise sources in the biquad

On the other hand, the distortion of the biquad at the center frequency is given by:

$$\left.\frac{\Delta H(s)}{H(s)}\right|_{s = j\omega_0} \approx \frac{\Delta G_{mi}}{G_{mi}} + \frac{2\Delta G_{mg}}{1/(R_{oi} \parallel R_{og}) + 1/R_{og}} + \frac{\Delta G_{m\text{-}}}{G_{m\text{-}}} \tag{8.6}$$

where $G_{m\text{-}}$ is the transconductance of the Q-compensation circuit and R_o's are output impedance of the G_m cells. In high-Q filters, R_o's are large and, therefore, the overall linearity is dominated by the linearity of G_{mg} cells, which could not be improved without sacrificing either noise performance or power consumption.

In our design, because the Q value is extremely high (as high as 350) and the power consumption is limited to less than 100 mW with a 2.5-V supply, the filter inevitably suffers from limited performance in terms of noise and linearity, which are 43 dB and -9 dBm, respectively.

8.4 70-MHz Band-Pass Sigma-Delta ADC

A second-order 70-MHz continuous-time band-pass sigma-delta modulator [55] is used as the analog-to-digital converter, as shown in Fig. 8.5. The transfer function of the

continuous-time loop-filter is derived using the impulse-invariant transformation, and the filter is implemented using a second-order G_m-C filter. The G_m cells, also shown in Fig. 8.5, are implemented using triode-region input transistors to maximize their linearity [55]. A latched-type comparator and a true-single-phase-clock D flip-flop are used to realize the quantizer. The sampling frequency is 280 MHz, which is four times of the input IF frequency, and an inverter chain is embedded to achieve a total loop delay of one sampling period to maximize the signal-to-noise performance.

According to the HSPICE simulation, the ADC achieves an SNDR of 50 dB when the input signal is a 70.05 MHz 50 mV amplitude sinusoid. The ADC consumes 14 mA current from a 2.5-V supply.

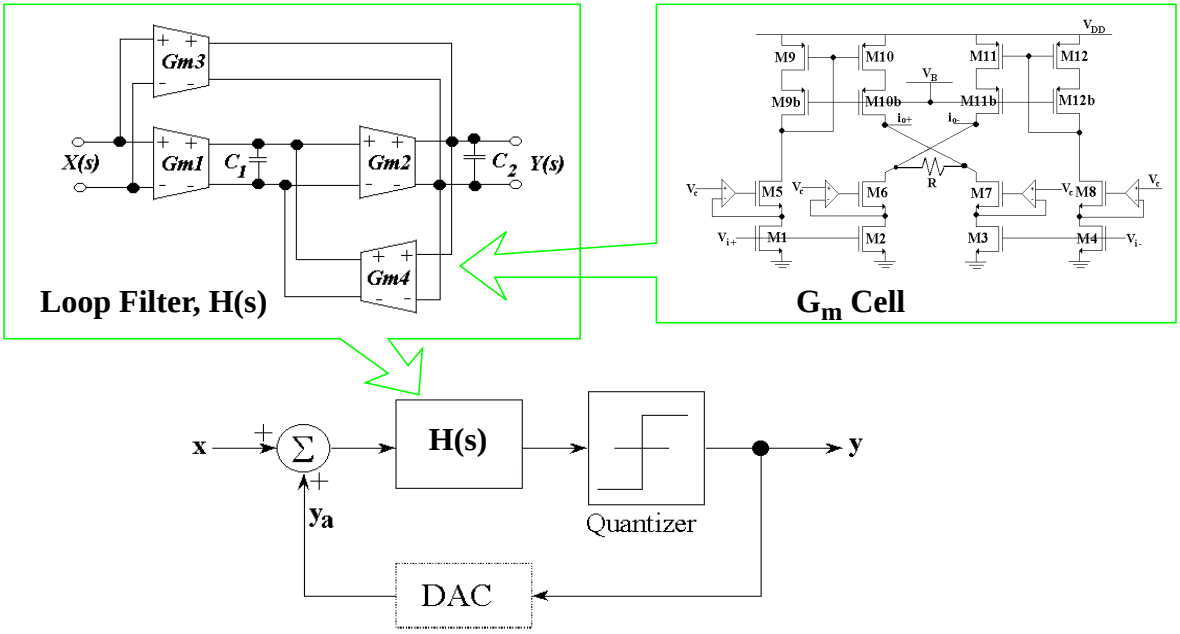


Fig. 8.5 Block diagram of the bandpass sigma-delta analog-to-digital converter

8.5 Class-E Power Amplifier

A power amplifier (PA) is used to amplify the RF signal and drive the antenna. Because a constant envelope modulation is used in the transmitter, a class-E power amplifier [56], which is a non-linear PA, can be used to improve the power added efficiency (PAE), as

shown in Fig. 8.6. A class-E power amplifier with ideal components can achieve a theoretical PAE of 100%. However, in reality, the turn-on resistor of the switch, M1, and the loss in the on-chip inductors limit the PAE.

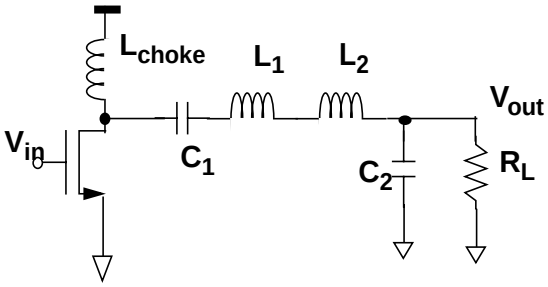


Fig. 8.6 Class-E Power Amplifier

A buffer, including a source-coupled pair and five inverters in cascade, are used to drive the PA, as shown in Fig. 8.7. The five inverters are used to drive the switch of the PA. The source-coupled pair is used to isolate the loading effect from the inverter to the VCO output. The bias of the source-couple pair can be turned on or off to enable or disable the PA when the transceiver is in transmitting mode or receiving mode, respectively.

The PA used in the proposed transceiver obtains an output power of 100mW with a PAE of 20%.

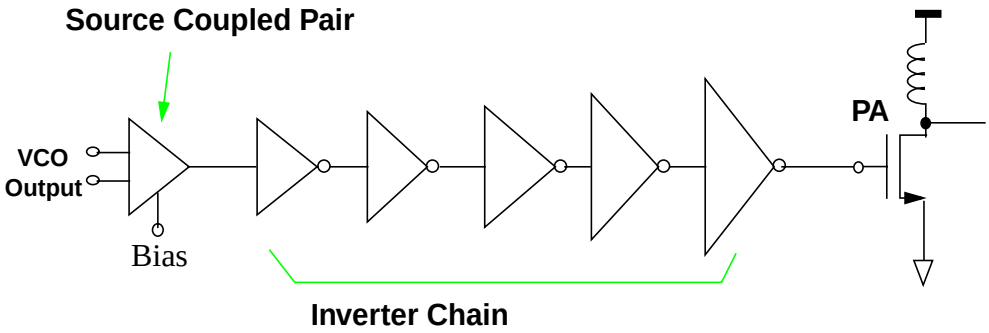


Fig. 8.7 Buffer driving the PA

Chapter 9

EFFECT OF IF ON SYTEM PERFORMANCE

In Chapter 3, the architecture of a receiver has been discussed. The architecture design is related to the choice of IF frequency. Different values of IF frequencies give different tradeoffs among image rejection, Q of IF filter, DC offset, and noise performance. In this chapter, the effect of the IF frequency on the image rejection, the noise figure and the power consumption of the receiver are discussed in more details.

9.1 Effect of IF on Image Rejection

As discussed in the Chapter 3, the amount of image rejection depends on the choice of the IF frequency. If a simple n^{th}-order bandpass filter is used as the image-rejection filter, the roll-off of the frequency response is n×10 dB per decade. When $\omega >> \omega_o$, it can be written as:

$$20\log(|A(j\omega)|) = 20 \times \log\left(A_o \Big/ \left(\frac{\omega - \omega_o}{B_{rec}}\right)^{\frac{n}{2}}\right) \tag{9.1}$$

The frequency offset of the image signal to the center frequency is $2\omega_{IF}$. The amount of the image rejection achieved by this filter, IR, equals the difference between the gain at ω_o and the gain at ω_o-$2\omega_{IF}$. In log-scale, it is:

$$\begin{aligned} IR &= 20\log(A_o) - 20\times\log\left(A_o \Big/ \left(\frac{2\omega_{IF}}{B_{rec}}\right)^{\frac{n}{2}}\right) \\ &\approx 10\times\log\left(\left(\frac{2\omega_{IF}}{B_{rec}}\right)^{n}\right) \\ &= n\times 3 + n\times 10\log\left(\frac{\omega_{IF}}{B_{rec}}\right) \end{aligned} \tag{9.2}$$

where B_{rec} is the receiving band.

For a system with a image signal power of P_{im}, and a minimum required signal-to-noise ratio of SNR_{out}, the best achievable sensitivity of a receiver due to the image signal, $P_{sen,im,}$ is

$$P_{sen,im} = P_{im} - IR_{tot} + SNR_{out} = P_{im} + SNR_{out} - n\times 3 + n\times 10\log(IF/B_{rec}) + IR_{other} \tag{9.3}$$

According to this equation, higher order, n, of the image-rejection filter or higher IF frequency is required to achieve a better sensitivity, when the sensitivity is not limited by the noise and linearity performance.

In the proposed receiver, the receiving band is B_{rec}=25 MHz and the IF frequency is 70 MHz, the image rejection is:

$$IR = n\times 3 + n\times 10\log\left(\frac{70}{25}\right) = 3n + 4.5n = 7.5n. \tag{9.4}$$

Assume the image-rejection mixers can only achieve an image rejection of 30 dB, the LNA with two parallel resonant tank is a 4^{th}-order bandpass filter is used, the image rejection achieved is 30+7.5×4=60 dB. However, with the help of Notch filter, the image rejection in the LNA can be improved to 50 dB. Therefore, the total image rejection is IR_{tot}=30+50=80 dB. For the system with an image signal power of -23 dBm, and a minimum SNR_{out} of 9dB, the best sensitivity is $P_{sen,im}$ = -23 - 80 + 9 = - 94 dBm.

9.2 Effect of IF on Noise Figure

Different IF frequencies give a different NF of the whole system when the NF of the system is limited by the IF circuits, especially the IF filter.

The IF frequency is the center of the IF channel selection filter (IF FIlter). The Q of the filter is defined by center frequency divided channel bandwidth. The channel bandwidth of the filter is determined by the application, which is 200kHz in this application. Therefore, the Q of the filter is directly proportional to the IF frequency. When the IF is 70 MHz, the Q can be as high as 350.

The channel selection filter is implemented with 3 Gm-C filter in cascade, as discussed in Chapter 8. Each of them has a center frequency ω_o.

$$\omega_o = \sqrt{\frac{g_{m2}g_{m2}}{C_1C_2}} \tag{9.5}$$

$$\text{and} \quad Q = \frac{\omega_o}{B_{ch}} = \omega_o C_1 R_o = g_{m2,3} R_o \tag{9.6}$$

The NF of the filter is related to Q, [68]

$$NF = 10 \times \log\left(1 + \frac{2\gamma Q}{75 A g_{m1}}\right) = 10 \times \log\left(1 + \frac{2\gamma}{75 A g_{m1}} \times \frac{\omega_{IF}}{B_{ch}}\right) \tag{9.7}$$

where A is the gain of the filter. In the proposed IF filter, A=10, g_{m1}=100μA/V, γ=2 and B_{ch}=200kHz, B_{ch}=200kHz, ω_{IF}=70MHz, and

$$NF = 10 \times \log\left(1 + \frac{2 \times 2}{75 \times 10 \times 10^{-4}} \times \frac{70}{0.2}\right) = 43\text{dB}$$

The best achievable sensitivity of the receiver due to the noise of the IF filter, $P_{sen,n}$ is

$$P_{sen,n} = P_{ns} + 10\log(B_{ch}) + NF_{filter} - A_{RF} + SNR_{out}. \tag{9.8}$$

where P_{ns} =-174 dBm/Hz is the source noise power of 50Ω resistor in 1-Hz channel bandwidth, B_{ch} is the channel bandwidth, A_{RF} is the total gain before the IF filter, and SNR_{out} is the minimum required SNR at the receiver output.

In the prosed receiver, for an IF frequency of 70 MHz, the noise figure of the IF filter is 43 dB. Therefore the sensitivity is:

$$P_{sen,n}=-174 +10\log(200k) + 43 - 20 + 9 = 89 \text{ dBm}. \tag{9.9}$$

To achieve a better sensitivity, it is necessary to have a lower IF frequency and a smaller NF in the IF filter. However, lower IF frequency will degrade the image rejection of the receiver.

9.3 Effect of IF on Linearity

According to the experimental results, the linearity of the system is also limited by that of the IF filter. The signal distortion is caused by the nonlinearity of the filter, which can be expressed as the variation of the frequency response, ΔH(s), as a function of variations of the transconductances of all Gm-cells [54][68]:

$$\left.\frac{\Delta H(s)}{H(s)}\right|_{s = j\omega_0} \approx \frac{\Delta G_{mi}}{G_{mi}} + \frac{2\Delta G_{m2}}{1/R_o + 1/R_{o2}} + \frac{\Delta G_{m-}}{G_{m-}} \tag{9.10}$$

where G_{mi} is the transconductance of the input devices, G_{m2} is the transconductance of the devices in the biquads, G_{m-} is the transconductance of the Q-compensation circuit, R_{o2} is output impedance of the G_m cells and R_o is the overall output impedance of the biquad. Because of the nonlinearity of the circuits, when the signal amplitude increases, the transconductances decrease and the frequency response of the filter decreases. As a result, the signal waveform is distorted.

For high-IF receivers, the Q of the IF filter is very high, and R_o's are large. Therefore, the overall nonlinearity is dominated by the nonlinearity of $G_{m2,3}$ cells. In this case, the Eq. (9.10) can be simplified as:

$$\left.\frac{\Delta H(s)}{H(s)}\right|_{s=j\omega_0} \approx 2\Delta G_{m2} Q / G_{m2} = 2\Delta G_{m2} \frac{\omega_{IF}}{B_{ch}} \frac{1}{G_{m2}} \tag{9.11}$$

To reduce the signal distortion and improve the overall linearity of the filter, smaller IF frequency is more desirable.

9.4 Effect of IF on Power Consumption

9.4.1 Power Consumption of the IF filter

The Q of the IF filter is proportional to the IF frequency,

$$Q = \frac{\omega_{IF}}{B_{ch}} \tag{9.12}$$

Substitute Eq. (9.12) into Eq. (9.5) and Eq. (9.6),

$$\omega_{IF} = \sqrt{\frac{g_{m2} g_{m3}}{C_1 C_2}} \tag{9.13}$$

$$\frac{\omega_{IF}}{B_{ch}} = g_{m2,3} R_o \tag{9.14}$$

Assume V_{gs}-V_t of each transistor remains unchanged to keep the same linearity, g_m of each transistor is proportional to the bias current.

$$g_{m2} = \frac{2I_{B2}}{V_{gs} - V_t} = \frac{2I_{B2}}{\Delta V_{gs}} \tag{9.15}$$

$$g_{m3} = \frac{2I_{B3}}{V_{gs} - V_t} = \frac{2I_{B3}}{\Delta V_{gs}} \tag{9.16}$$

Substitute Eq. (9.15) and Eq. (9.16) into Eq. (9.13) and Eq. (9.14),

$$\omega_{IF} = \sqrt{\frac{1}{C_1 C_2}} \times \frac{2I_{B2}}{\Delta V_{gs}} \tag{9.17}$$

$$\frac{\omega_{IF}}{B_{ch}} = \frac{2I_{B2,3}}{\Delta V_{gs}} R_o \tag{9.18}$$

Therefore, the bias current in g_{m2} and g_{m3} is:

$$I_{B2,3} = \frac{1}{2R_o} \Delta V_{gs} \frac{\omega_{IF}}{B_{ch}} \tag{9.19}$$

Assume the gain of the filter is kept same and the same capacitors are used. From Eq. (9.19), the power consumption of g_{m2} and g_{m3} is directly proportional to IF frequency.

9.4.2 Power Consumption of the VGA

Assume the capacitance loading is dominant in the variable gain amplifier (VGA), which is true in this design, the gain of the VGA can be expressed as

$$A_{IF} = \left| g_m \frac{R_o}{1 + j\omega_{IF} C_L R_o} \right| \approx \frac{g_m}{\omega_{IF} C_L} \tag{9.20}$$

where C_L is the capacitance loading of each stage. Assume $\Delta V_{gs}=V_{gs}-V_t$ remains unchanged to maintain certain linearity, g_m is proportional to the bias current.

$$g_m = \frac{2I_B}{V_{gs} - V_t} = \frac{2I_B}{\Delta V_{gs}} \tag{9.21}$$

Substitute Eq. (9.21) into Eq. (9.20),

$$A_{IF} = \frac{1}{\omega_{IF} C_L} \times \frac{2I_B}{\Delta V_{gs}} \tag{9.22}$$

From Eq. (9.22), to maintain the same gain at the IF frequency, ω_{IF}, the bias current of the input transistors are proportional to the IF frequency. Assume that the transistors in

offset-cancellation circuit have the same current as the input transistors to achieve 0 dB gain at DC. The power consumption of the offset cancellation circuit is also proportional to IF frequency. Therefore, the total bias current of each VGA stage is:

$$I_{tot1}=2\times2\times I_B=4\times A_{IF}\times\omega_{IF}\times C_L\times\Delta V_{gs}/2$$

And the total current of the whole VGA with 3 stages is:

$$I_{tot}=3\times I_{tot1}=6\times A_{IF}\times\omega_{IF}\times C_L\times\Delta V_{gs}. \quad (9.23)$$

In this design, C_L is about 1pF, assume ΔVgs=0.2V, and the gain of each stage at 70 MHz is 20 dB, then the total current is about 5.3mA.

9.4.3 Power Consumption of the ADC

The IF frequency affects the design of loop filter in Bandpass Sigma-Delta ADC (BPSD). The loop filter in BPSD is also a Gm-C filter [54], which has the same structure as the IF filter. As discussed above, the center frequency of the filter affects the power consumption of the filter almost proportionally.

The sampling frequency, f_s, of BPSD is four times of IF frequency, $f_s=4f_{IF}$. The dynamic power consumption of the digital circuits in BPSD is proportional to the sampling frequency. Therefore, as IF frequency increases, the power consumption of the BPSD increases accordingly.

9.5 Summary

The sensitivity of the receiver is limited by the image rejection, the NF and the linearity of the whole receiver. From Eq. (9.2), if the IF frequency increases, the image rejection increases. Therefore, the sensitivity due to the image signal is better. However, the NF of the IF filter increases if IF frequency increases. As a result, from Eq. (9.8), the sensitivity due to the noise of IF filter decreases. The linearity of the IF filter decreases if IF

frequency increases. Finally, the IF of the receiver is set at 70 MHz to balance between the image rejection and the NF and linearity of the IF filter.

Chapter 10

LAYOUT & EXPERIMENTAL RESULTS

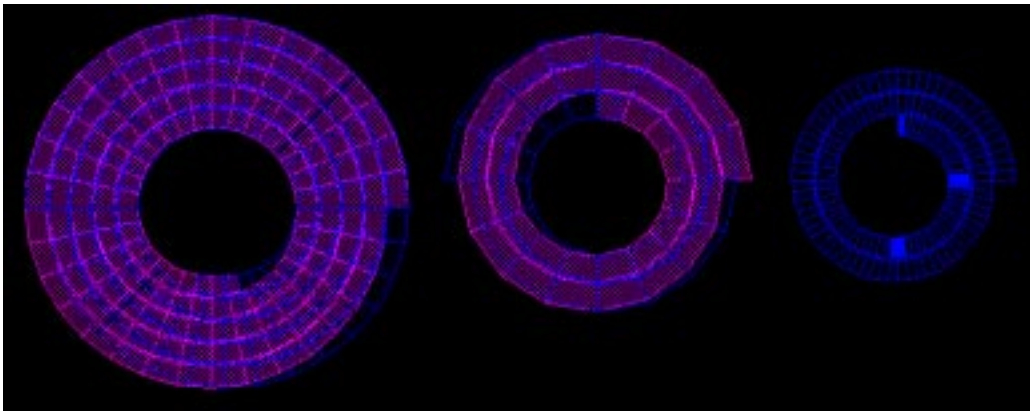
The layout and the experimental results of the transceiver is presented in this chapter.

10.1 Layout of the Transceiver

The transceiver is designed in 0.5-μm CMOS process with 3 metal layers and 1 poly layer. The total chip area is 8.1 mm^2.

10.1.1 Layout of Building Blocks

The layouts of the inductors used in the LNA are shown in Fig. 10.1. The gate inductor and the output inductor are double-layer (M2, M3) spiral inductors and the source inductor is a single layer (M3) spiral inductor.



260×260μm 190×190μm 150×150μm

(a) Gate inductor (b) Output inductor (c) Source inductor

Fig. 10.1 Layout of Inductors Used in the LNA

The layout of double-unit-cap used in the SCAs of the LNA is shown in Fig. 10.2. It is a 200-fF capacitor, which is twice of the unit cap. The whole 5-bit SCA, used for differential signal, includes 30 double-unit-caps and two unit-caps.

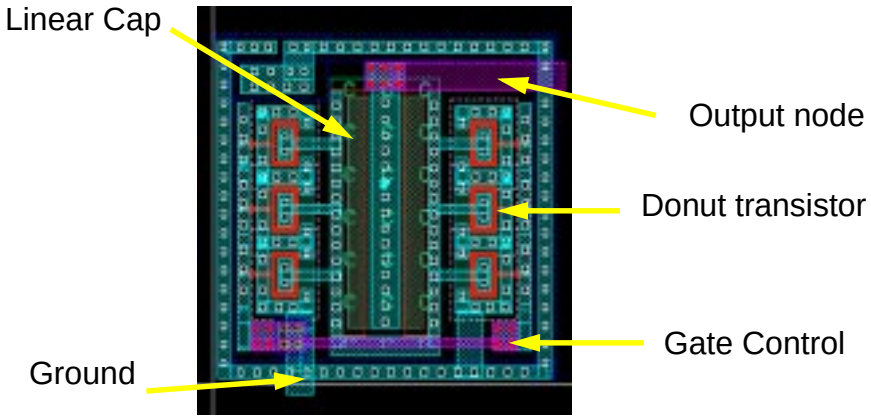
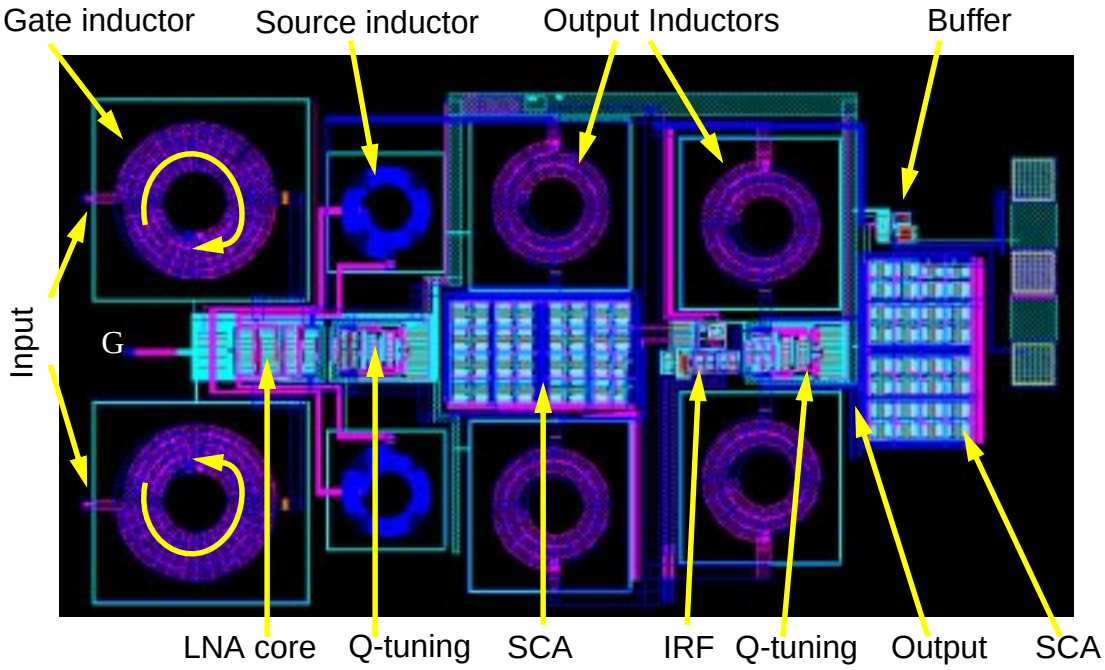


Fig. 10.2 Layout of Double-Unit-Caps Used in the LNA

The Layout of the LNA used in the receiver is shown in Fig. 10.3. It is completely symmetrical to improve the matching between two differential ends.



1460×850 μm^2

Fig. 10.3 Layout of the LNA in the Receiver

The layout of the notch filter is shown in Fig. 10.4. It uses the same output inductors and SCA as those of the LNA and IRF to achieve matching between center frequencies of the LNA and the notch filter. As a result, the image frequency will shifted in the same amount as that of the signal frequency if the process variations are same for both LNA and notch filter.

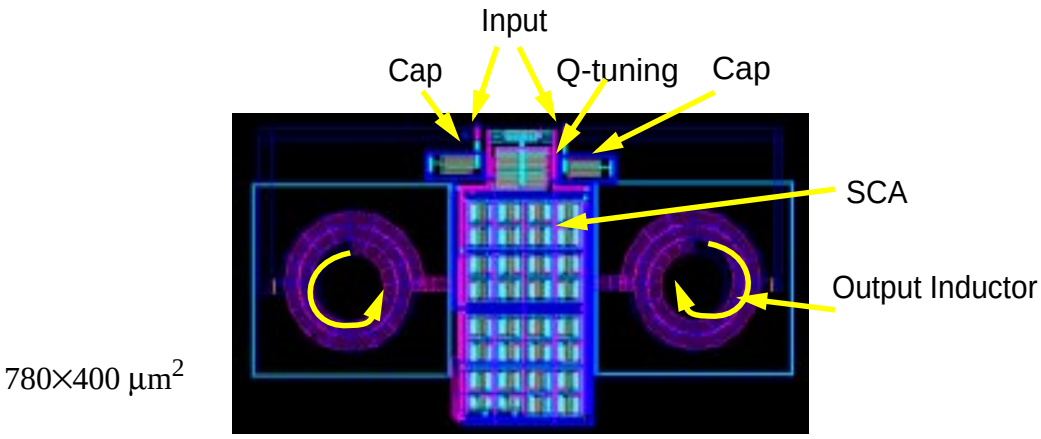


Fig. 10.4 Layout of the Notch Filter in the Receiver

The layout of the synthesizer is shown in Fig. 10.5. The baseband and reference signal are put at upper-right corner, which is far from the output of the synthesizer to reduce the coupling the digital noise to the RF signal.

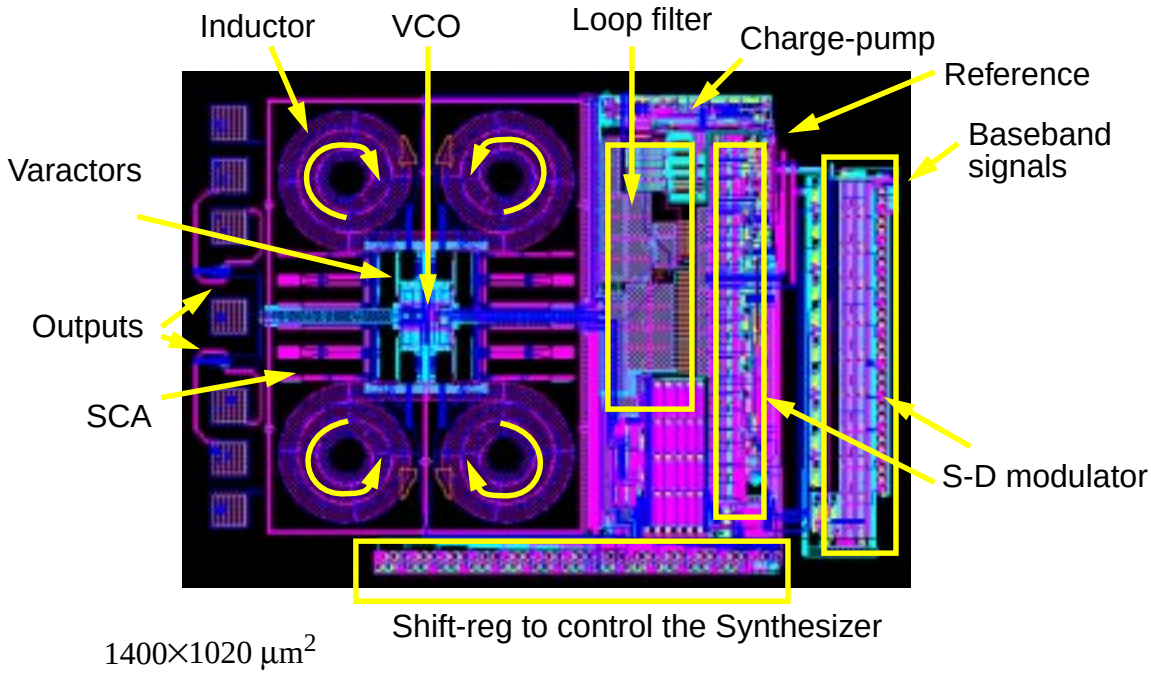


Fig. 10.5 Layout of the Synthesizer in the Transceiver

The layout of each stage of the VGA is shown in Fig. 10.6. The whole VGA consists three stages with total area of 200×380 μm^2, as shown in.

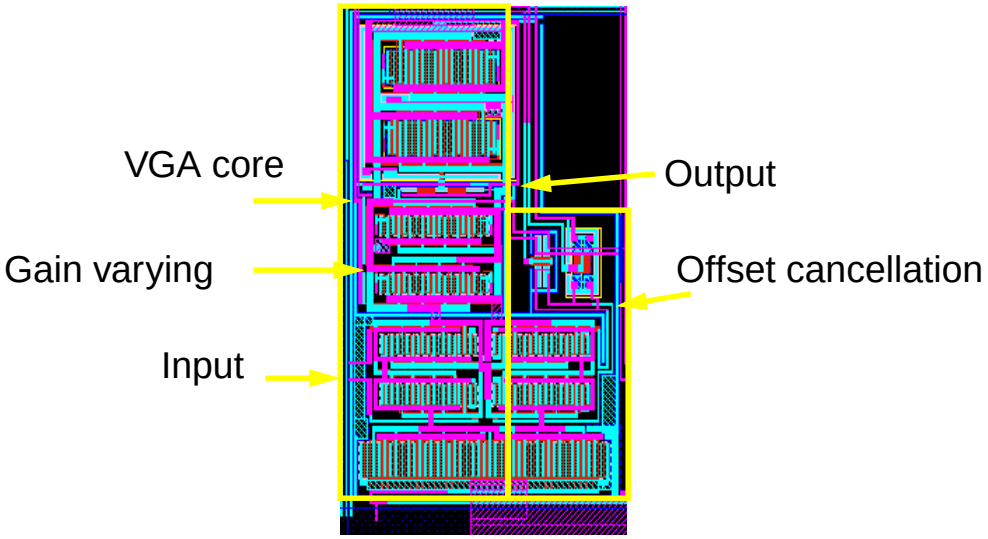


Fig. 10.6 Layout of each stage of the VGA

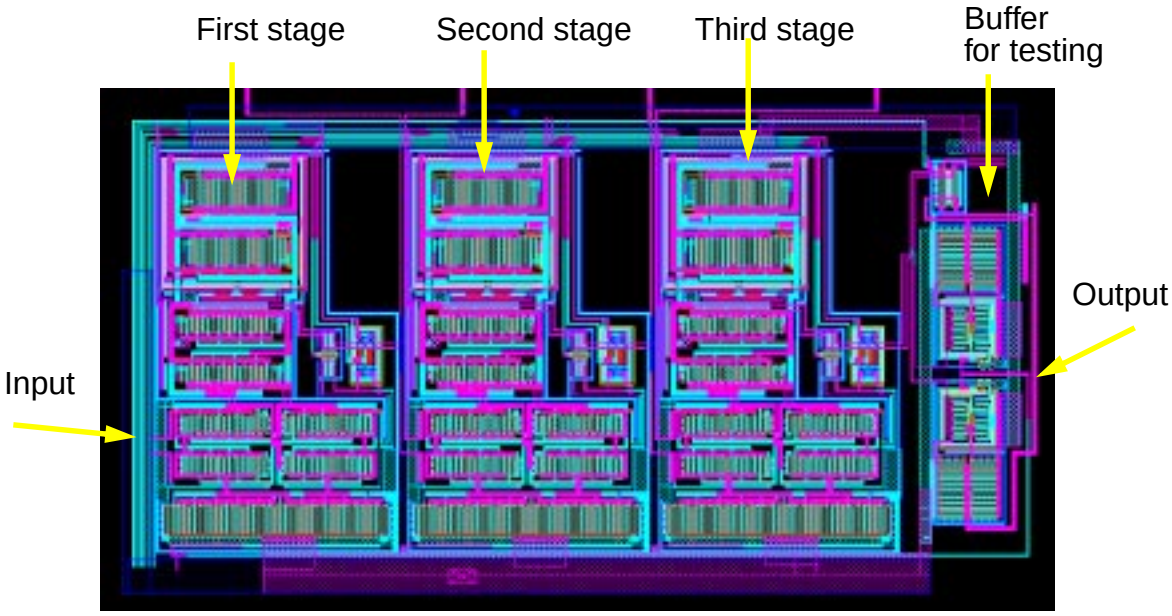


Fig. 10.7 Layout of the whole VGA

The layout of the RSSI used in the AGC loop is shown in Fig. 10.8. It has a small area of 100×110μm^2. The resistor and capacitor of the AGC loop are implemented with external components.

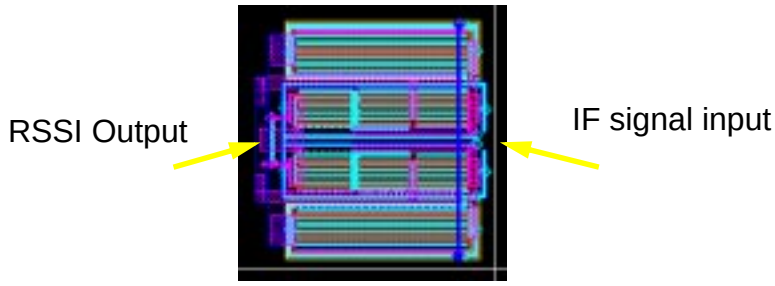


Fig. 10.8 Layout of the RSSI

10.1.2 Layout of the Transceiver

The layout of the whole transceiver is shown in Fig. 10.9. The total core area is 8.1 mm^2. The layout is extremely critical and carefully done to minimize the coupling among the building blocks.

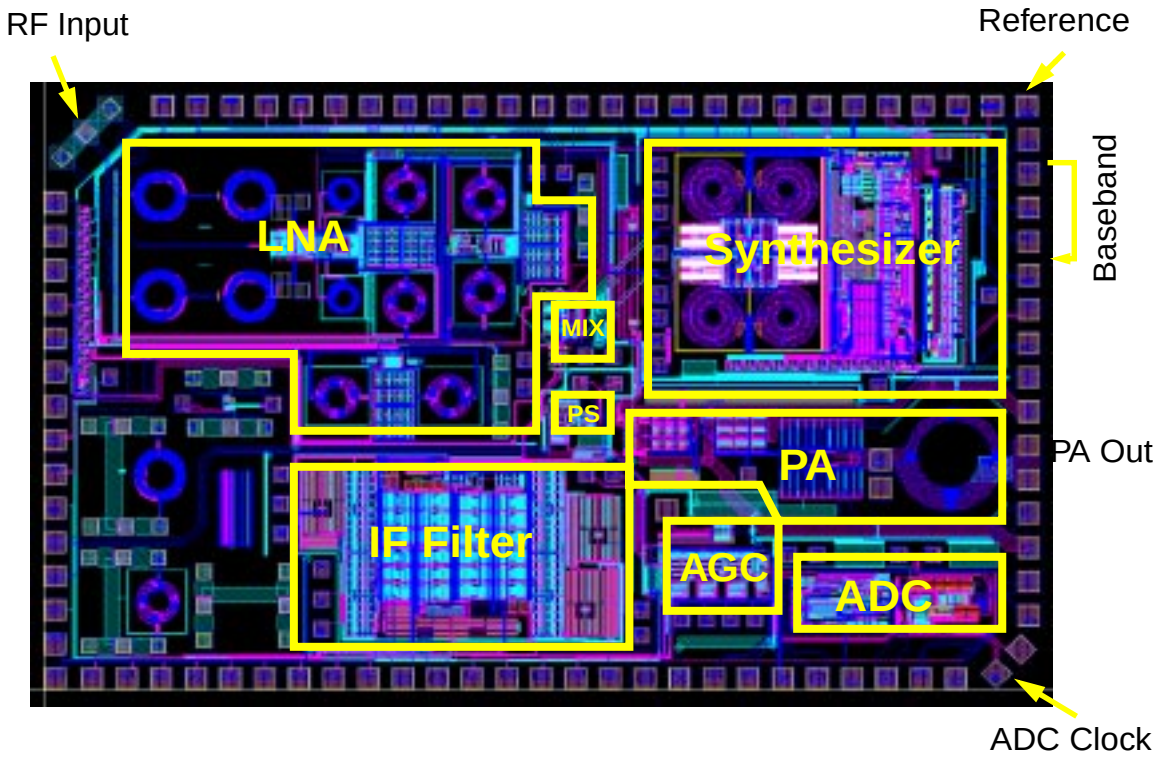


Fig. 10.9 Layout of Whole Transceiver

The input pads of the LNA are put at the upper-left corner of the chip to reduce the noise coupling from the other building blocks. Small pads of 75μm-75μm, with shielding grounds underneath, are used as the input pads to reduce the noise coupling from the substrate. The LNA is fully differential and the layout of the LNA is completely symmetrical to reduce the noise coupled from the substrate. All inductors used are surrounded by the guard-rings. The notch-filer is put very close to the LNA to reduce the parasitic inductance and capacitance of the wires connecting them.

The LNA and the synthesizer are put in a symmetrical direction to minimize the mismatch in the differential ends. The digital circuits in the synthesizer are put far away from the LNA to reduce the coupling of digital noise to the LNA. The reference signal of the synthesizer is put at the upper-right corner.

The image-rejection mixers are put close to the outputs of both the LNA and the synthesizer to reduce the loading effect and coupling of the RF signal to the IF circuits. The phase shifters are put right after the mixers to improve the matching between the I and Q channels.

The IF filter is put at the lower-left corner and the VGA and ADC are put at the lower-right corner to reduce the coupling of high power IF signal to the LNA. The clock signal and the output signal of the ADC are put at the lower-right corner. The digital ground of the ADC is separated from the substrate ground to minimize the noise coupling from the ADC to other circuits.

The power amplifier is put close to the synthesizer to minimize the loading effect of the PA to the VCO. A few big capacitors are put between the PA and the synthesizer to isolate the PA from the synthesizer.

The RF input signal, the reference signal of the synthesizer and the clock signal of the ADC are put at three corners to minimize the coupling of the digital noise to the RF signal. Each building block is surrounded by a guard-ring, which is implemented by many p-substrate contact close to each other. Each guard-ring has a gap one corner to avoid the loop current. Any large free space inside the transceiver is filled with many substrate contacts. The guard-ring are connected to an independent ground line to reduce cross coupling between each building block.

The chip area of each building block is summarized in Table 10.1.

Table 10.1 Chip Area of Each Block and Transceiver

Block	**Area, mm^2**	**Block**	**Area, mm^2**
LNA	1.24	IF Filter	1.2
Notch	0.31	VGA & RSSI	0.11
Synthesizer	1.43	ADC	0.27
Mixer	0.04	PA	0.73
Phase Shifter	0.09	**Total**	8.1

10.1.3 The Die-photo of the Transceiver

The die photo is shown in Fig. 10.10, and the total core area is 8.1 mm^2.

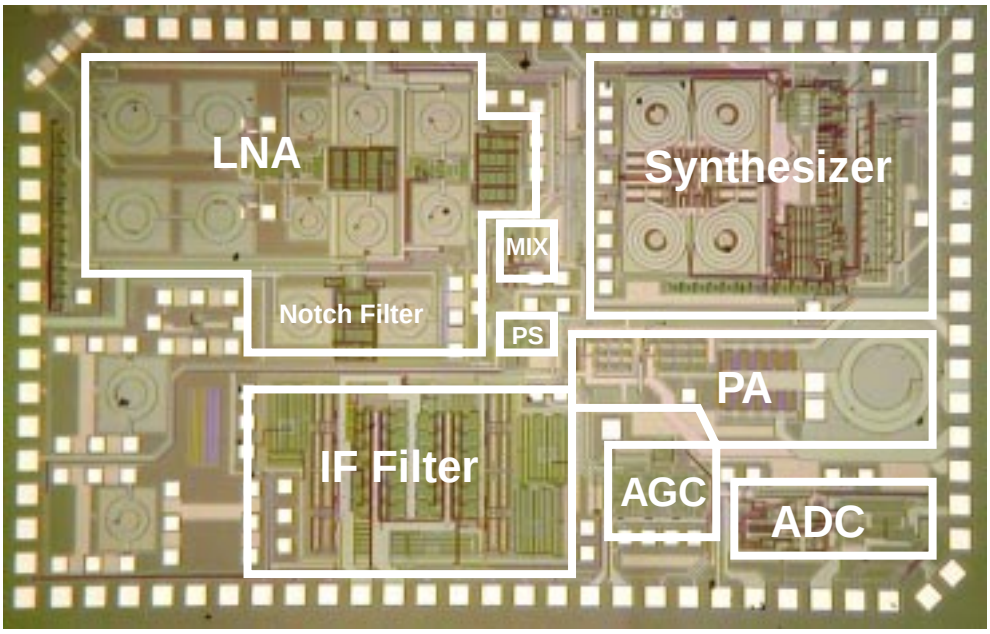


Fig. 10.10 Die Photo of the Transceiver

10.2 Testing Setup

The receiver is tested on the bare die with the RF input signal applied from the high-speed probe. The signal at the output of each building is measured from the LNA to the the ADC.

10.2.1 Setup of the LNA Testing

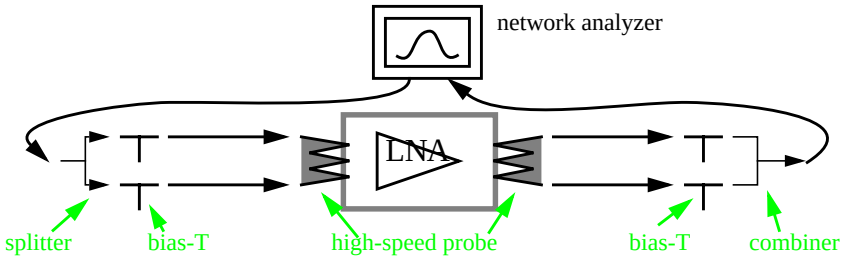
The setup for the LNA testing is shown in Fig. 10.11. The setup for frequency response measurements is shown in part (a). A network analyzer is used to measure the frequency response, the image rejection and the input matching of the LNA. The port 1 of the network analyzer is connected to a power splitter with 180^o phase difference to convert the single-ended signal to differential format. Two bias-T's are used to add a DC voltage to the input signal so that it is suitable for the LNA input devices. An S-GG-S high-speed probe is

used to apply the input signal to the input pads of the LNA. Another S-GG-S high-speed probe is used to pick up the output signal of the LNA after a 50-Ω buffer. Two bias-T's are used after the probe to remove the DC voltage from the output signal. A power combiner is used to convert the differential signal to a single-ended signal. The output signal is finally connected the port 2 of the network analyzer.

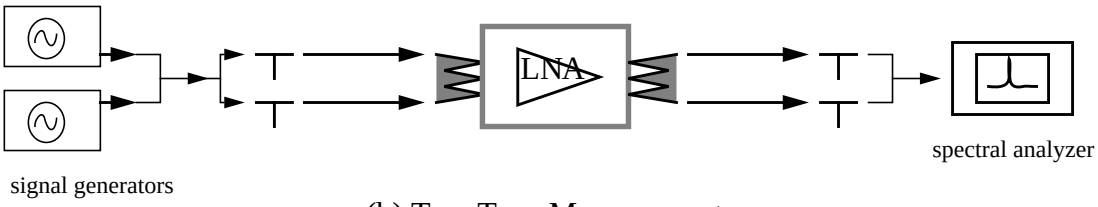
With this setup, the frequency response can be directly plotted by the network analyzer. The image rejection of the LNA can be found from the frequency response. To measure the S11 of the LNA, only port 1 of the network analyzer is used, and the signal is applied to the LNA in single-ended. The other end of the LNA input is connected to a DC voltage.

The setup for two-tone measurements is shown in Fig. 10.11, part (b). Two signal generators are used at the input of the LNA to apply two signals at different frequencies. The wo signals are combined together by a power combiner. The two input signals are connected to the LNA with a power splitter, two bias-T's and a high-speed probe. The output signal of the LNA is measured by a spectrum analyzer which is connected to the LNA output by a high-speed probe, two bias-T's and a power combiner.

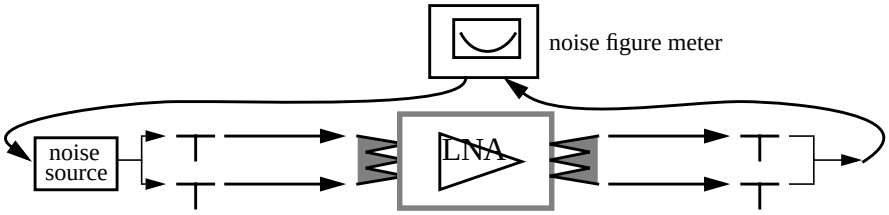
The setup for the NF measurement is shown in Fig. 10.11 part (c). The setup is similar as that for the frequency response measurements. However, the network analyzer is replaced with a noise figure meter. An accurate noise source is used at the input of the LNA. The noise figure of the LNA at different frequency can be directly read from the noise figure meter.



(a) Frequency Response, IR, Input Matching



(b) Two-Tone Measurement



(c) Noise Figure Measurement

Fig. 10.11 Setup of LNA Testing

The setup for the Notch filter testing is shown in Fig. 10.12. The input impedance of the Notch filter is measured by a network analyzer and plotted as a function of frequency.

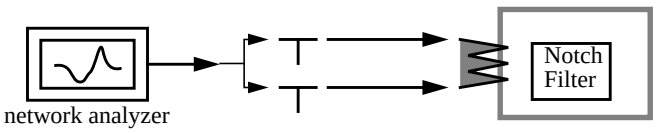


Fig. 10.12 Setup of Notch Filter Testing

10.2.2 Setup of Synthesizer Testing

The setup for the synthesizer testing is shown in Fig. 10.13. A signal generator is used to generate the reference signal for the synthesizer. A computer is used to control the channel number and the SCAs in the VCO. An open source NMOS transistor is used as a buffer after the VCO. The output of the buffer is bonded to the printed-circuit-board (PCB) and connected to a bias-T which works as the load of the open source transistor. A spectrum analyzer is used to measure the output signal power and phase noise of the synthesizer.

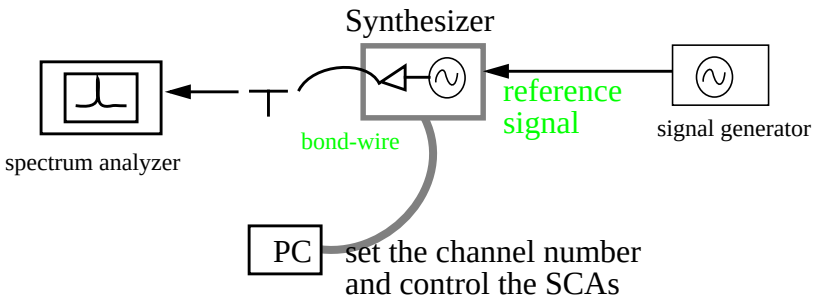


Fig. 10.13 Setup of Synthesizer Testing

10.2.3 Setup of RF Front-End Testing

The setup of the RF front-end testing is shown in Fig. 10.14. The input RF signal is applied to the LNA with high-speed probe. The image-rejection mixers are driven by the output of the LNA and the on-chip synthesizer. After the mixers, the phase shifters and the buffer, the output IF signals of the mixers are bonded to the PCB and measured by a spectrum analyzer. The buffer sums the IF signals from the I and Q channels to cancelled the image signal. Therefore the image rejection of the whole receiver can be measured with this setup. The gain, linearity and noise figure of the front end can be measured with this setup as well. The noise figure is extrapolated from the noise floor of the buffer output, which is measured with the spectrum analyzer.

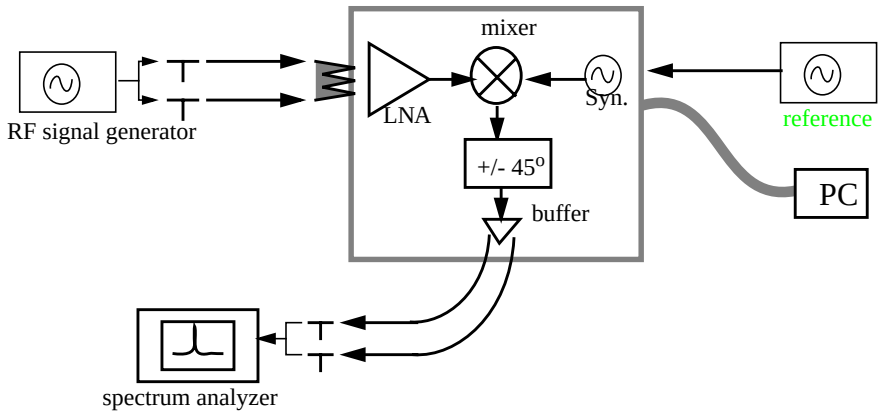
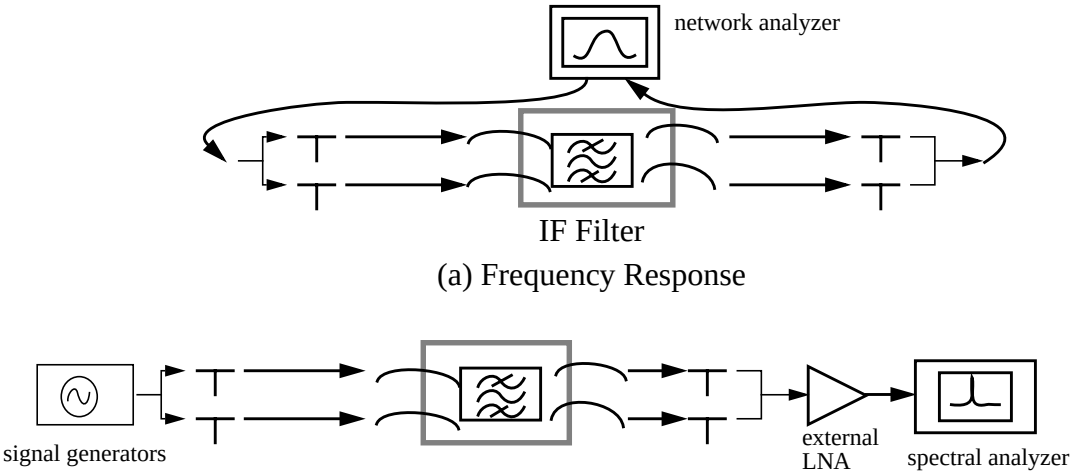


Fig. 10.14 Setup of RF Front-End Testing

10.2.4 Setup of IF Filter Testing

The setup of the IF filter testing is shown in Fig. 10.15. Because the 50-Ω matching is easily achieved at the IF frequency of 70 MHz on the PCB. The input pads and output pads are bonded to the PCB and the filter is measured on the PCB with SMA connectors. The frequency response is measured with the network analyzer. The noise figure is measured with the spectrum analyzer. The IIP3 of the filter is measured with the similar setup as that of the NF measurement. However, two signal generators are used to generate two signals at the IF frequency, 70.8 MHz and 71.6 MHz.



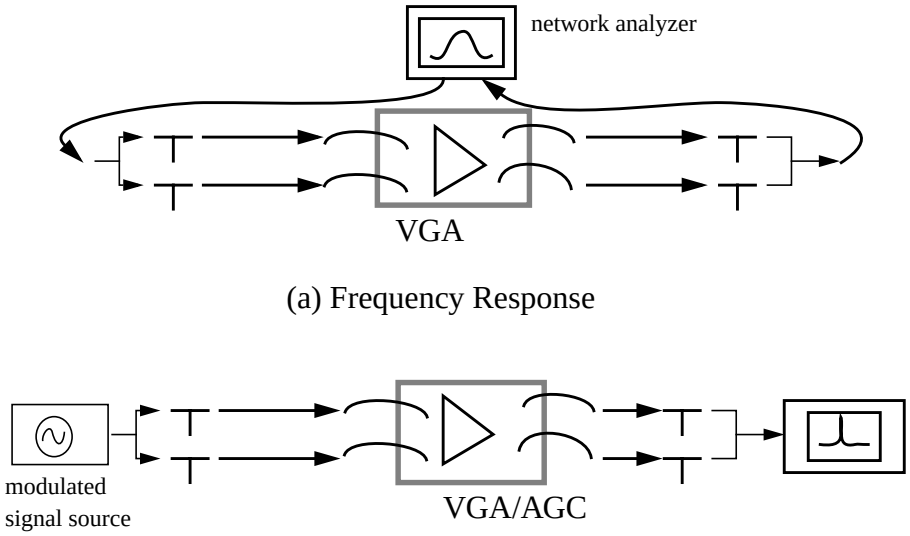
(a) Frequency Response

(b) Noise Figure Measurement

Fig. 10.15 Setup of IF Filter Testing

10.2.5 Setup of VGA Testing

The setup of the VGA testing is shown in Fig. 10.16, part (a). The frequency response is measured with a network analyzer. The setup of AGC testing is shown in Fig. 10.16, part (b). An AM signal is applied to the VGA input and the VGA output is measured with a spectrum analyzer.



(a) Frequency Response

(b) AM Suppression Measurement

Fig. 10.16 Setup of VGA Testing

10.2.6 Setup of ADC Testing

The testing setup of band-pass sigma-delta ADC is shown in Fig. 10.17. A clock signal of 280MHz is generated from HP80000 pattern generator. A S-G probe is used to apply the clock signal to the ADC. The IF signal is generated from a signal generator and applied the ADC with bond-wires. A high-impedance probe is used to connect the output of the ADC to a spectrum analyzer.

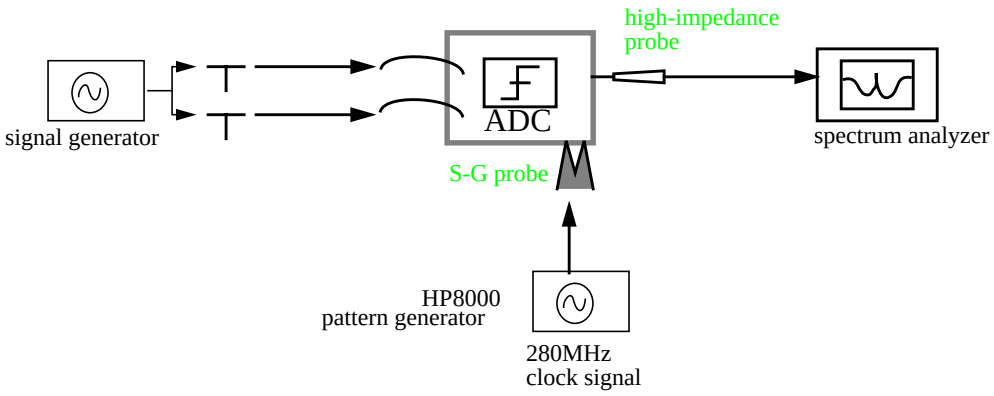


Fig. 10.17 Setup of ADC Testing

10.2.7 Setup of Receiver Testing

The testing setup of the whole receiver is shown in Fig. 10.18. The RF signal is applied to the LNA input pads with high-speed probe. A high-impedance probe is used to measure the signal at the output of each stage in the receiver. The reference signal of the synthesizer is generated from a signal generator and applied to the synthesizer with a bond-wire. The clock signal of the ADC is generated from an HP80000 pattern generator and applied to the ADC with a S-G probe. A personal computer (PC) is used to control the channel number and the SCAs the synthesizer. The SCAs in the LNA, Notch filter and IF filter is also controlled by this computer.

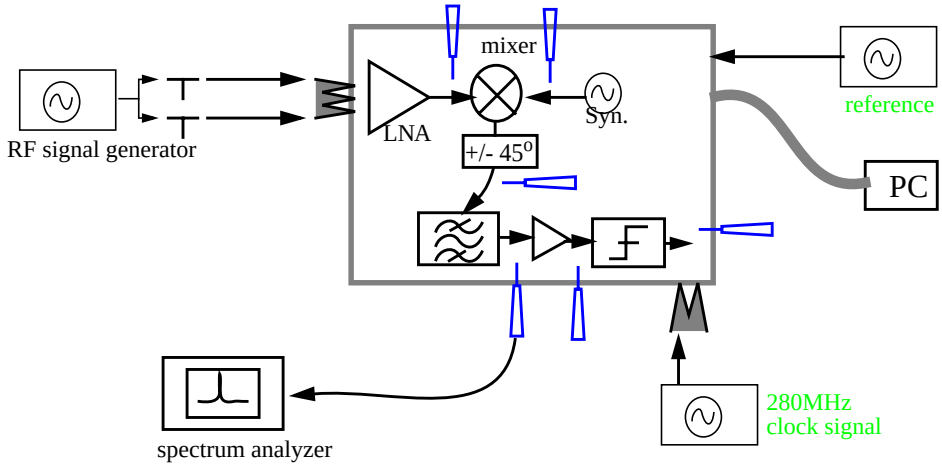


Fig. 10.18 Setup of Receiver Testing

The gain, linearity, image rejection and noise figure of the receiver can be measured with this setup.

10.2.8 Setup of PA and Transmitter Testing

The testing setup of the transmitter and the PA is shown in Fig. 10.19. The transmission date is generated and filtered with Matlab in a computer. The transmission data is downloaded to the HP80000 pattern generator in series bit-stream format. The bit-stream is fed to the transmitter and converted to parallel format by an on-chip shift-register. The data after the shift-register is used to modulate the divider in the synthesizer. A high-impedance probe is used to connect the synthesizer output to a spectrum analyzer. An external matching network is used for the PA to achieve high output power. The output of the match network is connected a spectrum analyzer directly to measure the output RF power.

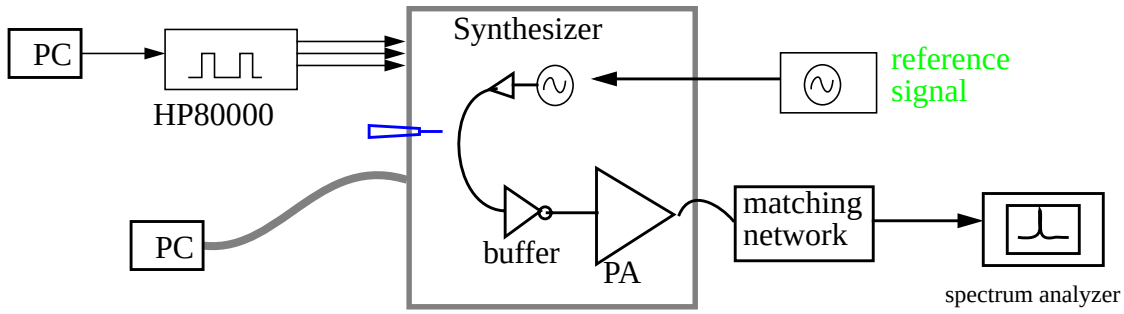


Fig. 10.19 Setup of PA and Transmitter Testing

10.3 Experimental Results

10.3.1 Inductors

Experimental results of inductors used in the transceiver are listed in Table 10.2, together with the design parameters and simulation results from Asitic. The measured inductance is larger than the simulated one. The measured Q's are lower than the simulated Q's because the Asitic doesn't include the loss due to eddy current for circular spiral inductors.

Table 10.2 Measurement Results of On-Chip Inductors in LNA

	Lg[a]	**Lg2**	**Lo**	**Lv**
Metal Layers	M2/M3	M2/M3	M2/M3	M2/M3
Sides of Each Turn	32	64	16	64
Metal Width, μm	14.25	14.25	18	36/26
Metal Spacing, μm	1.2	1.05	1.2	1.8
No. of Turns	4.75	2.25	2.25	2.5/3.5
Center-to-Edge Radius	135	110	100	150
Inductance (nH) (simulation)	18.1	8.7	4.3	6.6
Q at 950 MHz (simulation)	3.3	3.2	3.6	N/A
Self-Resonant Frequency GHz (simulation)	1.5	3.2	4.9	N/A
Inductance (nH) (measured)	21	10	4.5	6.4
Q at 950 MHz (measured)	1.5	2.6	3	2.1
Self-Resonant Frequency GHz (measured)	1.5	3	3.2	2.3

a. Lg is the gate inductor used in the RFIC2C, Lg2 is the gate inductor used in RFIC2D, Lo is the output inductor of the LNA, Lv is the inductor used in the VCO.

10.3.2 LNA

The measured input matching of the LNA is shown in Fig. 10.20. Due to the high parasitic capacitance of the gate inductor, the center frequency of the S11 is shifted to lower frequency. However, it can still achieve S11 of -10 dB at the desired frequency, 947 MHz. The overall frequency response of the LNA and the IRF is measured and plotted in Fig. 10.21. The gain of the LNA is 22 dB at 947 MHz with a bandwidth of 25 MHz, which corresponds to a high Q of 38. Together with the IRF, the LNA achieves a total image rejection of 50 dB, which is high enough to eliminate an off-chip image-rejection RF filter.

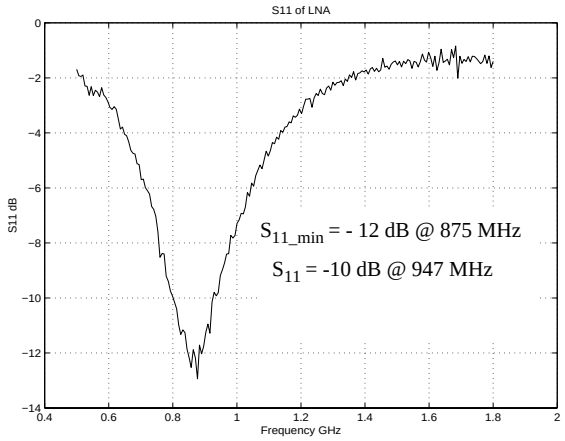


Fig. 10.20 S11 of LNA

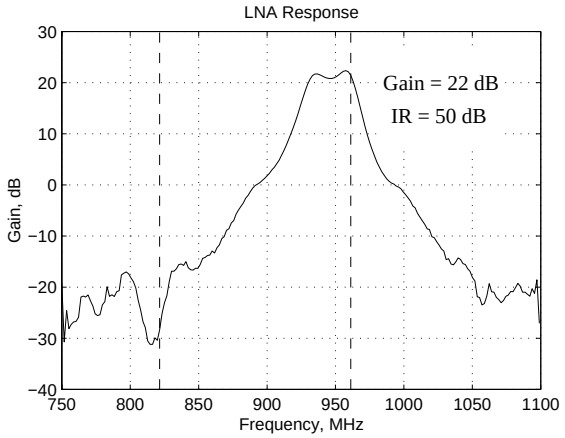


Fig. 10.21 Frequency Response of LNA and IRF

The two-tone measurement result is shown in Fig. 10.22. Two input signals are located at 800 KHz away from each other. The IIP3 is measured to be -17 dBm.

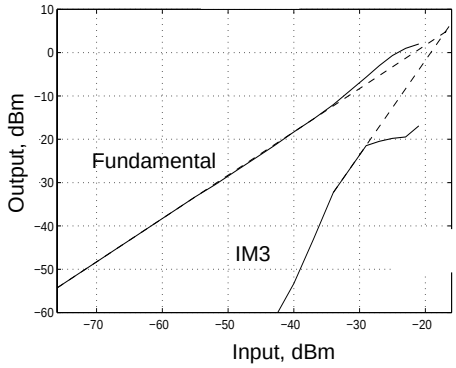
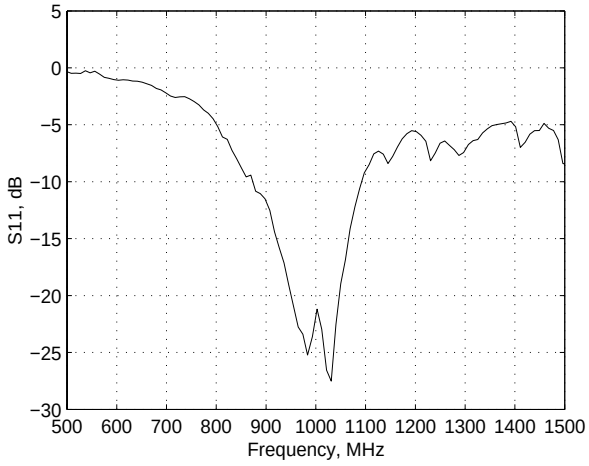


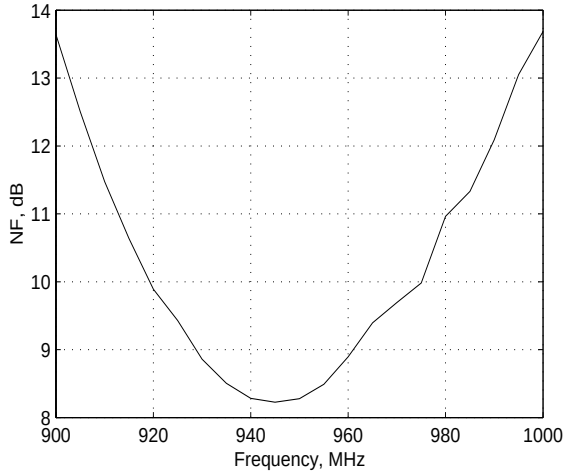
Fig. 10.22 Two-Tone Measurement of the LNA

The noise figure is 10 dB, which is dominated by the low Q of the very big on-chip inductors used for input matching. With bond-wire inductors used as the gate inductors, the S11 can be improved to -20 dB and the NF can be improved to 8.2 dB, as shown in Fig. 10.23 and Fig. 10.24.



S_{11}=-20dB

Fig. 10.23 S11 of LNA with Bond-wire Inductors as Gate Inductors



NF=8.2dB

Fig. 10.24 NF of LNA with Bond-wire Inductors as Gate Inductors

10.3.3 Synthesizer

The measured output frequency tuning range of the synthesizer is from 857.6 to 922.8MHz with a minimal resolution of 25 kHz. As shown in Fig. 10.25, the phase noises of the synthesizer at 400 kHz and 600 kHz offset are -116 dBc/Hz and -118 dBc/Hz, respectively. Since the frequencies are out of the loop bandwidth, they are mainly determined by the phase noise of the free-running VCO. However, the phase noise of the VCO is limited by the poor quality of the spiral inductors. Within 200 kHz offset, the phase noise, with a slope of -30 dBc/decade, is dominated by the flicker noise of the transistors in the VCO. Despite the high tolerance of substrate noise, the reference frequency of 25.6 MHz still couples to the VCO, and spurs of -67 dBc at 25.6-MHz offset are observed, as shown in Fig. 10.26. The coupling is found to be mainly due to the short separation (~200 μm) for a compact layout between the circuits that are clocked by the reference frequency and the VCO. The measured loop bandwidth is 200kHz. In the case of a maximal change in the tuning voltage of the varactors, the measured settling time is less than 150 μs, as shown in Fig. 10.27.

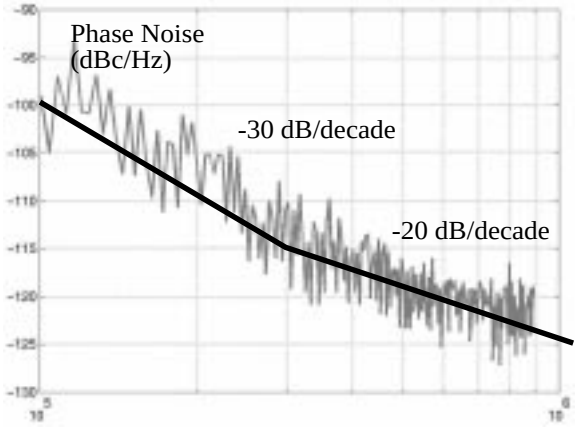


Fig. 10.25 Measured output phase noise of the synthesizer

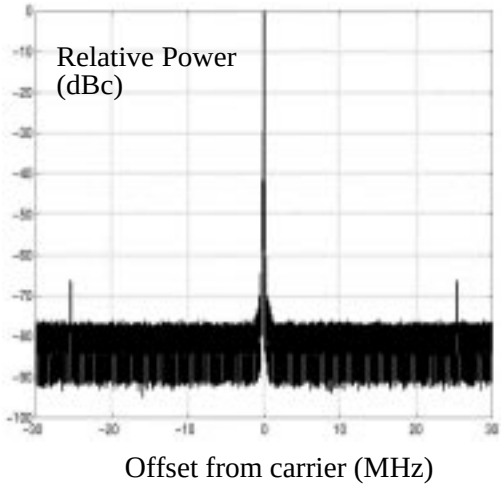


Fig. 10.26 Output spurs of the synthesizer

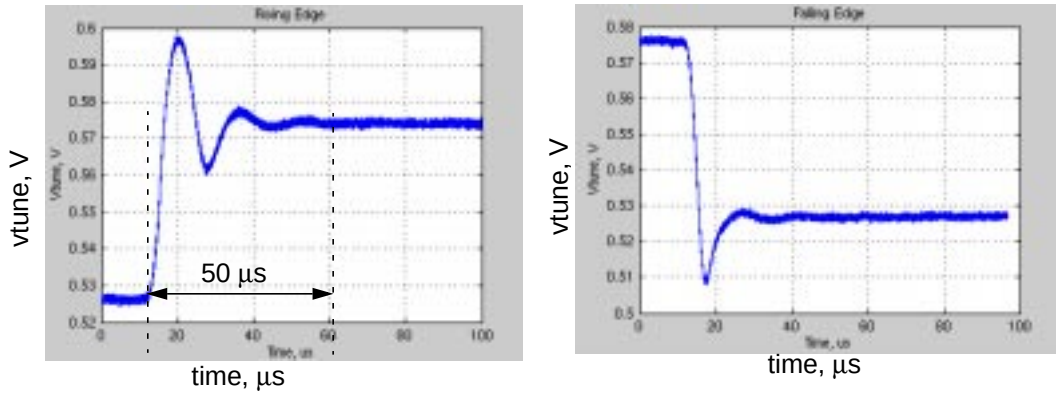


Fig. 10.27 Measured Step Response of the synthesizer

10.3.4 Mixers

Each of the image-rejection mixers measures a conversion gain of -2 dB with an IIP3 of 7 dB and a NF of 27 dB. The output signals of the in-phase and quadrature-phase mixers are summed after passing through two phase-shifters, and an image-rejection of 29 dB is measured with this I-Q structure.

10.3.5 IF Filter

The channel-selection IF filter achieves a measured bandwidth of about 200 KHz at 70 MHz (Q = 350) while consuming a power of 90 mW, as shown in Fig. 10.28. The measured input equivalent noise is 36.3 μV, which corresponds to a NF of 43 dB, and the measured IIP_3 is –5 dBm. The two-tone measurement of the IF filter is shown in Fig. 10.29.

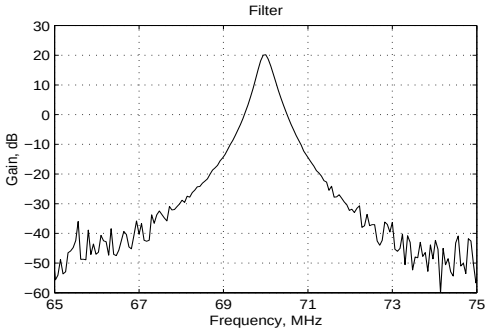


Fig. 10.28 Frequency Response of the IF Filter

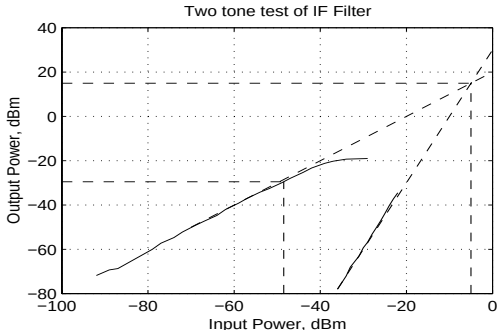


Fig. 10.29 Two-tone measurement of the IF Filter

10.3.6 VGA

The measured frequency response of the VGA is shown in Fig. 10.30. It achieves a maximum gain of 78 dB at 70 MHz and a very low gain at low frequency (0 dB at DC). Therefore it can amplify the IF signal without suffering from the DC offset. As plotted in Fig. 10.31, the gain control range is measured to be from -50 dB to 78 dB.

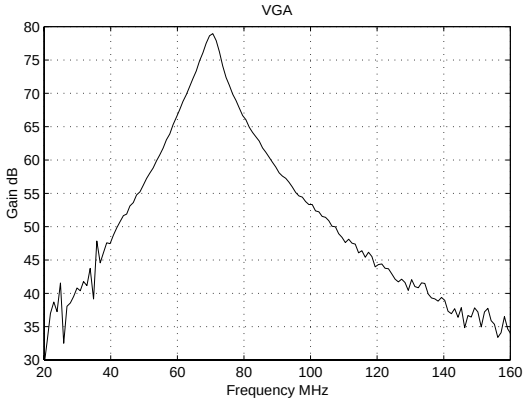


Fig. 10.30 Frequency Response of the VGA

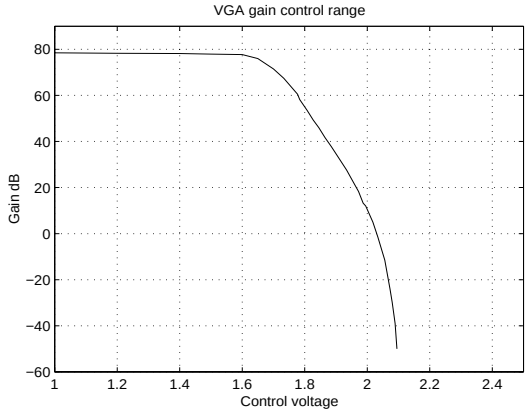


Fig. 10.31 VGA Gain Control Range

Fig. 10.32 shows the gain of the VGA as a function of offset voltage. An input signal of -90 dBm at 70 MHz is applied to the VGA input together with a DC offset voltage. As the offset voltage varies around the zero, the gain of the VGA also varies. Without offset cancellation, the gain is very sensitive to the input offset voltage. Even an offset voltage as

small as 0.5 mV at the input will be amplified by the VGA to more than 1 V, and the operation point of the VGA will be shifted far away from the optimum value, which results in a significant drop of the gain. However, with offset cancellation, the offset voltage at input is not amplified and has little effect on the operation point, and as a result, the gain of the VGA is quite insensitive to the input offset voltage. Quantitatively, the maximum tolerable offset voltage, defined as the offset voltage with which the gain decreases by 1 dB, is measured to be 0.1 mV without offset cancellation and 50 mV with offset cancellation.

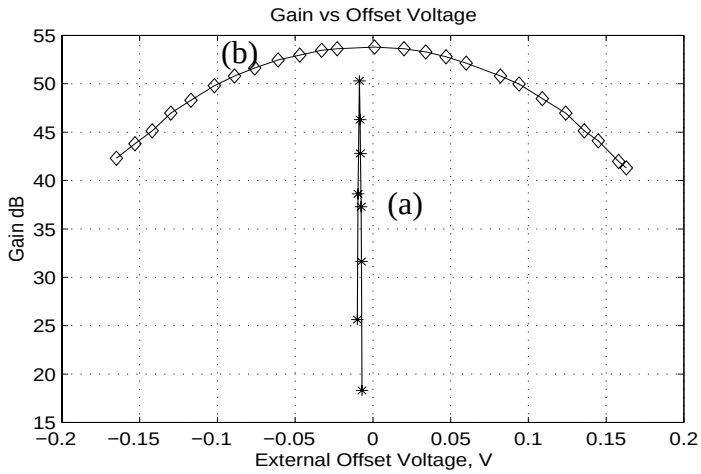


Fig. 10.32 VGA Gain Variation due to Offset Voltage

(a) Without Offset Cancellation
(b) With Offset Cancellation

The output power as a function of input power is shown in Fig. 10.33. The output power is relatively constant at -9 dBm, which is optimum for ADC input.

An amplitude-modulation (AM) signal is used to measure the AGC loop bandwidth. Because the AGC loop has an ability of removing the variation in the signal power, the modulation index, which indicates how much the carrier power is varied by the modulation signal, of an AM signal is suppressed at the output of the AGC loop. The measured AM suppression as a function of frequency is shown in Fig. 10.34. The modulation index is suppressed by about 9 dB at the output of the AGC loop when the frequency of the modulation

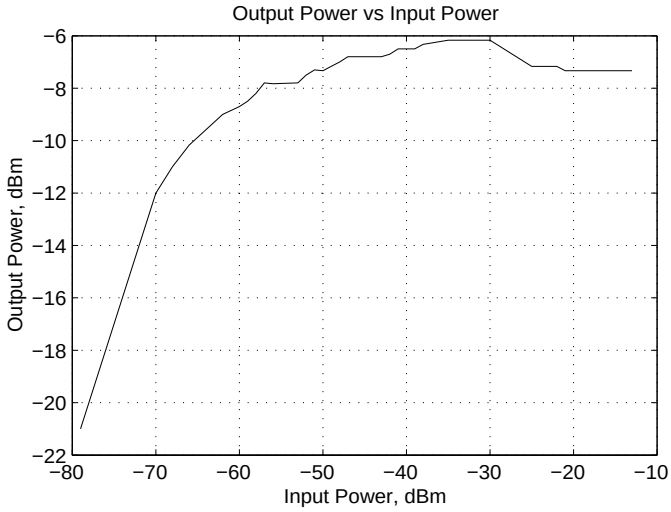


Fig. 10.33 AGC Input Power and Output Power

signal is no more than 700kHz. In other words, the AGC loop has a loop bandwidth of about 700kHz.

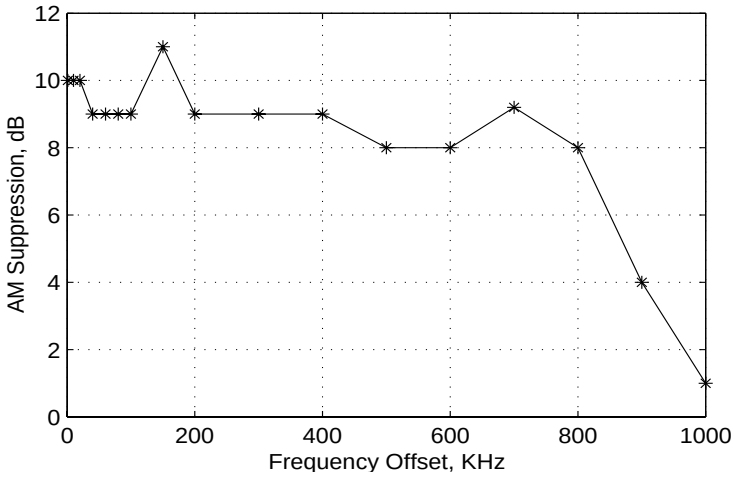


Fig. 10.34 AM Suppression of the AGC Loop

10.3.7 BPSD ADC

The measured output frequency spectrum of the band-pass sigma-delta (BPSD) ADC and its zoomed-in version are shown in Fig. 10.35. The maximum SNDR achieved is 47 dB, which corresponds to a resolution of more than 7 bits.

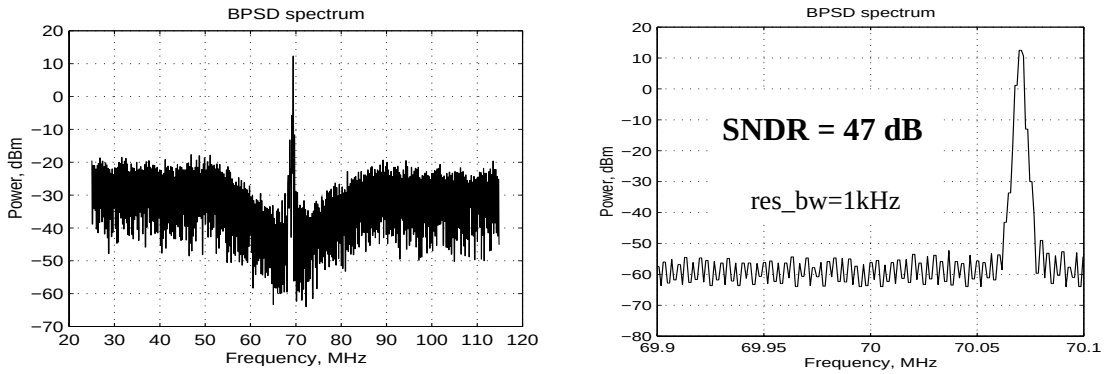


Fig. 10.35 Output Spectrum of the BPSD ADC

10.3.8 Receiver

The output spectrum of the whole receiver system, at the ADC output with an input signal of -90-dBm being applied to LNA, is shown in Fig. 10.36. A SNDR of 9dB is measured. Fig. 10.37 illustrates the signal-level diagram of the receiver together with the gain, NF, and IIP_3 of each building block. The whole receiver measures an overall sensitivity of -90 dBm, a total image rejection of 79 dB, an IIP_3 of -24 dBm, and a noise figure of 22 dB with a power consumption of 227 mW.

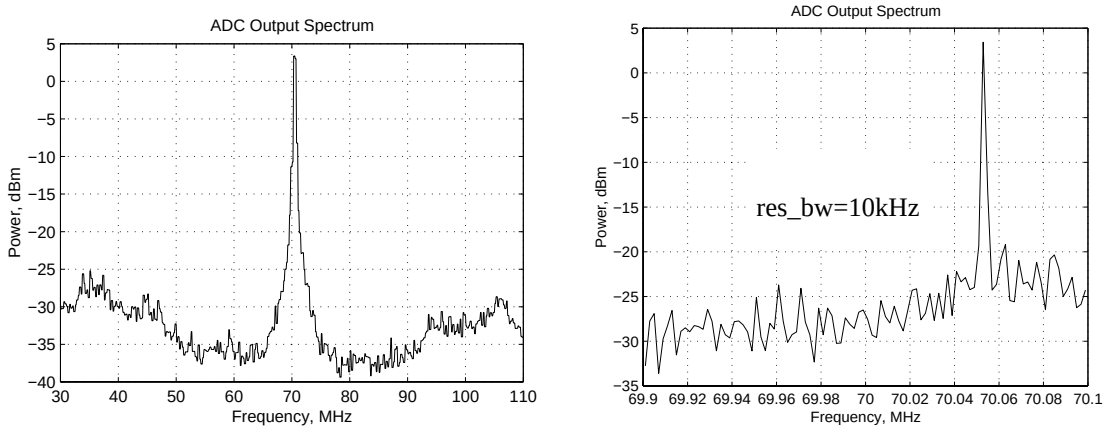
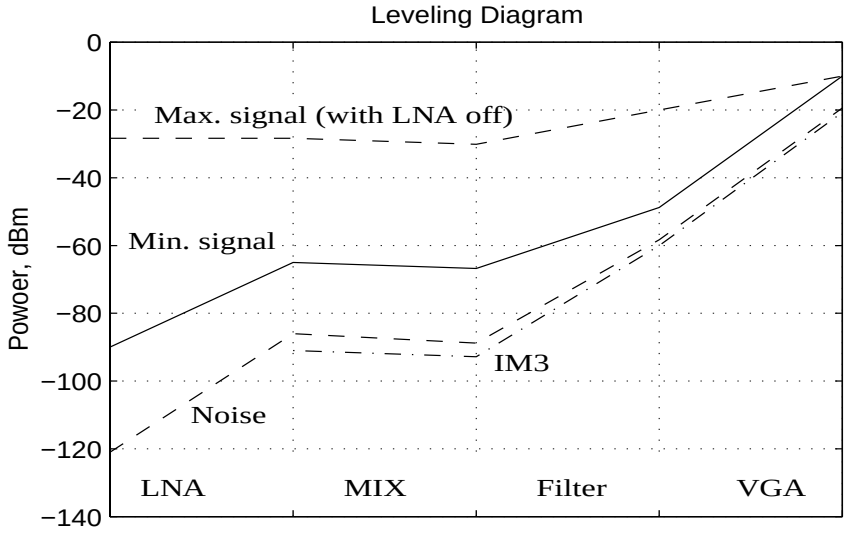


Fig. 10.36 Measured output spectrum of the whole receiver with a -90-dBm input to LNA

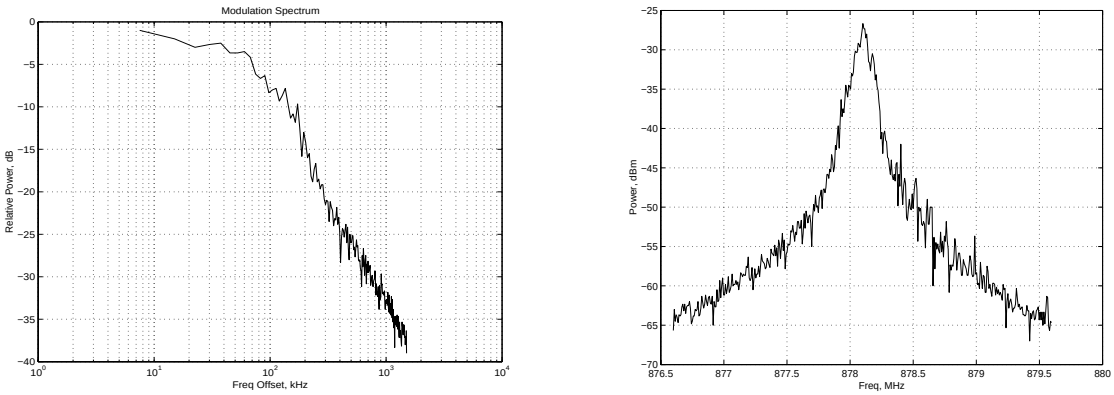


Gain	22dB	-2 dB	19 dB	0 - 78 dB
NF	10 dB	27 dB	43 dB	20 dB
IIP3	-17 dBm	7 dBm	-5 dBm	7 dBm (OIP3)

Fig. 10.37 Signal-level diagram of the proposed receiver

10.3.9 Transmitter

The output spectrum of the synthesizer in the transmitting mode is shown in Fig. 10.38. The input signal to the modulator is a filtered 270kbps random sequence. The power of modulated RF signal is mainly located within 200kHz double-sided bandwidth.



Single-sided

Double-sided

Res_bw=30kHz

Fig. 10.38 Modulated RF Spectrum

The power amplifier measures an output power of 55mW with a power added efficiency (PAE) of 21%. The output power is 3 dB lower than the simulated value because the output matching network including the bond-wired is not accurate. The PAE is similar to the simulation value.

10.3.10Problem of Clock feed-through from ADC to VCO

The clock frequency of the band-pass sigma-delta ADC is 280 MHz, which has a third-order harmonics at 840 MHz, very close to the VCO frequency, 870 MHz. Because of the digital circuits used in the BPSD, the clock signal inside the ADC is always a square wave signal, no matter the input clock signal is a sine wave or square. Therefore, the power of the third-order harmonic is fixed. 840-MHz harmonic signal is coupled to the VCO and pull the VCO output signal in the first prototype.

To reduce the pulling effect, the digital ground of the ADC circuits is separated from the substrate contact in the second prototype. The substrate under the ADC is connected to an independent ground line. As such, the feed-through of the clock signal to the VCO is reduced.

10.4 Summary

The experimental results together with the specifications are listed in Table 10.3.

Table 10.3 Summary of the Experimental Results and Specifications

Building block	Parameters	specifications	Experimental Results
Receiver Front-end	Sensitivity	- 90 dBm	-90 dBm
	SNR	9 dB	9 dB
	NF	22 dB	22 dB
	Input IP3	- 25.5 dBm	- 25 dBm
	Image rejection	76 dB	79 dB
	Power	N/A	227 mW
LNA	Noise Figure	19 dB	9 dB
	Gain	23 dB	22 dB

Table 10.3 Summary of the Experimental Results and Specifications

Building block	**Parameters**	**specifications**	**Experimental Results**
	Input IP3	-22.5 dBm	- 17 dBm
	Passband	935-960 MHz	935 - 960 Mhz
	Image Rejection	46 dB	50 dB
	Power	60 mW	60 mW
	Vdd	2 V	2 V
Downconversion mixers	IF frequency	70 MHz	70 MHz
	Input bandwidth	1 GHz	1 GHz
	Noise Figure	39 dB	27 dB
	Conversion gain	0 dB	-2 dB
	Input IP3	0.5 dBm	7 dBm
	power	N/A	8 mW
	Vdd	2 V	2 V
Synthesizer	Carrier frequency	935 MHz ~ 960 MHz for RX 890 MHz ~ 915 MHz for TX	780 - 980 MHz
	Phase noise	-109 dBc/Hz @ 600 kHz	- 118 dBc/Hz @ 600kHz
	Loop Bandwidth	200 kHz	200 kHz
	Phase mismatch	$< 1^{o}$	$< 1^{o}$
	Amplitude mismatch	< 0.1 dB	<0.1 dB
	power	N/A	20 mW
	Vdd	1.5 V	1.5 V
IF bandpass filter	Centre frequency	70 MHz	70 MHz
	Bandwidth	200 KHz	200 kHz
	NF	42 dB	43 dB
	IIP3	- 2.5 dBm	- 5 dBm
	Power	< 100 mW	90 mW
	Vdd	2.5 V	2.5 V
VGA	Gain Control Range	78 dB	78 dB
	Power	N/A	15 mW
	Vdd	2.5 V	2.5 V
A/D converters	Centre frequency	70 MHz	70 Mhz
	Input bandwidth	200 KHz	200 kHz

Table 10.3 Summary of the Experimental Results and Specifications

Building block	**Parameters**	**specifications**	**Experimental Results**
	Dynamic range	6 bit	7 bit
	Power	N/A	34 mW
	Vdd	2.5	2.5
PA	Output Power	100 mW	55 mW
	PAE	20%	21%
	Vdd	2.5 V	2.5 V

The experimental results of the transceiver are presented in this chapter. Designed in a standard 0.5-μm CMOS process and without any off-chip component, the receiver achieves a total image rejection of 79 dB, a sensitivity of -90 dBm, and an IIP3 of -25 dBm. With a high IF of 70 MHz, the chip area is only 8.1 mm^2. The measured noise figure and the power consumption are 22 dB and 227 mW, respectively, both of which are high, mainly due to the high-Q channel-selection IF filter and the lossy on-chip inductors.The transmitter has an output bandwidth of about 200 kHz and an output power of 55mW with a PAE of 21%.

Chapter 11

CONCLUSION AND FUTURE WORK

Challenges in integrating a monolithic CMOS transceiver is discussed in this chapter. Key features of the proposed transceiver are also described. A conclusion is drawn and possible improvements of the transceiver is also included.

11.1 Challenges in a Monolithic CMOS Transceiver

A monolithic CMOS transceiver has many advantages. CMOS processes are much cheaper than GaAs or BiCMOS. Because the CMOS processes are compatible with those used in DSP circuits, it is possible to integrate a whole product in one single-chip. As a result, the size of the whole product is smaller and the number of assembling steps of the product is reduced. Therefore, the cost of the product is reduced and more function can be added to the product. However, there are some limitations in the CMOS processes that prevent the monolithic CMOS transceivers from being widely used in modern wireless applications.

A. Lack of High-Q On-chip Inductors

In order to make a transceiver work in applications with receiving band of only 25 MHz, inductive loadings must be used. However, on-chip CMOS inductors usually have very low quality-factors, Q, as low as 2.5. The low-Q inductors introduce a lot of noise to the receiver and decrease the receiver sensitivity. In addition, the gain of the LNA is also reduced because the equivalent parallel resistance of the low-Q inductors is very low. Therefore, the sensitivity of the receiver is degraded further by a larger equivalent input-referred noise.

Q-compensation circuits must be used to compensate the loss due to the on-chip inductors and achieve a high gain in the LNA. However, the noise from the low-Q inductors cannot be removed and the nonlinearity of the Q-compensation circuits may degrade the sensitivity of the receiver as well.

B. High Image Rejection Is Required

A high image rejection is usually required for a receiver with high-IF architecture. Traditionally, it is realized by off-chip image-rejection filters, but they are bulky and cannot be integrated on the same chip. In order to achieve high image rejection in a monolithic CMOS transceiver, an on-chip image-rejection filter is essential.

C. High-Q IF Filter

It is extremely difficult to integrate an on-chip high-Q IF filter. The high-Q IF filter introduces a high noise to the receiver and degrade the receiver sensitivity. The linearity of the high-Q IF filter is also low. Actually, the IF filter is a barrier of the monolithic integration of the transceiver.

D. High Resolution ADC at IF Frequency

In traditional receivers, the received signal is converted to the digital domain at baseband frequencies after a second downconversion mixer. However, the second downconversion mixer also suffers from the problem of image signals. To avoid this problem, it is necessary to have a high resolution ADC at the IF frequency. However, traditional ADCs cannot achieve the required resolution at the IF frequency of 70MHz.

E. Cross-Coupling Between Digital Circuits and Analog Circuits

Because CMOS processes have high conductive substrates, the noise coupling from digital circuits to the analog front-end is very high. The high substrate noise will degrade the noise performance of the RF front-end. A careful layout and floor plan must be done to reduce the cross coupling as much as possible.

11.2 Key Features of the Proposed Transceiver

The proposed transceiver is a monolithic CMOS transceiver with on-chip inductors. It has a high-IF architecture with I-Q downconversion mixers and on-chip RF and IF filters. It has a direct-modulation transmitter with a sigma-delta modulated fractional-N frequency synthesizer, which is shared by the receiver as well. In addition. it has the following key features to overcome the challenges mentioned above.

A. LNA and Notch Filter

Unbalanced -Gm cells are used in the LNA as Q-compensation circuits to compensate the loss due to the low-Q on-chip inductors. A constant negative g_m is obtained in a large dynamic range. As such, the linearity of the Q-compensation circuits are increased. With the Q-compensation circuits, a bandwidth of 25 MHz and a gain of 22 dB are achieved.

A third-order notch filter is used to improve the image rejection of the LNA to 50 dB and the total image rejection of the receiver to 79 dB, which is high enough to eliminate the external image-rejection filter.

Switched-capacitor arrays are used in the LNA to tune the center frequency which may be shifted by the process variations. The SCAs have less noise contribution, better linearity and smaller power consumption compared with other frequency tuning techniques, e.g. Miller-capacitors.

B. Synthesizer

A fractional-N frequency synthesizer with sigma-delta modulation is used to achieve a fine frequency resolution. Switched-capacitor arrays are used in the VCO to achieve a fast switching. The synthesizer can work as a direct-modulation transmitter to reduce the chip area and save power consumption in the transmitter.

C. Mixer

A highly-linear mixer, with source followers as current modulator, is used in the receiver to improve the linearity and reduce the supply voltage.

D. IF Filter

A high-Q Gm-C filter is used to select the IF signal and suppress the interferences. A high Q of 350 is achieved with Q-compensation circuits. However, the noise figure of the filter is as high as 43 dB and the IIP3 is only - 5 dBm, which limit the receiver sensitivity.

E. VGA

High gain amplifiers usually suffer a problem from DC offset voltage, which can be more than 10 mV in CMOS circuits. A continuous-time offset cancellation technique is adopted in the VGA to suppress the DC offset so that the VGA will not be saturated by the offset voltage.

F. Bandpass Sigma-Delta ADC

A bandpass sigma-delta ADC is used to convert the IF signal to digital domain. It can achieve a high resolution of 7 bits at high frequency of 70 MHz.

11.3 Conclusion

According to the author's knowledge, the proposed transceiver is the first truly monolithic integration. The receiver doesn't use any external component and still achieves a high image rejection of 79 dB, which is the best ever reported, and a small chip area of 8.1mm^2. Because of the fully-differential topology and the high level of integration, in particular the integration of a high-Q bandpass IF filter and the use of all on-chip low-Q inductors, the noise figure, linearity, and power consumption are not as good as other work [1]-[4]. However, the sensitivity achieved is still as good as -90 dBm, and the performance still meet specifications for short-distance wireless receivers. The power consumption is rather

high but could be significantly reduced if the proposed receiver is designed in a more advanced CMOS process with higher-Q on-chip inductors or uses a single-ended topology for the front-end. A direct-modulation transmitter is also implemented on-chip with sigma-delta modulated fractional-N frequency synthesizer.

11.4 Future Work

The proposed receiver can achieve a sensitivity of -90 dBm, which can be used for short-distance wireless communications. The sensitivity is limited by the high-Q on-chip IF Gm-C filter. Gm-C filter is chosen in this design because it can work at high IF frequency 70 MHz. However the linearity and noise figure of the high-Q Gm-C filter are not good and limit the receiver performance. In the future, switched-cap filters, L-C filters and low-IF architectures can be considered to improve the receiver performance.

Currently the switched-cap filter cannot work at 70 MHz because the unit-gain frequency of the amplifier used in the switched-cap filter is not high enough. With more advanced technology in the future, the parasitic capacitance can be reduced with smaller device size. As a result, the unit-gain frequency of the amplifier can be improved. Therefore, it is possible to implement a switched-cap filter at 70 MHz.

L-C filters cannot be used for the IF filter at this moment because on-chip inductor with large inductance and high Q are not available. Bond-wire inductors can achieve high inductance with higher Q. However, they will increase the cost and reduce the yielding efficiency. If large inductors with higher Q are available in the future with more advanced technologies, L-C filters are also potential solutions for the IF filter.

The noise figure and the linearity of the Gm-C filter is limited by the large Q. Therefore, it is possible to improve the performance of the filter by using lower IF and reducing the Q requirement of the filter. Although the image rejection achieved from the IRF

will be reduced, the image rejection can still be improved by using double quadrature architecture [70] [71].

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