Hong Kong University of Science and Technology

A 2-V 900-MHz Monolithic CMOS Dual-Loop Frequency Synthesizer for GSM Receivers

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by

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Abstract

This master thesis presents the design of a 2-V 900-MHz monolithic CMOS dual-loop frequency synthesizer for GSM receivers with good phase-noise performance.

Designing fully integrated frequency synthesizers for system integration is always desirable but most challenging. This first requirement is to achieve high frequency operation with reasonable power consumption. However, the most critical challenges for the frequency synthesizer are the phase-noise and spurious-tone performance. Finally, small chip area is essential to monolithic system integration.

The dual-loop design consists of two reference signals and two phase-locked loops (PLLs) in cascode configuration. Because of the dual-loop architecture, input frequencies of the two PLLs are scaled from 200 kHz to 1.6 MHz and 11.3 MHz. Therefore, the loop bandwidths of both PLLs can be increased, so that both switching time and chip area can be reduced.

Implemented in a 0.5-μm CMOS technology and at 2-V supply voltage, the dual-loop frequency synthesizer has a low power consumption of 34 mW. At 900 MHz, the phase noise of the dual-loop design is less than -121.83 dBc/Hz at 600-kHz frequency offset. The spurious tones are -79.5 dBc@1.6MHz, -82.0 dBc@11.3MHz and -82.88 dBc@16MHz. The worst-case switching time is less than 830 μs. The chip area is 2.64 mm^2. However, the peak close-in phase noise is -65.67 dBc/Hz at 15-kHz frequency offset which is 15 dB worse than the specification of GSM 900.

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I would like to take this opportunity to express my gratitude to many individuals who have given me a lot of supports during my master program in the HKUST.

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Table of Contents

List of Figures

List of Tables

Chapter 1

Introduction

1.1 Motivation: Single-Chip GSM Receiver

In recent years, the rapid development of mobile radio systems leads to an increasing demand of low-cost high-performance communication integrated circuits. For the GSM receiver front-end as shown in Figure 1.1, the RF-input signal (935.2 ~ 959.8 MHz) is first filtered by LNA and RF-filter, down-converted by mixers to intermediate frequency IF of 70 MHz for base-band signal processing. The function of the frequency synthesizer is to generate local oscillator LO signal (865.2 ~ 889.8 MHz) for channel selection. In order to develop the monolithic CMOS GSM receiver front-end, CMOS RF building blocks including low-noise amplifiers LNAs, RF-band-pass filters, down-conversion mixers and frequency synthesizers are

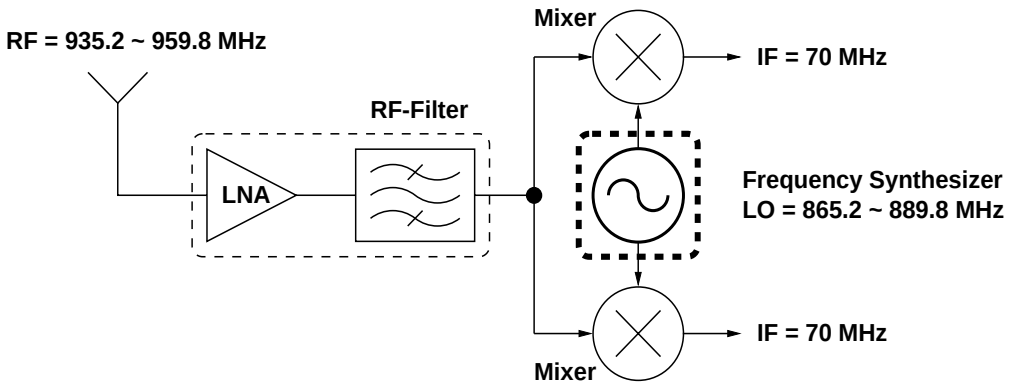


Figure 1.1 Block diagram of the GSM receiver front-end.

needed. However, despite of much progress in designing LNAs [1] and mixers [2], only little results on frequency synthesizers that meet GSM specifications have been reported [3].

1.2 Operating Principle of Phase-Locked Loop

Phase-Locked Loop PLL is a circuit in which the phase of a local oscillator is locked to the phase of an external signal. As shown in Figure 1.2, PLL consists of a crystal oscillator XTAL, a phase-frequency detector PFD, a charge pump CP, a loop filter LF, a voltage-controlled oscillator VCO, and a programmable frequency divider. Crystal oscillator aims to provide an accurate and clean input reference signal to the frequency synthesizer. Then, phase-frequency detector compares the phase and frequency difference between the reference signal and the output signal of programmable frequency divider. According to the phase and frequency difference, the charge pump injects appropriate current to adjust the control voltage of the VCO. The loop filter filters out the high frequency components and extracts the average VCO control voltage to improve the spectral purity of the VCO output. The VCO is adjusted by the loop so that phase of VCO and that of input reference become matched. In order to program the output frequency at desired channels (865.2 ~ 889.8 MHz) with a fixed input reference (200 kHz), a programmable frequency divider (N = 4326 ~ 4449) is included in the feedback path.

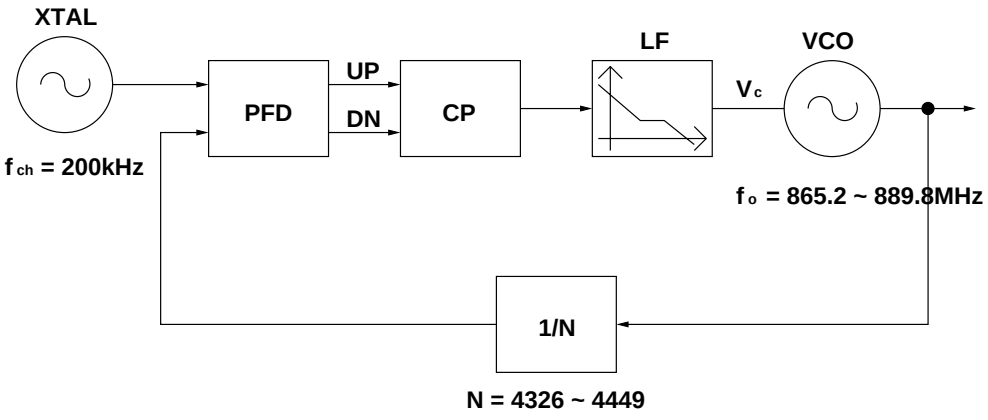


Figure 1.2 Block diagram of the single-loop frequency synthesizer.

1.3 Problems of Single-Loop Frequency Synthesizer

Although frequency synthesizers can be simply built by a phase-locked loop PLL with programmable divider in the feedback path, the single-loop design has the following problems.

1.3.1 Long Switching Time

For the single-loop design, the input reference frequency (f_{ref}) is equal to the channel spacing (f_{ch} = 200 kHz). Therefore, the loop bandwidth of the synthesizer is limited to be one tenth of the channel spacing (f_u < 20 kHz) for loop stability consideration [4]. In addition, because of the small reference frequency, the loop bandwidth should be further reduced in order to meet reference spurious-level specification which will be mentioned in Section 2.2.2. Since the loop bandwidth is reduced according to the reference frequency, the long loop settling time limits the switching time of the frequency synthesizer.

1.3.2 Large Chip Area

Similar to the cause of long switching time, the loop bandwidth is small because of the small reference frequency. Therefore, to implement the loop filter, very large capacitors (> 10 nF) and resistors (> 100 kΩ) are required. For example, a 1-nF capacitor needs around 1 × 1-mm^2 chip area. Therefore, a large chip area is required, which makes the monolithic implementation of the single-loop frequency synthesizer not feasible.

1.3.3 Large Frequency-Division Ratio

Due to the large difference between the reference frequency which is fixed by the channel spacing and the output frequency which is defined by the GSM receiver band, large frequency-division ratios (4326 ~ 4449) are required. As a results, the design of the programmable frequency divider becomes very complicated and inefficient.

1.4 Goals of the Project

After the discussion of the problems of the single-loop frequency synthesizer, the follows are the goals of this master project.

1.4.1 Higher Input Frequency

As the loop bandwidth of synthesizers is limited by input frequency for stability consideration and spurious-level requirement, the input frequency should be increased in order to achieve faster settling time, smaller loop-filter area, and thus make the monolithic implementation more feasible.

Although a larger loop bandwidth can improve the in-band phase-noise contribution of the voltage-controlled oscillator, the most critical phase noise requirement is -141 dBc/Hz at a frequency offset of 3 MHz. However, the loop bandwidth is limited to be 27 kHz in this design which is limited by spurious-tone specification as discussed in Section 4.9.4. Therefore, the increase in input reference frequency is not for VCO phase-noise suppression.

1.4.2 Lower Frequency-Division Ratio

As the number of GSM channels is 124, the frequency division ratio of the programmable frequency divider should be reduced to make the divider implementation less complicated and efficient.

1.4.3 Lower Supply Voltage

As the improvement in device technology is very rapid, device performance becomes better in terms of speed and power consumption for digital circuits. Most digital circuits (e.g. DSP) can function at a lower supply voltage for the same system requirement. Therefore, a lower supply voltage is also desirable for the analog parts of the GSM receiver front-end to achieve better compatibility to the digital part of the receiver.

Although speed is improved by device scaling, the breakdown voltage of devices is scaled down at the same time. By designing at a lower supply voltage, the reliability of the synthesizer can be improved if the synthesizer is implemented by deep-submicron process in the future.

1.5 Thesis Overview

This thesis is divided into 7 parts. The first chapter is the introduction of the single-loop frequency synthesizer and its problems. Chapter 2 derives and shows the design specification of the frequency synthesizer, such as phase noise, spurious tones and switching time, for its application in a GSM receiver front-end. Chapter 3 presents the architecture of the dual-loop frequency synthesizer proposed in [7] and shows how the dual-loop design can improve switching speed, chip area and frequency-divider complexity. Based on the system specification, Chapter 4 shows the circuit implementation and design optimization of the dual-loop frequency synthesizer, including, LC-oscillator, frequency dividers, mixer, ring oscillator, phase-frequency detectors, charge pumps and loop filters. After the design issues, Chapter 5 discusses the layout techniques and floor planing of the frequency synthesizer. To verify the design and analysis, the measurement results of the synthesizer's performance, in terms of phase noise, spurious tones and switching time, are presented in Chapter 6. At the end, conclusion is drawn in Chapter 7.

Chapter 2

Design Specification

2.1 Blocking Profile of GSM 900

In receiver band for GSM specification, which is 25 MHz wide, ranges from 935 to 960 MHz. It consists of 124 channels with channel bandwidth of 200 kHz. The center frequencies of the channels ($f_{channel}$) are

$$f_{channel} = 935.2 + 0.2 \cdot (N - 1) \text{ MHz} \quad (2.1)$$

where N = 1, 2,..., 124.

Figure 2.1 shows the profile of the blocking and adjacent signals of GSM 900 [5]. The minimum power of the desired RF signals can be as low as -102 dBm. Around the desired channel, the adjacent-channel power at ±200-kHz, ±400-kHz and ±600-kHz frequency offset are 9 dB, 41 dB and 49 dB above the desired signal respectively. Beside the adjacent channels, blocking signals exist at ±600-kHz, ±1.6-MHz and ±3-MHz frequency offset with power of -43 dBm, -33 dBm and -23 dBm respectively. Outside the receiver band, the power of blocking signals can be up to 0 dBm. If the LNA and the RF filters provide sufficient filtering of out-of-band blocking signals, the effect of these blocking signals can be ignored.

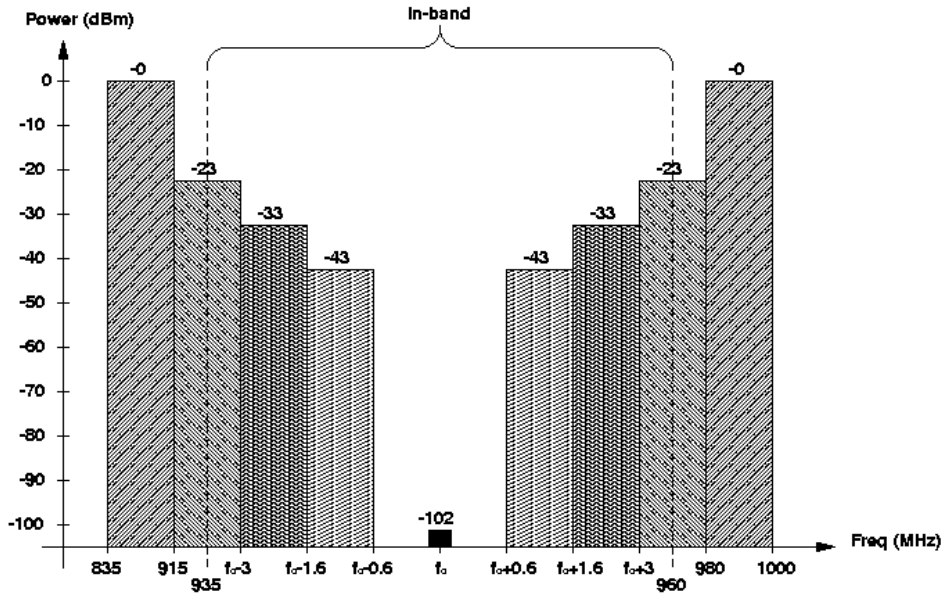


Figure 2.1 Blocking profile for GSM 900.

2.2 Design-Specification Derivation

For GSM receiver front-end application, frequency synthesizer can be characterized by the phase noise, spurious tones and switching speed. Their specifications are discussed in this chapter.

2.2.1 Phase Noise

Phase noise is characterized in the frequency domain. For an oscillator operating at frequency ω_o, the VCO output can be expressed as

$$V_o = A \cdot \sin(\omega_o t + \theta(t)) \tag{2.2}$$

where A is the output amplitude, and $\theta(t)$ is the output phase which is time-varying due to the existence of phase noise. Due to random phase fluctuations, the VCO-output spectrum has side-band noise close to the oscillation frequency as shown in Figure 2.3.

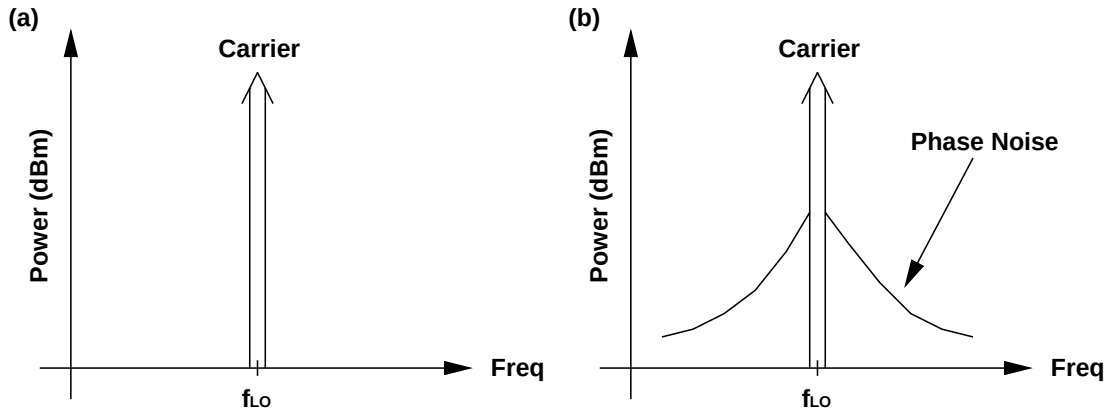


Figure 2.2 (a) Ideal VCO output spectrum and (b) VCO spectrum with phase noise.

Phase noise is quantified by the ratio between the carrier power and the noise power within a unit bandwidth at certain offset frequency $\Delta\omega$. The single-side-band phase noise $L\{\Delta\omega\}$is in units of decibel carrier per Hertz (dBc/Hz):

$$L\{\Delta\omega_o\} = 10 \cdot \log\left(\frac{\text{noise power in a 1-Hz bandwidth at frequency } \omega_o + \Delta\omega}{\text{carrier power}}\right) \qquad (2.3)$$

In a GSM receiver front-end, desired signals are down-converted by the LO signal to the IF frequency. However, blocking signals are also down-converted by the LO signal and the phase noise at the same time as shown in Figure 2.3. Since the power of the blocking signals shown in Figure 2.1 typically can be much larger than that of the desired signal, the phase-noise power of the blocking signals, which falls in the IF frequency, at the mixer output becomes dominant unless the phase noise is small enough. Therefore, given specifications on the blocking signals and minimum SNR, there exists a maximum phase noise requirement for the synthesizer.

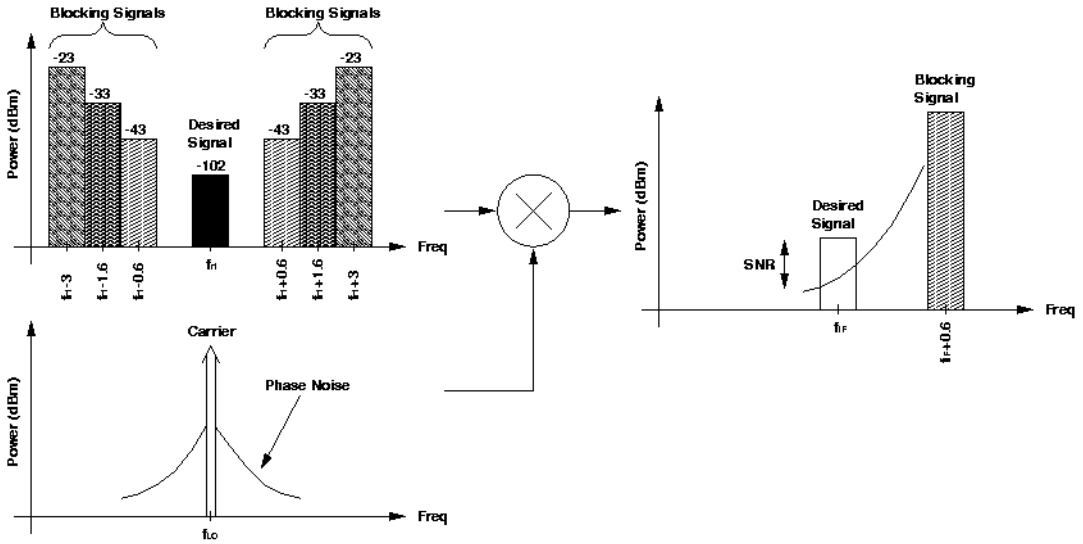


Figure 2.3 Degradation of SNR due to phase noise.

To derive the phase-noise specification, SNR is calculated with the effect of phase noise. Assume the conversion gain of down-conversion mixer to carrier and phase noise are the same, and power spectral density of phase noise is flat within a channel, the SNR is calculated as follows

$$\begin{aligned} SNR &= S_{desired} - S_{phase-noise} \\ SNR &= S_{desired} - (S_{block} + \mathrm{L}\{\Delta\omega\} + 10 \cdot \log(f_{ch})) \end{aligned} \tag{2.4}$$

where $S_{desired}$ is the power of desired signal, $S_{phase\text{-}noise}$ is the noise power due to phase noise, S_{block} is the power of blocking signal, f_{ch} is the channel bandwidth. To meet the GSM requirement, the required SNR (SNR_{req}) must be larger than 9 dB. Therefore, the phase-noise requirement of the frequency synthesizer is -121 dBc/Hz at 600-kHz frequency offset.

$$\begin{aligned} & S_{desired} - (S_{block} + \mathrm{L}\{\Delta\omega\} + 10 \cdot \log(f_{ch})) > SNR_{req} \\ & \mathrm{L}\{\Delta\omega\} < S_{desired} - S_{block} - SNR_{req} - 10 \cdot \log(f_{ch}) \\ & \mathrm{L}\{\Delta\omega\} < -102 - (-23) - 9 - 10 \cdot \log(200\times10^{3}) \\ & \mathrm{L}\{\Delta\omega\} < -121 \text{ dBc/Hz@600kHz} \end{aligned} \tag{2.5}$$

The same method shows the phase noise specification at offset frequencies of 1.6 MHz and 3 MHz are -131 and -141 dBc/Hz respectively. Assuming a dependence of 20 dB per decade on offset frequency [3], the most critical phase-noise requirement which is referred to 600-kHz frequency offset is actually at the 3-MHz frequency offset (-127 dBc/Hz@600kHz). However, the state of the art on-chip voltage-controlled oscillator still cannot meet phase-noise specification at 3-MHz offset [6]. Therefore, this synthesizer is designed to satisfy the phase-noise requirement only at 600-kHz frequency offset.

2.2.2 Spurious-Tone Specification

According to Figure 1.2, the phase-frequency detector and the charge pump in the synthesizer operate at input reference frequency (f_{ref}). They modulate the input control node of the VCO at f_{ref} due to the incomplete spurious-tone filtering of the loop filter. Consequently, the VCO output signal is FM modulated and includes a pair of spurious tones at a frequency offset of f_{ref} as shown in Figure 2.4.

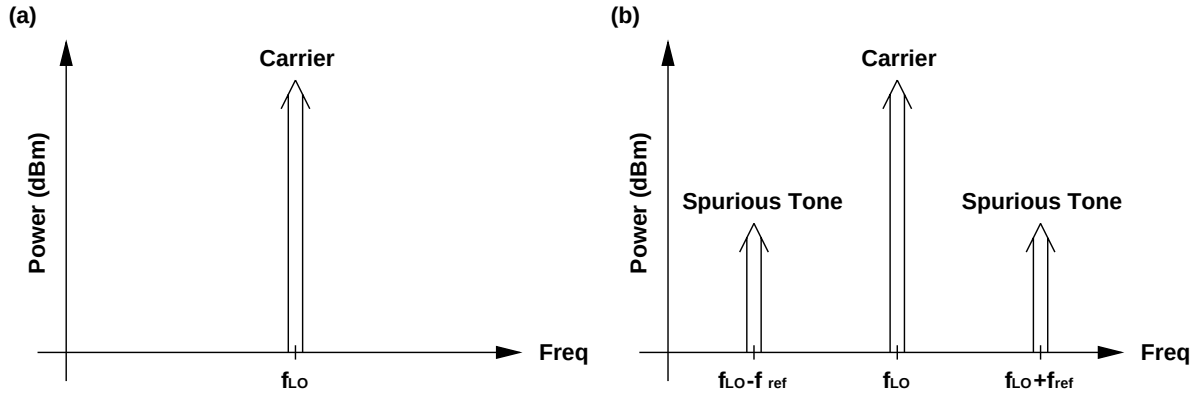


Figure 2.4 a) Ideal VCO output spectrum and (b) VCO spectrum with spurious tones.

Due to the existence of spurious tones, blocking signals, which are located at f_{ref} away from the desired signals, are also down-converted to the IF frequency. Since the power of the blocking signal can be very large, the interference at the IF frequency due to the blocking signals and spurious tones can overwhelm the desired signals. Therefore, spurious tones need

to be kept minimal in order not to degrade the SNR significantly.

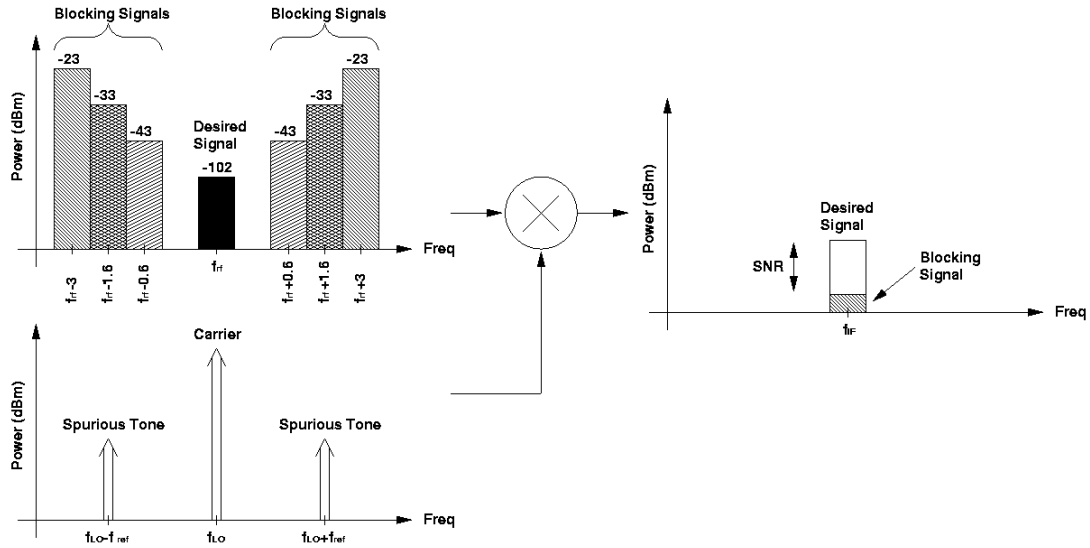


Figure 2.5 Degradation of SNR due to spurious tone.

The derivation of spurious-tone specification is similar to that of phase-noise specification except the channel bandwidth is not included.

$$\begin{aligned} SNR &= S_{desired} - S_{spur} \\ SNR &= S_{desired} - (S_{block} + S) > SNR_{req} \\ S &< S_{desired} - S_{block} - SNR_{req} \\ S &< -102 - (-23) - 9 = -88 \text{ dBc} \end{aligned} \tag{2.6}$$

where S_{spur} is the noise power due to spurious tone. As shown, the maximum spurious-tone requirement (S) of the frequency synthesizer for a SNR of 9 dB is -88 dBc.

2.2.3 Switching Time

Although GSM 900 is globally a frequency-division-multiple-access (FDMA) system, time-division-multiple-access (TDMA) is adopted within each frequency channel. As shown in Figure 2.6, each frequency channel is divided into 8 time slots, each of which is 577 μs long. In time slot #1, signal is received. Then, signal will be transmitted in time slot #4. For system monitoring purpose, a time slot between slot #6 and slot #7 is occupied. The most critical

switching time is from transmission period (slot #4) to system-monitoring period (between slot #6 and slot #7). Therefore, the settling-time requirement of the frequency synthesizer is 1.5 time slots which is equal to 870 μs. As a consequent, to meet the specification with a frequency step of 100 MHz and frequency accuracy of 100 Hz, minimum loop bandwidth of a first-order loop is 3.1 kHz.

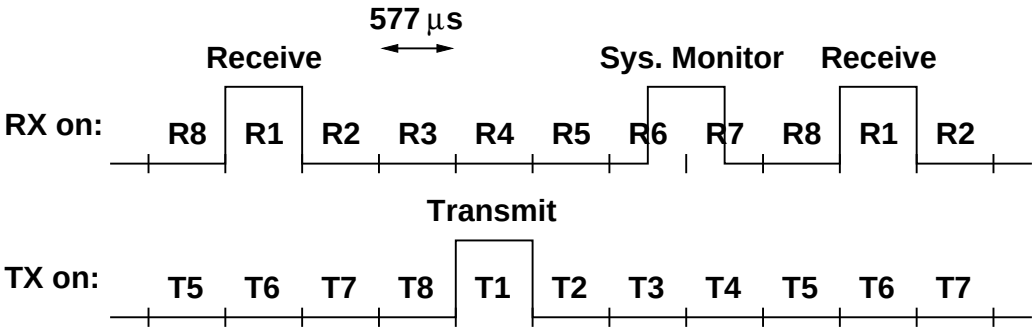


Figure 2.6 GSM 900 receive (RX) and transmit (TX) time slots.

Table 2.1 summaries the design specifications of the frequency synthesizer for GSM receiver application. The requirement derivation of phase noise, spurious tones and switching time are explained in the previous sections. The supply voltage is reduced to 2 V for better digital-circuit compatibility and better reliability for device scaling down to deep-submicron process. The power consumption is designed not to be larger than what has been reported [3]. The chip area is limited to be less than 2×2 mm^2 which is the minimum chip size of the process.

Parameters	Specification
Phase Noise	< -121 dBc/Hz@600kHz
Spurious Tones	< -88 dBc
Settling Time	< 870 μs
Supply Voltage	2 V
Power	< 50 mW
Area	$< 2 \times 2$ mm^2
Process	HP 0.5-μm CMOS

Table 2.1 Design specifications of the frequency synthesizer.

The synthesizer is implemented by HP 0.5-μm CMOS process which provides linear capacitor and silicide-blocked polysilicon for the implementation of the on-chip loop filters.

Chapter 3

Dual-Loop Frequency Synthesizer

3.1 Architecture of Dual-Loop Design

To reduce the chip area and switching time, a higher input-reference frequency is desired. Moreover, to improve frequency-divider complexity, a lower frequency-division ratio is desirable for the programmable divider. Therefore, a dual-loop frequency synthesizer is considered [7]. As shown in Figure 3.1, the proposed dual-loop synthesizer to be designed and presented in this thesis consists of two crystal oscillators and two phase-locked loops connected in series. The low-frequency loop (LFL), which is on the left hand side, has a programmable frequency divider N_1 for channel selection. The high-frequency loop (HFL), which is on the

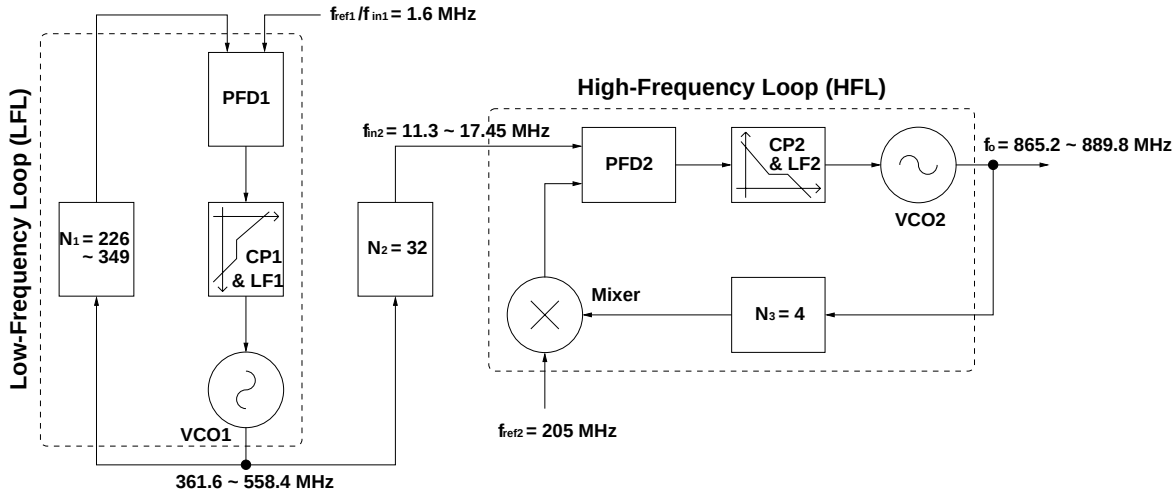


Figure 3.1 Block diagrams of the proposed dual-loop frequency synthesizer.

right hand side, has a down-conversion mixer in its feedback path to provide a constant frequency offset at the output. In between LFL and HFL, a fixed frequency divider N_2 is included for phase-noise and spurious-tone suppression of the low-frequency loop

When both phase-locked loops lock, the output frequency (f_o) of synthesizer is expressed as follows

$$f_o = N_3 f_{ref2} + N_1\left(\frac{N_3}{N_2}\right) f_{ref1} = 865.2 \sim 889.8 \text{ MHz} \tag{3.1}$$

where f_{ref1} and f_{ref2} are reference frequencies of two crystal oscillators, N_1 is the division ratio of the programmable frequency divider, N_2 and N_3 are division ratios of the fixed frequency dividers. The output frequency can be expressed in terms of constant frequency offset (f_{offset}) and channel spacing (f_{ch}) as follows.

$$f_o = f_{offset} + N_1 f_{ch} \tag{3.2}$$

By mapping the terms in (3.1) and (3.2), the offset frequency f_{offset} and the channel spacing f_{ch} can then be expressed in terms of the PLL parameters.

$$f_{offset} = N_3 f_{ref2} = 4 \times 205 = 820 \text{ MHz} \tag{3.3}$$

$$\begin{aligned} f_{ch} &= \left(\frac{N_3}{N_2}\right) f_{ref1} \\ \Rightarrow f_{ref1} &= \left(\frac{N_2}{N_3}\right) f_{ch} = \left(\frac{32}{4}\right) \cdot 200\text{k} = 1.6 \text{ MHz} \end{aligned} \tag{3.4}$$

From (3.3), the offset frequency is designed at 820 MHz so that the frequency-division ratios of N_2 and N_3 are multiples of 2 which makes the implementation of the frequency dividers much easier. From (3.4), it can be found that the input reference frequency of the low-frequency loop (f_{ref1}) is increased by 8 times which is limited by the frequency range of the VCO in the

low-frequency loop as discussed in Section 3.3.1. The increase in reference frequency relaxes the loop-bandwidth requirement.

3.2 Advantages of the Dual-Loop Design

3.2.1 Smaller Chip Area and Faster Switching Time

Due to the dual-loop architecture, input frequencies of both low-frequency and high-frequency loops are scaled up to f_{in1} = 1.6 MHz and f_{in2} = 11.3 ~ 17.45 MHz respectively. Therefore, the loop bandwidths of both PLLs can be increased to achieve smaller chip area and faster settling time.

3.2.2 Simpler Programmable-Frequency-Divider Design

As a down-conversion mixer is included in the feedback path of the high-frequency loop, a constant frequency offset (f_{offset}) is created by the second reference frequency (f_{ref2}). Therefore, the frequency-division ratio of the programmable divider N_1 can be reduced from 4236 ~ 4449 to 226 ~ 349. The reduced division ratio simplifies the design and reduces phase-noise contribution from input reference.

3.3 Potential Disadvantages of the Dual-Loop Design

3.3.1 Requirement of a Larger VCO-Tuning Range

Although the low-frequency-loop input frequency is scaled up from 200 kHz to 1.6 MHz, the frequency-tuning range of the VCO1 in the low-frequency loop is scaled up from 25 MHz to 200 MHz at the same time which corresponds to an increase in the tuning range from 4% to 33%. Because of the large frequency-tuning range requirement, LC-oscillators cannot be adopted and only ring oscillators can be used. It is very challenging to design a ring oscillator with low phase noise (-103 dBc/Hz@600kHz), high frequency (600 MHz), and wide

tuning-range (50%).

3.3.2 Additional Chip area and Phase Noise

Since the dual-loop design consists of two PLLs, the additional PLL may require extra chip area and contribute extra phase noise and spurious tones. However, as the combination of frequency dividers N_2 and N_3 provides 18-dB suppression of phase-noise and spurious-tone contributed by the low-frequency loop, the design specification of the low-frequency loop is relaxed. Therefore, phase-noise contribution from the LFL is suppressed and a smaller loop filter can be adopted to achieve the same spurious-tone requirement. Phase-noise and spurious-tone performance of the whole frequency synthesizer is dominated by that of the high-frequency loop.

3.3.3 Long Switching Time

As the dual-loop design has two PLLs in cascade configuration, the switching time of the dual-loop design is slower than a single-loop design. However, the switching-time requirement of the GSM receiver is 865 μs which is not very fast. Therefore, if both low-frequency and high-frequency loops have loop bandwidth larger than 6 kHz, the switching-time requirement can be satisfied.

3.3.4 Image-Output Frequency

Due to the existence of the down-conversion mixer in the feedback path of the high-frequency loop, the proposed synthesizer can also be locked at the image-output frequency $f_{o\text{-}image}$

$$f_{o-\text{image}} = N_3 f_{ref2} - N_1\left(\frac{N_3}{N_2}\right) f_{ref1} = 750.2 \sim 774.8 \text{ MHz} \quad (3.5)$$

Fortunately, the VCO of the high-frequency loop is implemented by a LC oscillator which does

not operate in the image-output frequency range. Therefore, image-rejection mixer is not required for the implementation of the down-conversion mixer.

3.3.5 Additional Design Effort

As the proposed dual-loop frequency synthesizer consists of two VCOs, two loop filters, three frequency dividers, two PFDs, two charge pumps and a down-conversion mixer, more design effort is required.

Chapter 4

Circuit Implementation

4.1 Introduction

In this chapter, circuit implementation of all the building blocks of the dual-loop frequency synthesizer is discussed. Analysis, design and simulation results of the circuit are presented for each building block. In the first part of this chapter, building blocks of the high-frequency loop, including the voltage-controlled oscillator VCO2, the frequency dividers N_2 and N_3, and the down-conversion mixer are analysed and discussed. Then the building blocks of the low-frequency loop, including the voltage-controlled oscillator VCO1, and the programmable frequency N_1 are described. After that, the blocks common in both PLLs, such as phase-frequency detectors PFDs, charge pumps CPs, and loop filters LFs are discussed. At the end, the simulation and estimated results of the dual-loop frequency synthesizer will be presented.

4.2 Voltage-Controlled Oscillator VCO2

4.2.1 Design Requirement

Voltage-controlled oscillator VCO2, which generates output frequency, locates in the high-frequency loop as shown in Figure 4.1. The design requirement of VCO2 is as follows

- It should cover the output frequencies from 865.2 to 889.8 MHz.
- It should satisfy the phase-noise performance -121 dBc/Hz@600kHz with minimum power consumption.
- It should generate output signals with single-ended amplitude larger than 0.5 V to drive the fixed frequency divider N_3.

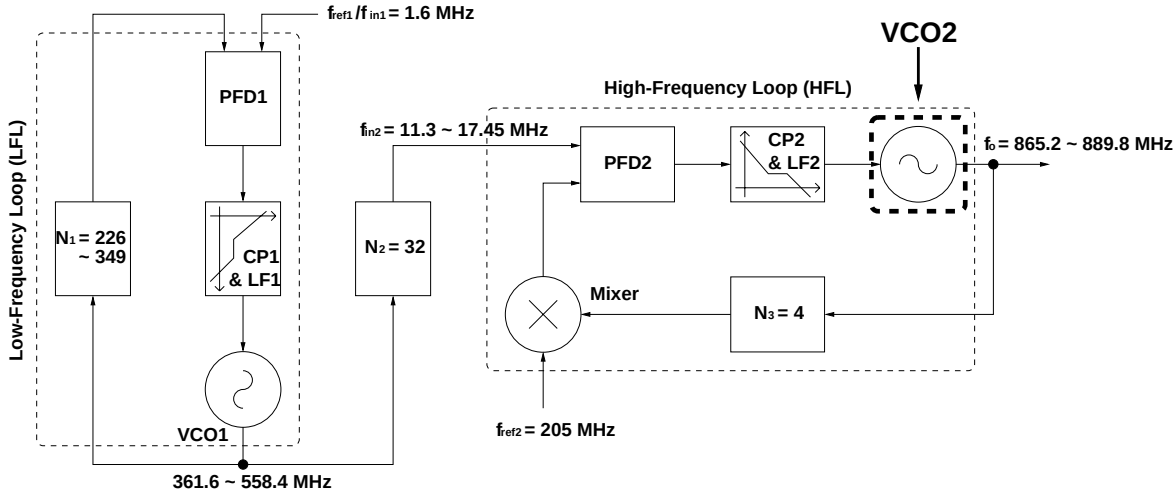


Figure 4.1 Location of the LC-oscillator VCO2.

4.2.2 Circuit Implementation

VCO2 is implemented by an LC-oscillator because the required frequency-tuning range is only 25 MHz (3-% tuning range) and because the phase-noise performance of LC-oscillator is much better than ring oscillator in general [3].

Figure 4.2 shows the circuit schematic of the LC-oscillator. It consists of on-chip spiral inductors and pn-junction varactors for frequency tuning, cross-coupled NMOS transistors pair (M_{n1}) for oscillation start-up, and current source (M_{b1}) for biasing purpose. The output common mode voltage of this oscillator is equal to gate-to-source voltage of transistors M_{n1} (V_{gsn1}) which is good for driving the fixed frequency divider N_3. For another oscillator configuration in Figure 4.3, the pn-junction varactors, which is more reverse biased, has less N-well region. Therefore, the pn-junction varactors have reduced resistance and higher quality factor (15 ~ 20) than that of Figure 4.2 (5 ~ 10). However, the design in Figure 4.3 has output common voltage at V_{dd} which is not good for driving the next stage. In addition, PMOS current source is used in

the design of Figure 4.2 to reduce flicker-noise component. Therefore, the oscillator configuration in Figure 4.2 is adopted.

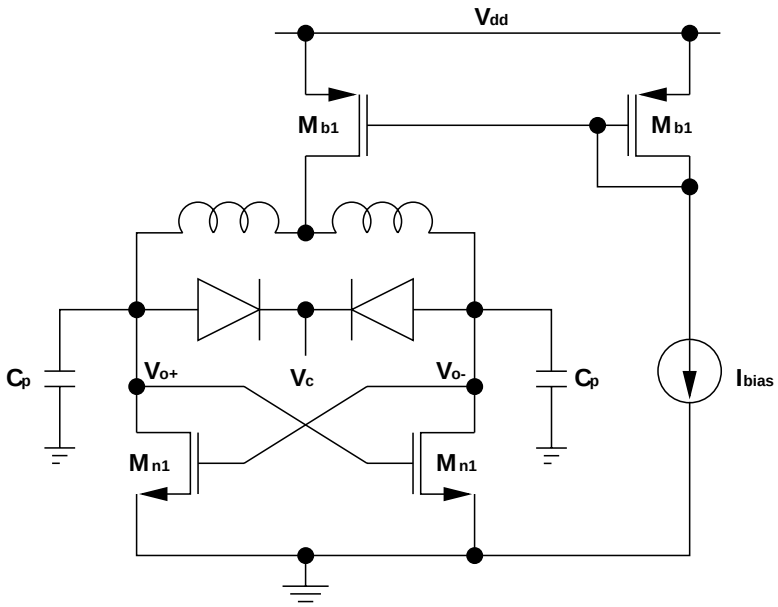


Figure 4.2 Circuit implementation of the LC-oscillator VCO2.

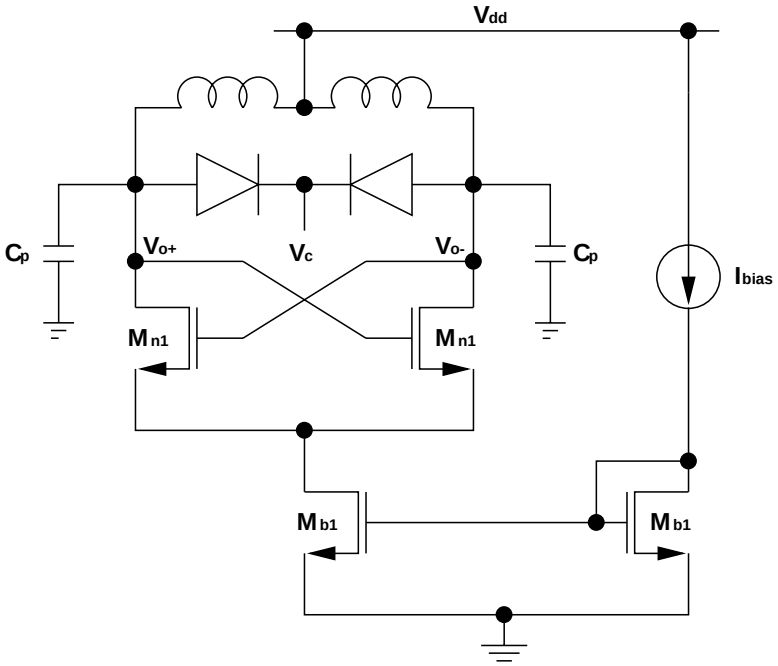


Figure 4.3 Another possible implementation of the LC-oscillator.

4.2.3 LC-Oscillator Analysis

To analyse the power consumption, oscillating frequency and phase noise of the

LC-oscillator, the linear circuit model of the LC tank in Figure 4.4 is used. The model consists of an on-chip inductor, pn-junction varactor and the parasitics of transistor M_{n1}.

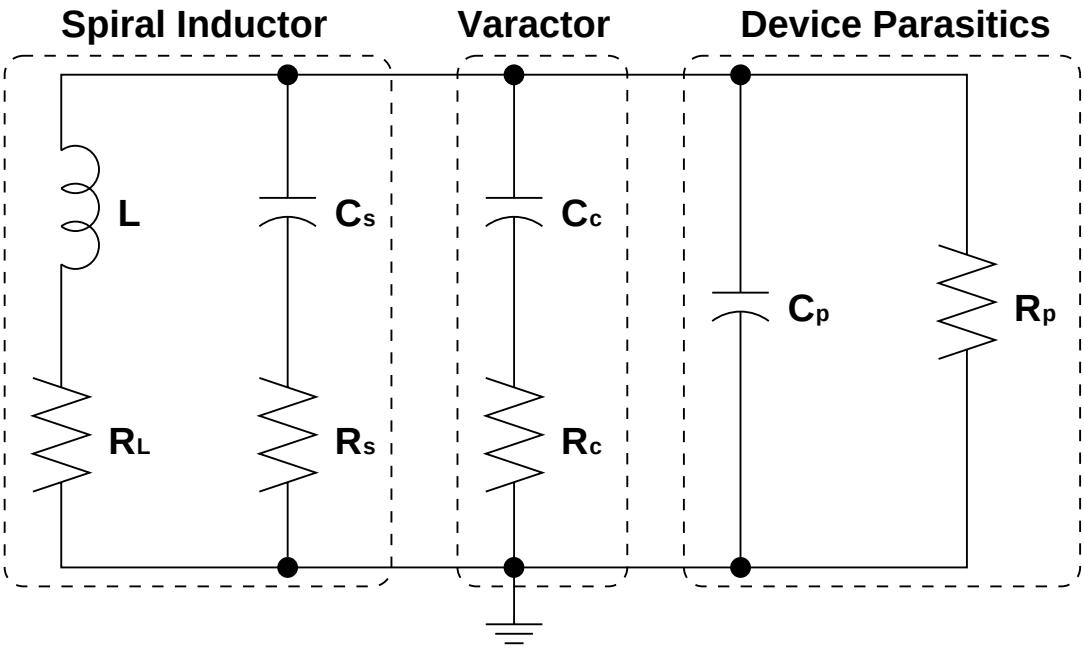


Figure 4.4 Linear circuit model of the LC tank.

The single-ended output admittance of the LC-tank $Y_{LC}\{\omega\}$ is expressed as follows

$$Y_{LC}\{\omega\} = \left\{\frac{R_L}{R_L^2 + (\omega L)^2} + \frac{R_s(\omega C_s)^2}{1 + (\omega R_s C_s)^2} + \frac{1}{R_p} + \frac{R_c(\omega C_c)^2}{1 + (\omega R_c^2 C_c^2)}\right\} + j\omega \cdot \left\{\frac{-L}{R_L^2 + (\omega L)^2} + \frac{C_s}{1 + (\omega R_s C_s)^2} + C_p + \frac{C_c}{1 + (\omega R_c^2 C_c^2)}\right\} \quad (4.1)$$

where L, R_L, C_s, R_s are inductance, series resistance, substrate capacitance, series substrate resistance of the on-chip spiral inductor respectively, C_c and R_c are capacitance and series resistance of the pn-junction of varactor respectively, C_p and R_p are the device parasitics of transistor M_{n1}.

4.2.3.1 Power Consumption

The minimum transconductance G_{m_min} of the transistors M_{n1}, which starts the oscillation, should be larger or equal to the real part of LC-tank admittance $Real[Y_{LC}\{\omega\}]$ [8].

$$G_{m\_min} \geq Real[Y_{LC}\{\omega\}] \tag{4.2}$$

To ensure the oscillation start-up against any process variation, transconductance of M_{n1} (g_{mn1}) is designed to be twice larger than the minimum transconductance G_{m_min}. Since transconductance is directly proportional to the square root of current, then the power consumption of the oscillator can be expressed as follows

$$\begin{aligned} g_{mn1} &= \sqrt{2\mu_n C_{ox}(W/L)_n I_{dn1}} = 2G_{m\_min} \\ Power &= 2V_{dd}I_{dn1} = \frac{4V_{dd}G_{m\_min}^2}{\mu_n C_{ox}(W/L)_{n1}} \\ Power &= \frac{4V_{dd}}{\mu_n C_{ox}\left(\frac{W}{L}\right)_{n1}} \cdot \left\{ \frac{R_L}{R_L^2 + (\omega L)^2} + \frac{R_s(\omega C_s)^2}{1 + (\omega R_s C_s)^2} + \frac{1}{R_p} + \frac{R_c(\omega C_c)^2}{1 + (\omega R_c^2 C_c^2)} \right\}^2 \end{aligned} \tag{4.3}$$

where μ_n is the NMOS mobility constant, C_{ox} is the oxide capacitance, W_{n1} and L_{n1} are channel width and length of transistor M_{n1} respectively.

To minimize the power consumption, the design guides are as follows.

- increase inductance (L) and reduce series resistance (R_L) for spiral inductor.
- reduce capacitance (C_s, C_c) and series resistance (R_s, R_c) of substrate parasitics and pn-junction varactor respectively.
- reduce supply voltage (V_{dd})
- maximize g_{mn1}/I_{dn1} ratio by increasing the size of transistors M_{n1}, but it is limited by the device-parasitic capacitance.

4.2.3.2 Oscillating Frequency

Assume the loss of LC-tank is compensated by the negative transconductor ($g_{mn1} > G_{m\_min}$) and C_s is relative small which quality factor has unnoticable effect, the oscillating frequency f_o of the LC-oscillator can be derived by equating the imaginary part of the LC-tank admittance $Imag[Y\{\omega\}]$ to be zero [8].

$$Imag[Y\{\omega\}] \approx \frac{-L}{R_L^2 + (\omega L)^2} + C_s + C_p + \frac{C_c}{1 + (\omega R_c^2 C_c^2)} = 0$$

$$f_o = \frac{1}{2\pi\sqrt{L(C_c + C_s + C_p)}} \cdot \sqrt{1 - \frac{(C_c + C_s + C_p) + \frac{(C_s + C_p - L/R_L^2)(R_c C_c)^2}{L(C_c + C_s + C_p)}}{\frac{L}{R_L^2} + \frac{(C_s + C_p - L/R_L^2)(R_c C_c)^2}{L(C_c + C_s + C_p)}}} \qquad (4.4)$$

$$f_o = \frac{1}{2\pi\sqrt{L(C_c + C_s + C_p)}} \qquad \text{when} \qquad R_L = R_C = 0$$

The first term in (4.4) is the oscillating frequency with perfect inductor and varactor. The second term describes the frequency degradation due to the series resistance of spiral inductor and pn-junction varactor. Since the frequency deviation caused by the second term in (4.4) can be up to 10%, attention should be paid on the parasitics of the transistors and passive components to achieve reasonable frequency accuracy. In any case, for good oscillating-frequency accuracy, passive components with high quality factors are required.

4.2.3.3 Phase Noise

The phase-noise estimation of the LC-oscillator is based on the theory by Ali Hajimiri [9]. In this phase-noise theory, an oscillator is considered as a time-variant system as shown in Figure 4.5. The phase deviation $\Delta\phi$ (phase noise) is maximum when the noise current impulse *i(t)* is injected at zero crossing point, and is minimum when the noise impulse is injected at the peak.

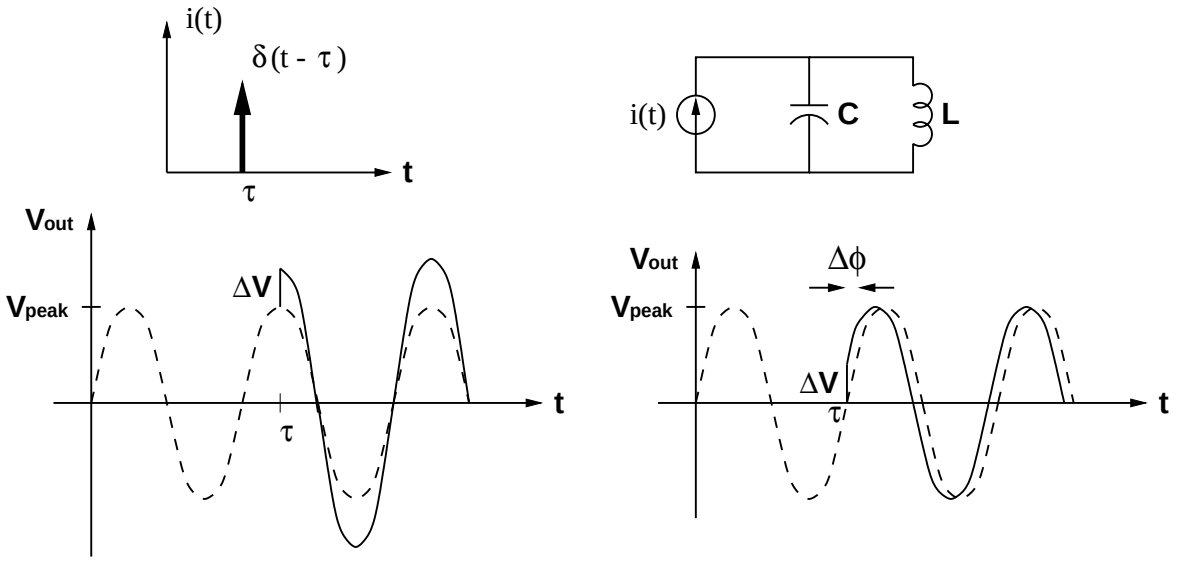


Figure 4.5 Time-variant phenomenon of the LC-oscillator.

To model the time-variant characteristics of the oscillator, the phase deviation $\Delta\phi$ is related to voltage disturbance ΔV by impulse sensitivity function (ISF)

$$\Delta\phi = \Gamma(x) \cdot \frac{\Delta V}{V_{peak}} \tag{4.5}$$

where x is phase which is 2π periodic, $\Gamma(x)$ is the impulse sensitivity function (ISF), V_{peak} is the output peak voltage of oscillator. With the power-spectral density of total noise current $\overline{i_n^2}/\Delta f$ and ISF of oscillator, the single-side-band phase noise $\mathsf{L}_{VCO2}\{\Delta\omega\}$ at a frequency offset $\Delta\omega$ can be calculated as follows

$$\mathsf{L}_{VCO2}\{\Delta\omega\} = 10 \cdot \log\left(\frac{\Gamma_{rms}^2}{C_L^2 V_p^2} \cdot \frac{\overline{i_n^2}/\Delta f}{2\Delta\omega^2}\right) \tag{4.6}$$

where C_L is the total parallel capacitance of the LC-tank. With transistors M_{n1} and M_{b1}, spiral inductor, pn-junction varactor and substrate parasitics, the total noise-power-spectral density can be expressed as follows

$$\frac{i_n^2}{\Delta f} = 2 \cdot 4kT \cdot \left(3 \cdot g_{mn1} + 3 \cdot \frac{g_{mb1}}{2} + \frac{1}{R_L(1+Q_L^2)} + \frac{1}{R_s(1+Q_S^2)} + \frac{1}{R_c(1+Q_C^2)} \right) \quad (4.7)$$

$$Q_L = \omega L / R_L \qquad Q_S = 1/\omega R_S C_S \qquad Q_C = 1/\omega R_C C_C$$

where k is Boltzmann's constant, T is absolute temperature, Q_L, Q_S and Q_C are quality factors of inductor, substrate parasitics and varactor respectively. The first coefficient "2" in (4.7) accounts for the double noise sources of the differential design.

To minimize phase noise, the design guidelines are as follows

- do not over-compensate the LC-tank too much ($g_{mn1} > 2G_{m\_min}$) to reduce the required g_{mn1}.
- reduce g_{mb1}/I_{db1} ratio by increasing the size of transistors M_{b1}.
- minimize series resistance R_L, R_S, R_C and maximize the quality factor Q_L, Q_S, Q_C for spiral inductor, substrate parasitics and pn-junction varactor respectively.
- maximize output amplitude V_p by increasing the bias current.

To achieve a low power, good frequency accuracy and low phase noise for the oscillator, passive components, such as inductors and varactors, with good quality factors are required in general. The design of on-chip spiral inductors and pn-junction varactors will be discussed in the next two sections.

4.2.4 Design of the On-Chip Spiral Inductor

Since most standard CMOS process is for digital circuit application, metal layers are less than 1 μm and epitaxial substrate is used for latchup consideration. Due to the metal resistance, skin effect and substrate loss in epitaxial substrate, quality factor of on-chip spiral inductor is difficult to be larger than three. This section summaries the design guidelines of the on-chip spiral-inductor design.

4.2.4.1 Circular Spiral Inductor

On-chip spiral inductor can be built in different geometries like square, octagon and

circle. Compared to a circular inductor, a square spiral inductor has larger inductance-to-area ratio but contributes more series resistance at the coil corners. Therefore, a circular spiral inductor is adopted to eliminate the corner resistance and thus enhance the quality-factor optimization.

4.2.4.2 Minimum Metal Spacing

By adopting minimum metal spacing, the magnetic coupling between adjacent metal lines is maximized [10]. The additional inter-winding capacitance from tighter coupling of the electric field between adjacent conductors reduces the self-resonant frequency to around 3 GHz, but it has little impact on performance in 900-MHz operation. Therefore, minimum metal spacing maximizes the quality factor and reduces the chip area for a given inductor layout.

4.2.4.3 Limited Metal Width

At high frequency operation, skin effect causes a non-uniform current flow in metal lines, and increases the series resistance of the spiral inductor. From the analysis by Jan Craninckx [11], two inductors with metal width of 15 μm and 30 μm, while other parameters are the same, are simulated. The simulation results at 2 GHz show the series resistance with metal width 30 μm is only 30% lower than the other one. Moreover, widening the metal lines of inductors with a fixed area will result in a smaller inductance value. To keep the inductance value constant, inductor area must be increased and result in larger substrate capacitance. The increase in capacitance causes lower self-resonant frequency and more substrate loss. Therefore, very wide metal (> 30 μm) is not desirable for inductor optimization.

4.2.4.4 Hollow-Spiral Inductor

To maximize the inductance per unit area, it seems that inductor coil should fill up the whole area. However, quality factor of spiral inductor is degraded by eddy current generated in the inner coils as shown in Figure 4.6. The inductor has a current I_{coil} which induces a magnetic

field B_{coil} with maximum intensity at the center of the inductor. According to the theory by Faraday-Lenz, the magnetic field B_{coil} generates a circular eddy current I_{eddy}. Such generated eddy current degrades the quality factor of spiral inductor in two folds. First, the eddy current induces a magnetic field B_{eddy}, which opposes the original magnetic field, so inductance value decreases. Second, the eddy current causes a non-uniform current flow in the inner coil of inductor, so current is pushed inside the metal line and series resistance is increased [11].

Therefore, to eliminate the quality-factor degradation of spiral inductor, hollow spiral inductor with 50-% inner-hole size is adopted in this design [11].

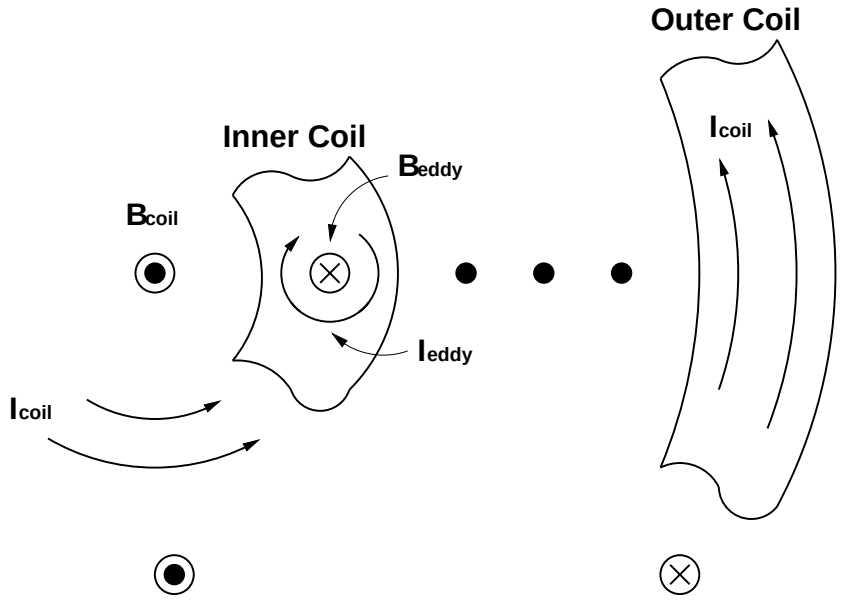


Figure 4.6 Generation of eddy currents in spiral inductor.

4.2.4.5 Limited Inductor Area

As epi-wafer is used in this technology, currents induced by the magnetic field of the inductor are free to flow, which causes extra quality-factor degradation of inductors as shown in Figure 4.7. According to the theory by Faraday-Lenz, electrical current is magnetically induced in substrate. The induced substrate current flows in a direction opposite to the current in the inductor and thus causes quality-factor degradation.

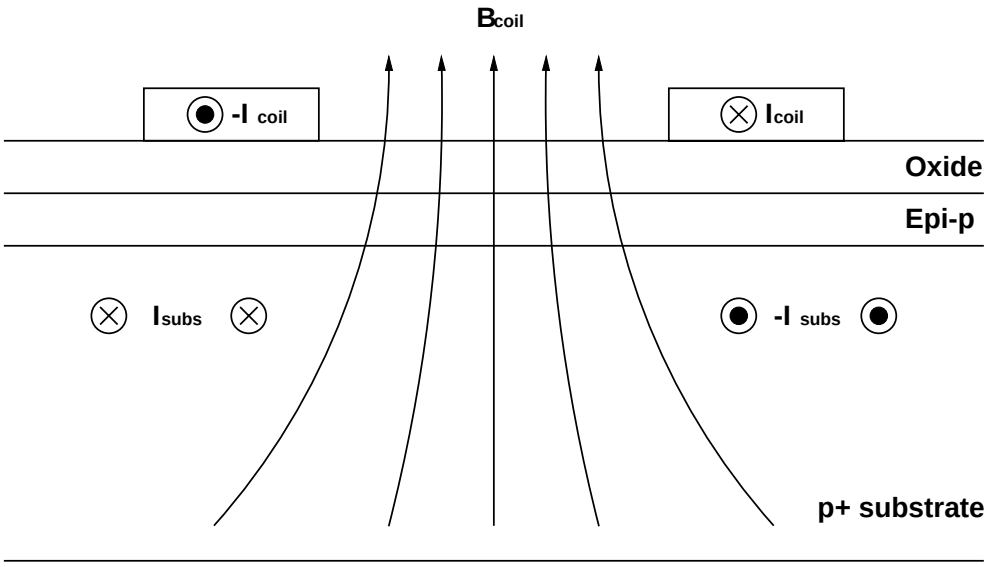


Figure 4.7 Generation of substrate currents on spiral inductors.

From the analysis by Jan Craninckx [11], which uses a 0.4-μm CMOS process with epitaxial layer, the series resistance contributed by substrate and metal are approximately the same at coil radius between 125 μm and 150 μm. Therefore, spiral inductor should be designed with coil radius less than 150 μm so that the magnetic field of the inductor penetrates less deep into the substrate and thus causes less substrate losses. Although the process adopted is not exactly equal to the process used by Jan Craninckx [11], similar substrate conditions for both standard CMOS process are assumed to be similar. In addition, a patterned N-well shield is put under the spiral inductor to make the substrate less conductive and thus to reduce eddy current induced in the substrate.

4.2.4.6 Two-Layer Inductor

From the design equation (4.3), larger inductance is desirable for low power dissipation. Within a chip area of 300 × 300 μm^2, only an on-chip spiral inductor with inductance less than 5 nH can be built by only the top layer of metal (Metal 3). To increase the inductance while maintaining reasonable quality factor, two-layer inductors are adopted [12]. The general relationship between inductor and its dimension can be expressed as follows

$$L \propto N^2 A / l$$
$$R_L \propto N \tag{4.8}$$

where N is number of turn, A is cross-section area, and l is the length of solenoids. By connecting two layers of spiral inductors in series, inductance can increased by 4 times with the same inductor area since inductance is proportional to N^2. Moreover, series resistance is only proportional to N, quality factor of inductor can also be improved simultaneously. However, the quality-factor improvement of two-layer inductors is smaller than twice since the lower layer of metal has higher sheet resistance and larger substrate capacitance.

4.2.4.7 Inductor Simulation and Modelling

To estimate the inductance and resistance values, a program called "Analysis of Si Inductors and transformers for ICs" (ASITIC) is adopted [13]. ASITIC can simulate inductance L, series resistance R_L, substrate capacitance C_{S1} & C_{S2}, and substrate resistance R_{S1} & R_{S2}, and all the parameters are put into the model of Figure 4.8. However, ASITIC cannot simulate the effect of eddy current which is discussed in Section 4.2.4.4 and Section 4.2.4.5. To maintain good agreement between simulation and measurement results, hollow spiral inductors with radius less than 150 μm is used

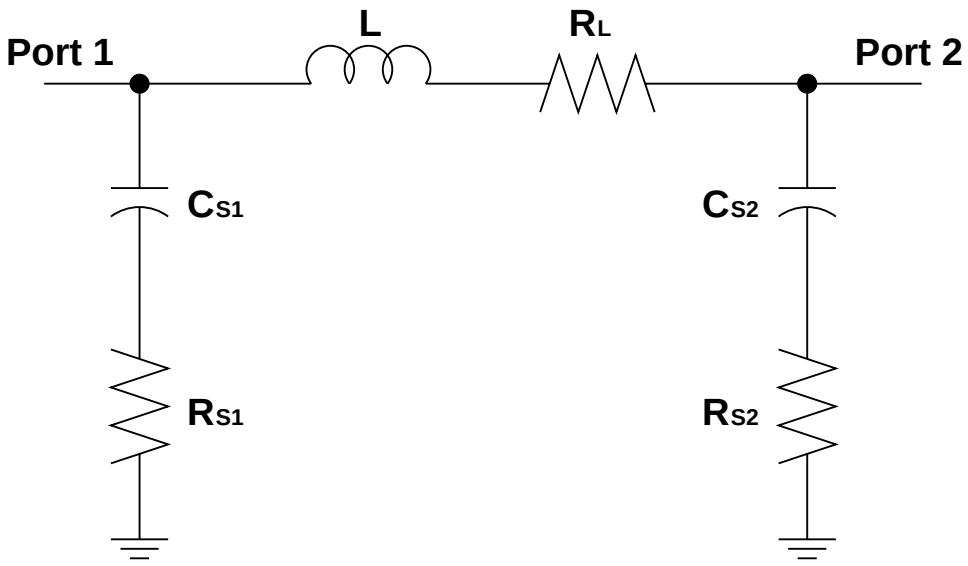


Figure 4.8 On-chip spiral inductor model in ASITIC.

4.2.5 Design of the PN-Junction Varactor

To implement the frequency-tuning function of the LC oscillator, pn-junction varactors are adopted. By tuning the bias of the varactor, the depletion capacitance is adjusted and thus the frequency tuning of the LC oscillator can be achieved. Like on-chip spiral inductors, pn-junction varactors also require high quality factor in order to satisfy phase-noise and power-consumption specification. This section discusses the design guidelines of the pn-junction varactor.

4.2.5.1 Minimum Junction Spacing

Figure 4.9 shows the cross-section of a pn-junction varactor. The varactor consists of p+junctions on N-well to form diodes and n+contacts to reduce contact resistance. Since the series resistance is proportional to the region that is not depleted, minimum junction spacing can minimize the series resistance.

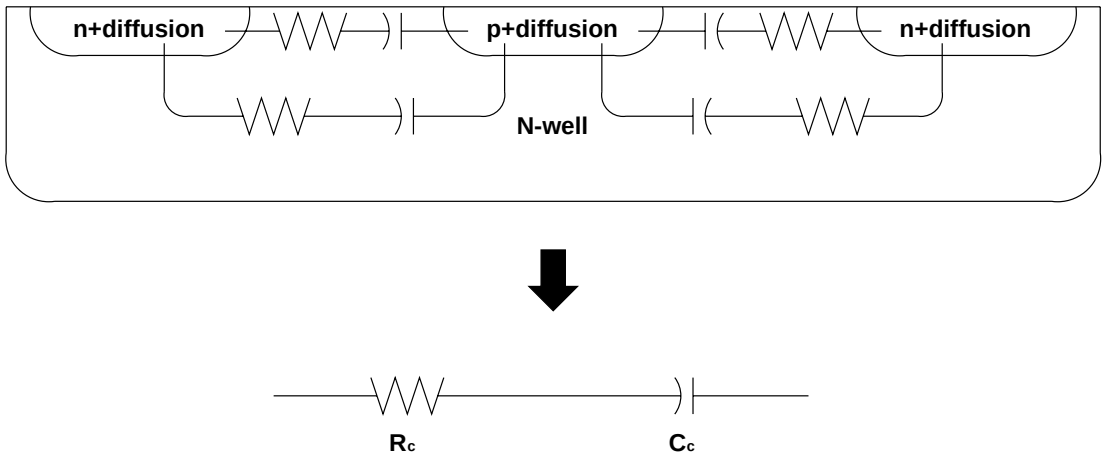


Figure 4.9 Cross-section and circuit model of pn-junction varactor.

4.2.5.2 Non-Minimum Junction Width

As the resistance from the center of p+diffusion to n+diffusion is larger than that at the edge of p+diffusion, it seems that a higher quality factor can be achieved by reducing the size of p+diffusion. However, as shown in Figure 4.10, measurement results of two pn-junction

varactors with p+diffusion width of 6.6 and 1.5 μm show different trend. For the varactor with 6.6-μm junction width, its quality factor is around three times larger the one with 1.5-μm junction width. Although the resistance between p+diffusion and n+diffusion is minimized with minimum junction width, the number of junction contact between p+diffusion and metal is also reduced by 16 times. Therefore, the series resistance may be dominated by the junction-to-metal contact resistance and thus the optimal quality factor cannot be achieved with minimum junction width.

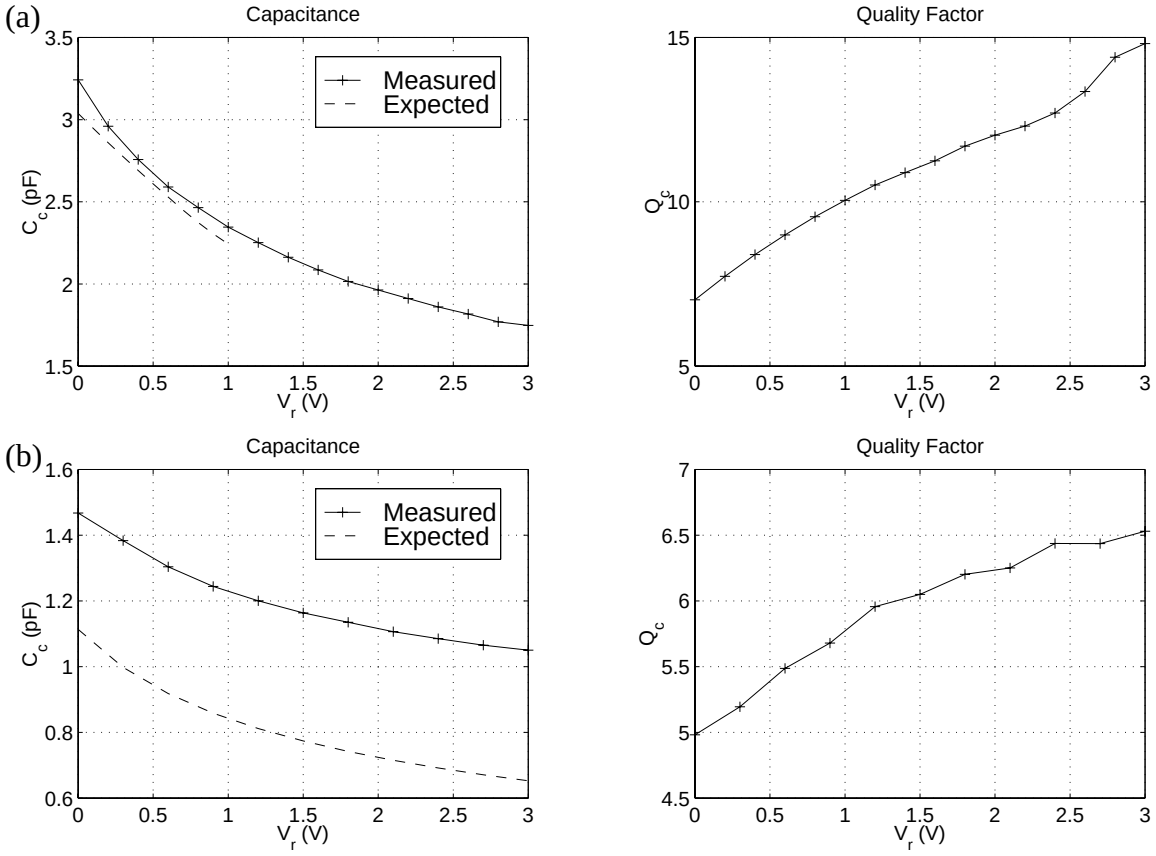


Figure 4.10 Measurement results of two pn-junction varactors with different junction width (a) 6.6 μm and (b) 1.5 μm.

Besides the degradation of quality factor, the capacitance accuracy and the tuning range are also not optimal with minimum junction width. Comparing to the measured capacitance and expected capacitance, varactor with junction width 6.6 μm shows more accurate estimation than that with 1.5 μm. As junction width becomes smaller, the ratio between

the area capacitance and the periphery capacitance is reduced, and thus the capacitance-estimation accuracy is degraded. Moreover, the periphery capacitance suffers from a smaller junction-grading coefficient. Therefore, the increase in periphery capacitance degrades the capacitance-tuning range.

4.2.6 Design and Optimization

In the LC-oscillator design, the objective is to satisfy the phase-noise specification

Metal Width	No. of Turn	L (nH)	R_L (Ω)	C_{S1} (fF)	R_{S1} (Ω)
9 μm	2	9.79	23.1	101	228
	2.5	13.8	28.5	121	198
	3	18.8	34.8	127	185
12 μm	2	8.81	16.7	120	195
	2.5	12.1	20.5	144	167
	3	16.4	24.9	151	158
	3.5	20.2	28.4	172	140
15 μm	2	7.97	12.9	137	171
	2.5	10.7	15.7	165	145
	3	14.3	18.8	173	138
	3.5	17.2	21.3	196	123
	4	20.8	24.5	203	119
18 μm	2	7.19	10.4	154	153
	2.5	9.5	12.4	184	131
	3	12.4	14.8	192	125
	3.5	14.6	16.5	216	112
	4	17.2	18.6	224	108
21 μm	2	6.53	8.52	169	139
	2.5	8.45	10.1	201	119
	3	10.8	11.9	210	114
	3.5	12.4	13.1	234	104
24 μm	2	5.94	7.15	181	130
	2.5	7.52	8.42	214	112
	3	9.35	9.7	223	107

Table 4.1 Simulated inductor parameters applied to the LC-oscillator optimization.

with minimum power consumption. As there is no formula for the calculation of inductance and series resistance, inductors with different metal width and number of turns are simulated by ASITIC and the data are shown in Table 4.1. With the simulated inductor parameters, the capacitance of varactor can then be determined by the required oscillating frequency.

For the pn-junction varactor, the capacitance is modelled by the junction capacitance in the device model of PMOS transistors. Except for the parasitic capacitance due to the negative transconductor and the output buffer, the varactor capacitance is maximized to increase the frequency-tuning range. To achieve a good capacitance-estimation accuracy and a high quality factor, a junction width of 4.5 μm is adopted to keep a balance between N-well and contact resistance. Moreover, series resistance can be estimated by the measurement results of the varactor with 6.6-μm junction width in Figure 4.10a.

For the transistors M_{n1} in the negative transconductor, its characteristics at different gate-to-source voltage V_{gsn1} is taken into account for optimization. Based on the calculation of

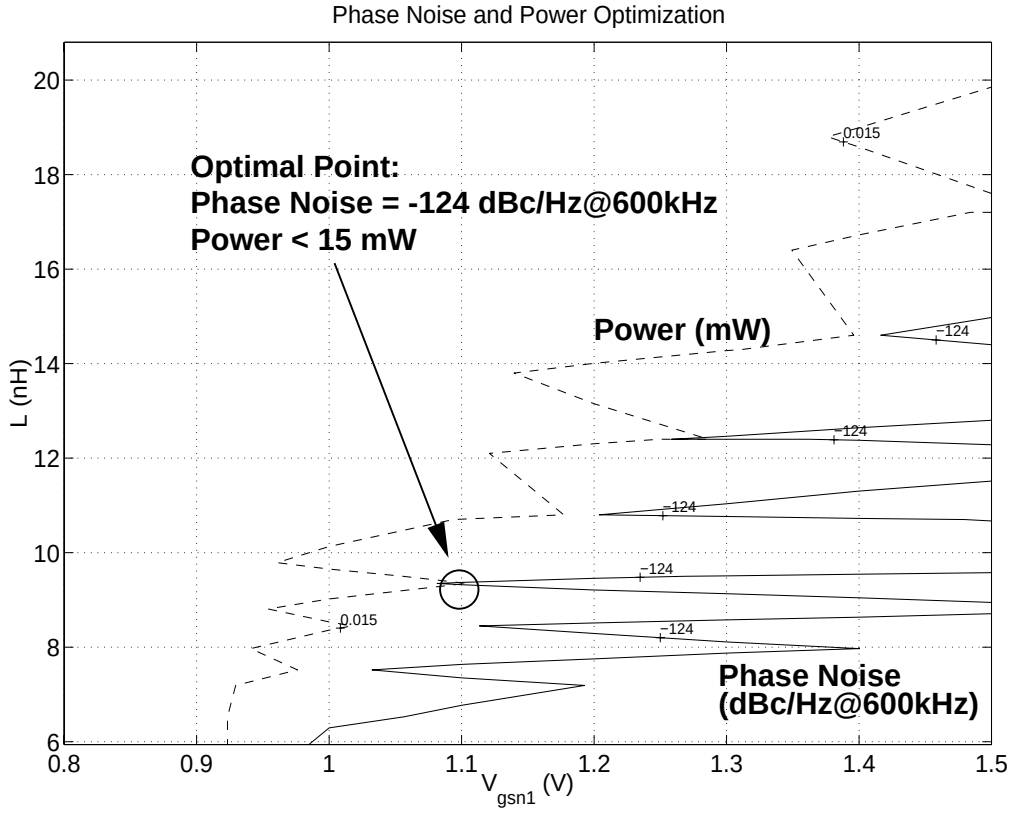


Figure 4.11 Phase-noise and power-consumption optimization of the LC-oscillator.

power consumption, oscillating frequency and phase noise in Section 4.2.3, the optimal design of the LC-oscillator is determined as shown in Figure 4.11. In Figure 4.11, power consumption and phase noise are calculated with different combinations of the inductor design in Table 4.1 and V_{gs} of transistors M_{n1}. The optimal design is determined where phase noise specification is achieved with minimum power consumption.

Although the phase-noise specification is -121 dBc/Hz@600kHz, -124 dBc/Hz @600kHz is designed for a 3-dB design margin. In Figure 4.11, the curves of phase noise at 600-kHz offset and power consumption only marginally touch. It shows that the minimum power consumption is around 15 mW for the required phase noise specification. There are two optimal points at (a) V_{gsn1} = 1.3 V, L = 12.5 nH, and (b) V_{gsn1} = 1.1 V, L = 9.35 nH. As the next stage is frequency divider N_3, which requires an optimal common-voltage close to 1 V, case (b) is chosen. The design parameters of the LC oscillator are summarized in Table 4.2.

Inductor					
Radius	150 μm	L	9.35 nH	R_L	11.6 Ω
Width	24 μm	C_{S1}	223 fF	R_{S1}	107 Ω
Spacing	0.9 μm	C_{S2}	429 fF	R_{S2}	52.6 Ω
No. of Turn	3				
Varactor				Transistor	
Width	6 μm	C_C	2.33 pF	$(W/L)_{n1}$	98.4/0.6
Spacing	1.2 μm	R_C	8 Ω	$(W/L)_{b1}$	2180.4/0.6
No. of Unit	102			I_{bias}	6.8 mA

Table 4.2 Design parameters of the LC oscillator.

The LC oscillator is simulated by *SpectreRF* [14], the simulation results of oscillating frequency f_o, the single-ended peak-to-peak output amplitude V_{pp} and the VCO gain K_{VCO} are shown in Figure 4.12. The oscillating frequency is between 655 and 981 MHz, the single-ended amplitude is between 0.37 and 1.71 V_{pp}, and VCO gain is between 72 and 274.5 MHz/V. For

the phase-noise performance, *SpectreRF* [14] is used to perform the periodic-steady-state (PSS) function, the phase-noise simulation results of the LC-oscillator shown in Figure 4.13 is close to the expected results.

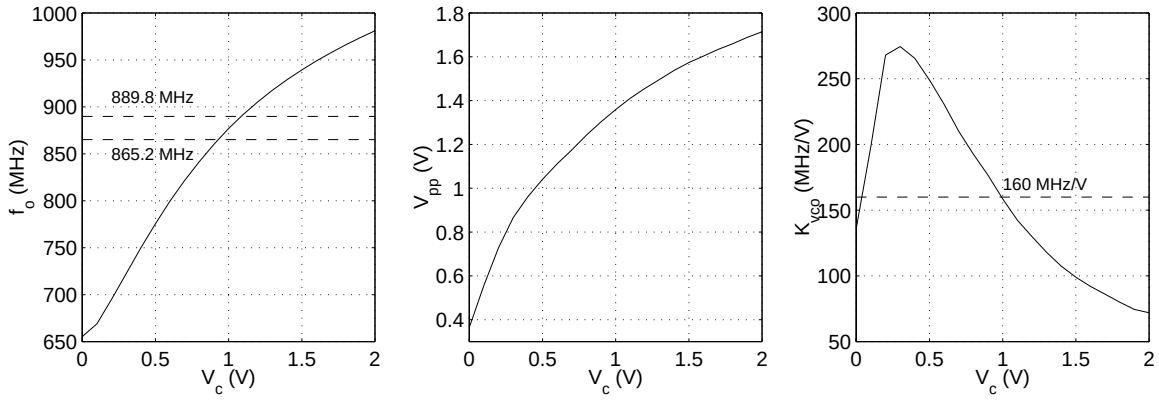


Figure 4.12 Oscillating frequency, single-ended peak-to-peak output amplitude and VCO gain of the LC oscillator.

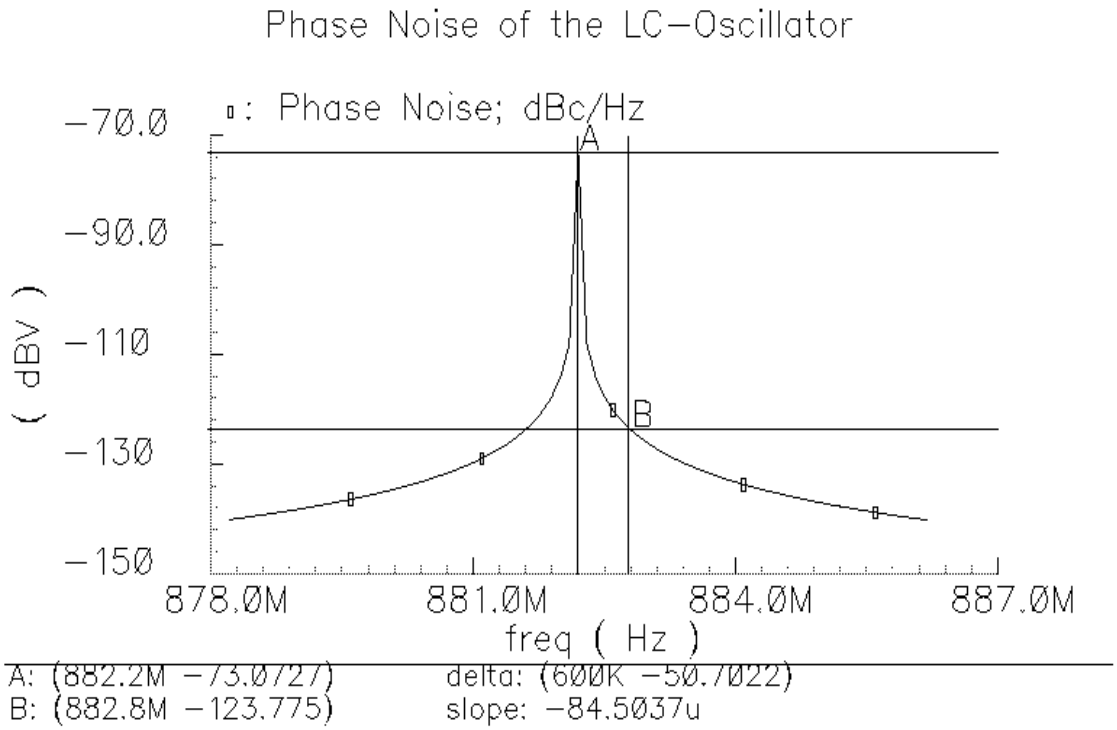


Figure 4.13 Phase-noise simulation results of the LC oscillator by *SpectreRF*.

4.3 Frequency divider N_3

4.3.1 Design Requirement

After the LC oscillator, a divide-by-4 frequency divider N_3 is included in the feedback path of the high-frequency loop as shown in Figure 4.14. The design requirement of the frequency divider N_3 is as follows

- operate up to 1 GHz which is larger than the maximum operating frequency of the LC oscillator.
- operate with peak-to-peak amplitude as low as 1 V_{pp} since output of the LC-oscillator is sinusoidal.
- generate full-swing output with rise time and fall time less than 10% of the total output period.

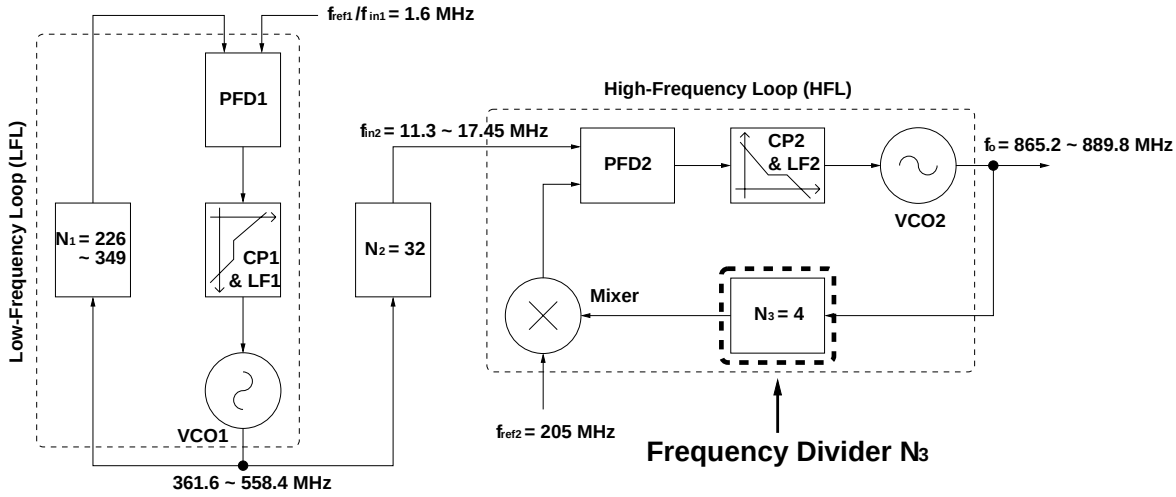


Figure 4.14 Location of the frequency divider N_3.

The input operating frequency of the frequency divider N_3 has to be larger than that of the VCO2. Suppose the oscillating frequency of VCO2 is lower than the required value, the PFD2 generates an UP signal to pull the frequency up. If the loop dynamics is not designed properly, the frequency over-shoot may be very large. If the maximum operating frequency of divider N_3 is lower than that of VCO2, the output frequency of divider N_3 (input of PFD2) may become zero (no division) or lower than reference frequency (divide more than 4). Therefore, the PLL still pulls the frequency up and the loop becomes out of lock.

Although the peak-to-peak amplitude of LC-oscillator is 1.4 V_{pp}, its output amplitude

may decrease due to the quality-factor degradation of the inductors and varactors. Therefore, the input is assumed to be around 1 V_{pp} for design margin.

To reduce phase noise contributed by frequency divider, it is desirable to reduce the rise and fall time of the frequency divider. However, smaller rise and fall time requires larger transistors and thus larger power is consumed. Therefore, rise and fall times are designed to be less than 10% of the output period compromising the frequency-divider phase noise and power consumption.

4.3.2 Circuit Implementation

The design of the divide-by-4 frequency divider N_3 consists of two divide-by-2 dividers in a cascade configuration as shown in Figure 4.15. The first divide-by-2 divider senses the 900-MHz sinusoidal output of the LC oscillator and generates full-swing output at 450 MHz. The second divide-by-2 divider has the 450-MHz full-swing input, as its input and outputs a 225-MHz full-swing signal for the mixer.

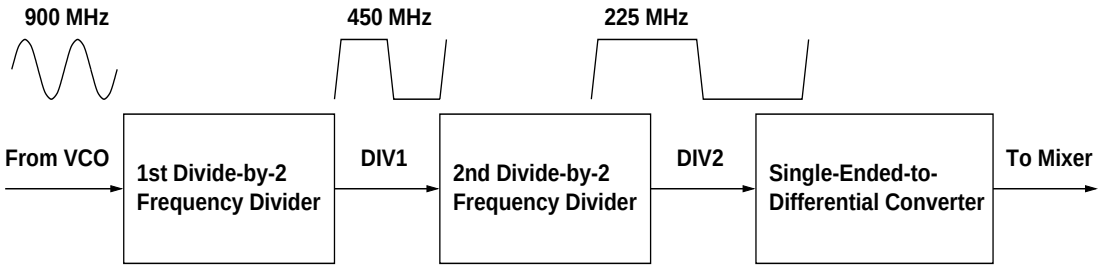


Figure 4.15 Cascade configuration of the frequency divider N_3.

4.3.2.1 The First Divide-by-2 Divider

As the first stage needs to divide 0.5-V_{pp} sinusoidal signals 900 MHz, the conventional static logic cannot achieve this goal. Therefore, pseudo-NMOS logic is adopted in this frequency-divider design as shown in Figure 4.16. The input stage is a pseudo-NMOS inverter (transistors M_{n1} and M_{p1}) which amplifies sinusoidal signals into square-wave signals. The remaining stage is a pseudo-NMOS negative-edge-triggering divide-by-2 frequency divider

[15]. For high-frequency operation, the concept of zero stand-by power consumption is not so meaningful because the transition time of a signal takes a considerable portion of a clock period. Therefore, a ratioed logic (pseudo-NMOS logic) can replace a ratioless logic (complementary logic) without paying much penalty on the power consumption.

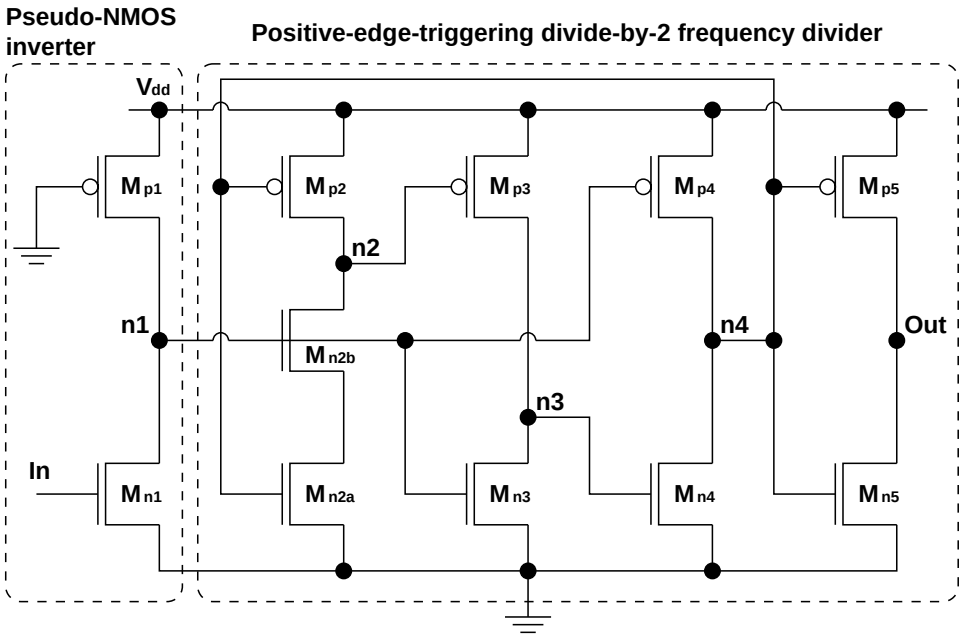


Figure 4.16 The first divide-by-2 frequency divider of divider N_3.

As shown in Figure 4.17, in the precharge phase (V_{n1} = “1”), transistors M_{n2} and M_{p2} operate as inverter to pre-charge the node *n2*. M_{n3} discharges node *n3* to turn off M_{n4} and M_{p4} is turned off, so that node *n4* becomes floating. In the evaluation phase (V_{n1} = “0”), the pre-charged node *n2* becomes transparent to output node *n4*. However, M_{n4} must be strong enough to draw output voltage close to “0”. By connecting the node *n4* to the gate of M_{n2a} and M_{p2}, which is equivalent to a D-flip-flop with $\overline{Q}$ connected to *D*, a divide-by-2 function is achieved. Transistors M_{n5} and M_{p5} form an inverter to serve as an output buffer.

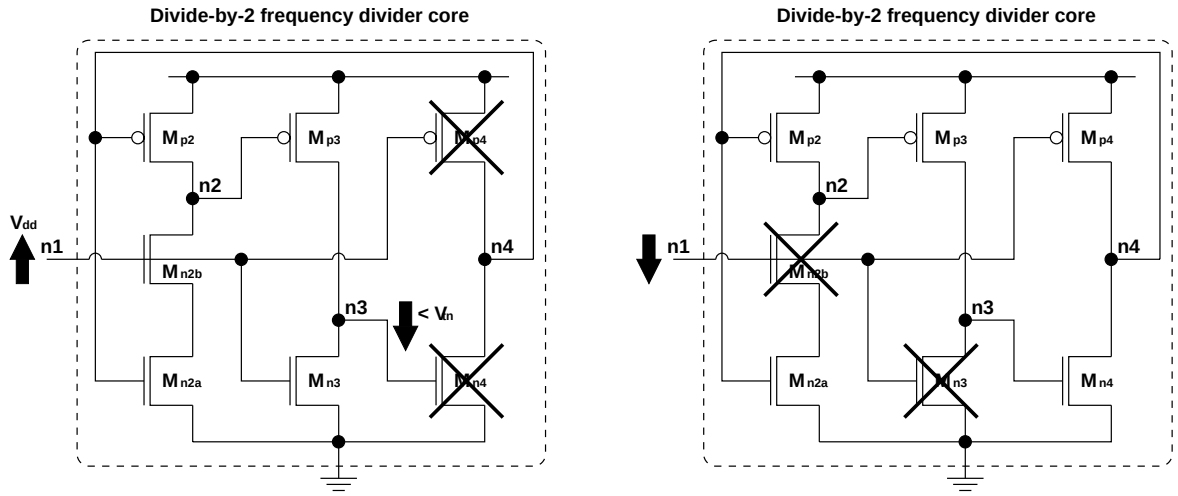


Figure 4.17 The operation of the pseudo-NMOS divide-by-two divider in (a) precharge phase and (b) evaluation phase.

As the pseudo-NMOS logic is a ratioed logic, care must be taken on the aspect ratio between NMOS and PMOS transistors. For M_{n1} and M_{p1}, its ratio is designed so that the voltage of logic level "0" is smaller than the threshold voltage of NMOS transistors V_{tn}. By calculating NMOS and PMOS IV characteristics, the ratio of M_{n1} and M_{p1} can be expressed as follows

$$\mu_n C_{ox}\left(\frac{W}{L}\right)_n\left(V_{max}-V_{tn}-\frac{V_{OL}}{2}\right)V_{OL} = \frac{\mu_p C_{ox}}{2}\left(\frac{W}{L}\right)_p(V_{dd}-V_{tp})^2$$

$$V_{OL} = (V_{max}-V_{tn})\left[1-\sqrt{1-\frac{\mu_p(W/L)_p(V_{dd}-V_{tp})^2}{\mu_n(W/L)_n(V_{max}-V_{tn})^2}}\right] \le V_{tn} \qquad (4.9)$$

$$\frac{(W/L)_p}{(W/L)_n} \le \frac{\mu_p(V_{dd}-V_{tp})^2}{\mu_n(V_{max}-V_{tn})^2}\left[1-\left(\frac{V_{max}-2V_{tn}}{V_{max}-V_{tn}}\right)^2\right]$$

where V_{max} is the maximum input of inverter, V_{OL} = 0.4 V is the voltage of logic "0" for pseudo-NMOS logic. As the common mode output of the LC-oscillator is 1.1 V and the peak-to-peak output is 1 V_{pp}, the maximum input V_{max} is 1.6 V. Therefore, the transistor ratio between M_{n1} and M_{p1} should be smaller than 0.8. In the hold mode (V_{n1} = "1"), M_{n3} must be strong enough so that voltage node *n2* is not transparent to node *n3*. In this case, V_{max} = 2 V, the transistor ratio between M_{n3} and M_{p3} should be smaller than 1.6. In evaluation mode (V_{n1} =

"0"), M_{n4} must be large enough to obtain V_{OL} at node *n4*, the ratio between M_{n4} and M_{p4} should be smaller than 1.6.

4.3.2.2 The Second Divide-by-2 Divider

As the first divide-by-2 frequency divider has already divided the input sinusoidal signals into full-swing output, the second divide-by-2 has relaxed speed (500 MHz) and input amplitude (full swing) requirement. True-Single-Phase-Clock (TSPC) Logic can construct an edge-triggering D-flip-flop with only 9 transistors, the reduced transistor parasitics enhances the high-speed low-power operation up to several hundreds mega hertz [16]. Therefore, TSPC Logic is adopted for the second-divider implementation as shown in Figure 4.18.

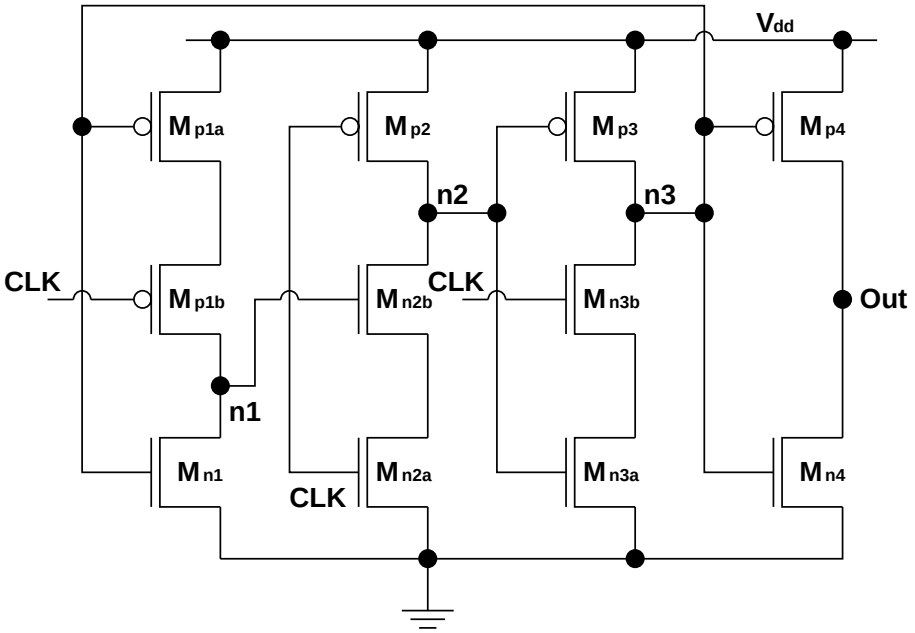


Figure 4.18 True-Single-Phase-Clock (TSPC) divide-by-2 frequency divider.

The operation of the TSPC divider is as shown in Figure 4.19. In the precharge phase (V_{clk} = "0"), node *n1* is pre-charged to a value depending on the input signal and node *n2* is pre-charged to V_{dd}. As transistors M_{n3b} and M_{p3} are turned off, node *n3* becomes floating. In the evaluation mode, if node *n1* is pre-charged to V_{dd}, node *n2* is discharged and V_{n3} is pulled up by transistor M_{p3}. If node *n1* is precharged to "0", node *n2* is not discharged, and node *n3* is pulled down by transistors M_{n3a} and M_{n3b}.

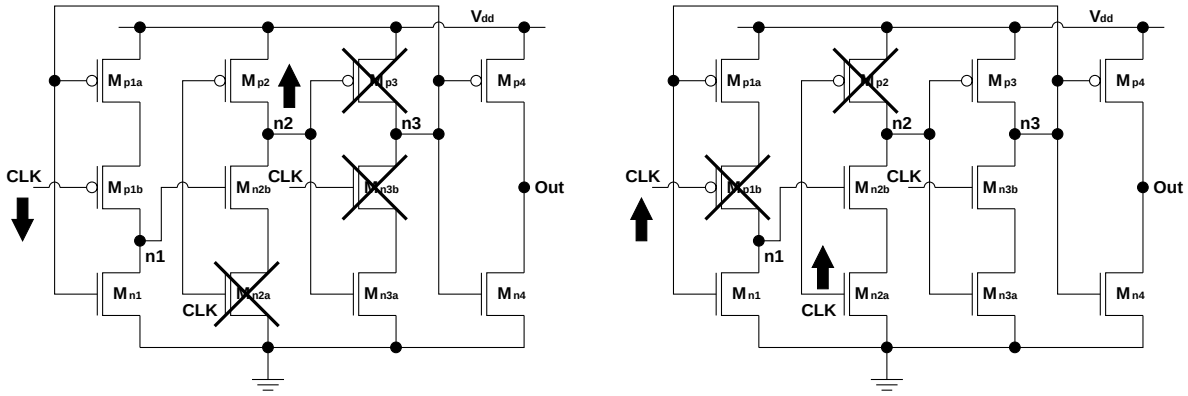


Figure 4.19 Operation of the TSPC divider in (a) hold mode and (b) evaluation mode.

To take the worst case situation into account, the divider is designed at 500 MHz with 20-% input rise and fall time. For digital circuit, power consumption can be expressed as follows

$$Power \propto C_L V_{dd}^2 f \tag{4.10}$$

As supply voltage V_{dd} and operating frequency f are fixed, power consumption can be minimized by minimizing the transistor size. However, transistors must be large enough to meet the rise and fall time requirement. To maintain output waveform more like square wave, rise and fall time of the output are designed to be 20% of input period (0.2 T_{CLK}). To derive the rise and fall time specification, the circuit operation must be considered. For example, to discharge node *n3* in evaluation mode, transistors M_{n3a} and M_{n3b} are turned on. However, M_{n3a} is turned on when *CLK* is low which is half clock period (0.5 T_{CLK}) earlier than the turn on of M_{n3b}. Therefore, the rise time of node *n2* can be up to 0.5 T_{CLK}. Another example, to charge up node *n3*, transistors M_{n2a}, M_{n2b} and M_{p3} are turned on. As M_{n2b} and M_{p3} are turned on in evaluation mode, the fall time of M_{n2b} and rise time of M_{p3} should be less than 0.2 T_{CLK}. The timing requirement of the TSPC divide-by-2 divider is shown in Figure 4.20. In general, the timing requirement triggered in hold mode and evaluation mode are 0.5 T_{CLK} and 0.2 T_{CLK} respectively.

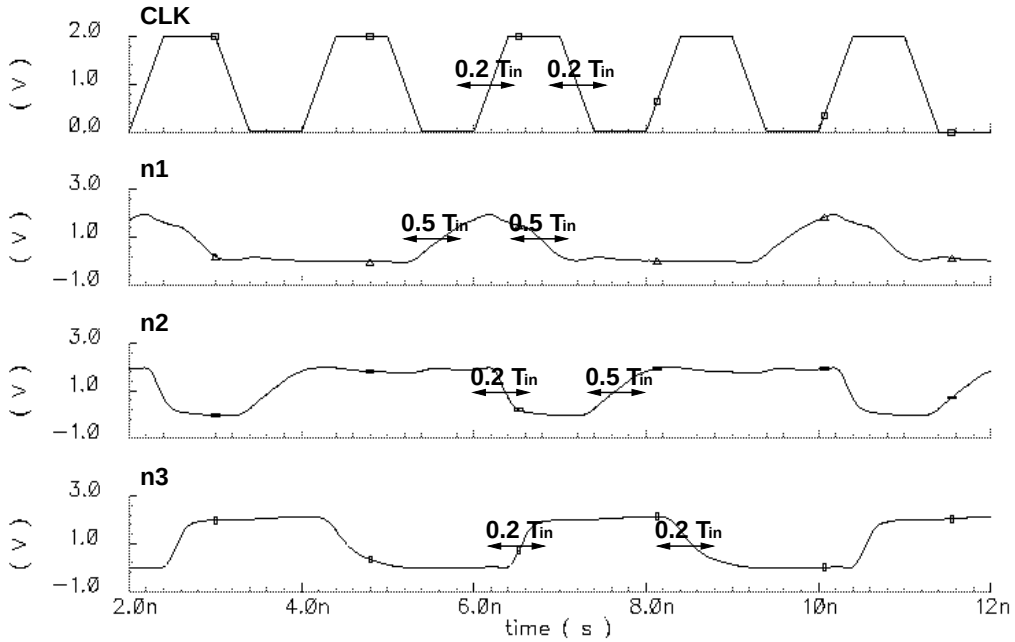


Figure 4.20 Timing requirement of a TSPC divide-by-2 divider.

4.3.2.3 Single-to-Differential Converter

As the down-conversion requires differential input and TSPC frequency divider can only provide single-ended output, a single-to-differential converter is needed. Figure 4.21 shows the schematic of the single-to-differential converter, it consists of 5 inverters and 1

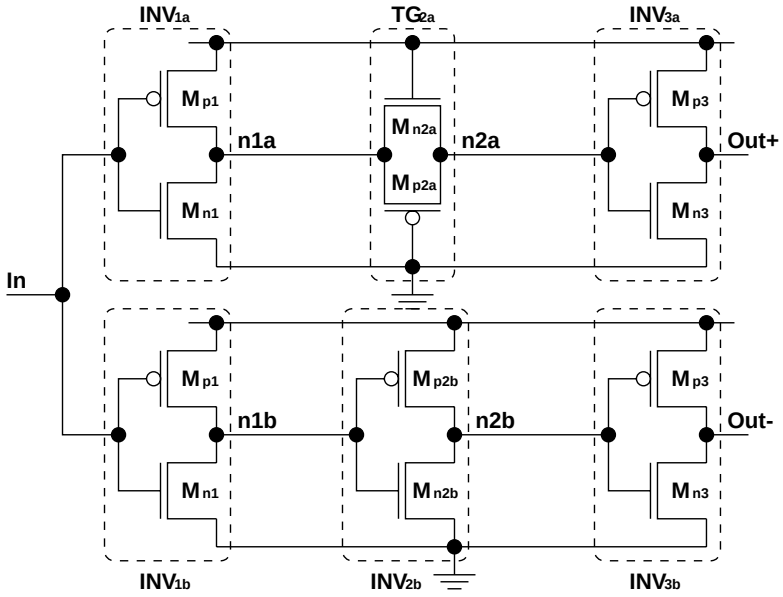


Figure 4.21 Circuit schematic of the single-to-differential converter.

transmission gate. To make the delay between two paths equal, the sizes of transmission gate TG_{2p} and inverter INV_{2n} are adjusted accordingly.

4.3.3 Design Parameters

According to the design guidelines of the frequency divider N_3, transistor sizes are designed so that the rise and fall time of all stages are less than 20% of input period. As there is no accurate calculation for digital circuit, the design highly depends on iterative simulation. Table 4.3 summaries all the design parameters of the frequency divider N_3 and the simulation results at 1 GHz are shown in Figure 4.22.

N_3 (1st stage)					
$(W/L)_{n1}$	96/0.6	$(W/L)_{n2}$	3/0.6	$(W/L)_{n3}$	4.5/0.6
$(W/L)_{p1}$	48/0.6	$(W/L)_{p2}$	4.5/0.6	$(W/L)_{p3}$	6/0.6
$(W/L)_{n4}$	18/0.6	$(W/L)_{n5}$	9/0.6		
$(W/L)_{p4}$	24/0.6	$(W/L)_{p5}$	42/0.6		
N_3 (2nd stage)					
$(W/L)_{n1}$	1.2/0.6	$(W/L)_{n2}$	9/0.6	$(W/L)_{n3}$	4.5/0.6
$(W/L)_{p1}$	3.6/0.6	$(W/L)_{p2}$	4.2/0.6	$(W/L)_{p3}$	18/0.6
$(W/L)_{n4}$	4.5/0.6				
$(W/L)_{p4}$	15.3/0.6				
N_3 (single-to-differential converter)					
$(W/L)_{n1}$	4.2/0.6	$(W/L)_{n2a}$	4.2/0.6	$(W/L)_{n2b}$	4.2/0.6
$(W/L)_{p1}$	15/0.6	$(W/L)_{p2a}$	15/0.6	$(W/L)_{p2b}$	15/0.6
$(W/L)_{n3}$	4.2/0.6				
$(W/L)_{p3}$	15/0.6				

Table 4.3 Design parameters of the frequency divider N_3.

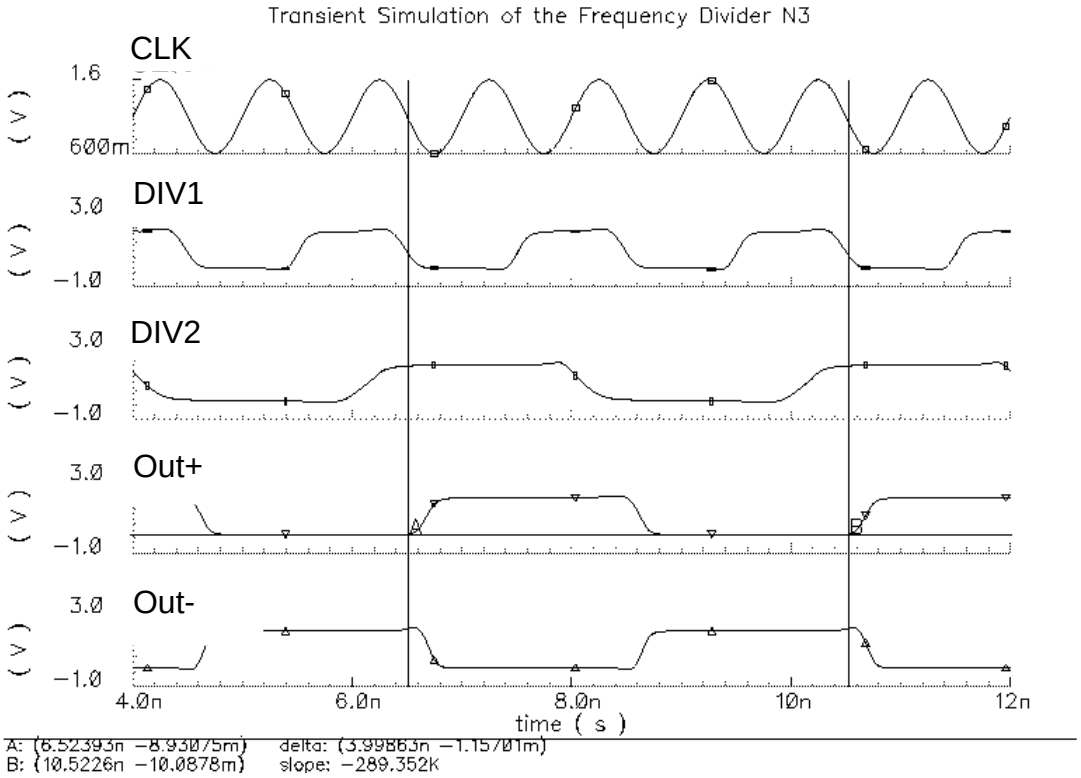


Figure 4.22 Simulation results of the whole frequency divider N_3.

4.4 Down-Conversion Mixer

4.4.1 Design Requirement

After the frequency divider N_3, a down-conversion mixer, which is illustrated in Figure 4.23, operates together with the second reference signal f_{ref2} to generate the frequency shift $N_3 f_{ref2}$. The design requirement of the down-conversion mixer is as follows

- operate at frequency up to 250 MHz for both inputs.
- output bandwidth is at 10 MHz to eliminate high frequency glitches.
- generate full-swing output to drive the PFD.

As the input signals of the mixer are from the frequency divider N3 and the second reference signal, the maximum operating frequency is up to 250 MHz. When the high-frequency loop locks, the output frequency of the mixer ranges from 11.3 MHz to 17.45 MHz, so output bandwidth is designed at 10 MHz to eliminate output glitches. Since both inputs are full swing,

all the input devices act as switches. Moreover, because there is no adjacent-channel interference as the mixer in receiver front-end, the linearity of the mixer is not critical. Similar to frequency divider, phase noise contributed by mixer is insignificant if output rise and fall times are short enough.

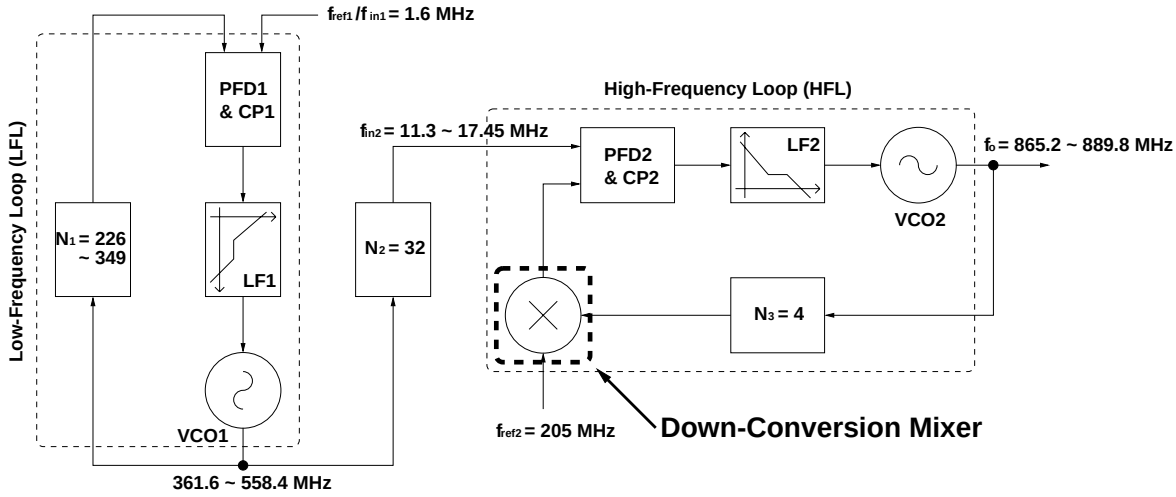


Figure 4.23 Location of the down-conversion mixer.

4.4.2 Circuit Implementation

The mixer shown in Figure 4.24 consists of a Gilbert-cell mixer, a low-pass filter and a differential-to-single-ended buffer. The Gilbert-cell mixer formed by transistors M_{n1} and M_{n2} performs the mixing function, and the high frequency tones are filtered by the low-pass filter formed by R_L and C_L. In order to drive the PFD, output of the Gilbert-cell mixer is effectively amplified by the differential-to-single-ended buffer to a full-swing output.

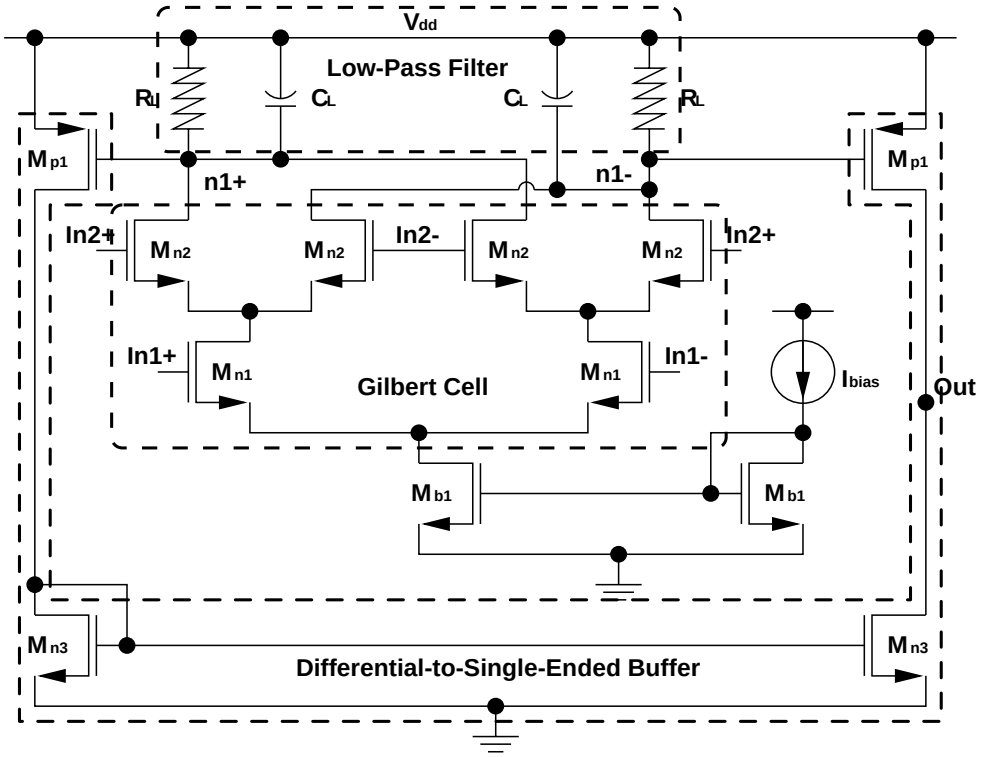


Figure 4.24 Circuit implementation of the down-conversion mixer.

4.4.3 Design Issues

As the output bandwidth is designed to be 10 MHz, load capacitance C_L and resistance R_L are determined based on the chip-area optimization. In order to provide appropriate input amplitude and gate bias for the transistors M_{p1}, the bias current I_{bias} is designed accordingly. For input transistors M_{n1} and M_{n2}, their aspect ratio is designed to keep the drain-to-source voltage V_{ds} to be less than 0.1 V. All the design parameters of the mixer are summarized in Table 4.4.

$(W/L)_{n1}$	15/0.6	$(W/L)_{n2}$	15/0.6	$(W/L)_{b1}$	30/1.2
$(W/L)_{p1}$	6/0.6	$(W/L)_{n3}$	1.5/0.6	I_{bias}	32 μA
R_L	70 kΩ	C_L	2 pF		

Table 4.4 Design parameters of the down-conversion mixer.

4.5 Voltage-Controlled Oscillator VCO1

4.5.1 Design Requirement

After the discussion of the building blocks in the high-frequency loop, the implementation and design of the building blocks in the low-frequency loop is discussed. Figure 4.25 shows the location of the voltage-controlled oscillator VCO1. The design requirement of the oscillator is shown as follows

- cover frequency range between 361.6 and 558.4 MHz.
- satisfy the phase-noise specification of -103 dBc/Hz at 600-kHz frequency offset with minimum power consumption.
- generate full-swing output to drive the frequency dividers N_1 and N_2.

As the frequency-division ratio between N_2 and N_3 is 8, the phase-noise attenuation of the oscillator is 18 dB. Therefore, the phase-noise requirement of VCO1 is -121 + 18 = 103 dBc/Hz@600kHz.

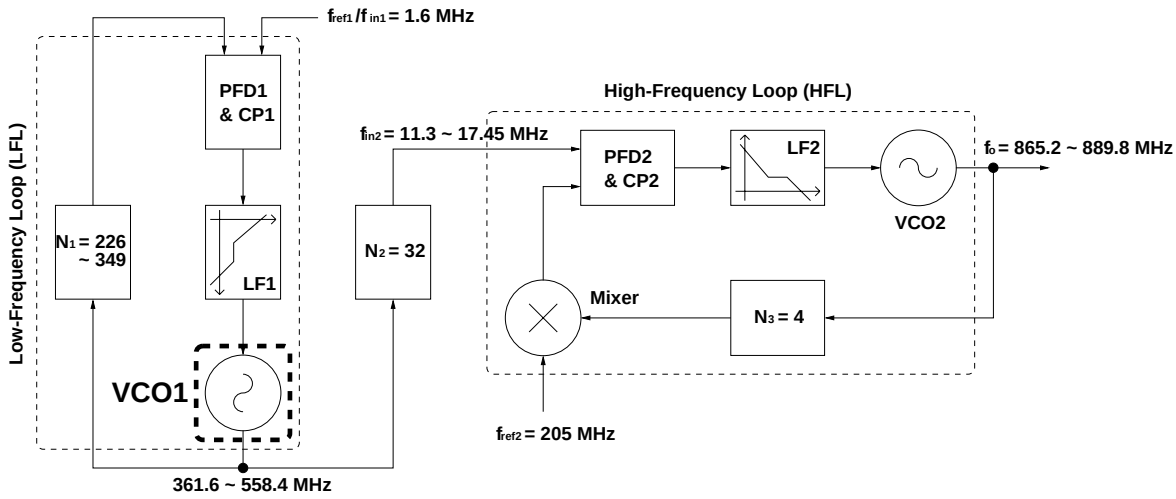


Figure 4.25 Location of the voltage-controlled oscillator VCO1.

4.5.2 Circuit Implementation

As VCO1 requires over 200-MHz (40%) frequency-tuning range, ring oscillator is adopted. The circuit schematics of the delay cell and the two-stage ring oscillator are shown in

Figure 4.26. The delay cell consists of a pair of NMOS input transistors M_{n1}, a pair of PMOS positive feedback transistor M_{p1} for maintaining oscillation, a pair of diode-connected PMOS transistors M_{p2}, and a current bias transistor M_{b1} for frequency tuning. The ring oscillator consists of two delay cells (instead of four) for power-consumption and phase-noise suppression.

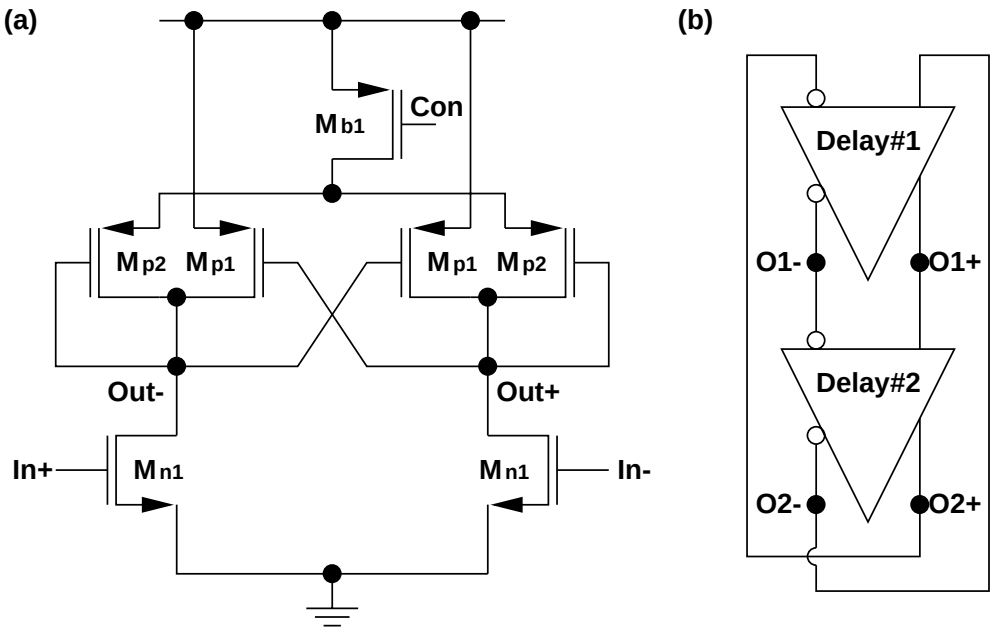


Figure 4.26 Schematics of (a) delay cell and (b) ring oscillator.

In this design, high operating frequency (600 MHz), wide tuning range (50%), low power consumption and low phase noise (-103 dBc/Hz@600kHz) are simultaneously desired. The design guidelines which determine the delay-cell design are as follows

4.5.2.1 High Frequency Operation

NMOS input pair is used to maximize the transconductance-to-capacitance ratio to achieve high operating frequency with low power dissipation. To reduce the g_m requirement and thus power dissipation, only parasitic capacitors of devices are utilized. Moreover, only two delay cells are included in the oscillator to minimize the power consumption.

4.5.2.2 Wide Frequency-Tuning Range

In this design, large tuning range is required to overcome the frequency-shift problem due to process variation. Operating frequency of the ring oscillator can be tuned by variable capacitor or by variable load impedance. Varactor is typically implemented by pn-junction and therefore frequency-tuning range is limited to be within 10 ~ 20%. In this design, frequency tuning is achieved by tuning the transconductance g_m of the diode-connected PMOS transistors M_{p2}. By controlling the bias current of M_{b1}, g_{mp2} can be adjusted from zero to a value close to g_{mp1}. Therefore, over 50-% tuning range can be easily achieved.

4.5.2.3 Low Phase-Noise Performance

As phase noise is defined as the difference between carrier power and noise power, phase-noise performance can be improved by either increasing carrier power or suppressing noise power. In the proposed design, the source nodes of devices M_{p1} are directly connected to supply to eliminate current limitation of the output nodes and thus maximize output amplitude. Since output amplitude becomes large, transistors are turned off periodically. As shown in Figure 4.27, noise current i_{nn1}, i_{np1}, i_{np2} become zero periodically when output amplitude is large [17]. Therefore, phase-noise performance is enhanced in this ring-oscillator design.

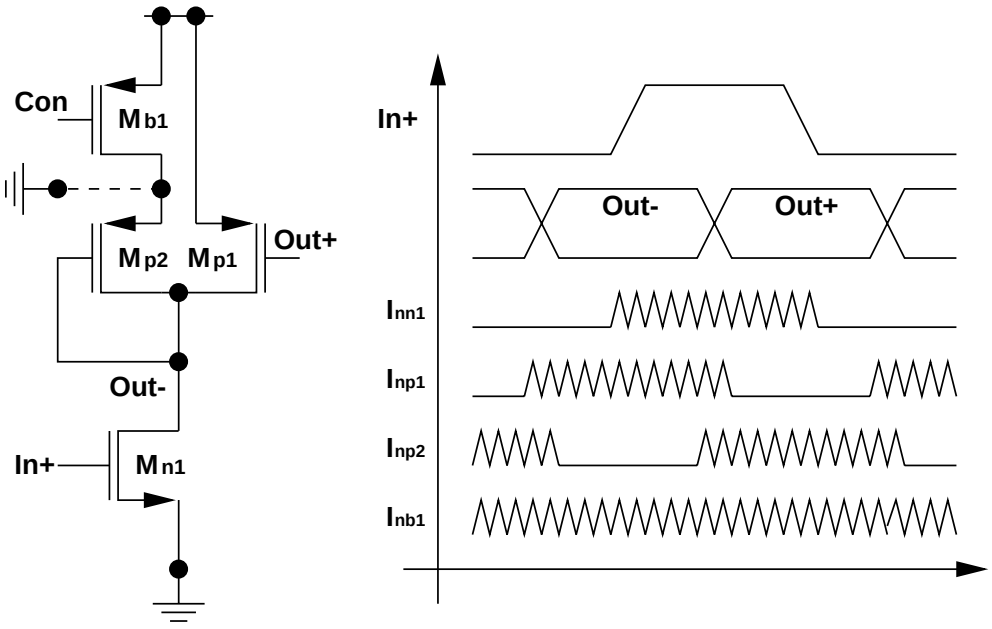


Figure 4.27 Delay cell waveforms and corresponding thermal noise current.

4.5.3 Ring-Oscillator Analysis

4.5.3.1 Operating-Frequency Range

To derive the operating frequency of the oscillator, half circuit of the delay cell in Figure 4.28 is considered. The transfer function of the delay cell *A(s)* is shown as follows

$$\begin{aligned} A(s) &= \frac{V_o}{V_{in}} = \frac{g_{mn1}}{(-g_{mp1} + g_{mp2} + G_L) + sC_L} \\ G_L &= g_{dn1} + g_{dp1} + g_{dp2} \\ C_L &= C_{gsn1} + 2C_{gdn1} + C_{dbn1} + C_{gsp1} + 2C_{gdp1} + C_{dbp1} \\ &\quad + C_{gsp2} + C_{dbp2} + C_{buffer} \end{aligned} \tag{4.11}$$

where g_m is transconductance, g_d is channel conductance, C_{gs} is gate-to-source capacitance, C_{gd} is gate-to-drain capacitance, C_{db} is drain-to-bulk capacitance, C_{buffer} is capacitance of output buffer for measurement purpose.

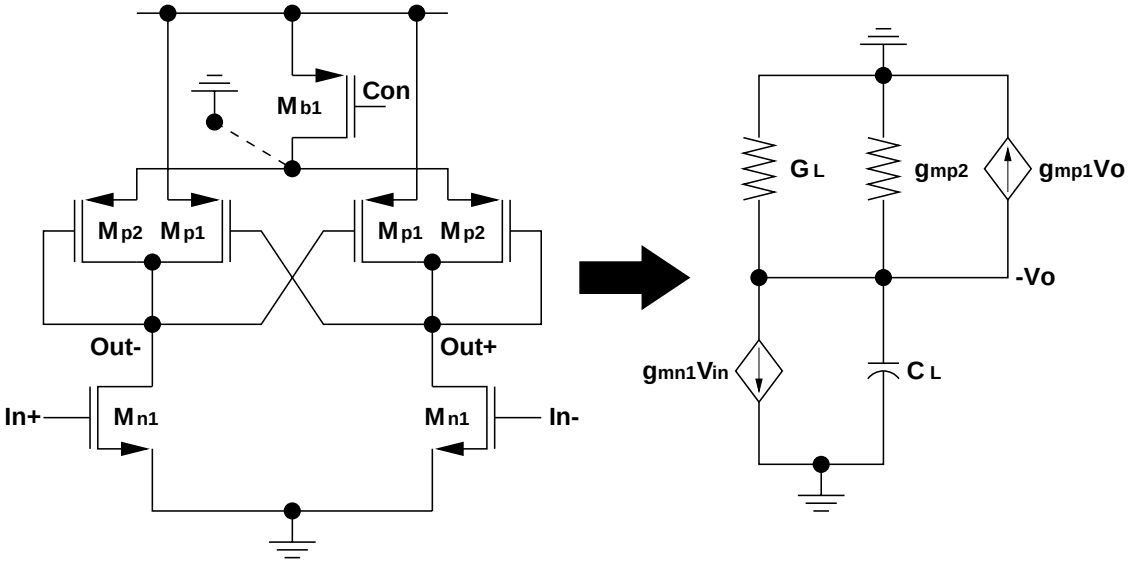


Figure 4.28 Half circuit of the delay cell for operating frequency analysis.

To maintain oscillation, the negative transconductance g_{mp1} must be large enough to overcome the output load G_L ($g_{mp1} > G_L$). By equating the voltage gain of the delay cell to be unity, oscillating frequency of the ring oscillator can be derived as follows

$$f_{osc} = \frac{1}{2\pi}\sqrt{\frac{g_{mn1}^2 - (-g_{mp1} + g_{mp2} + G_L)^2}{C_L^2}} \tag{4.12}$$

By controlling the g_m of diode-connected PMOS devices M_{p2}, oscillating frequency f_{osc} can be tuned. At the maximum oscillating frequency f_{max}, negative transconductance g_{mp1} is just large enough to completely compensate the load G_L ($g_{mp1} = G_L$). At the minimum oscillating frequency f_{min}, diode-connected PMOS transistors M_{p2} are turned off ($g_{mp2} = 0$). Then, maximum frequency f_{max}, minimum frequency f_{min} and operating frequency range f_{range} can be calculated.

$$f_{max} \approx \frac{1}{2\pi} \cdot \frac{g_{mn1}}{C_L} \qquad f_{min} \approx \frac{1}{2\pi} \cdot \sqrt{\frac{g_{mn1}^2 - g_{mp1}^2}{C_L^2}}$$
$$f_{range} \approx f_{max} \cdot \left(1 - \sqrt{1 - \left(\frac{g_{mp1}}{g_{mn1}}\right)^2}\right) \tag{4.13}$$

The maximum oscillating frequency is proportional to g_{mn1}/C_L. Therefore, NMOS input devices are adopted to reduce the corresponding power consumption. From (4.13), 50-% frequency-tuning range can be achieved with transconductance ratio between transistors M_{n1} and M_{p1} to be $g_{mp1}/g_{mn1} = 3/4$.

4.5.3.2 Phase-Noise Analysis

Phase-noise analysis of the ring oscillator is performed based on the ring-oscillator analysis by Ali Hajimiri [18]. Approximate impulse-stimulus function (ISF) of ring oscillator is shown in Figure 4.29. Single-side-band phase noise $\mathrm{L}_{VCO2}\{\Delta\omega\}$ of the two-stage ring oscillator can then be calculated as follows

$$\Gamma_{rms}^2 = \frac{2}{\pi}\int_0^{\pi/2} x^2 dx = \frac{\pi^2}{12}$$
$$\mathcal{L}_{VCO2}\{\Delta\omega\} = N \cdot \frac{\Gamma_{rms}^2}{2 \cdot \Delta\omega^2} \cdot \frac{\overline{i_n^2}/\Delta f}{C_L^2 V_p^2} \quad (4.14)$$

where Γ_{rms} is root-mean square of ISF, $N = 4$ is the number of noise sources, $\Delta\omega$ is frequency offset for phase-noise analysis, V_p is the peak output amplitude, and $\overline{i_n^2}/\Delta f$ is total device noise-power-spectral density. Calculation shows that the phase noise is approximately -107 dBc/Hz at 600-kHz offset.

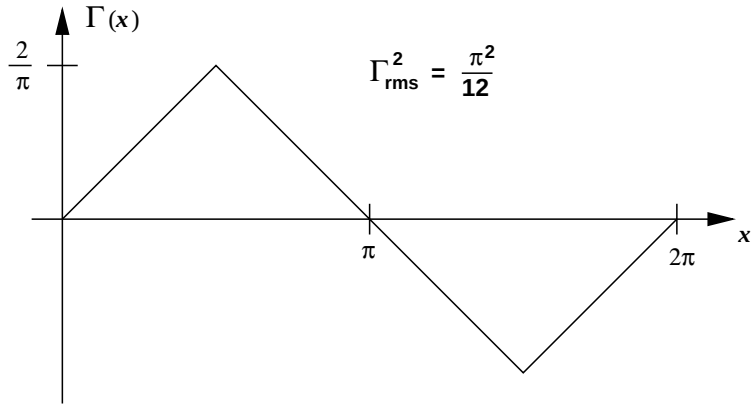


Figure 4.29 Approximate ISF for the ring-oscillator phase-noise analysis.

4.5.4 Design Optimization

Based on the analysis of frequency range and phase noise in Section 4.5.3.1 and Section 4.5.3.2, design optimization of the ring oscillator is done. To reduce parasitic capacitance, all transistors are designed with minimum channel length. In order to achieve the maximum operating frequency, current of transistors M_{p1} and M_{p2} are equal. As shown in Figure 4.30, the maximum operating frequency, tuning range and phase noise at 600-kHz frequency offset are plotted at different W_{n1} and V_{gsn1}.

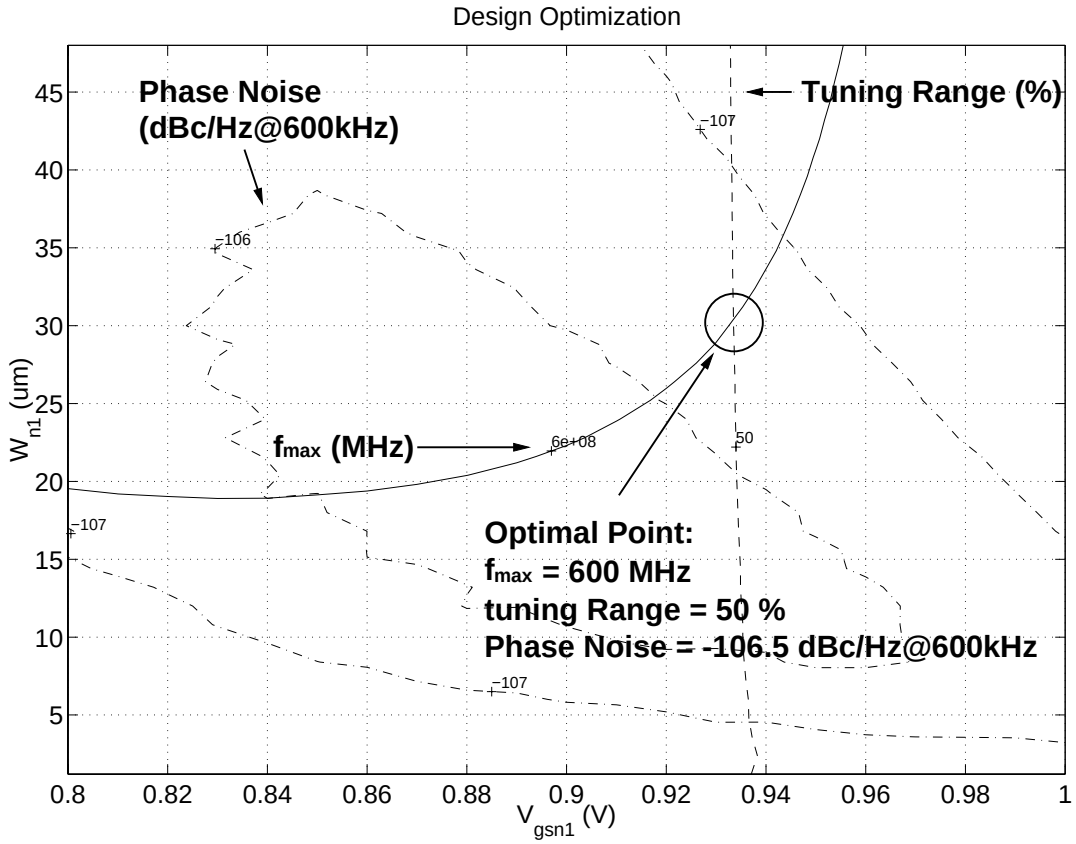


Figure 4.30 Design optimization of the ring oscillator VCO1.

The optimal design solution is found at the point with 600-MHz maximum operating frequency and 50-% tuning range. At that point, phase noise, which is relatively insensitive to W_{n1} and V_{gsn1}, is -106.5 dBc/Hz@600kHz. As supply voltage and current of transistors M_{p1} and M_{p2} are equal, all the other transistors can be determined by W_{n1}. Table 4.5 summaries all the design parameters of the ring oscillator core VCO1 and inverter buffers.

Oscillator Core				Output Buffer	
$(W/L)_{n1}$	30/0.6	$(W/L)_{p1}$	51.6/0.6	$(W/L)_{bn1}$	16.8/0.6
$(W/L)_{p2}$	51.6/0.6	$(W/L)_{b1}$	110.4/0.6	$(W/L)_{bp1}$	48/0.6

Table 4.5 Design parameters of the ring oscillator VCO1.

The ring oscillator is simulated by *SpectreRF*, the simulation results of oscillating frequency f_o, VCO gain K_{vco} and power consumption are shown in Figure 4.31. The oscillating frequency is between 303.6 and 595.6 MHz, single-ended peak-to-peak amplitude is between

1.48 and 2 V_{pp}, and VCO gain is between -600.5 and 0 MHz/V. The phase-noise performance is simulated by the periodic-steady-state (PSS) function of *SpectreRF*. The phase-noise simulation results of the ring oscillator is shown in Figure 4.32

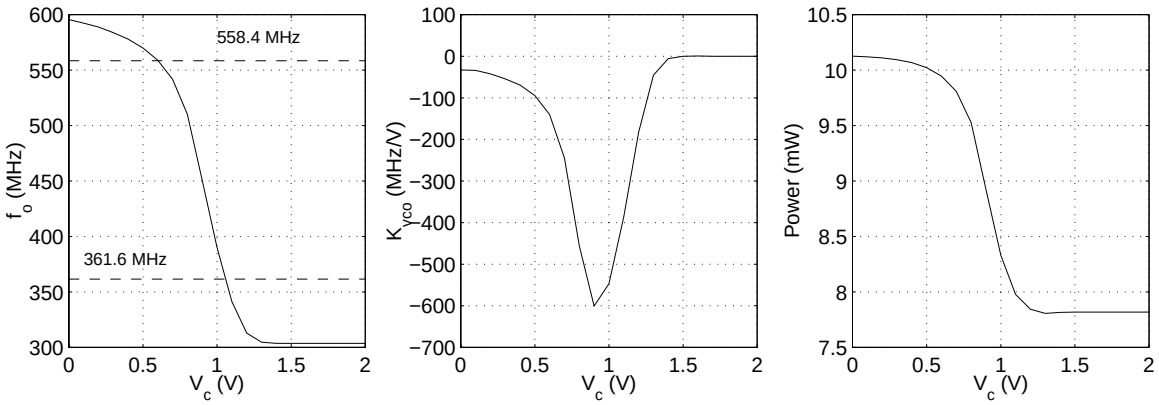


Figure 4.31 Operating frequency, VCO gain and power consumption of the ring oscillator VCO2.

It can be found that the simulated phase noise is around 5 dB lower than the estimation results. As the output amplitude is large, transistors are turned off periodically. Therefore, the transistor-noise sources contribute less phase noise. However, for the LC-oscillator, the main noise sources are from the inductors and pn-junction varactors. Therefore, the large-signal

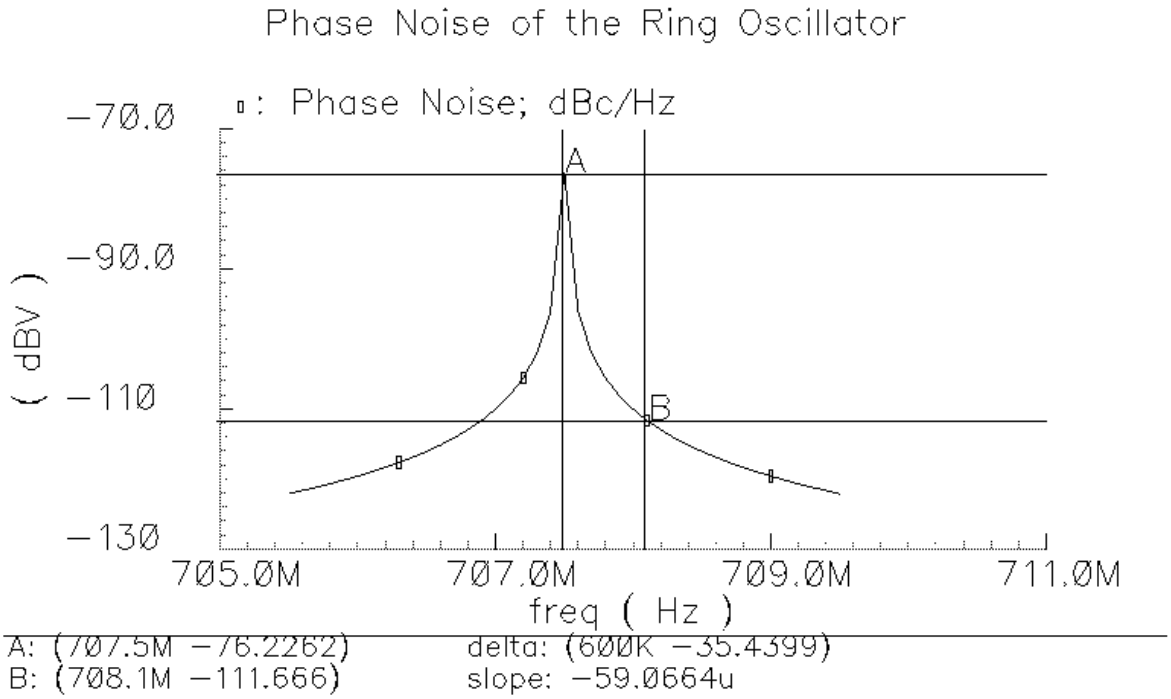


Figure 4.32 Phase-noise performance of the ring oscillator VCO2.

effect of transistors is not significant and simulation results show good agreement to the estimation results for the LC oscillator.

4.6 Frequency Divider N_2

4.6.1 Design Requirement

The frequency divider N_2, which locates in Figure 4.33, is a divide-by-32 frequency divider. It divides the output signals of the ring oscillator VCO1 by 32 and feeds the output signals into the PFD2 of the high-frequency loop. The frequency divider N_2 needs to operate at input frequency is up to 600 MHz.

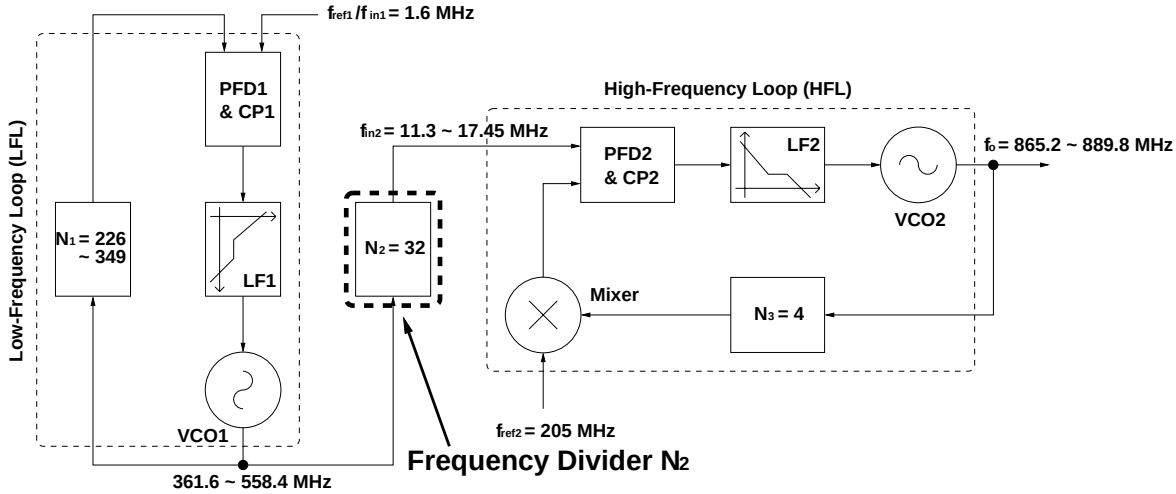


Figure 4.33 Location of the divide-by-32 frequency divider N_2.

4.6.2 Circuit implementation

The divide-by-32 frequency divider N_2 consists of 5 divide-by-2 frequency dividers. The divide-by-2 frequency-divider implementation is the same the one in Figure 4.18. For simplicity, 5 stages are same and the design optimization is similar to that of Figure 4.20. Table 4.6 summaries all the design parameters of the frequency divider N_2. The transient simulation results are shown in Figure 4.34.

$(W/L)_{n1}$	1.5/0.6	$(W/L)_{n2}$	5.4/0.6	$(W/L)_{n3}$	5.4/0.6	$(W/L)_{n4}$	1.5/0.6
$(W/L)_{p1}$	0.9/0.6	$(W/L)_{p2}$	0.9/0.6	$(W/L)_{p3}$	1.5/0.6	$(W/L)_{p4}$	0.9/0.6

Table 4.6 Design parameters of the divide-by-32 frequency divider N_2.

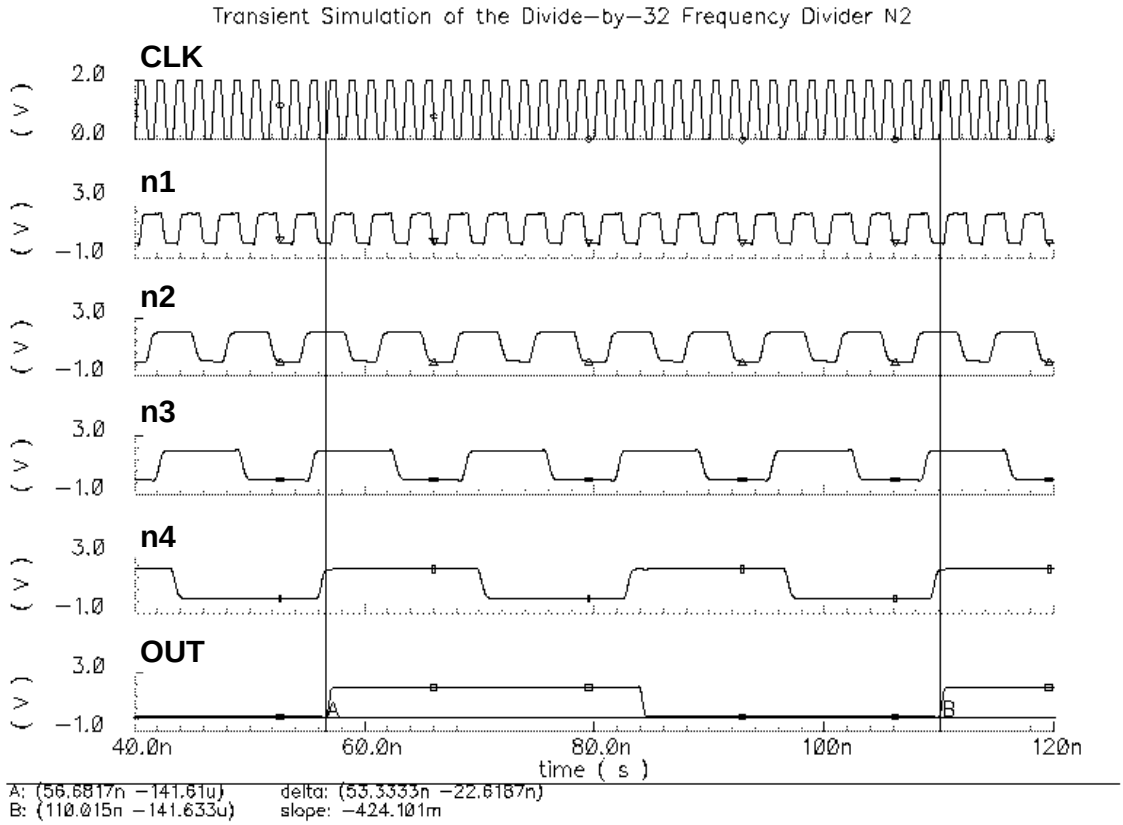


Figure 4.34 Transient simulation of the divide-by-32 frequency divider N_2.

4.7 Programmable-Frequency Divider N_1

4.7.1 Design Requirement

In the feedback path of the low-frequency loop, a programmable-frequency divider N_1 is included for channel selection. Figure 4.35 shows the location of the programmable frequency divider N_1. The design requirement of the divider N_1 is summarized as follows

- operate at frequency up to 600 MHz with minimum power consumption.
- frequency-division ratio is programmable between 226 and 349.

- generate full-swing output with rise time and fall time less than 10% of the total output period.

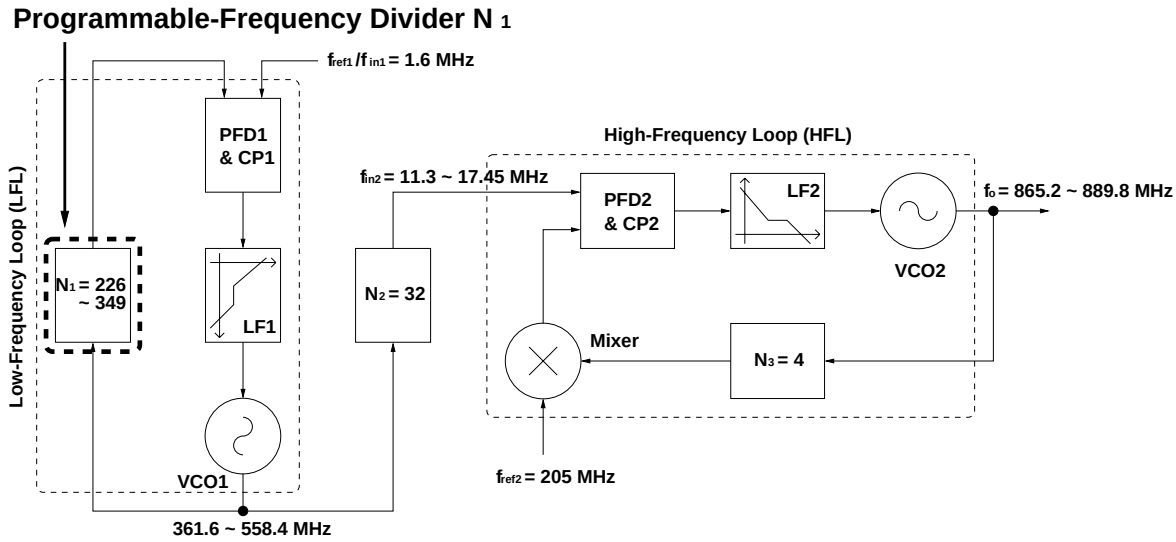
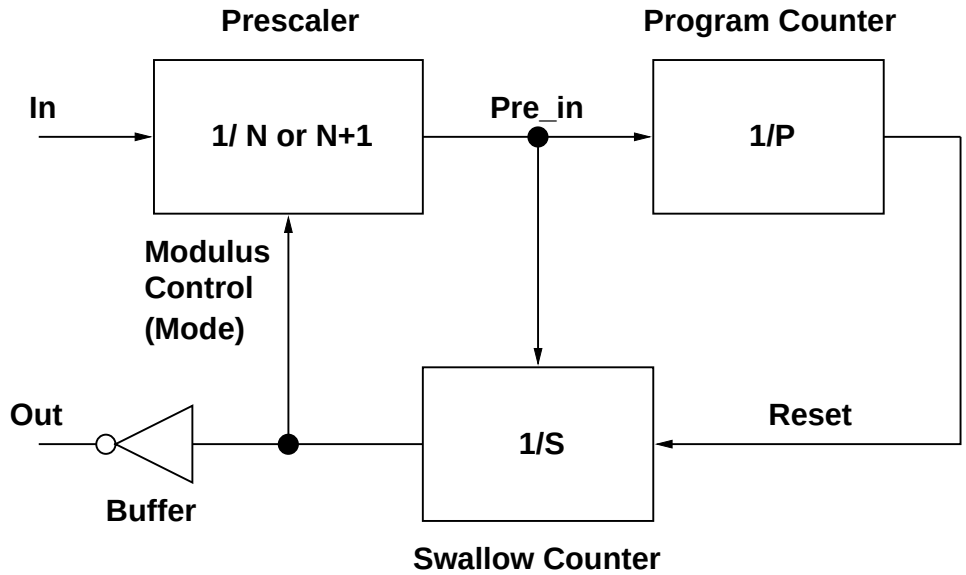


Figure 4.35 Location of the programmable frequency divider N_1.

4.7.2 Circuit Implementation

The programmable-frequency divider N_1 shown in Figure 4.36 consists of a dual-modulus *N/N+1* prescaler, a program counter (*P* counter) and a swallow counter (*S* counter) [18]. The *N/N+1* prescaler divides the input signal by either *N* or *N+1*. The *P* counter,



$$N_1 = (N + 1)\,S + N\,(P - S) = PN + S$$

Figure 4.36 Implementation of the programmable-frequency divider N_1.

which is itself a programmable frequency divider, divides the prescaler output by *P*. The S counter, which is a programmable counter, counts the prescaler output by *S*.

When the programmable divider begins from the reset state, the prescaler divides input signals by *N+1*. The prescaler output is counted by both the *P* counter and the *S* counter. When *S* counter has counted *S* pulses, which is equivalent to *(N+1)S* input cycles, the *S* counter changes the state of the modulus control line *Mode* and the prescaler divides input by *N*. Since the *P* counter has already sensed *S* pulses, it counts the remaining *P - S* cycles, corresponding to *(P - S)N* pulses at the main input, to reach overflow. Finally, the programmable divider generates one complete cycle for every $(N + 1)S + (P - S)N = PN + S$ input cycles. The operation repeats after the *S* counter is reset.

4.7.3 System-Design Optimization

As the frequency-division ratio (between 226 and 349) can be achieved with different combinations of *N*, *S* and *P*, different combinations have their own effect on the frequency divider performance. Therefore, before the design optimization in transistor level, system design optimization should be done. In this programmable-divider design, minimum power consumption is the top criterion. The system design guidelines are shown as follows

- division ratio of *P* counter must be larger than that of *S* counter.
- minimize the operating frequency and number of bits for both *P* and *S* counters.

The prescaler divides by *N + 1* in the first *S* cycles and *N* in the remaining *P - S* cycles. If *S* is larger than *P*, *S* counter will be reset before *S* counter completes its counting and thus the divider cannot function properly. Therefore, *P* must be larger than *S*. In general, a programmable counter is more power consuming than a non-programmable one. Therefore, operating frequency and complexity of both *P* and *S* counters should be minimized.

Table 4.7 shows different combinations of *N*, *P* and *S* which can implement the desired division ratio. In Case 1, it shows the highest operating frequency and the largest number of bits

for *P* counter which is not good for power consideration. In Case 4, it shows the lowest operating frequency. However, since the maximum value of *S* counter is larger than the minimum value of *P* counter, it makes some desired division ratio not programmable. Between Case 2 and 3, Case 3 shows a lower operating frequency with the same counter complexity. However, the design of Case 2 is adopted due to the prescaler implementation issues which will be discussed later in Section 4.7.4.

Case	*N*	Counter-Operating Frequency	*P*	No. of bit	*S*	No. of bit
1	10	55.8 MHz	22 ~ 34	6	0 ~ 9	4
2	12	46.5 MHz	18 ~ 29	5	0 ~ 11	4
3	14	39.9 MHz	16 ~ 24	5	0 ~ 13	4
4	16	34.9 MHz	14 ~ 21	5	0 ~ 15	5

Table 4.7 System design optimization of the programmable frequency divider N_1.

4.7.4 Dual-Modulus Prescaler

4.7.4.1 Operation

The dual-modulus *N*/*N+1* prescaler with *N* = 12 shown in Figure 4.37 is implemented using the back-carrier-propagation approach [19]. The prescaler consists of a gated inverter GINV, two asynchronous divide-by-2 frequency dividers DIV1 & DIV2, a divide-by-3 frequency divider DIV3, a NOR-gate-embedded D-flip-flop NORDFF, and other logic gates INV, NOR and NAND. The gated inverter GINV, which drives the first asynchronous divide-by-2 frequency divider, is transparent to *CLK* = "0" but not transparent to *CLK* = "1" when signal *BLK* = "0". When modulus control signal *MODE* = "1", all the logic gates are disabled and *BLK* is kept high. Therefore, the prescaler functions as an asynchronous divide-by-12 frequency divider. When *MODE* = "0" and the logic gates detect the state *D2,1,0 = "010"*, *BLK* signal is pulled down and thus blocks the propagation of the input clock by one

cycle. With the one-period delay, the prescaler functions as a divide-by-13 frequency divider.

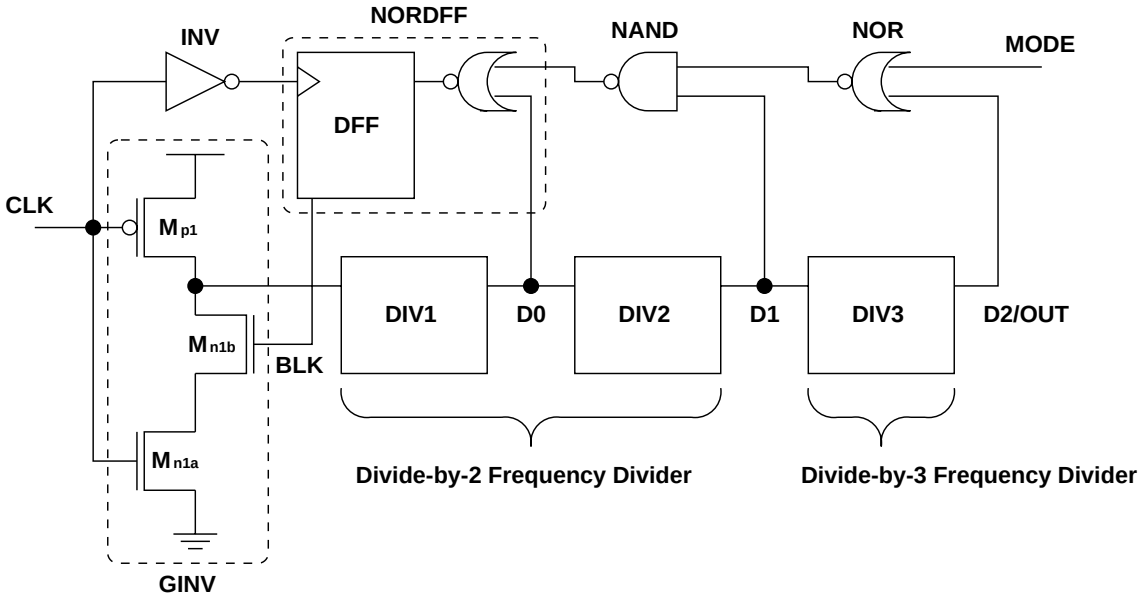


Figure 4.37 Circuit implementation of the dual-modulus prescaler:

The advantage of back-carrier-propagation approach can be shown in Figure 4.38. The asynchronous frequency divider counts from “101”, “001” to “010”. In each division period, the higher order bits *D2* of the counter reach the final state “010” before the lower order bit *D0*. Therefore, the earlier arriving information can be combined first and only quick detection of *D0*

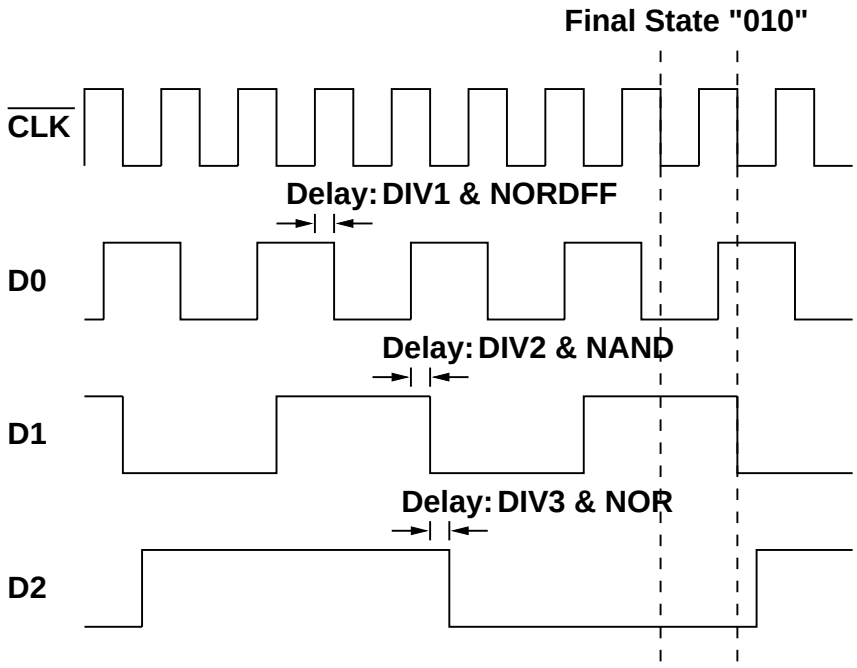


Figure 4.38 Relaxed timing requirement of the back-carrier-propagation approach.

is needed. Such approach provides relaxed delay requirement and thus allows the use of asynchronous frequency divider.

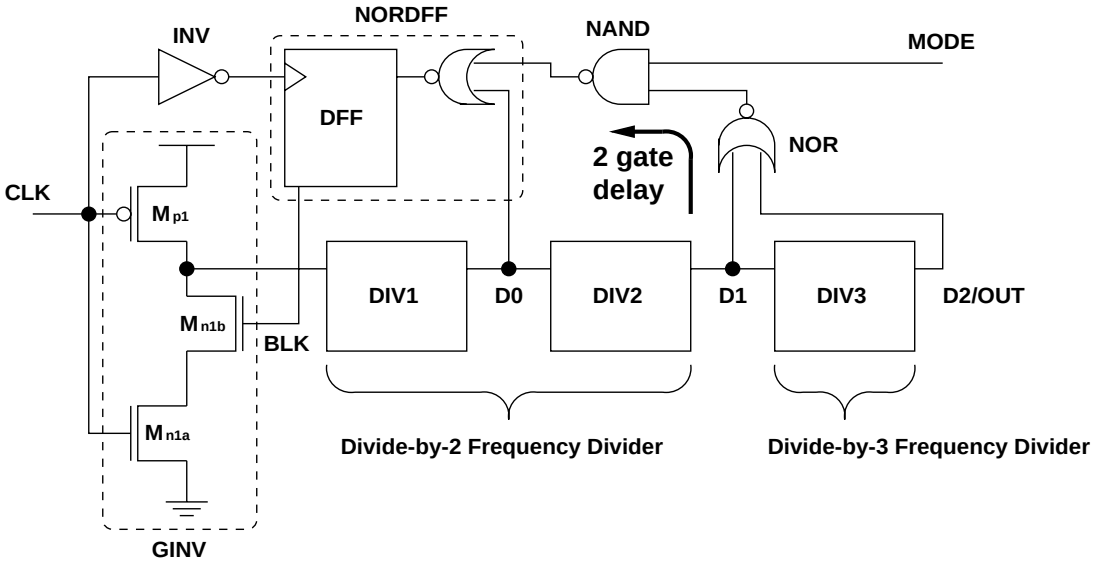


Figure 4.39 Circuit implementation with “000” detection.

Although state “000” can be detected instead of “010”, such configuration requires signal *D1* to tolerate an extra gate delay as shown in Figure 4.39 which is not optimal for speed consideration.

4.7.4.2 Circuit Implementation

The prescaler is implemented by True-Single-Phase-Clock (TSPC) Logic. The divide-by-2 frequency dividers DIV1 & DIV2 are the same that in Figure 4.18. The divide-by-3 divider is implemented by including a half-transparent register before the TSPC D-flip-flop as shown in Figure 4.40 [20]. The half-transparent register provides one-clock-cycle delay to data “1” and no delay for data “0”, and thus the divide-by-3 function can be realized.

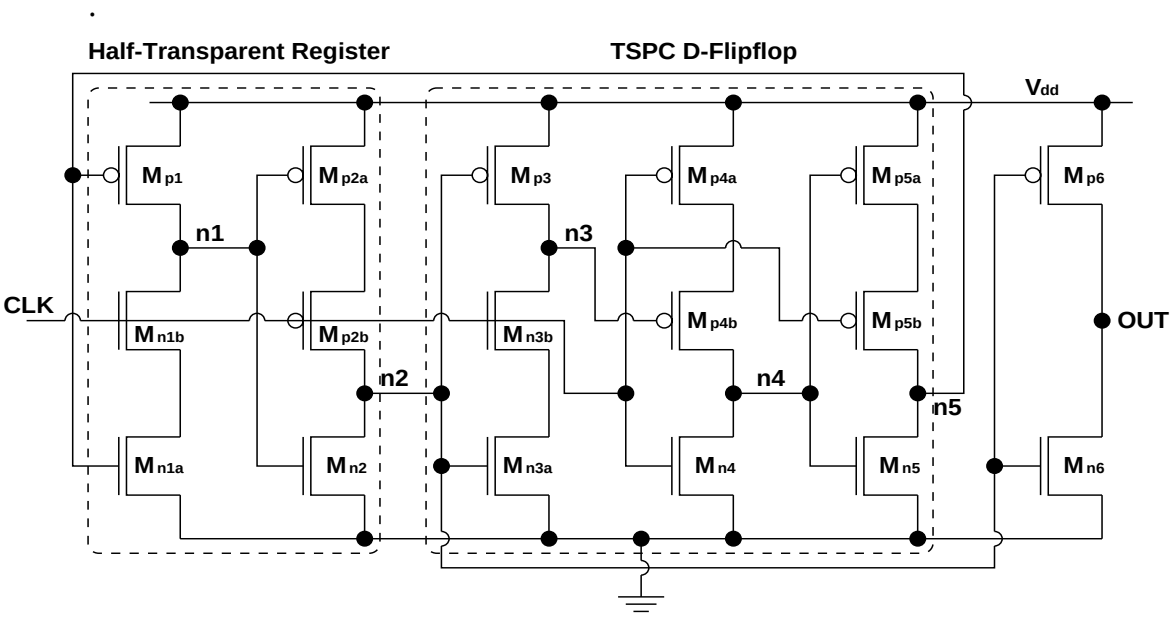


Figure 4.40 Circuit implementation of the divide-by-3 frequency divider DIV3.

The NOR-gate-embedded D-flip-flop NORDFF shown in Figure 4.41 is realized by embedding a NOR gate in the input stage of the TSPC D-flip-flop. Although there are three PMOS transistors in cascode which may degrade the speed, the speed requirement of the first stage is only 50% of input period. In the TSPC D-flip-flop, an transistor M_{p2b} is included so that the node *n2* is not pre-charged every clock cycle and thus output glitch can be eliminated [21].

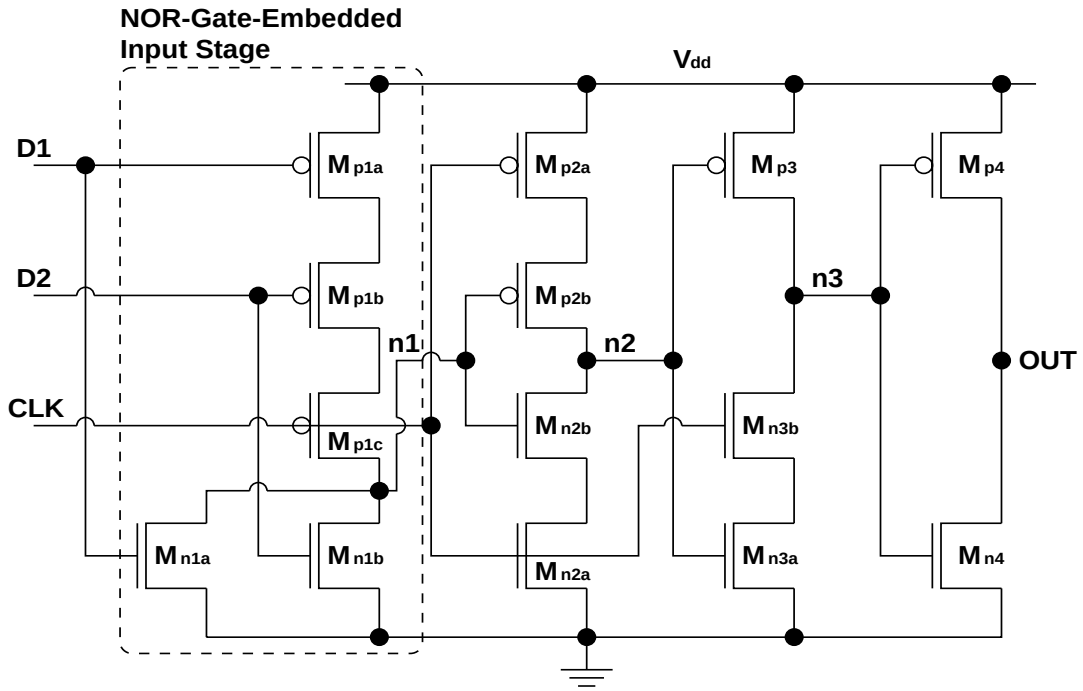


Figure 4.41 Circuit implementation of the NOR-gate-embedded D-flip-flop NORDFF.

The dual-modulus prescaler design optimization is similar to that of the divide-by-2 frequency divider. First, timing requirement of each node is identified by the circuit operation. According to the timing requirement as shown in Figure 4.38, the dual-modulus prescaler is designed by iterative simulation. Design parameters of the dual-modulus prescaler are summarized in Table 4.8.

First Divide-by-2 Frequency Divider DIV1							
$(W/L)_{n1}$	2.4/0.6	$(W/L)_{n2}$	12/0.6	$(W/L)_{n3}$	18/0.6	$(W/L)_{n4}$	3/0.6
$(W/L)_{p1}$	6/0.6	$(W/L)_{p2}$	12/0.6	$(W/L)_{p3}$	39.6/0.6	$(W/L)_{p4}$	7.5/0.6
Second Divide-by-2 Frequency Divider DIV2							
$(W/L)_{n1}$	1.2/0.6	$(W/L)_{n2}$	4.5/0.6	$(W/L)_{n3}$	3.6/0.6	$(W/L)_{n4}$	3/0.6
$(W/L)_{p1}$	2.4/0.6	$(W/L)_{p2}$	2.4/0.6	$(W/L)_{p3}$	15.5/0.6	$(W/L)_{p4}$	10.8/0.6
Divide-by-3 Frequency Divider DIV3							
$(W/L)_{n1}$	1.8/0.6	$(W/L)_{n2}$	1.8/0.6	$(W/L)_{n3}$	1.8/0.6	$(W/L)_{n4}$	1.8/0.6
$(W/L)_{p1}$	3/0.6	$(W/L)_{p2}$	5.4/0.6	$(W/L)_{p3}$	3/0.6	$(W/L)_{p4}$	3/0.6
$(W/L)_{n5}$	1.8/0.6	$(W/L)_{p5}$	3/0.6	$(W/L)_{n6}$	3.6/0.6	$(W/L)_{p6}$	10.8/0.6
NOR-Gate-Embedded D-Flip-Flop NORDFF							
$(W/L)_{n1}$	6/0.6	$(W/L)_{n2}$	9/0.6	$(W/L)_{n3}$	9/0.6	$(W/L)_{n4}$	6/0.6
$(W/L)_{p1}$	30/0.6	$(W/L)_{p2}$	18/0.6	$(W/L)_{p3}$	18/0.6	$(W/L)_{p4}$	21.6/0.6
GINV		INV		NOR		NAND	
$(W/L)_{n1}$	16.8/0.6	$(W/L)_{n1}$	12/0.6	$(W/L)_{n1}$	1.8/0.6	$(W/L)_{n1}$	10.5/0.6
$(W/L)_{p1}$	33.6/0.6	$(W/L)_{p1}$	39.6/0.6	$(W/L)_{p1}$	9/0.6	$(W/L)_{p1}$	18/0.6

Table 4.8 Design parameters of the dual-modulus prescaler.

The prescaler is simulated by *SpectreRF* at 700 MHz. The modulus-control signal *MODE* is switched from “1” to “0” to change the frequency-division ratio. When *N = 13, BLK* signal is activated to provide the required one-clock delay. Simulation results in Figure 4.42 shows that the prescaler functions properly at 700 MHz.

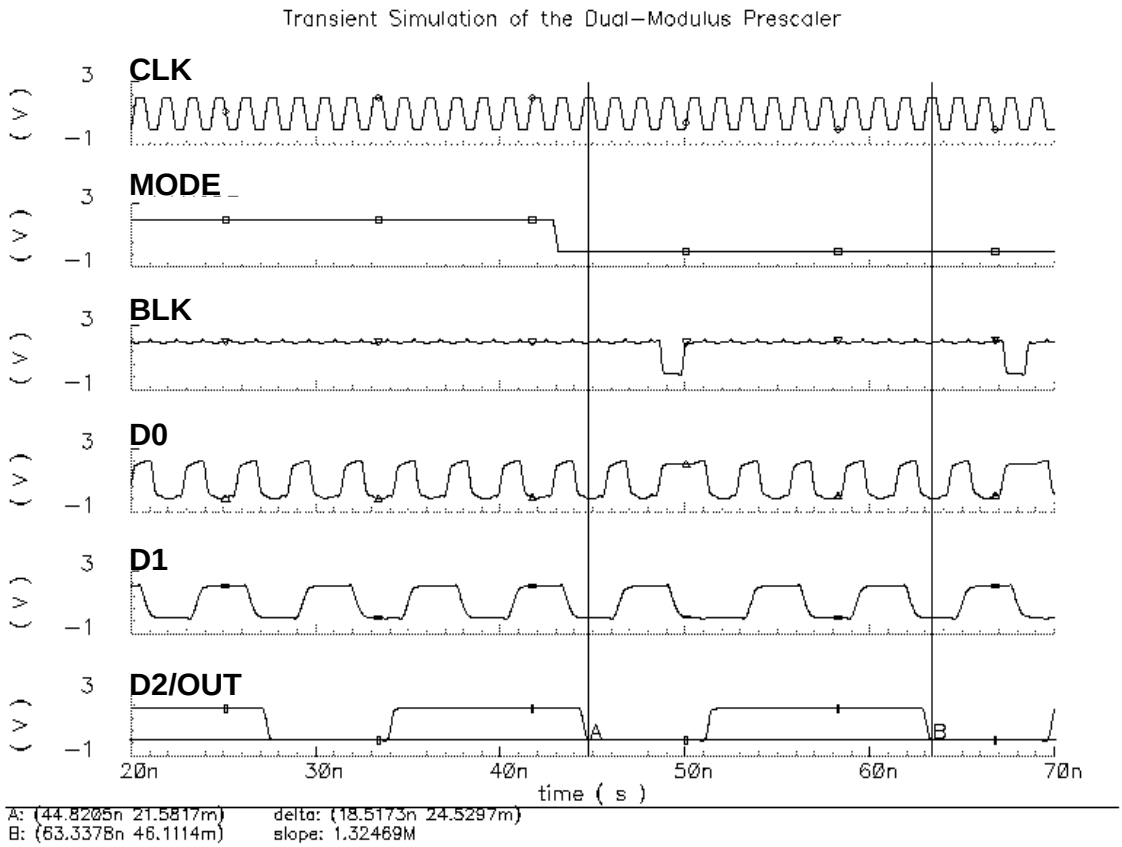


Figure 4.42 Transient simulation of the dual-modulus prescaler at 700 MHz.

4.7.5 *P* and *S* Counters

4.7.5.1 Operation

The 5-bit *P* and 4-bit *S* counters are also implemented by back-carrier-propagation approach. The *P* counter shown in Figure 4.43a consists of five loadable TSPC D-flip-flops (DFF1,...5) as a loadable ripple counter, two static logic gates NAND1 & NAND2 for final state detection, and a NOR-gate-embedded D-flip-flop NORDFF. At the beginning, input *P0* to *P4* is loaded into signal *LV* (stands for Load Value) of all the TSPC D-flip-flops. The counter then counts down to the final state. At the final state, NORDFF generates the reload signal *LOAD* so that signal *LD* (stands for LoaD) of all the flip-flops are reloaded and such operation repeats afterwards.

The implementation of the *S* counter shown in Figure 4.43b is similar to that of the *P* counter. The difference is that a stop signal *STOP* is generated to stop the counter operation at the final state. The *S* counter will be reloaded when *P* counter finishes its counting, and such operation repeats afterwards.

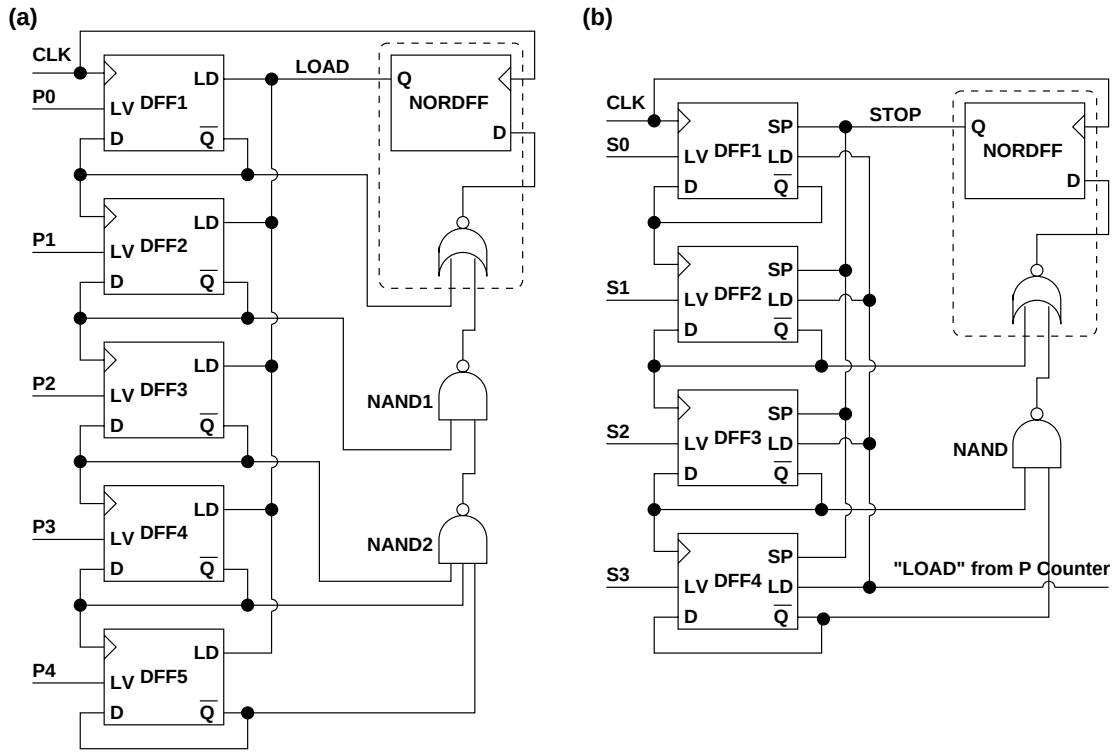


Figure 4.43 Circuit implementation of the (a) *P* counter and (b) *S* counter.

4.7.5.2 Circuit Implementation of the *P* and *S* Counters

The implementation of the loadable TSPC D-flip-flops for the *P* counter is shown in Figure 4.44. To implement the load function, transistors M_{n1b}, M_{p2a}, M_{n3}, M_{p3}, M_{n4}, M_{p4} and M_{n5c} are included. When signal *LOAD* is "1", node *n1* is discharged to "0" to isolate the input signal *D* and output signal $\overline{Q}$. At the same time, nodes *n2*, *n3* and *Q* are made transparent to the load value *LV*. The loadable TSPC D-flip-flop for the *S* counter is the same as that of P counter except that the first load pin *LD* is changed to stop pin *SP*. Since both *P* and *S* counters operate at only 80 MHz, small transistor widths (1.2 μm and 3.0 μm for NMOS and PMOS respectively) are used.

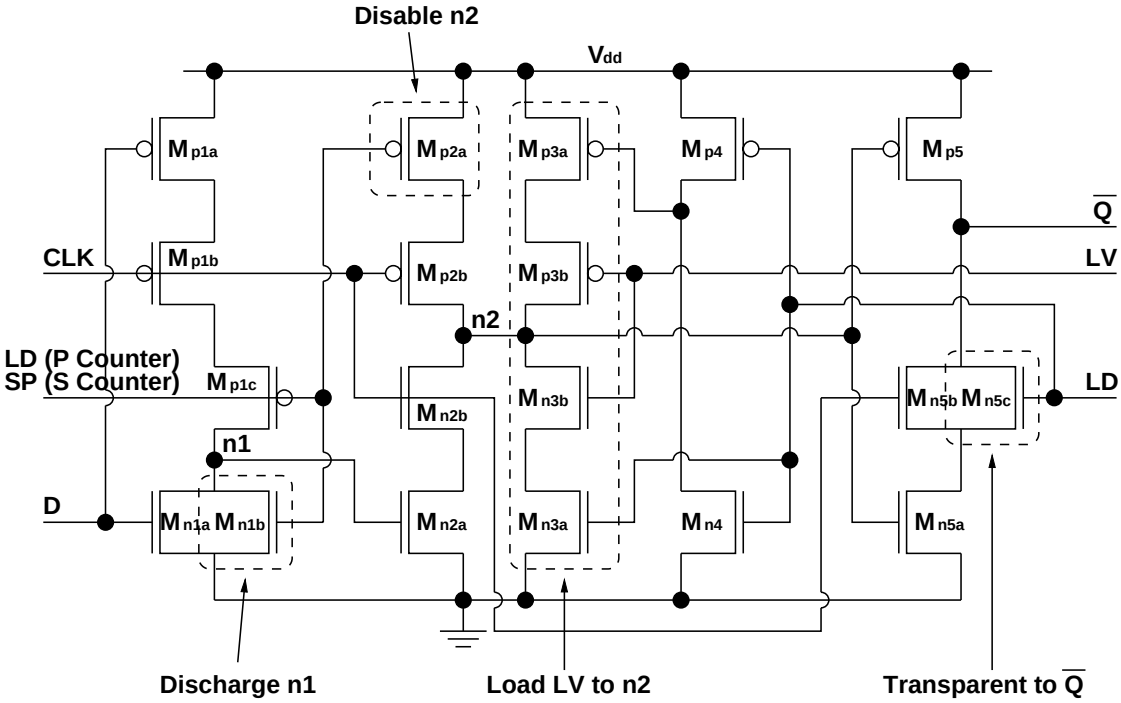


Figure 4.44 Circuit implementation of the loadable TSPC D-flip-flops for both *P* and *S* counters.

4.7.6 Simulation Results

The whole programmable-frequency divider N_1 is simulated by *SpectreRF* with frequency-division ratio N_1 = 349 at 700 MHz and the results are shown in Figure 4.45. The power consumption of the frequency divider is 2.3 mW. The functionality of the programmable-frequency divider at different frequency-division ratio are also verified by transient simulation.

When the frequency division ratio is changed, the divider N_1 may not change its division ratio instantaneously. The worst-case delay is one output cycle (625 ns). However, such delay is negligible when compared to the switching requirement of the system. Therefore, the switching delay of the programmable-frequency divider N_1 is not critical in such application.

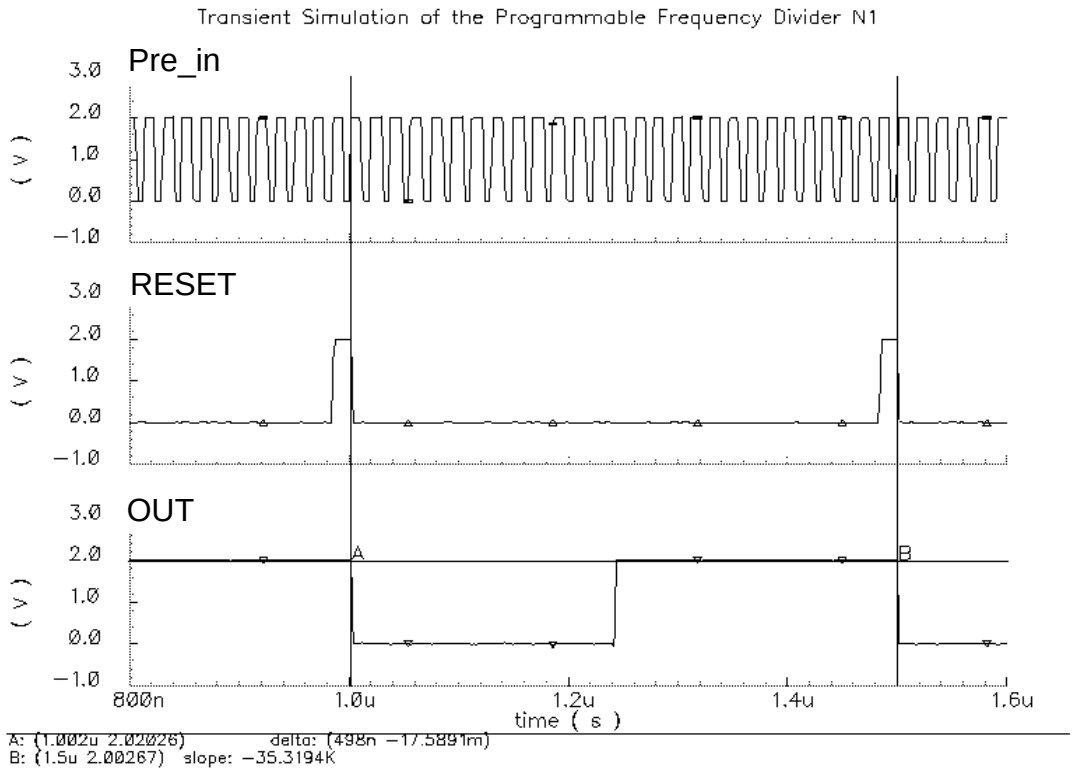


Figure 4.45 Transient simulation of the programmable-frequency divider N_1 = 349.

4.8 Phase-Frequency Detector PDF1 & PFD2

4.8.1 Design Requirement

Figure 4.46 shows the location of both PFD1 and PFD2. The PFDs compare the phases between the reference input and the frequency-divider output and generates the corresponding output signal to control the VCO frequencies. To simplify the design, the same PFD is used in both low-frequency and high-frequency loops. The design requirement of the PFD is as follows

- operate at frequency up to 20 MHz.
- detect both phase and frequency error.
- eliminate dead-zone problem which limits the close-in phase-noise suppression.

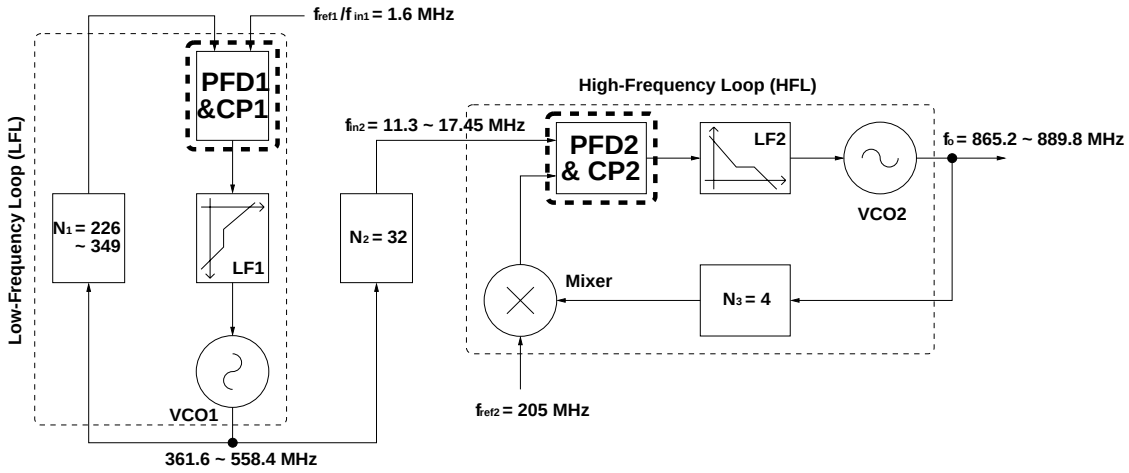


Figure 4.46 Location of the Phase-Frequency Detectors PFD1 & PFD2.

The origin of the dead zone in the PFD is the inability of digital logic gate to generate infinitely short pulses. When phase error $\Delta\phi$ is very small, the PFD cannot compare phase error and the PFD gain K_{PFD} becomes zero as shown in Figure 4.47a. As the loop is broken, both reference and VCO phase noise cannot be suppressed by the loop and thus close-in phase-noise is significantly degraded as shown in Figure 4.47b [22].

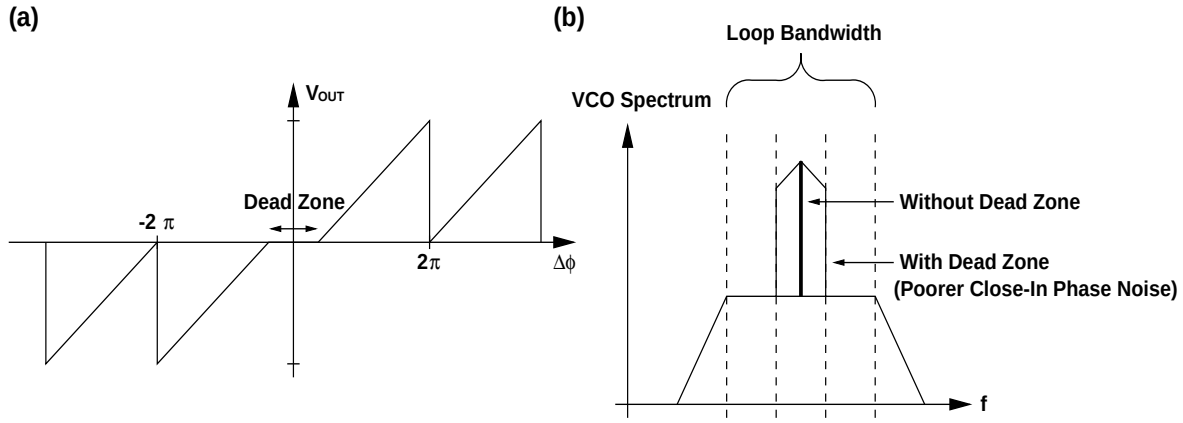


Figure 4.47 The effect of (a) PFD transfer function and (b) close-in phase noise of the PFD with/without dead zone.

4.8.2 Circuit Implementation

The implementation of the PFD is shown in Figure 4.48a. The PFD consists of two TSPC half-transparent registers, a NAND gate and an inverter. As shown in Figure 4.48b, when

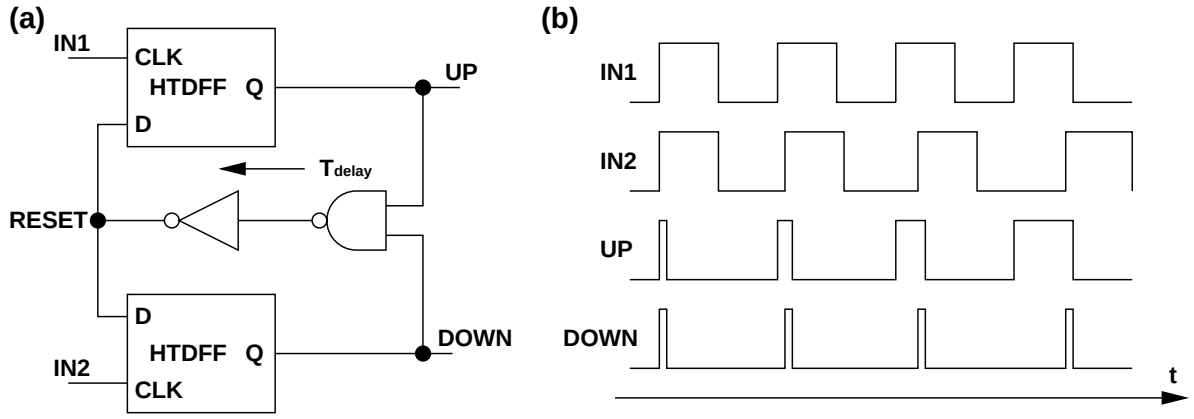


Figure 4.48 PFD implementation: (a) block diagram and (b) operation.

PFD input *IN1* has a rising edge first, a *UP* signal is generated to raise the oscillator frequency. After certain time, PFD input *IN2* has a rising edge, a *DOWN* signal is generated to stop the oscillator-frequency increment. Due to the delay of the NAND gate and inverter (T_{delay}), both *UP* and *DOWN* signals are turned on simultaneously for a period of T_{delay}. The pulse width of both *UP* and *DOWN* signals are kept finite so that dead zone problem can be eliminated. After T_{delay}, a *RESET* signal is generated to reset both TSPC half-transparent registers. If the frequency of *IN1* is larger than that of *IN2*, the pulse width of *UP* signal increases gradually so that frequency difference can also be detected.

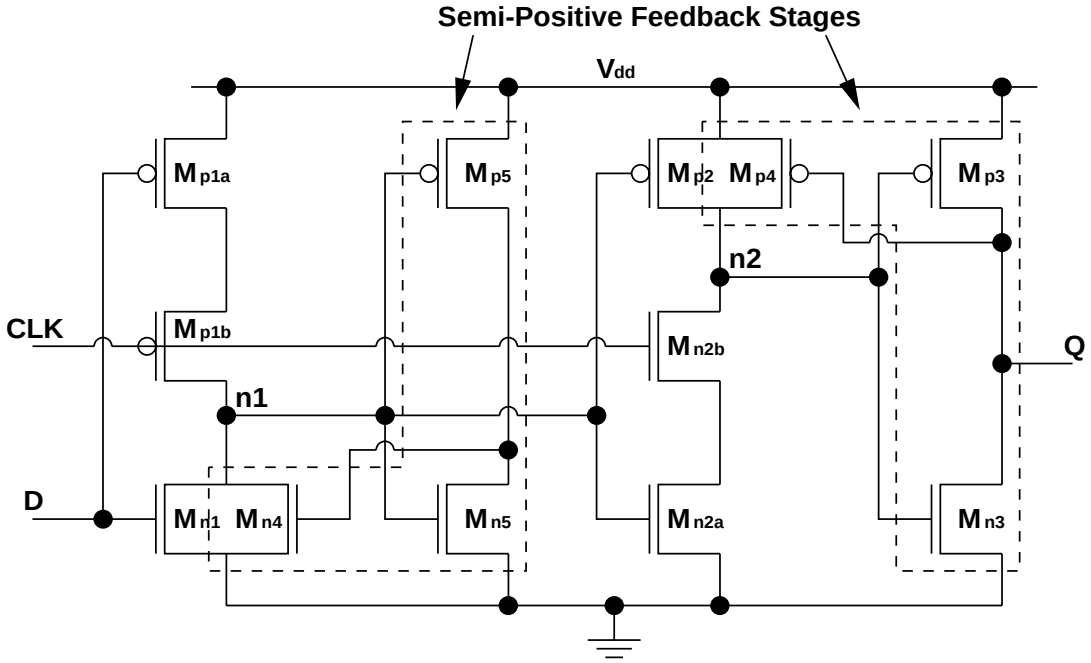


Figure 4.49 Implementation of the TSPC half-transparent D-flip-flop of the PFDs.

The TSPC half-transparent D-flip-flop is implemented as shown in Figure 4.49 which is similar to the one in Figure 4.40 [23]. The half-transparent D-flip-flop HTDFF is transparent to *D* = "1" and has one-clock delay to *D* = "0". As the PFDs operate at frequency down to 1.6 MHz in the low-frequency loop, junction leakage of transistors may cause the charges of the pre-charged nodes *n1* and *n2* to leak out significantly. Therefore, semi-positive feedback stages (M_{n4}, M_{p4}, M_{n5} and M_{p5}) are added to the nodes *n1* and *n2* in order to maintain the pre-charged node voltages [24].

4.8.3 Design and Simulation

As the PFDs are operating at low frequencies, the transistor sizes can be very small. For the semi-positive feedback stages, long channel devices are used for transistors M_{n3} and M_{p3} to provide the weak positive feedback. All the design parameters are summarized in Table 4.9.

Half-Transparent D-Flip-Flop HTDFF				NAND	
$(W/L)_{n1}$	0.9/0.6	$(W/L)_{p1}$	3.9/0.6	$(W/L)_{n1}$	0.9/0.6
$(W/L)_{n2}$	1.8/0.6	$(W/L)_{p2}$	1.2/0.6	$(W/L)_{p1}$	0.9/0.6
$(W/L)_{n3}$	0.9/0.6	$(W/L)_{p3}$	2.1/0.6	INV	
$(W/L)_{n4}$	0.9/1.8	$(W/L)_{p4}$	0.9/1.8	$(W/L)_{n1}$	0.9/0.6
$(W/L)_{n5}$	0.9/0.6	$(W/L)_{p5}$	0.9/0.6	$(W/L)_{p1}$	1.5/0.6

Table 4.9 Design parameters of the PFDs.

To simulate the PFD, two input signals at frequencies 2 MHz and 2.2 MHz are applied to the PFD. As shown in Figure 4.50, the increasing pulse width of the DOWN signal means that the PFD functions properly.

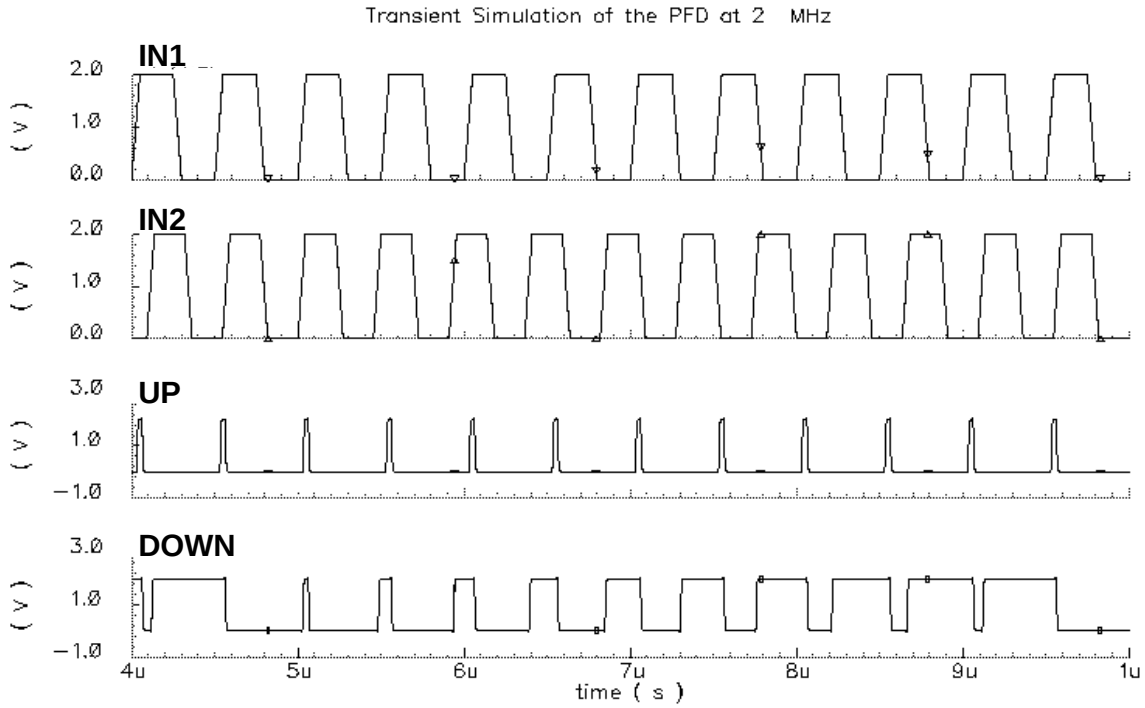


Figure 4.50 Simulation results of the PFDs at 2 MHz.

4.9 Charge Pumps and Loop Filters

4.9.1 Design Requirement

Figure 4.51 shows the location of the charge pumps CP1 & CP2, and loop filters LF1 & LF2 of both loops. According to the *UP* and *DOWN* signals of the PFDs, charge pumps inject or sink current to or from the loop filters. The loop filters filter out the high frequency components, to maintain the spectral purity of the VCO. The design requirement of the charge-pumps and loop filters are as follows

- operate at frequency up to 20 MHz.
- minimize the loop-filter chip area.
- satisfy the spurious-tone specification (< -88 dBc) and the phase-noise specification (< -121 dBc/Hz@600kHz) of the frequency synthesizer.

To satisfy both the phase-noise and spurious-tone specification, the loop bandwidth of both loops are reduced to several tens kHz. Therefore, large capacitors (~ 1 nF) and resistors (~ 100 kΩ) used for the loop-filter implementation are the very critical to the synthesizer integration.

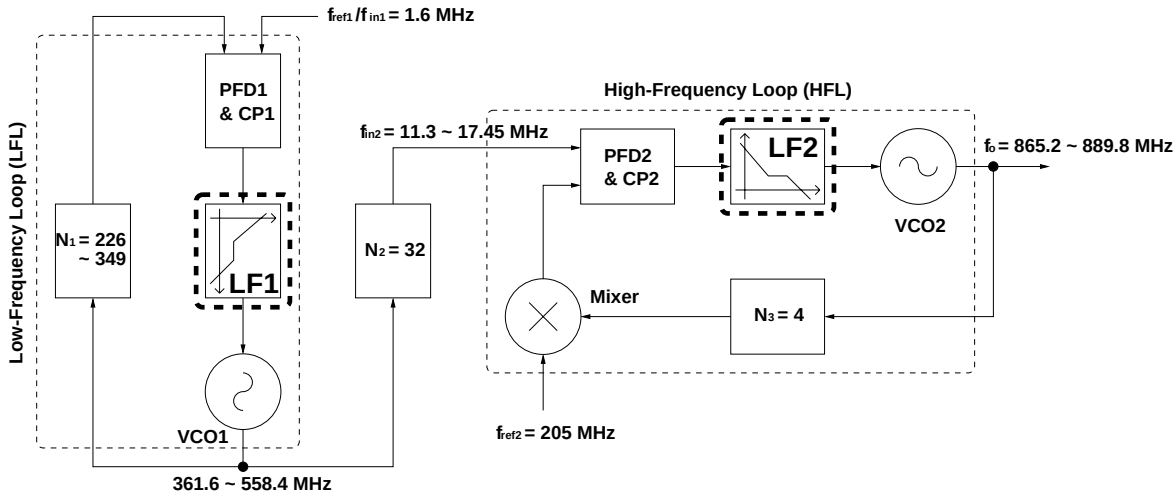


Figure 4.51 Location of the charge-pumps CP1 & CP2, and loop filters LF1 & LF2.

4.9.2 Circuit Implementation

4.9.2.1 Charge Pumps CP1 & CP2

Figure 4.52 shows the circuit implementation of the charge pumps. High-swing-cascode current sources are adopted to achieve both high output-impedance and low supply-voltage requirement. In the design of charge-pump current, the current level is in the order of 1 μA which cannot be accurately measured by an ammeter. Therefore, current mirror input is made sixteen times larger than that of the charge-pump core to make the charge-pump current measurable. Moreover, current-source mismatch degrades the spurious-tone performance as discussed in the Section 4.9.4.1. Therefore, long channel devices are used to reduce current mismatch.

For single-ended charge-pump design (without SW1b & 2b), current sources are turned off when switches are off. To turn off the current sources, nodes *ns* and *ps* are discharged to *gnd* and V_{dd} respectively. Therefore, long time is needed to charge up these nodes again when the switches are turned on. To eliminate current-source-charge-up time, differential design (with SW1b & 2b) is adopted so that voltages of nodes *ns* and *ps* are close to the loop-filter output voltage.

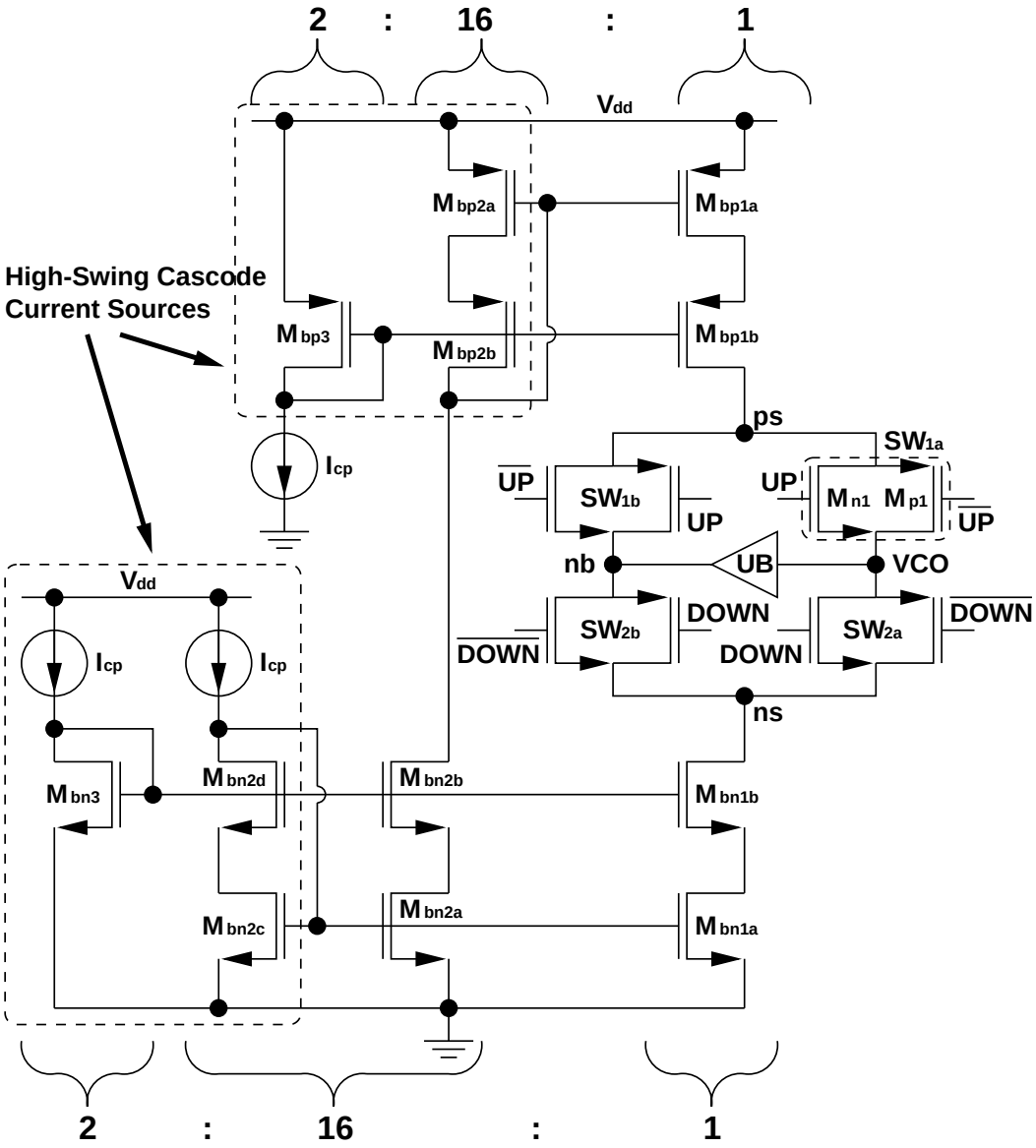


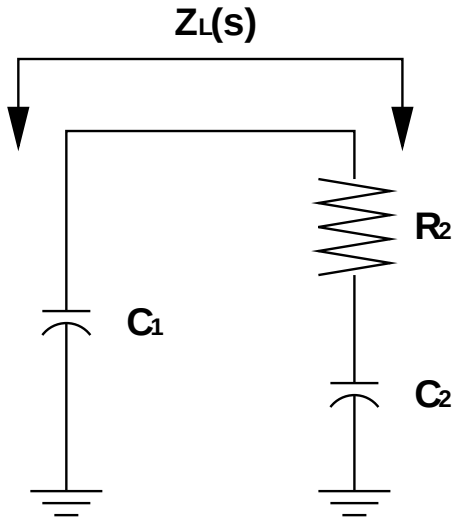
Figure 4.52 Circuit implementation of the charge pumps CP1 & CP2.

As discussed in Section 4.9.4.2, complementary switches (SW1a, 1b, 2a & 2b) are used to cancel out the clock feed through of the switches. Between nodes *OUT* and *nb*, an unity-gain buffer UB is included to keep the voltages of nodes *ns*, *ps* and *nb* to be the same as that of node *OUT*. As discussed in Section 4.9.4.3, charge sharing between nodes *ns*, *ps* and *OUT* can be minimized with this buffer [25].

4.9.2.2 Loop-Filter Implementation LF1 & LF2

The loop filters of the frequency synthesizer are shown in Figure 4.53. It consists of a

capacitor C_1 for zero phase error, a series resistor R_2 for loop-stability consideration, and another capacitor C_2 for high-frequency-spur filtering. With the pole and zero location given, the required capacitance and resistance values can be determined.



Loop-Filter Impedance:

$$Z_L(s) = \frac{1 + sR_2C_2}{s(C_1 + C_2)(1 + sR_2(C_1 \| C_2))}$$

$$Z_L(s) = \frac{1 + s\tau_z}{s\tau_i(1 + s\tau_p)}$$

Figure 4.53 Circuit implementation of the loop filters LF1 & LF2.

The resistor R_2 is implemented by the silicide-blocked polysilicon to achieve high resistance with small chip area and small parasitic capacitance. The capacitors C_1 & C_2 are implemented by linear capacitor, which is the oxide capacitor between polysilicon and n+diffusion inside N-well as shown in Figure 4.54a. To eliminate the parasitic N-well capacitance, n+ nodes are connected to ground terminal.

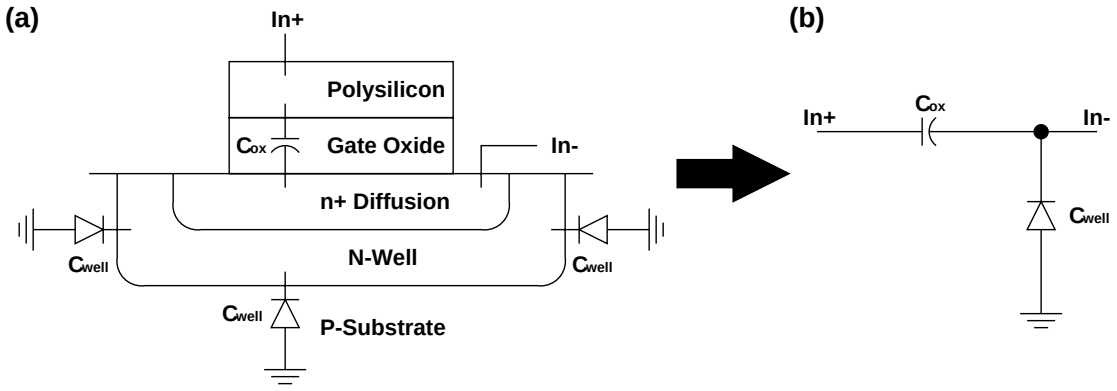


Figure 4.54 Linear capacitor for loop-filter-capacitor implementation C_1 & C_2: (a) device structure and (b) circuit model.

4.9.3 Frequency-Synthesizer Modelling

In the design of the charge pumps and loop filters, a lot of consideration must be paid on the spurious tones, phase noise, loop stability, and chip area. To achieve the optimal solution which satisfies all the specification with minimum chip area, spurious tones, phase noise and loop stability must be carefully modelled analyzed, the modelling of the frequency synthesizer is discussed in this section.

Figure 4.55 shows the linear model of the dual-loop frequency synthesizer.This linear model models the relationship between output phase of the synthesizer θ_{o2} and phases of both reference signals θ_{ref1} & θ_{ref2}. The phase-frequency detectors PFD1 & PFD2, and charge

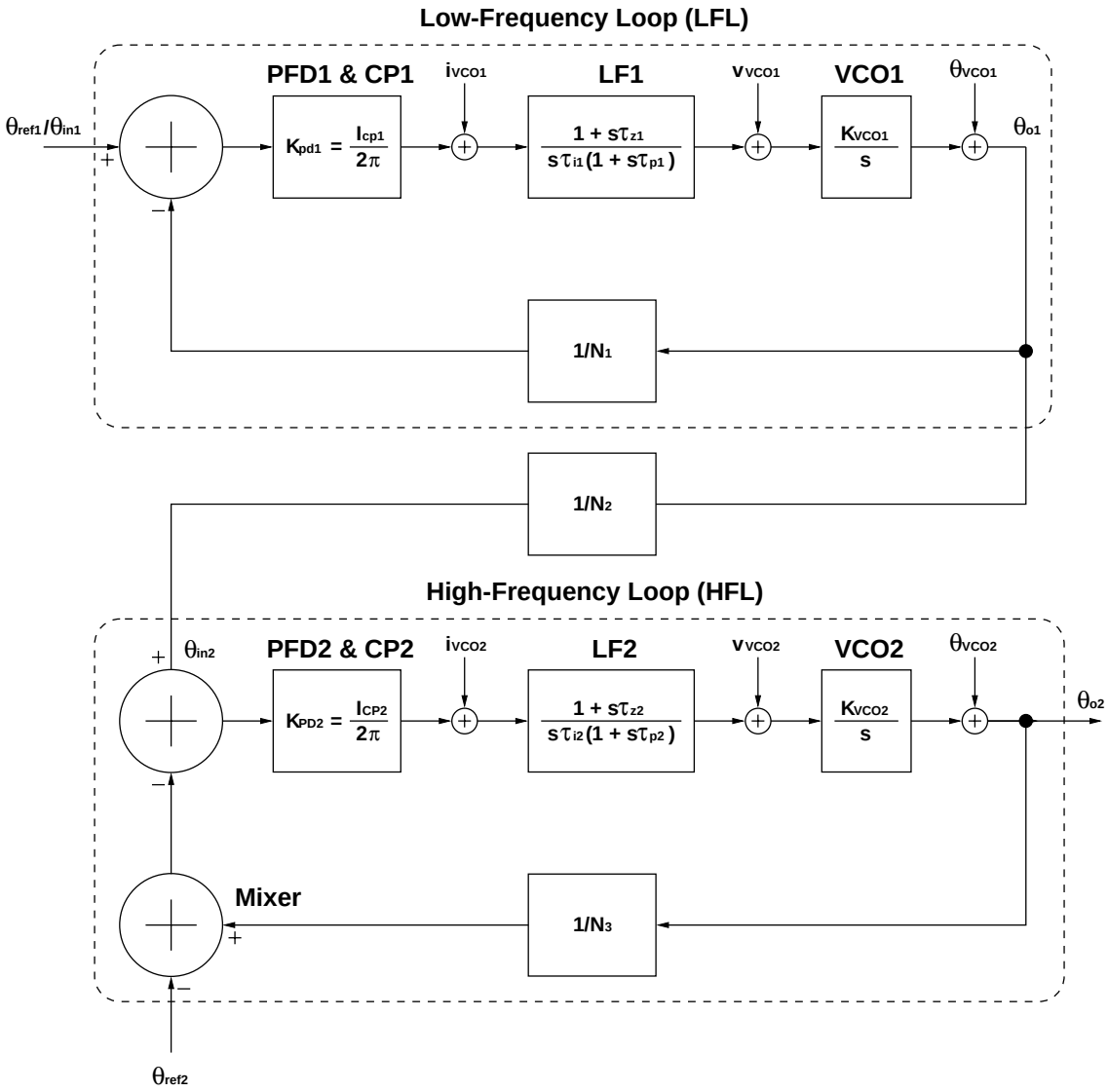


Figure 4.55 Linear model of the dual-loop frequency synthesizer.

pumps CP1 & CP2 are modelled by subtractors which generate charge-pump current I_{CP} according to the phase difference. Although the phase-detector gain K_{PD} shown in Figure 4.47 is non-linear, this model well models the linear characteristics of the PFDs. The loop filters are modelled by an integrator τ_i for zero phase error, a zero τ_z for stability consideration and another pole τ_p for high-frequency-spur filtering. For the voltage-controlled oscillators VCO1 & VCO2, output frequency f_o is proportional to the VCO-control voltage v_{VCO}. Therefore, the VCO, which is the transfer function between control voltage v_{VCO} to output phase θ_{o2}, is modelled by the product of an integrator and VCO gain K_{VCO}. As frequency division is the same as phase division, frequency dividers N_1, N_2 *and* N_3 are modelled by gain factors $1/N_1$, $1/N_2$ and $1/N_3$ respectively. Since down-conversion mixing produces frequency substraction as well as phase subtraction, the down-conversion mixer is modelled by a subtractor.

Based on the linear model of the frequency synthesizer, transfer function from input phase θ_{in} to output phase θ_o of both low-frequency and high-frequency loops can be expressed as follows

$$\begin{aligned}\frac{\theta_{o1}}{\theta_{in1}}(s) &= \frac{N_1(1+s\tau_{z1})}{1+s\tau_{z1}+(N_1\tau_{i1}/K_{PD1}K_{VCO1})s^2(1+s\tau_{p1_1})}\\ \frac{\theta_{o2}}{\theta_{in2}}(s) &= \frac{N_3(1+s\tau_{z2})}{1+s\tau_{z2}+(N_3\tau_{i2}/K_{PD2}K_{VCO2})s^2(1+s\tau_{p2_1})}\end{aligned} \tag{4.15}$$

where K_{PD} is phase-detector gain, K_{VCO} is VCO gain, τ_i is integrator time constant, τ_z is zero time constant, and τ_p is pole time constant. For the spurious-tone analysis in Section 4.9.4, the transfer functions from charge-pump current i_{CP} to output phase θ_o can be expressed as follows

$$\begin{aligned}\frac{\theta_{o1}}{i_{CP1}}(s) &= \frac{(N_1/K_{PD1})(1+s\tau_{z1})}{1+s\tau_{z1}+(N_1\tau_{i1}/K_{PD1}K_{VCO1})s^2(1+s\tau_{p1_1})}\\ \frac{\theta_{o2}}{i_{CP2}}(s) &= \frac{(N_3/K_{PD2})(1+s\tau_{z2})}{1+s\tau_{z2}+(N_3\tau_{i2}/K_{PD2}K_{VCO2})s^2(1+s\tau_{p2_1})}\end{aligned} \tag{4.16}$$

For the phase-noise analysis of charge pumps and loop filters in Section 4.9.5.1, the transfer functions from VCO-control voltage v_{VCO} to output phase θ_o can be expressed as follows

$$\begin{aligned}\frac{\theta_{o1}}{v_{VCO1}}(s) &= \frac{(N_1/K_{VCO1})s(1+s\tau_{p1})}{1+s\tau_{z1}+(N_1\tau_{i1}/K_{PD1}K_{VCO1})s^2(1+s\tau_{p1_1})} \\ \frac{\theta_{o2}}{v_{VCO2}}(s) &= \frac{(N_3/K_{VCO2})s(1+s\tau_{p2})}{1+s\tau_{z2}+(N_3\tau_{i2}/K_{PD2}K_{VCO2})s^2(1+s\tau_{p2_1})}\end{aligned} \tag{4.17}$$

For the phase-noise analysis of VCOs in Section 4.9.5.2, the transfer functions from VCO-output phase θ_{VCO} to output phase θ_o can be expressed as follows

$$\begin{aligned}\frac{\theta_{o1}}{\theta_{VCO1}}(s) &= \frac{(N_1/K_{PD1}K_{VCO1})s^2(1+s\tau_{p1})}{1+s\tau_{z1}+(N_1\tau_{i1}/K_{pd1}K_{VCO1})s^2(1+s\tau_{p1_1})} \\ \frac{\theta_{o2}}{\theta_{VCO2}}(s) &= \frac{(N_3/K_{PD2}K_{VCO2})s^2(1+s\tau_{p2})}{1+s\tau_{z2}+(N_3\tau_{i2}/K_{pd2}K_{VCO2})s^2(1+s\tau_{p2_1})}\end{aligned} \tag{4.18}$$

4.9.4 Spurious-Tone Analysis

In this section, the spurious tones, which is mainly caused by the charge pumps, is discussed. Different causes of the spurious tones such as current mismatch, clock feed through, charge injection, and charge sharing are discussed and analyzed. Based on the analysis results, the charge pumps are designed accordingly to optimize the spurious-tone performance.

4.9.4.1 Current Mismatch

As discussed in Section 4.8.2, a feedback-delay time T_{delay} is added in the PFDs in order to eliminate the dead-zone problem. During the delay time, both pull-up and pull-down charge-pump current are turned on. In the ideal situation, these pull-up and pull-down current are exactly the same so that no net current is injected into the loop filter. However, the mismatch between pull-up and pull-down charge-pump current introduces current injection ΔI_{CP} as shown in Figure 4.56. Such current disturbs the node *VCO* and causes spurious tones.

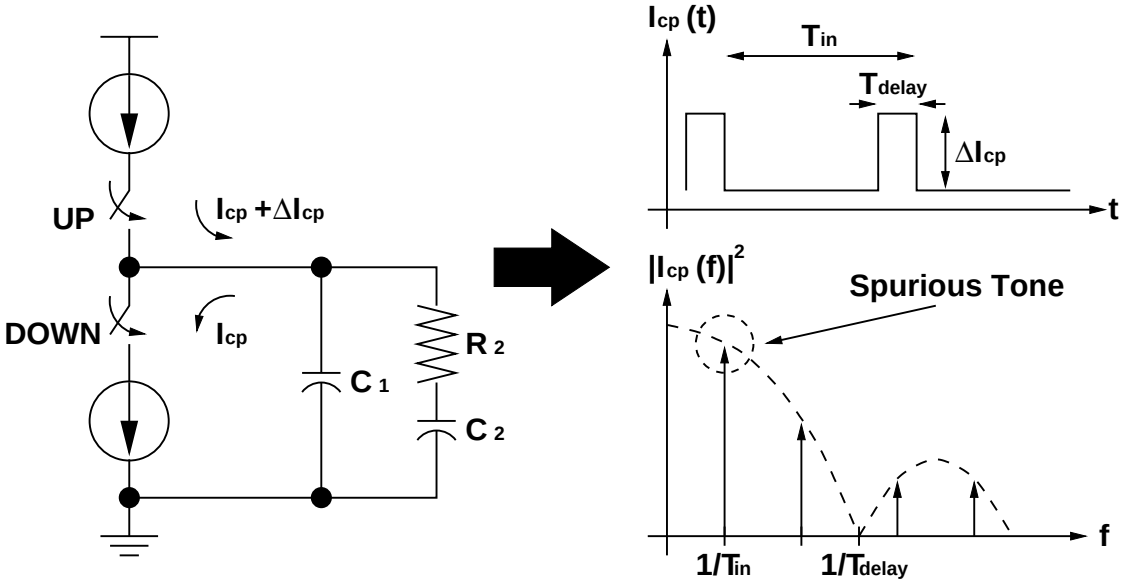


Figure 4.56 Charge-pump current-injection mismatch: (a) cause, (b) transient response, and (c) frequency response.

The cause of the current mismatch is mainly due to the mismatches of channel width *W*, channel length *L*, and threshold voltage V_t of current mirrors as shown in Figure 4.57. Assume that cascode transistors do not have any effect in the mismatch, the current mismatch of a current mirror can be expressed as follows

$$\frac{\Delta I}{I} = \frac{\Delta W}{W} + \frac{\Delta L}{L} + \frac{2V_t}{V_{gs} - V_t}\left(\frac{\Delta V_t}{V_t}\right) \tag{4.19}$$

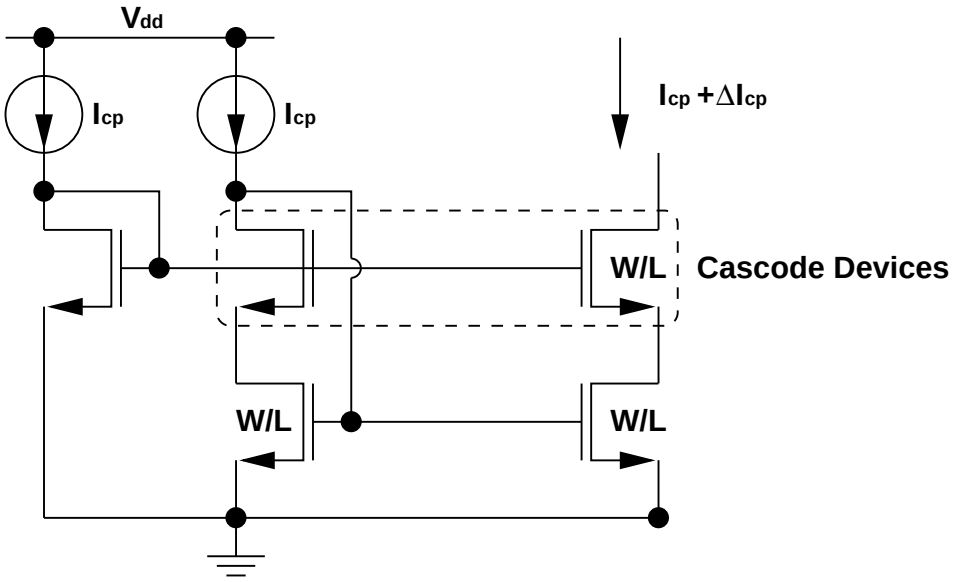


Figure 4.57 Current-mismatch analysis of a current mirror.

To reduce the current mismatch, wide and long channel devices (L = 3 μm) are used. Although V_{gs} - V_t should be increased to reduce current mismatch due to threshold-voltage mismatch, it reduce the output range of the charge pump. Therefore, V_{gs} - V_t is designed to be 0.2 V to compromise these two design criteria.

The total charge-pump current mismatch is caused by the mismatches between the NMOS and PMOS current mirrors in Figure 4.52. Based on the same disturbance analysis, the total charge-pump current mismatch can be expressed as follows

$$\begin{aligned}\frac{\Delta I_{CP}}{I_{CP}} &= \frac{\Delta W_{bn1}}{W_{bn1}} + \frac{\Delta L_{bn1}}{L_{bn1}} + \frac{2V_{tbn1}}{V_{gsbn1} - V_{tbn1}}\left(\frac{\Delta V_{tbn1}}{V_{tbn1}}\right) \\ &\quad + \frac{\Delta W_{bp1}}{W_{bp1}} + \frac{\Delta L_{bp1}}{L_{bp1}} + \frac{2V_{tbp1}}{V_{gsbp1} - V_{tbp1}}\left(\frac{\Delta V_{tbp1}}{V_{tb1}}\right)\end{aligned} \tag{4.20}$$

Assume the charge-pump current waveform is the same as that in Figure 4.56b, the spurious-tone performance due to the charge-pump current mismatch of both loops S_{CM_CP1} & S_{CM_CP2} can be expressed as follows

$$\begin{aligned}S_{CM\_CP1}\{\omega_{in1}\} &= \frac{1}{2}\cdot\left(\frac{2\Delta I_{CP1}}{\pi}\right)^2 \sin^2\left(\frac{\pi T_{delay1}}{T_{in1}}\right)\cdot\left|\frac{\theta_{o1}}{i_{CP1}}(\omega_{in1})\right|^2\cdot\left(\frac{1}{N_2}\right)^2\cdot\left|\frac{\theta_{o2}}{\theta_{in2}}(\omega_{in1})\right|^2 \\ S_{CM\_CP2}\{\omega_{in2}\} &= \frac{1}{2}\cdot\left(\frac{2\Delta I_{CP2}}{\pi}\right)^2 \sin^2\left(\frac{\pi T_{delay2}}{T_{in2}}\right)\cdot\left|\frac{\theta_{o2}}{i_{CP2}}(\omega_{in2})\right|^2\end{aligned} \tag{4.21}$$

where $S_{CM\_CP1}\{\omega_{in1}\}$ and $S_{CM\_CP2}\{\omega_{in2}\}$ are the spurious-tone performance of charge pump current mismatch of the low-frequency loop and high-frequency loop respectively, ΔI_{CP1} & ΔI_{CP2} are charge-pump current mismatch of the low-frequency and high-frequency loops respectively, T_{delay1} & T_{delay2} are feedback-delay time of PFDs of both loops, and T_{in1} & T_{in2} are input periods of both loops.

To improve spurious-tone performance, charge-pump current mismatch should be reduced according to (4.20). Since the spur power is proportional to current-injection time,

feedback delay T_{delay} of the PFD is designed to be 1/20 of the input period T_{in}.

4.9.4.2 Switch Clock Feed Through and Charge Injection

In a conventional sample-and-hold circuit design, the output voltage is disturbed by clock feed through and charge injection. Similar effect takes place in charge pumps because every time when the switches are turned off, clock feed through and charge injection of switches disturb the VCO-control voltage. Figure 4.58 shows the switches SW_{1a} & SW_{2a} which are involved in the disturbance of VCO-control voltage.

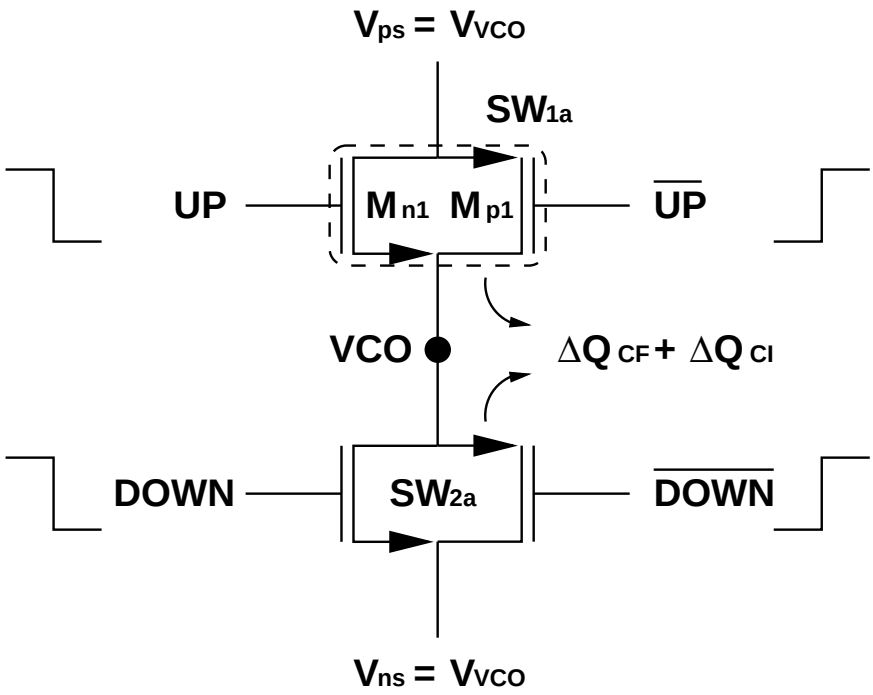


Figure 4.58 Effect of clock feed through and charge injection of switches on the spurious-tone performance.

To eliminate the clock feed-though, complementary switches with same transistor size ($W_n = W_p$) are adopted. However, overlap-capacitance and channel-width mismatches exist between NMOS and PMOS transistors. With the fast-case assumption, the charge disturbance due to clock feed through ΔQ_{CF} can be expressed as follows

$$\begin{aligned} \Delta Q_{CF} &= 2(C_{ovn}W_n - C_{ovp}W_p) \\ \Delta Q_{CF} &\approx C_{ov}W\left(\frac{\Delta C_{ov}}{C_{ov}} + \frac{\Delta W}{W}\right) \end{aligned} \tag{4.22}$$

where C_{ov} is the overlap-capacitance per unit width of transistor, W is the transistor width. To minimize the clock feed through of the switches, minimum transistor size is adopted.

For the charge injection, the source and drain voltages of all transistors are almost equal to the VCO-control voltage V_{VCO}. Then the charge disturbance due to the charge injection of the switches ΔQ_{CI} can be expressed as follows

$$\begin{aligned} \Delta Q_{CI} &= 2 \cdot \left[-\frac{1}{2} \cdot C_{ox} W_n L_n (V_{dd} - V_{VCO} - V_{tn}) + \frac{1}{2} \cdot C_{ox} W_p L_p (V_{VCO} - V_{tp}) \right] \\ \Delta Q_{CI} &= C_{ox} WL (V_{dd} - 2V_{VCO} - V_{tn} + V_{tp}) \end{aligned} \tag{4.23}$$

To minimize the charge injection, minimum transistor size is adopted for the switches. During the design stage, the lower limit of the VCO-control voltage V_{VCO} is used for the worst case estimation.

Assume that the charge disturbance can be decomposed into $\Delta Q = \Delta I \cdot \Delta T$ where ΔI is disturbance current and ΔT is disturbance time. Since the clock feed through and the charge injection take place in a very short instant $\Delta T \to 0$, the spurious tones due to clock feed through and charge injection of the switches S_{CFCI_CP1} & S_{CFCI_CP2} can be estimated as follows

$$\begin{aligned} S_{CFCI\_CP1}\{\omega_{in1}\} &= \frac{1}{2} \cdot \left[\frac{2(\Delta Q_{CF1} + \Delta Q_{CI1})}{T_{in1}} \right]^2 \cdot \left| \frac{\theta_{o1}}{i_{CP1}} (\omega_{in1}) \right|^2 \cdot \left(\frac{1}{N_2} \right)^2 \cdot \left| \frac{\theta_{o2}}{\theta_{in2}} (\omega_{in1}) \right|^2 \\ S_{CFCI\_CP2}\{\omega_{in2}\} &= \frac{1}{2} \cdot \left[\frac{2(\Delta Q_{CF2} + \Delta Q_{CI2})}{T_{in2}} \right]^2 \cdot \left| \frac{\theta_{o2}}{i_{CP2}} (\omega_{in2}) \right|^2 \end{aligned} \tag{4.24}$$

where S_{CFCI_CP1} and S_{CFCI_CP2} are the spurious tones of charge pumps of the low-frequency and high-frequency loops respectively, ΔQ_{CF1} and ΔQ_{CI1} are the charge disturbance due to clock feed through and charge injection in the low-frequency loop, ΔQ_{CF2} and ΔQ_{CI2} are the charge disturbance due to clock feed through and charge injection in the high-frequency loop.

4.9.4.3 Charge Sharing

During the calculation of the switch-charge injection, voltages of nodes *ns* and *ps* are

assumed to be equal to that of node *VCO*. However, it is only valid after the switches SW_{1a} & SW_{2a} are turned on. In most of the period, the switches SW_{1b} and SW_{2b} are turned on, and voltages of nodes *ns* and *ps* are equal to that of node *nb* as shown in Figure 4.59a. Finally, when switches SW_{1a} and SW_{2a} are turned on, charge sharing between capacitors at nodes *ns*, *ps* and *VCO* occurs as shown in Figure 4.59b. The charge sharing causes charge disturbance at node *VCO* and thus degrades spurious-tone performance.

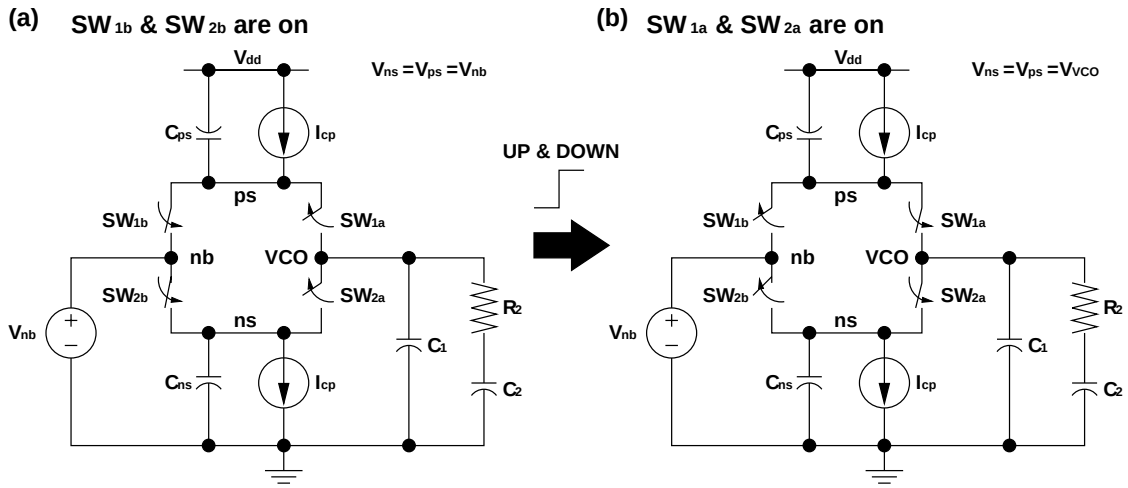


Figure 4.59 Effect of charge sharing: (a) SW_{1b} & SW_{2b} are on and (b) SW_{1a} & SW_{2a} are on.

To estimate the charge disturbance due to the charge sharing, the charge distribution of each capacitor should be considered in each case. When switches SW_{1b} and SW_{2b} are on, the charges in each capacitors are shown as follows

$$Q_{VCOa} = (C_1 + C_2)V_{VCOa} \qquad Q_{nsa} = C_{ns}V_{nb} \qquad Q_{psa} = C_{ps}V_{nb}$$
$$Q_{total} = Q_{VCOa} + Q_{nsa} + Q_{psa} \tag{4.25}$$

where Q_{VCOa}, Q_{nsa} and Q_{psa} are the charges of nodes *VCO*, *ns* and *ps* when switches SW_{1b} & SW_{2b} are on, V_{VCOa} is the voltage at node *VCO* when switches SW_{1b} & SW_{2b} are on, C_{ns} and C_{ps} are the capacitance at nodes *ns* and *ps* respectively. When switches SW_{1a} and SW_{2a} are turned on, the charges of capacitors C_1, C_2, C_{ns} and C_{ps} are shared. The voltage and charge at node *VCO* are shown as follows

$$\begin{aligned} V_{VCOb} &= \frac{(C_1 + C_2)V_{VCOa} + (C_{ns} + C_{ps})V_{nb}}{C_1 + C_2 + C_{ns} + C_{ps}} \\ Q_{VCOb} &= (C_1 + C_2)V_{VCOb} \end{aligned} \tag{4.26}$$

where V_{VCOb} and Q_{VCOb} are the voltage and charge at the *VCO* node respectively after switches SW_{1a} & SW_{2a} are turned on. Based on the charges of the *VCO* node in these two cases, the charge disturbance due to charge sharing ΔQ_{CS} can be expressed as follows

$$\begin{aligned} \Delta Q_{CS} &= (C_1 + C_2)(V_{VCOb} - V_{VCOa}) \\ \Delta Q_{CS} &= \frac{(C_1 + C_2)(C_{ns} + C_{ps})}{C_1 + C_2 + C_{ns} + C_{ps}}(V_{VCOa} - V_{nb}) \\ \Delta Q_{CS} &= \frac{(C_1 + C_2)(C_{ns} + C_{ps})}{C_1 + C_2 + C_{ns} + C_{ps}}V_{VCO\_ERR} \end{aligned} \tag{4.27}$$

where ΔQ_{CS} is the charge disturbance of node *VCO* due to charge sharing, V_{VCO_ERR} is the voltage difference between nodes *VCO* and *nb*. Similar to the analysis of clock feed through and charge injection of the switches, the spurious tones of the charge pumps of the low-frequency and high-frequency loops can be expressed as follows

$$\begin{aligned} S_{CS\_CP1}\{\omega_{in1}\} &= \frac{1}{2}\cdot\left[\frac{2\Delta Q_{CS1}}{T_{in1}}\right]^2\cdot\left|\frac{\theta_{o1}}{i_{CP1}}(\omega_{in1})\right|^2\cdot\left(\frac{1}{N_2}\right)^2\cdot\left|\frac{\theta_{o2}}{\theta_{in2}}(\omega_{in1})\right|^2 \\ S_{CS\_CP2}\{\omega_{in2}\} &= \frac{1}{2}\cdot\left[\frac{2\Delta Q_{CS2}}{T_{in2}}\right]^2\cdot\left|\frac{\theta_{o2}}{i_{CP2}}(\omega_{in2})\right|^2 \end{aligned} \tag{4.28}$$

where S_{CS_CP1} and S_{CS_CP2} are the spurious tones due to charge sharing of the low-frequency and high-frequency loops respectively, ΔQ_{CS1} and ΔQ_{CS2} are the charge disturbance due to charge charging of the low-frequency and high-frequency loops respectively.

To minimize the spurious tones due to charge sharing, capacitance C_{ns} and C_{p2} should be minimized in the layout. The most effective method to solve this charge-sharing problem is to keep the voltages of nodes *VCO* and *nb* to be the same. Therefore, an unity-gain buffer UB is included between nodes *VCO* and *nb* as shown in Figure 4.52.

4.9.4.4 Total Spurious-Tone Performance

In the previous sections, the spurious tones due to the current mismatch, clock feed through, charge injection and charge sharing are discussed and analyzed. Assume that all the spurious tones have the same phase for the worst case estimation, the total spurious tones of the charge pumps of the low-frequency and high-frequency loops can be expressed as follows

$$\begin{aligned} S_{CP1}\{\omega_{in1}\} &= \sqrt{S^2_{CM\_CP1}\{\omega_{in1}\} + S^2_{CFCI\_CP1}\{\omega_{in1}\} + S^2_{CS\_CP1}\{\omega_{in1}\}} \\ S_{CP2}\{\omega_{in2}\} &= \sqrt{S^2_{CM\_CP2}\{\omega_{in2}\} + S^2_{CFCI\_CP2}\{\omega_{in2}\} + S^2_{CS\_CP2}\{\omega_{in2}\}} \end{aligned} \tag{4.29}$$

4.9.4.5 Spurious-Tone Optimization

To improve the spurious-tone performance, the design guidelines are as follows

- use long-channel devices for the current sources to reduce current mismatch
- use minimum-size transistors for the switches to reduce clock feed through and charge injection.
- minimize the capacitance at nodes *ns* and *ps* to suppress charge-sharing effect.
- use an unity-gain buffer to keep voltages between nodes *VCO* and *nb* to be equal.
- reduce loop bandwidth to improve spurious-tone suppression.

The first four criteria are for the charge-pump design which can be achieved easily. However, the loop-bandwidth reduction increases the required loop-filter chip area. The loop-bandwidth design optimization will be discussed in Section 4.9.7.

4.9.5 Phase-Noise Analysis

In this section, phase noise of the dual-loop frequency synthesizer is discussed. For the reference signals and frequency dividers, their phase noise is very low. Therefore, the phase-noise discussion is focused on the charge pumps, loop filters and VCOs. The phase-noise analysis is similar to that of the spurious tones. First noise voltage of the node VCO is calculated, and phase noise can then be obtained by the VCO-voltage-to-output-phase transfer function in (4.17).

4.9.5.1 Charge-Pump and Loop-Filter Phase Noise

Figure 4.60 shows the small signal model for the phase-noise estimation of the charge pumps and loop filters. As the VCO-voltage-to-output-phase transfer function θ_o/v_{VCO} in (4.17) is a band-pass function with center frequency less than 100 kHz, all the parasitic capacitors are ignored for simplicity.

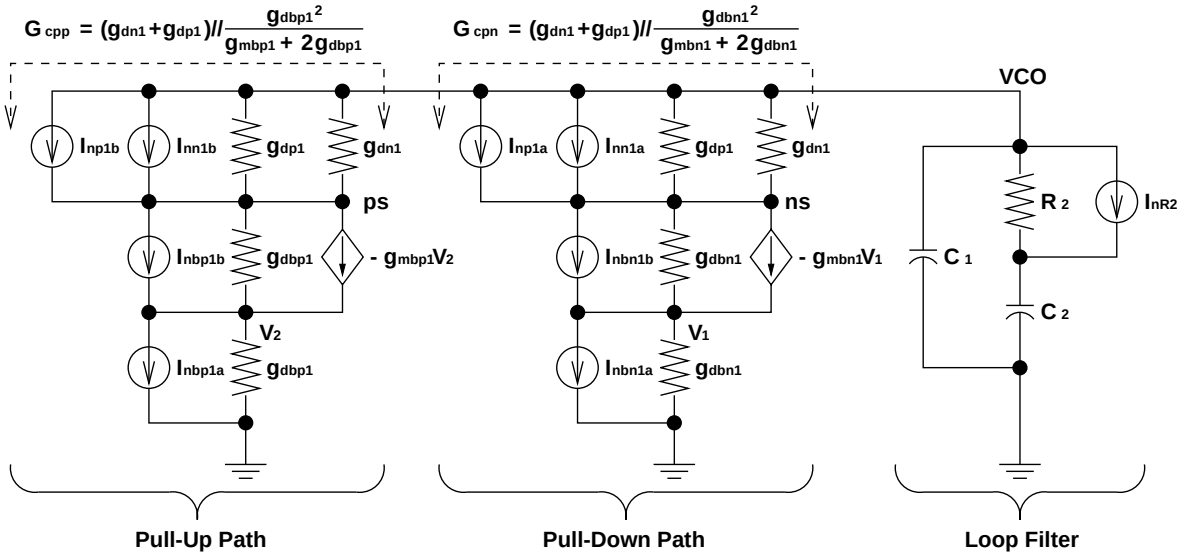


Figure 4.60 Small-signal model for the phase-noise analysis of the charge-pumps and loop filters.

Through standard calculation, the noise-current-to-VCO-voltage transfer function v_{VCO}/i_n of all the noise sources of the pull-down current path are expressed as follows

$$\begin{aligned}
\frac{v_{VCO}}{i_{nn1a}}(s) &= \frac{v_{VCO}}{i_{np1a}}(s) = \frac{g_{dbn1}^2(1+s\tau_z)}{D_n(s)} \\
\frac{v_{VCO}}{i_{nbn1a}}(s) &= \frac{(g_{mbn1}+g_{dbn1})(g_{dn1}+g_{dp1})(1+s\tau_z)}{D_n(s)} \\
\frac{v_{VCO}}{i_{nbn1b}}(s) &= \frac{(g_{dn1}+g_{dp1})g_{dbn1}(1+s\tau_z)}{D_n(s)} \qquad (4.30) \\
D_n(s) &= [G_{cpp}K_{Dn} + (g_{dn1}+g_{dp1})g_{dbn1}^2] \\
&\quad + s[(G_{cpp}\tau_z + \tau_i)K_{Dn} + \tau_z(g_{dn1}+g_{dp1})g_{dbn1}^2] + s^2\tau_i\tau_p K_{Dn} \\
K_{Dn} &= (g_{mbn1}+2g_{gdbn1})(g_{dn1}+g_{dp1}) + g_{dbp1}^2
\end{aligned}$$

where g_m is transconductance, g_d is channel conductance, τ_i, τ_z, τ_p are the integration, zero, and pole time constants of the loop filter. The noise-current-to-VCO-voltage transfer function of all the noise sources of the pull-up current path are expressed as follows

$$\begin{aligned}
\frac{v_{VCO}}{i_{nn1b}}(s) &= \frac{v_{VCO}}{i_{np1b}}(s) = \frac{g_{dbp1}^2(1+s\tau_z)}{D_p(s)} \\
\frac{v_{VCO}}{i_{nbp1a}}(s) &= \frac{(g_{mbp1}+g_{dbp1})(g_{dn1}+g_{dp1})(1+s\tau_z)}{D_p(s)} \\
\frac{v_{VCO}}{i_{nbp1b}}(s) &= \frac{(g_{dn1}+g_{dp1})g_{dbp1}(1+s\tau_z)}{D_p(s)} \\
D_n(s) &= [G_{cpn}K_{Dp} + (g_{dn1}+g_{dp1})g_{dbp1}^2] \\
&\quad + s[(G_{cpn}\tau_z+\tau_i)K_{Dp} + \tau_z(g_{dn1}+g_{dp1})g_{dbp1}^2] + s^2\tau_i\tau_p K_{Dp} \\
K_{Dp} &= (g_{mbp1}+2g_{gdbp1})(g_{dn1}+g_{dp1}) + g_{dbp1}^2
\end{aligned} \tag{4.31}$$

Similarly, the noise-current-to-VCO-voltage transfer function of the loop-filter resistor is expressed as follows

$$\frac{v_{VCO}}{i_{nR2}}(s) = \frac{sC_2}{(G_{cpn}G_{cpp} + s[C_1/R_2 + C_2(G_{cpn}+G_{cpp}+1/R_2)] + s^2C_1C_2)} \tag{4.32}$$

where i_{nR2} is the noise current of resistor R_2. To calculate the phase noise of each PLL, the equivalent noise-power-spectral density of the node *VCO* is expressed as follows

$$\begin{aligned}
\frac{\overline{v_{nVCO}^2}}{\Delta f}(\Delta\omega) &= 4kT\cdot\left(\left|\frac{v_{VCO}}{i_{nn1a}}(\Delta\omega)\right|^2 + \left|\frac{v_{VCO}}{i_{nn1b}}(\Delta\omega)\right|^2\right)\cdot 2\cdot(g_{dn1}+g_{dp1}) \\
&\quad + 4KT\cdot\left(\left|\frac{v_{VCO}}{i_{nbn1a}}(\Delta\omega)\right|^2 + \left|\frac{v_{VCO}}{i_{nbn1b}}(\Delta\omega)\right|^2\right)\cdot\frac{2}{3}\cdot g_{mbn1} \\
&\quad + 4KT\cdot\left(\left|\frac{v_{VCO}}{i_{nbp1a}}(\Delta\omega)\right|^2 + \left|\frac{v_{VCO}}{i_{nbp1b}}(\Delta\omega)\right|^2\right)\cdot\frac{2}{3}\cdot g_{mbp1} \\
&\quad + 4KT\cdot\left|\frac{v_{VCO}}{i_{nR2}}(\Delta\omega)\right|^2\cdot\frac{1}{R_2}
\end{aligned} \tag{4.33}$$

where $\overline{v_{nVCO}^2}/\Delta f$ is the noise power-spectral density of node *VCO* due to charge pump and loop filter, $\Delta\omega$ is the offset frequency in radian per second.

From the previous phase-noise equations, the phase-noise performance of the dual-loop frequency synthesizer due to the charge pumps and loop filters of the low-frequency and high frequency loops are expressed as follows

$$\begin{aligned} \mathcal{L}_{Total\_CP1}\{\Delta\omega\} &= \left|\frac{\theta_{o1}}{v_{VCO1}}(\Delta\omega)\right|^2 \cdot \left(\frac{1}{N_2}\right)^2 \cdot \left|\frac{\theta_{o2}}{\theta_{in2}}(\Delta\omega)\right|^2 \cdot \frac{\overline{v_{nVCO1}^2}}{\Delta f} \\ \mathcal{L}_{Total\_CP2}\{\Delta\omega\} &= \left|\frac{\theta_{o2}}{v_{VCO2}}(\Delta\omega)\right|^2 \cdot \frac{\overline{v_{nVCO2}^2}}{\Delta f} \end{aligned} \tag{4.34}$$

where $\mathcal{L}_{CP1}\{\Delta\omega\}$ and $\mathcal{L}_{CP2}\{\Delta\omega\}$ are phase noise due to charge pumps and loop filters of the low-frequency and high-frequency loops respectively, $\overline{v_{nVCO1}^2}/\Delta f$ and $\overline{v_{nVCO2}^2}/\Delta f$ are the noise power-spectral density at nodes *VCO1* and *VCO2* due to charge-pumps and loop filters of the low-frequency and high-frequency loops respectively.

4.9.5.2 Voltage-Controlled Oscillator Phase Noise

In Section 4.2.6 and Section 4.5.4, the phase noise at 600-kHz frequency offset of the LC and ring oscillators are simulated by *SpectreRF*. In general, the phase noise is inversely proportional to the square of offset frequency, the phase noise of both oscillators are expressed as follows

$$\begin{aligned} \mathcal{L}_{VCO1}\{\Delta\omega\} &= \frac{10^{-112/10}(2\pi\times 600\times 10^3)^2}{\Delta\omega^2} \\ \mathcal{L}_{VCO2}\{\Delta\omega\} &= \frac{10^{-124/10}(2\pi\times 600\times 10^3)^2}{\Delta\omega^2} \end{aligned} \tag{4.35}$$

where $\mathcal{L}_{VCO1}\{\Delta\omega\}$ and $\mathcal{L}_{VCO2}\{\Delta\omega\}$ are the phase noise of the oscillators *VCO1* and *VCO2*, $\Delta\omega$ is the offset frequency.

By equations (4.18) and (4.35), the phase noise of the synthesizer due to the VCOs of both low-frequency an high-frequency loops can be expressed as follows

$$\begin{aligned} \mathcal{L}_{Total\_VCO1}\{\Delta\omega\} &= \left|\frac{\theta_{o1}}{\theta_{nVCO1}}(\Delta\omega)\right|^2 \cdot \left(\frac{1}{N_2}\right)^2 \cdot \left|\frac{\theta_{o2}}{\theta_{in2}}(\Delta\omega)\right|^2 \cdot \mathcal{L}_{VCO1}\{\Delta\omega\} \\ \mathcal{L}_{Total\_VCO2}\{\Delta\omega\} &= \left|\frac{\theta_{o2}}{\theta_{nVCO2}}(\Delta\omega)\right|^2 \cdot \mathcal{L}_{VCO2}\{\Delta\omega\} \end{aligned} \tag{4.36}$$

4.9.5.3 Frequency-Synthesizer Phase Noise

After the discussion and derivation of the phase noise due to VCOs, charge pumps and loop filters, the total phase noise of the dual-loop frequency synthesizer is expressed as follows

$$\begin{aligned} \mathcal{L}_{Total}\{\Delta\omega\} &= \mathcal{L}_{Total\_CP1}\{\Delta\omega\} + \mathcal{L}_{Total\_CP2}\{\Delta\omega\} \\ &\quad + \mathcal{L}_{Total\_VCO1}\{\Delta\omega\} + \mathcal{L}_{Total\_VCO2}\{\Delta\omega\} \end{aligned} \tag{4.37}$$

$\mathcal{L}_{Total}\{\Delta\omega\}$ is the total phase noise of the synthesizer. This phase-noise expression will be used in the design optimization of the charge pumps and loop filters.

4.9.5.4 Phase-noise optimization

To optimize the phase-noise performance, the design guidelines are as the follows

- increase the V_{gs} - V_t of transistors M_{bn1} and M_{bp1} in Figure 4.52 to reduce noise power with the same current bias.
- reduce resistance R_2 and increase both capacitance C_1 and C_2 to reduce noise of the loop filters.
- reduce loop bandwidth to further suppress phase noise due to charge pumps and loop filters.

By reducing V_{gs} - V_t, the transconductance of transistors M_{bn1} and M_{bp1} are reduced and thus noise power can be reduced. Noise power can also be suppressed by reducing the resistance R_2. However, to maintain the same loop dynamics (bandwidth and phase margin), larger capacitors of C_1 and C_2 and thus larger chip area are needed. Similar to the spurious-tone suppression, smaller loop bandwidth improve the suppression of phase-noise contributed by charge pumps

and loop filters. From equation (4.36), it seems that phase noise due to the VCO can be reduced by increasing the loop bandwidth. However, this design criterion contradicts to the spurious-tone suppression which cannot be achieved by only optimizing the charge pump. Therefore, small loop bandwidth is designed for both low-frequency and high-frequency loops and there is no VCO-phase-noise suppression.

4.9.6 Loop Stability Consideration

To make the PLL lock to the desired output frequency, the loop must have enough phase margin for the loop stability consideration. By using the second-order loop filter in Figure 4.53, the open-loop transfer gain $A_{open}(s)$ can be express as follows

$$A_{open}(s) = \frac{I_{CP}}{2\pi} \cdot \frac{(1 + s\tau_z)}{s\tau_i(1 + s\tau_p)} \cdot \frac{K_{VCO}}{s} \cdot \frac{1}{N} \tag{4.38}$$

where I_{CP} is the charge-pump current, τ_i, τ_z and τ_p are the time constants of the integration, zero and pole of the loop filter, K_{VCO} is the VCO gain, N is the frequency-division ratio.

The magnitude and phase plots of the open-loop transfer gain $A_{open}(s)$ are plotted in Figure 4.61. There are two integrators and therefore the phase shift of the loop starts at -180°. For loop stability consideration, a zero at $1/\tau_z$ is included at the loop filter to raise the phase margin at the unity-gain frequency ω_u of the loop (loop bandwidth). To further improve the

spurious-tone suppression, a pole at $1/\tau_p$ is included in the loop filter.

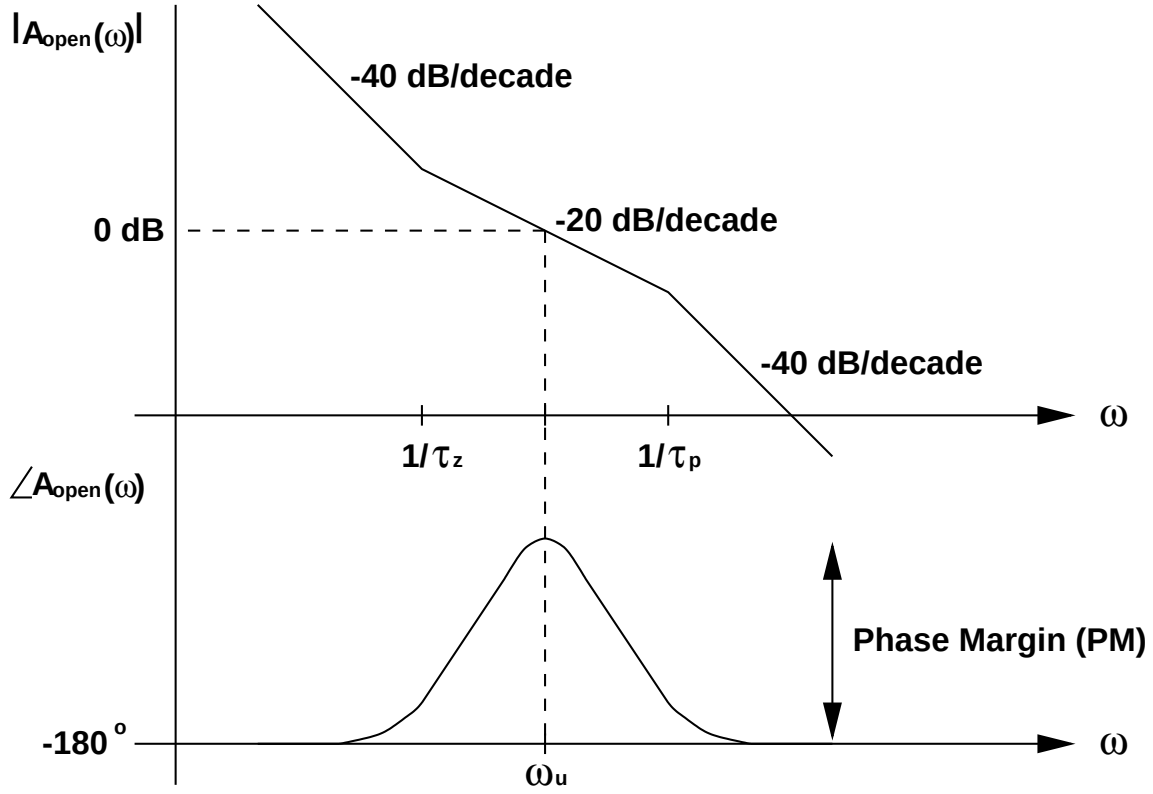


Figure 4.61 Bode plot of the open-loop transfer function.

Before the absolute value of loop bandwidth is designed, the optimal location of loop bandwidth in terms of the zero and pole is determined first. From (4.38), the phase shift of the loop is expressed as follows

$$\angle A_{open}(\omega) = -\pi + \tan^{-1}\left[\frac{\omega(\tau_z - \tau_p)}{1 + \omega^2 \tau_p \tau_z}\right] \tag{4.39}$$

The optimal design of the loop bandwidth is determined when the phase margin is the maximum. The solution can be obtained by differentiating the phase response of the open-loop transfer function. Then the optimal unity-gain frequency is expressed in terms of zero and pole as follows

$$\omega_u = 1/\sqrt{\tau_z \tau_p} \tag{4.40}$$

At the optimal unity-gain frequency, the phase margin can be expressed as follows

$$PM = \tan\left[\frac{\tau_z - \tau_p}{2\sqrt{\tau_z \tau_p}}\right] \tag{4.41}$$

By (4.40) and (4.41), the zero and pole time constants of the loop filter can be expressed in terms of loop bandwidth and phase margin as follows

$$\begin{aligned} \tau_z &= \frac{\tan(PM) + \sec(PM)}{\omega_u} \\ \tau_p &= \frac{1}{\omega_u(\tan(PM) + \sec(PM))} \end{aligned} \tag{4.42}$$

Then, by equating magnitude response of the open-loop transfer function to unity, the integration time constant τ_i can be expressed as follows

$$\tau_i = C_1 + C_2 = \left(\frac{I_{CP}K_{VCO}}{2\pi N\omega_u^2}\right)\cdot(\tan(PM) + \sec(PM)) \tag{4.43}$$

Finally, by the time-constant expression in (4.41), (4.42) and (4.43), the required values of resistance R_2, capacitance C_1 and C_2 can be determined as follows

$$\begin{aligned} C_1 &= \frac{\tau_p}{\tau_z}\cdot\left(\frac{I_{CP}K_{VCO}}{2\pi N\omega_u^2}\right)\cdot(\tan(PM) + \sec(PM)) \\ C_2 &= \left(1 - \frac{\tau_p}{\tau_z}\right)\cdot\left(\frac{I_{CP}K_{VCO}}{2\pi N\omega_u^2}\right)\cdot(\tan(PM) + \sec(PM)) \\ R_s &= \tau_z / C_2 \end{aligned} \tag{4.44}$$

Although the resistance and capacitance values depend on a lot of parameters, VCO gain K_{VCO} and frequency-division ratio N are already fixed. Therefore, the loop filter design is completely determined by the charge-pump current I_{cp}, loop bandwidth ω_u and phase margin PM.

4.9.7 Charge-Pump and Loop-Filter Design Optimization

After the detailed discussion of spurious tones, phase noise and loop stability of the PLLs, this section discusses the design optimization of both the low-frequency and high frequency loop.

4.9.7.1 Design Consideration

As stated in Section 4.9.1, the design requirement is to meet the phase-noise (< -121 dBc/Hz@600kHz) and spurious-tone specification (< -88 dBc) with minimum chip area.

From (4.43), it is found that the total capacitance is proportional to the charge-pump current I_{cp} and phase margin *PM*, but inversely proportional to square of loop bandwidth ω_u. Therefore, the optimal design requires small charge-pump current, small phase margin, and large loop bandwidth.

Although small charge-pump current is desired, the current should be large enough to be measurable by ammeter. On the other hand, the phase margin is typically limited between 45° and 60° to maintain loop stability against any process variation. As spurious tones cannot be completely eliminated by only optimizing the charge-pump design, the maximum loop bandwidth is limited by the spurious-tone performance.

4.9.7.2 High-Frequency Loop Design

From Figure 4.62, the VCO gain of the LC oscillator VCO2 varies from 75 to 275 MHz/V. However, such VCO gain variation only degrades the phase margin by less than 5° as shown in Figure 4.62. Instead, it modifies the loop bandwidth between 15 and 40 kHz which is still large enough for the GSM switching-time specification. Therefore, the phase margin of the high-frequency loop is designed to be 45°.

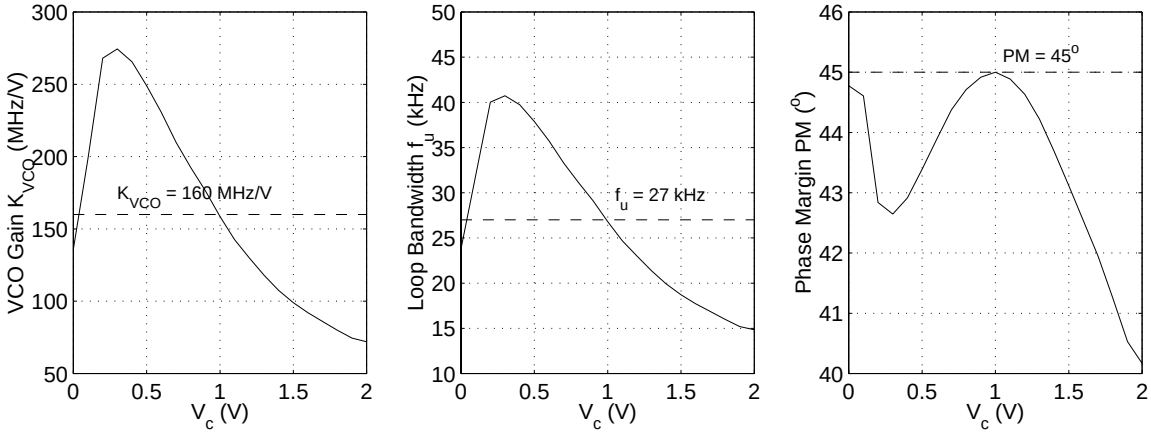


Figure 4.62 The variation of the loop bandwidth f_u and phase margin *PM* of the high-frequency loop due to the VCO-gain variation of the LC-oscillator

To design the charge-pump current I_{cp} and loop bandwidth ω_u, the spurious tones, the phase noise at 600-kHz frequency offset and loop-filter area in unit of μm^2 in log scale are plotted in Figure 4.63. For spurious-tone estimation, it is assumed that transistors suffer 1-%

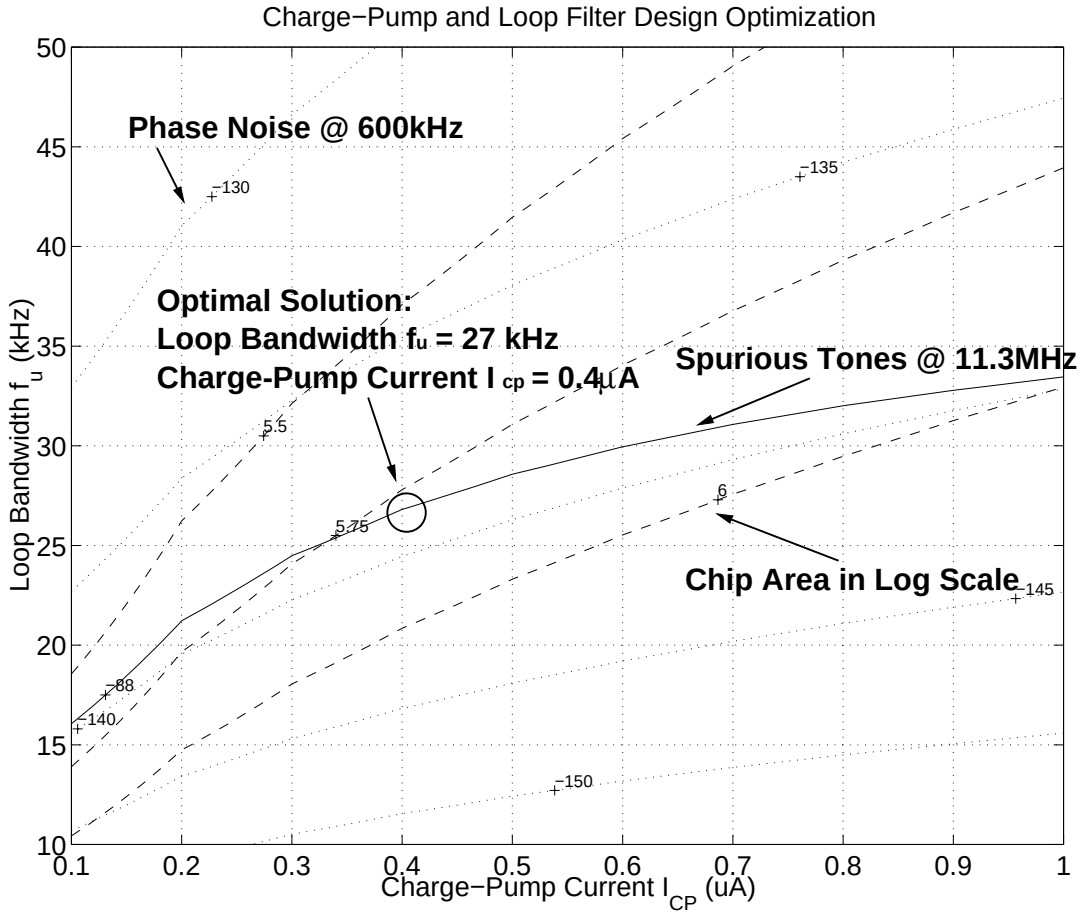


Figure 4.63 Design optimization of the charge pump and loop filter of the high-frequency loop.

parameter mismatch and offset voltage of unity gain buffer is 10 mV. The phase noise which is less than -130 dBc/Hz@600kHz does not limit the loop filter design. Therefore, the design is determined by the spurious tones and loop-filter area. The optimal design should meet the spurious-tone requirement (-88 dBc) with minimum chip area (< 1 mm^2) and measurable charge-pump current level (0.4 μA). Moreover, the loop bandwidth should be larger than 3 kHz even with VCO-gain variation. The optimal design is determined accordingly and the design parameters of the charge pump CP2 and loop filter LF2 of the high-frequency loop are summarized in Table 4.10.

Charge Pump of the High-Frequency Loop					
$(W/L)_{n1}$	0.9/0.6	$(W/L)_{p1}$	0.9/0.6	I_{cp}	0.4 μA
$(W/L)_{bn1}$	2.7/3.0	$(W/L)_{bn2}$	43.2/3.0	$(W/L)_{bn3}$	5.4/3.0
$(W/L)_{bp1}$	3.9/3.0	$(W/L)_{bp2}$	62.4/3.0	$(W/L)_{bp3}$	7.8/3.0
Loop Filter of the High-Frequency Loop					
C_1	230.3 pF	C_2	1.1 nF	R_2	12.8 kΩ

Table 4.10 Design parameters of the high-frequency loop.

4.9.7.3 Low-Frequency Loop Design

Figure 4.65 shows the variation of the loop dynamics due to the VCO-gain variation of the ring oscillator VCO1. Since the K_{VCO} of the ring oscillator changes from -600 to 0

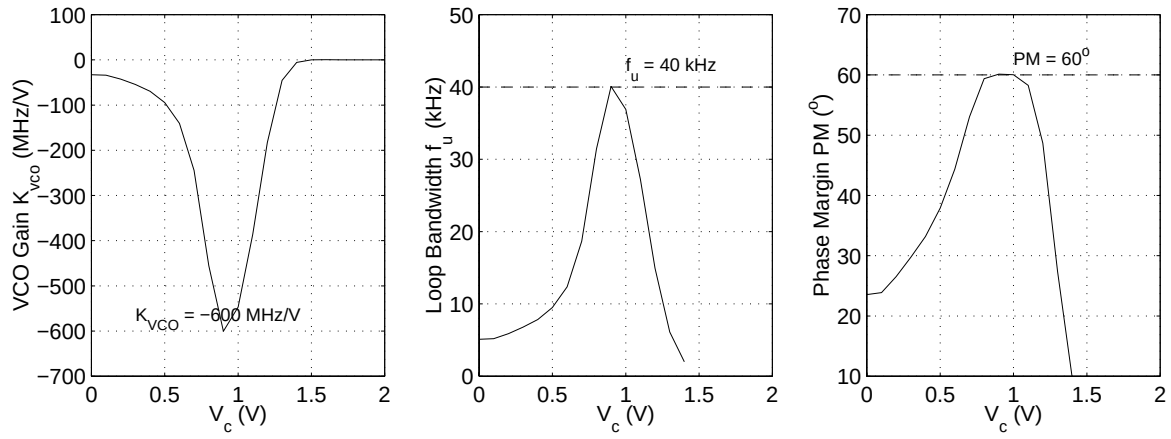


Figure 4.64 The variation of the loop bandwidth f_u and phase margin *PM* of the low-frequency loop due the VCO-gain variation of the ring oscillator VCO1.

MHz/V, the phase-margin variation is significant. Therefore, a higher phase margin 60° is designed for the low-frequency loop.

Similar to the design of the high-frequency loop, the spurious tones, phase noise and the loop-filter area in log scale are plotted against charge-pump current I_{CP} and loop bandwidth f_u in Figure 4.65. Because of the N_3/N_2 division ratio and the low-pass characteristic of the high-frequency loop, the phase noise and spurious tones of the low-frequency loop is greatly suppressed. Therefore, the charge pump and loop filter are designed so that its loop-filter area is around one tenth of that of the high-frequency loop. The design parameters of the charge-pump and loop filter are summarized in Table 4.11.

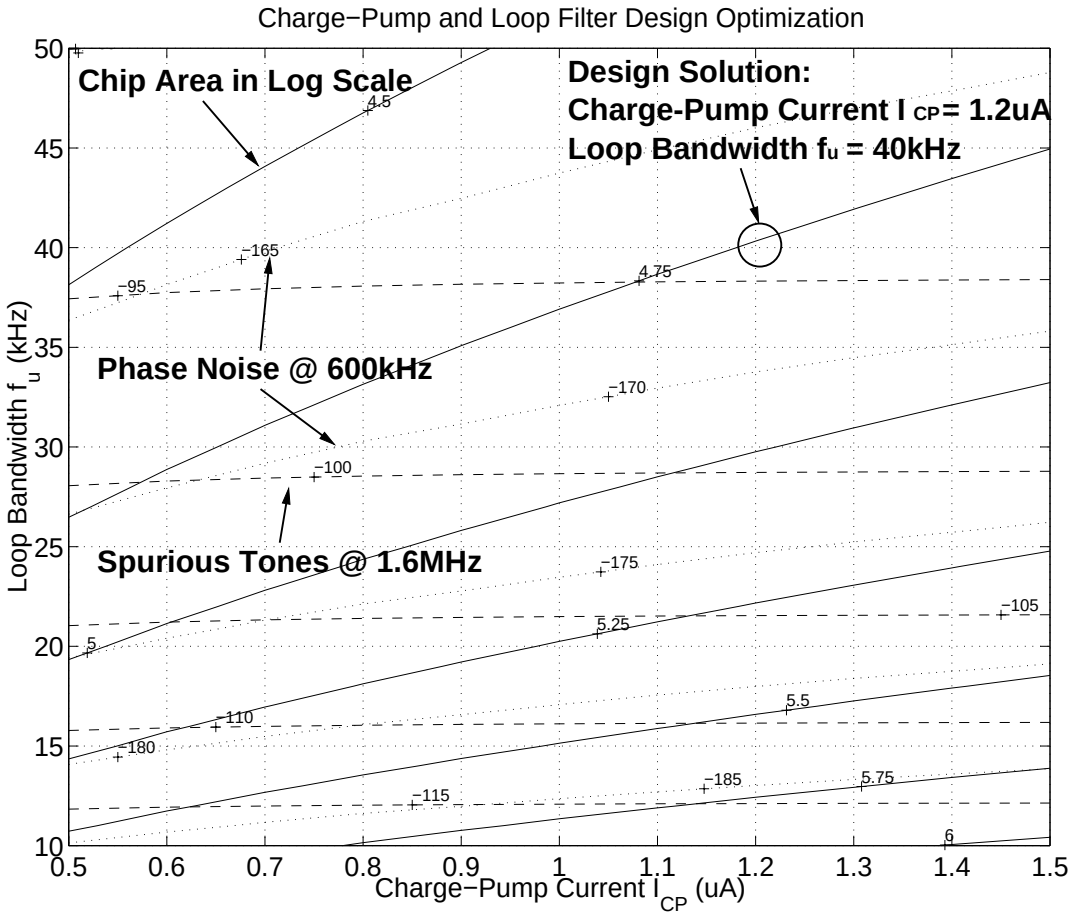


Figure 4.65 Design optimization of the charge pump and loop filter of the low-frequency loop.

Charge Pump of the Low-Frequency Loop					
$(W/L)_{n1}$	0.9/0.6	$(W/L)_{p1}$	0.9/0.6	I_{cp}	1.2 μA
$(W/L)_{bn1}$	7.5/3.0	$(W/L)_{bn2}$	120/3.0	$(W/L)_{bn3}$	15/3.0
$(W/L)_{bp1}$	11.4/3.0	$(W/L)_{bp2}$	182.4/3.0	$(W/L)_{bp3}$	22.8/3.0
Loop Filter of the Low-Frequency Loop					
C_1	8.7 pF	C_2	113.1 pF	R_2	131.3 kΩ

Table 4.11 Design parameters of the charge pump and loop filter of the low -frequency loop.

4.9.8 Performance Summary of the Dual-Loop Frequency Synthesizer

With the phase-noise estimation of all the building blocks, the phase noise of the whole dual-loop frequency synthesizer is plotted against offset frequency in Figure 4.66. It is found that the close-in phase noise is dominated by transistors M_{bn1a} and M_{bp1a} of the charge pump

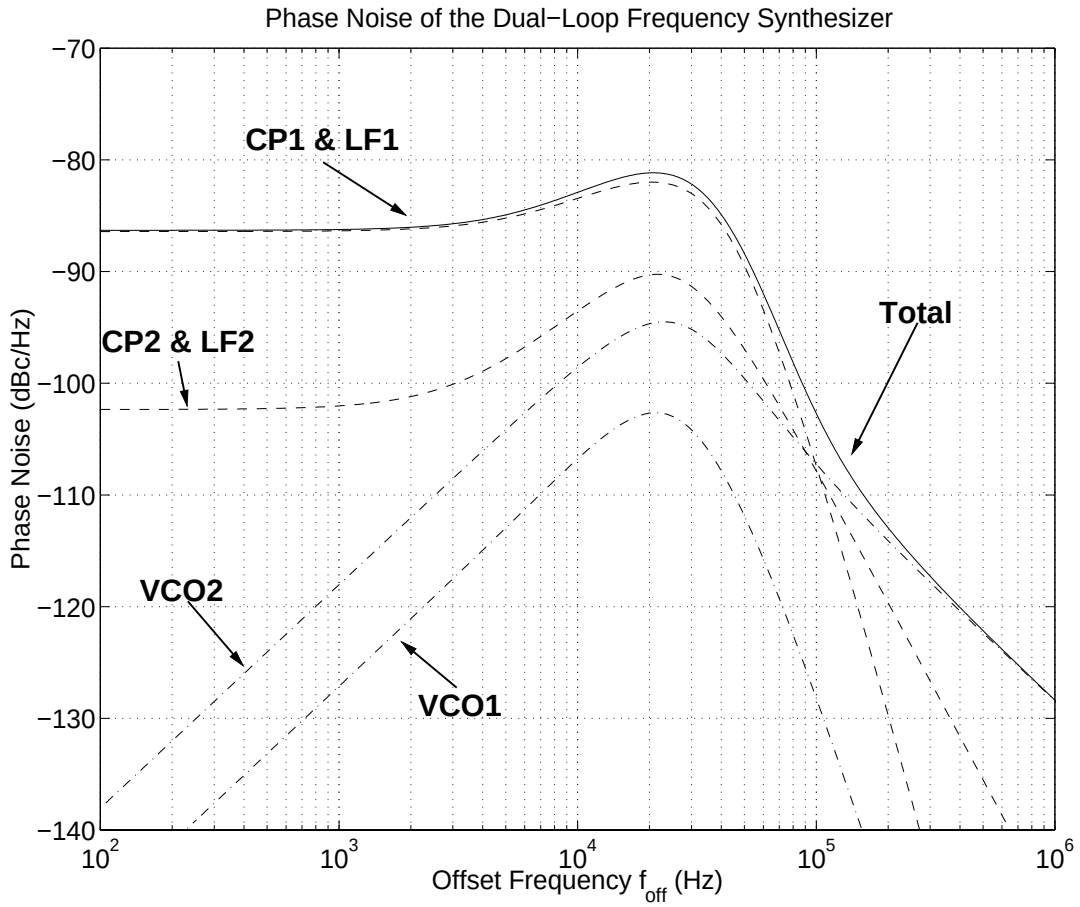


Figure 4.66 Phase noise of the whole dual-loop frequency synthesizer.

CP1 while the high-offset phase noise is dominated by VCO2. The total phase noise of the synthesizer is -123.8 dBc/Hz @ 600kHz.

After the discussion of design issues of all the building blocks, the performance such as, phase noise, chip area and power consumption, are summarized in Table 4.12. The total power consumption is 31.8 mW and the chip area is less than 2×2 cm^2.

Building Blocks	Implementation	Specification	Performance
VCO1	Ring Oscillator	-103 dBc/Hz @ 600kHz	Phase Noise = -112 dBc/Hz Power = 10.2 mW
VCO2	LC Oscillator	-121 dBc/Hz @ 600kHz	Phase Noise = -124 dBc/Hz Power = 13.8 mW
Divider N_1	True-Single-Phase-Clock (TSPC) Logic	N_1 = 226 ~ 349	Power = 2.2 mW
Divider N_2		N_2 = 32	Power = 0.6 mW
Divider N_3		N_3 = 4	Power = 5 mW
CP1 & LF1	Linear Capacitor & Silicide-Blocked Polysilicon	Area < 1 mm^2	Area = 0.06 mm^2
CP2 & LF2		Area < 1 mm^2	Area = 0.6 mm^2
Synthesizer		Phase Noise < -121 dBc/Hz	Phase Noise = -123.8 dBc/Hz
		Spurious Tones < -88 dBc	Spurious Tones = -88 dBc
		Power < 50 mW	Power = 31.8 mW

Table 4.12 Performance summary of the dual-loop frequency synthesizer.

Chapter 5

Layout

5.1 Introduction

In this chapter, the layout techniques which are critical for mixed-signal design are discussed. Since noise coupling between digital parts and analog parts are critical factor which limits the performance of the synthesizer, some special attentions are necessary to be made in the layout process to minimize these effects.

5.2 Loop-Filter Capacitor Layout

The loop filter shown in Figure 4.53 consists of two capacitors C_1 & C_2, and a resistor R_2. The capacitors are implemented by linear capacitors which provides a high capacitance-to-area ratio. In order to maintain the capacitance ratio between C_1 and C_2 against the process variation, two capacitors are inter-digitized and are arranged so that two capacitors have similar centroid as shown in Figure 5.1.

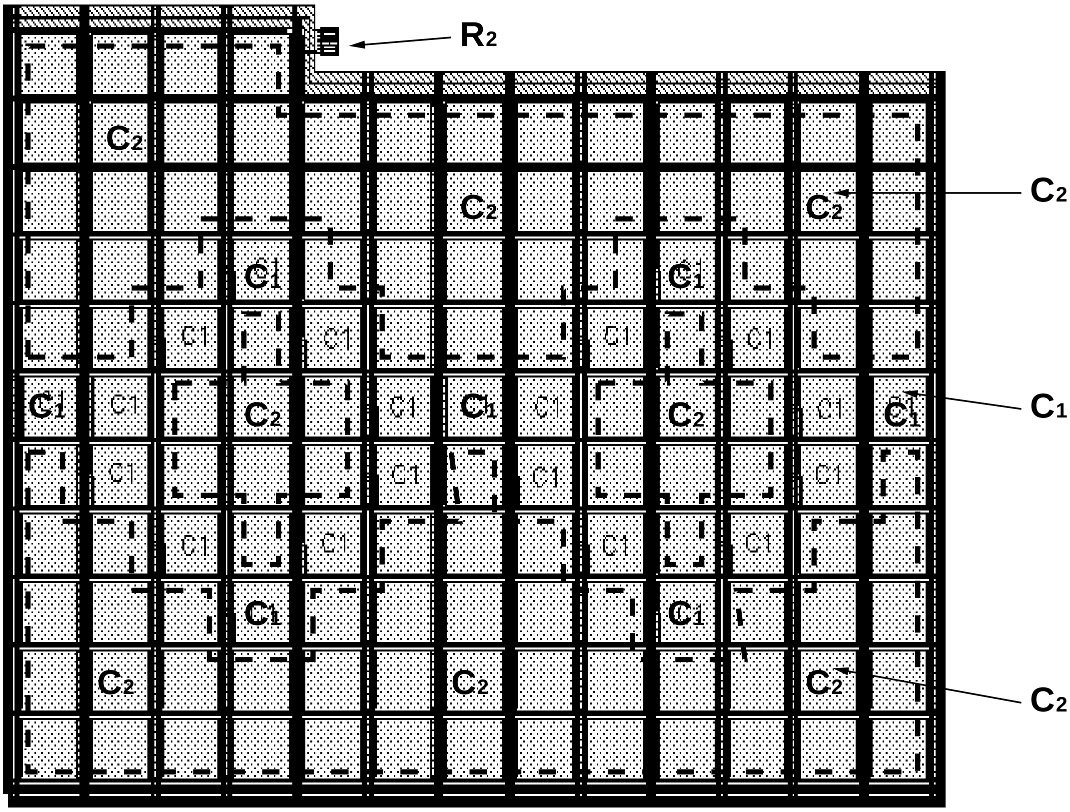


Figure 5.1 Layout of the loop-filter capacitors.

5.3 VCO-Inductor Layout

As mentioned in Section 4.2.4.4, patterned N-well is placed under the spiral inductor to suppress the effect of eddy current. The N-well fingers are drawn perpendicular to the flow direction of eddy current and are biased at supply voltage to block eddy current effectively. The layout of the on-chip spiral inductor is shown in Figure 5.2.

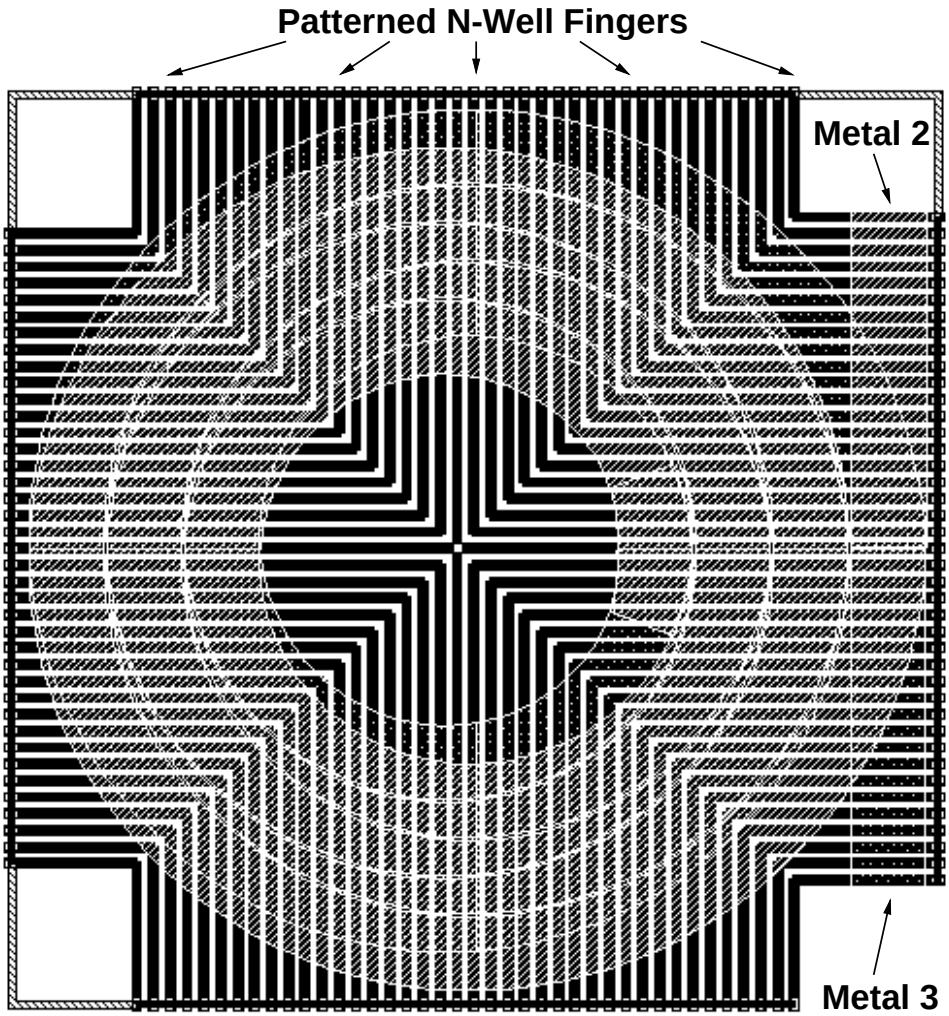


Figure 5.2 Layout of the VCO on-chip spiral inductor.

5.4 Supply-Line and Pad Layout

As the dual-loop frequency synthesizer consists of both the analog components and digital components, care must be taken to eliminate the noise coupling between two portions. To minimize the noise interaction of analog and digital power supplies, a decoupling filter is placed in between. As shown in Figure 5.3, the bonding wires and the by-pass capacitors act as the decoupling filter between the analog and digital portions [26].

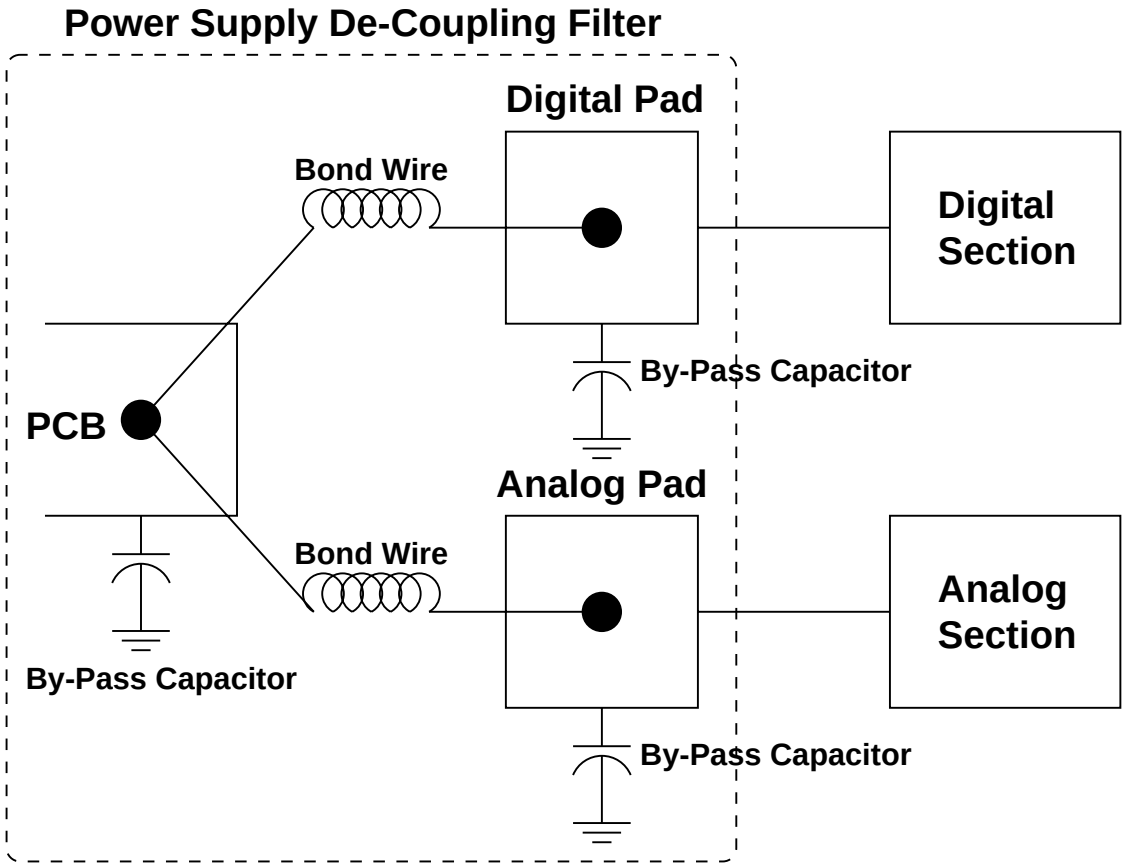


Figure 5.3 Noise de-coupling filter of the analog and digital supplies.

To further enhance the noise decoupling, the current of the analog and digital supply should be self-circulating. Therefore, on-chip by-pass linear capacitors are put under supply pads. Moreover, supply lines are constructed by n+diffusion within N-well which also acts as a by-pass capacitor.

5.5 Layout of the Dual-Loop Frequency Synthesizer

Figure 5.4 shows the floor plan of the whole dual-loop frequency synthesizer. To enhance the measurement feasibility, bonding pads are put on the left and right hand sides of the chip, and the probing pads are put on the top and bottom of the chip. Beside the testing of the whole frequency synthesizer, individual building blocks will also be tested. Supplies of different building blocks are separated so that the loop can be broken for individual component

testing. However, extra frequency dividers N_1, N_2 and N_3 are still included for their own testing because extra test pads, which increase the capacitive loadings of the oscillators VCO1 & VCO2, are needed.

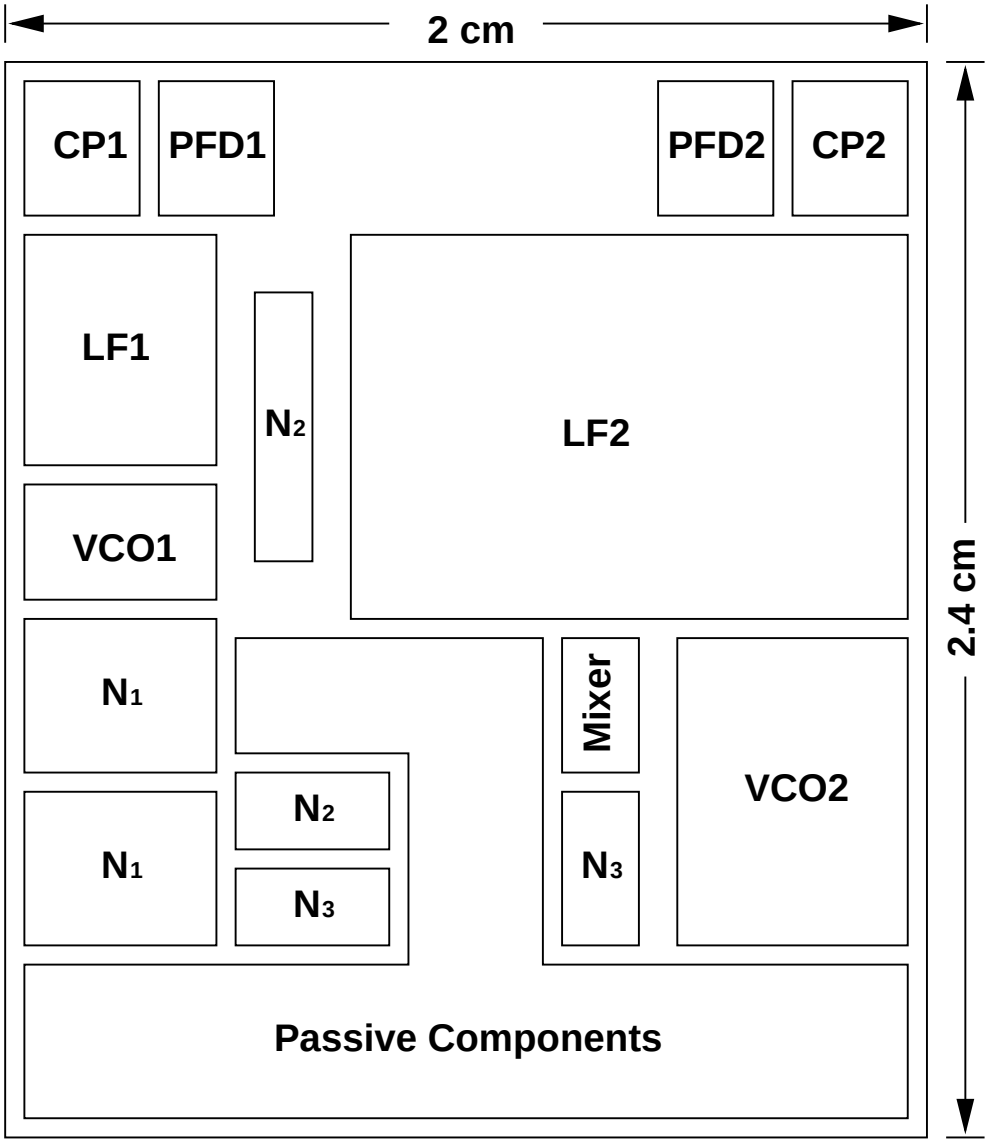


Figure 5.4 Floor plan of the dual-loop frequency synthesizer.

In the remaining space, passive components such as spiral inductor, pn-junction varactors are included for passive-element characterization. The total chip area is 2×2.4 mm^2 and the area of the dual-loop frequency synthesizer is less than 2.64 mm^2. The layout of the dual-loop frequency synthesizer is shown in Figure 5.5.

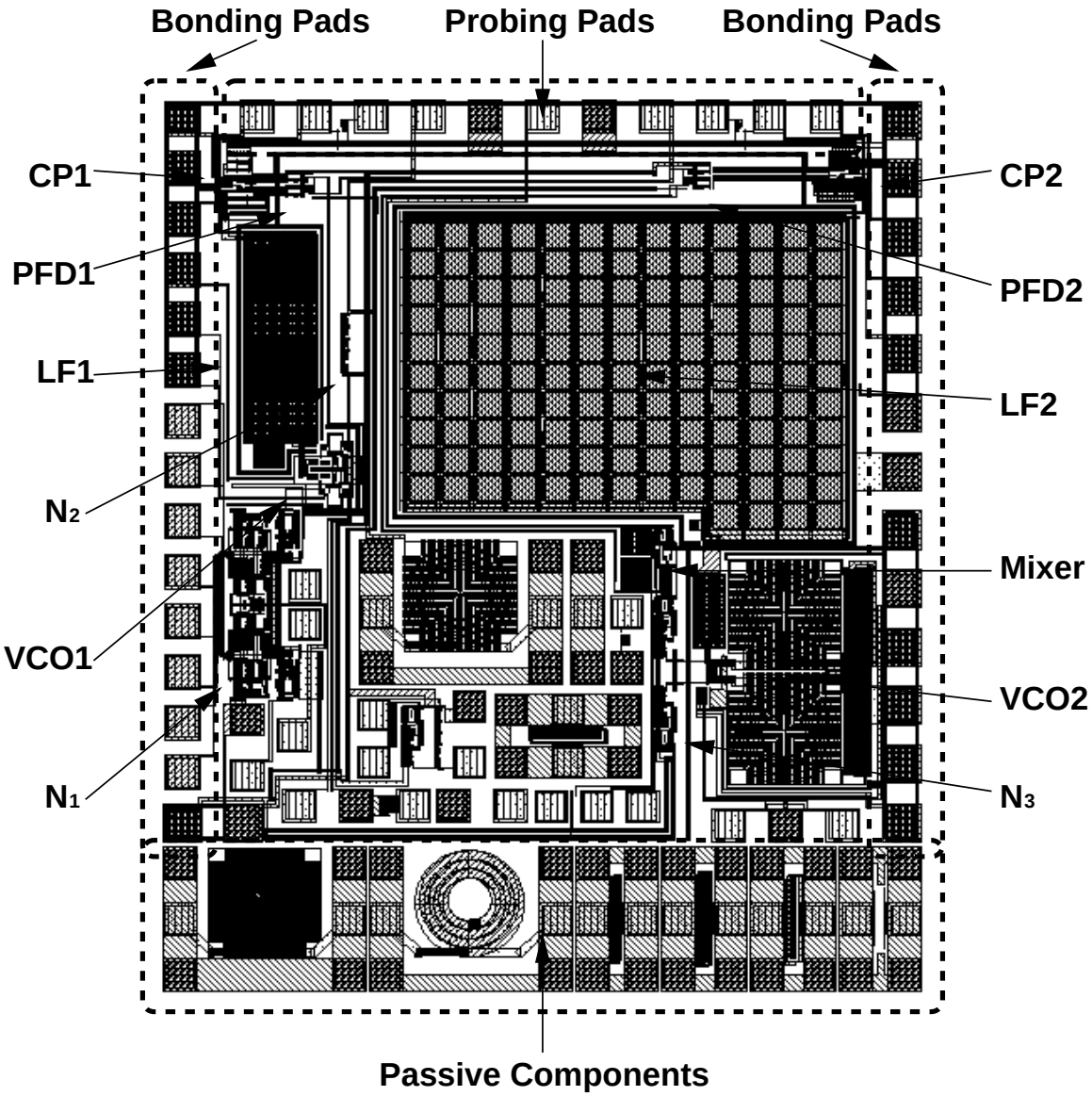


Figure 5.5 Layout of the dual-loop frequency synthesizer.

Chapter 6

Measurement

6.1 Introduction

The dual-loop frequency synthesizer is fabricated by the HP 0.5-μm single-poly-triple-metal N-well CMOS technology. From the parametric test results provided by HP, it is found that the device characteristics are closely matched with the simulation parameters used in the design stage. Before the measurement of the whole synthesizer, individual building blocks are measured and discussed.

6.2 LC Oscillator VCO2

6.2.1 Spiral Inductor & PN-Junction Varactor

The LC oscillator VCO2 consists of the LC tank and the negative transconductor. As both the center frequency and phase noise are mainly determined by the quality factor of the LC tank, the accuracy of the inductor and varactor are very important. The passive-component measurement also verifies the accuracy of inductor and varactor modelling.

6.2.1.1 Test Setup

The setup shown in Figure 6.1 is adopted to characterize the passive components. The

setup consists of a HP 8510C network analyzer, a pair of Picoprobe coplaner ground-signal-ground GSG probes and a power supply box. First, the network analyzer measures the S-parameters of both the passive device and open-pad structure. The measured S-parameters are then converted to Y-parameters in order to de-embed the parasitics of the probing pads as follows

$$Y_{Ind} = Y_{Meas} - Y_{Pad} \tag{6.1}$$

where Y_{Meas}, Y_{Pad} and Y_{Ind} are the Y-parameters of the measured inductor structure, open-pad structure and the de-embedded inductor respectively. Finally, the de-embedded Y-parameters are used to fit the models of inductor and capacitors shown in Figure 4.8 and Figure 4.9 respectively.

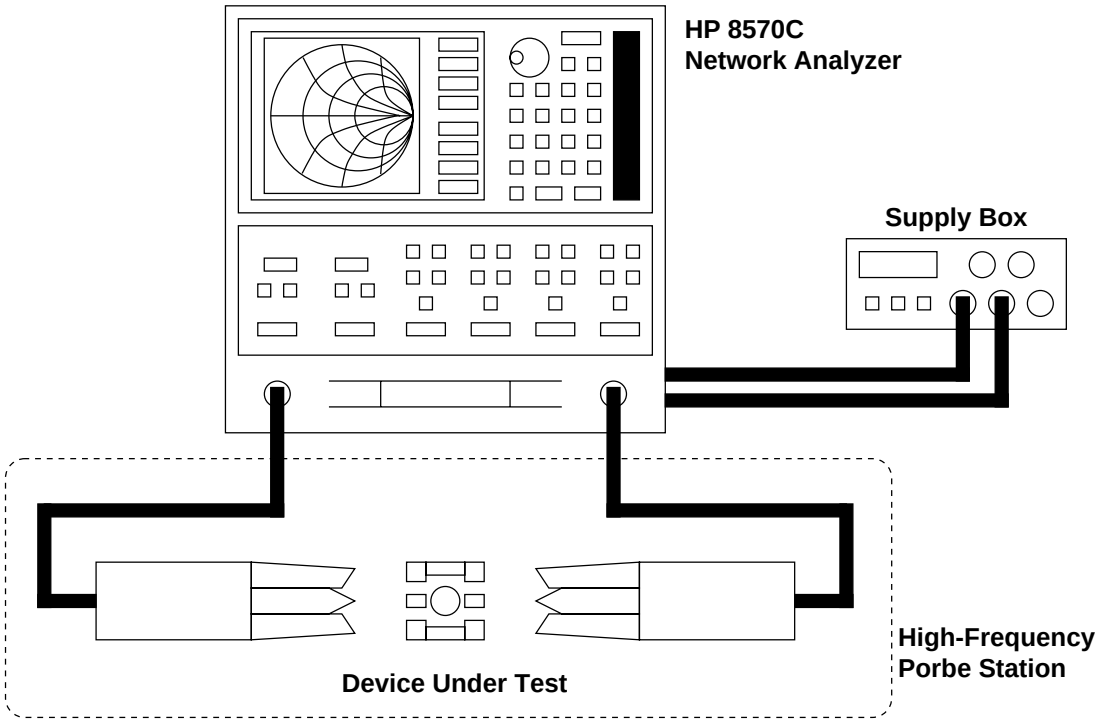


Figure 6.1 Measurement setup for the passive components.

6.2.1.2 Measurement Results of Spiral Inductor

Figure 6.2 shows the measurement results of the on-chip spiral inductor with laminated

N-well under the inductor. Comparing to the ASITIC simulation results, measured inductance is very close to the simulation results below 2 GHz, and it drops when frequency becomes close to the self-resonant frequency. Moreover, substrate capacitance C_{s1} and C_{s2} are also close to the expected values. However, series resistance R_L (30.2 Ω) is almost 3 three times larger than the expected value (11.6 Ω). The increase in series resistance is mainly due to the eddy current which cannot be simulated by ASITIC. Since series resistance increases a lot, quality factor looking into port 1 is limited to be around 1.6 at 900 MHz.

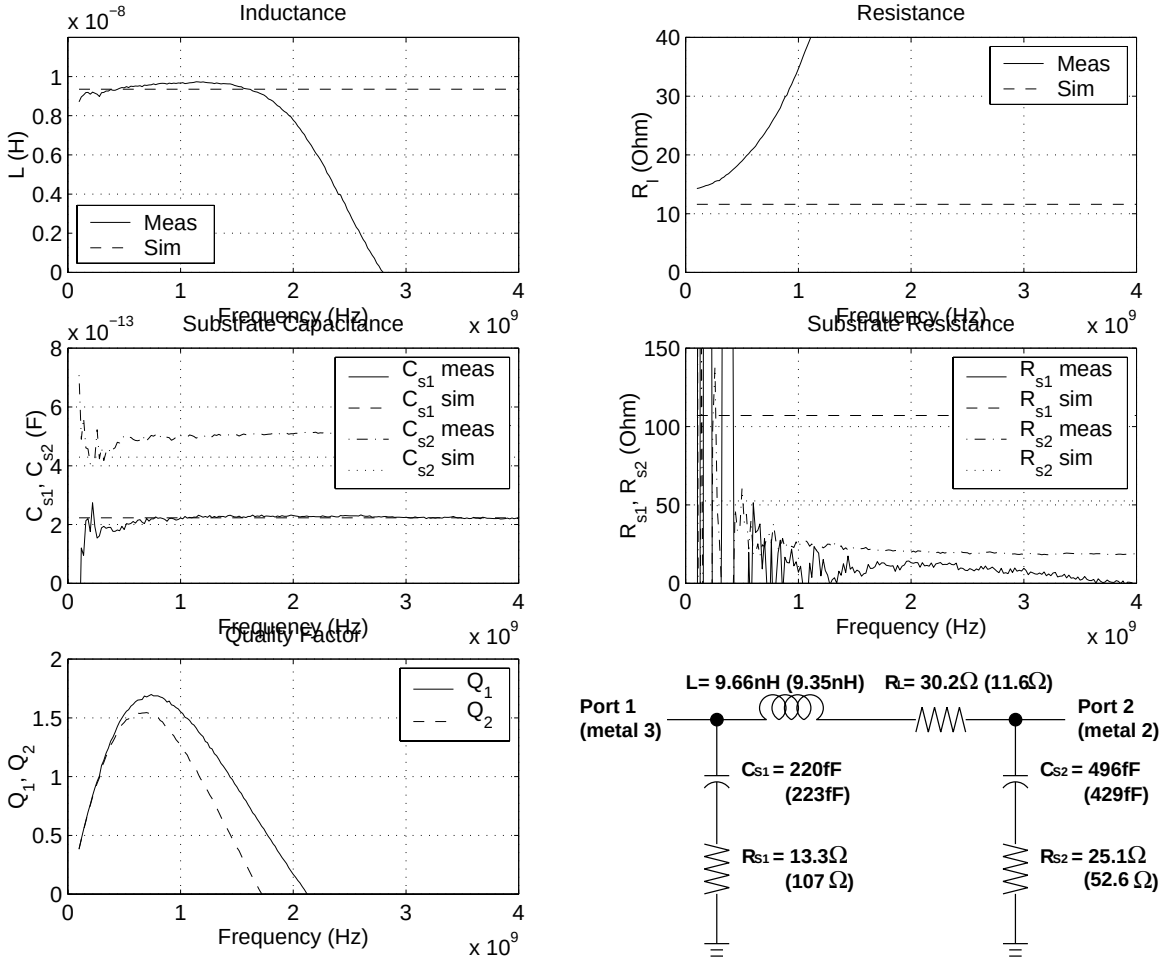


Figure 6.2 Measurement results and model of the on-chip spiral inductor which is used in the LC oscillator.

For comparison purpose, different inductor test structures which have the same spiral inductors but different substrate conditions are included on the same chip. Figure 6.3 shows the measurement results of the inductor test structures with laminated N-well, laminated

polysilicon and only P-substrate under the inductors. Since only port 1 parameters are important to the oscillator performance, port 2 parameters C_{S2}, R_{S2} and Q_2 are not shown for simplicity. Inductance L of the three inductors are close to each other. As N-well fingers form junction capacitance with P-substrate, the substrate capacitance C_{S1} is reduced in the case with laminated N-well. On the other hand, polysilicon fingers form additional capacitance, the substrate capacitance is largest in this case. The series resistance R_L of the cases with laminated polysilicon and only P-substrate are is only twice larger than that of the simulation results. Comparing the series resistance between the structures with laminated polysilicon and with only P-substrate, eddy current is induced only in substrate but not in polysilicon fingers. Since the sheet resistance of polysilicon (2.2 Ω/❑) is smaller than that of N-well (714 Ω/❑), the measurement results imply that the N-well fingers are not narrow enough such that eddy current

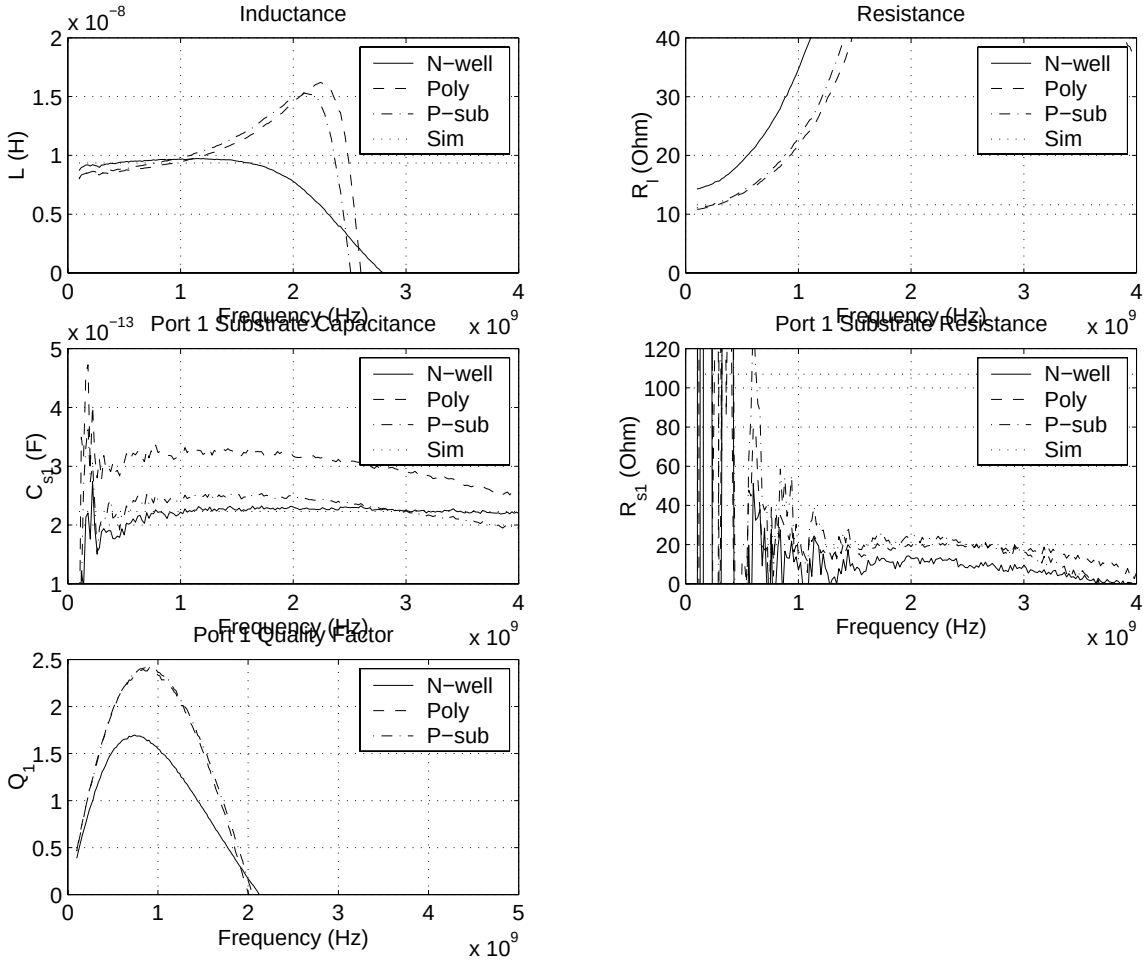


Figure 6.3 Measurement results of the inductor test structures with laminated N-well, laminated polysilicon and only P-substrate under the inductors.

is induced with the fingers. Since the width of N-well fingers (3.6 μm) and polysilicon fingers (1.5 μm) are designed according to design rules, it may be the cause of the additional eddy current induced in substrate. shows the models of different inductors, the additional eddy current degrades the quality factor by over 30%.

	N-well	Polysilicon	P-substrate
L (nH)	9.66	9.23	9.58
R_L (Ω)	30.2	19.2	20.3
C_{S1} (fF)	220	319	242
R_{S1} (Ω)	13.3	260	34.5
Q_1	1.64	2.40	2.42

Table 6.1 Measurement results of the inductors with laminated N-well, laminated polysilicon and only P-substrate at 900 MHz.

6.2.1.3 Measurement Results of PN-Junction Varactor

As the pn-junction varactor is connected to the LC oscillator VCO2, the pn-junction varactor is biased to be same as that of the LC oscillator. Therefore, p+junction of the varactor is biased at 1.16 V, which is the dc bias voltage of the oscillator core, and n+junction is swept from 0 V to 2 V. Figure 6.4 shows the measurement results of the pn-junction varactor at 900 MHz. As only the p+junction, which is connected to the oscillator core, is interested, only port 1 parameters are shown. The measured capacitance is close the simulation results in reverse bias region (V_{in} > 1.16 V). Since capacitance modelling of a diode is only valid in reverse bias region, the difference between measurement and simulation results becomes large in forward bias region (V_{in} < 1.16 V). The series resistance is around 2 Ω in reverse bias region because of the minimum junction spacing and non-minimum junction width design. As port 1 is the p+junction, port 1 substrate parasitic does have little effect on the performance of the varactor. With accurate capacitance and improved series resistance, the port 1 quality factor is around 30 at 900 MHz.

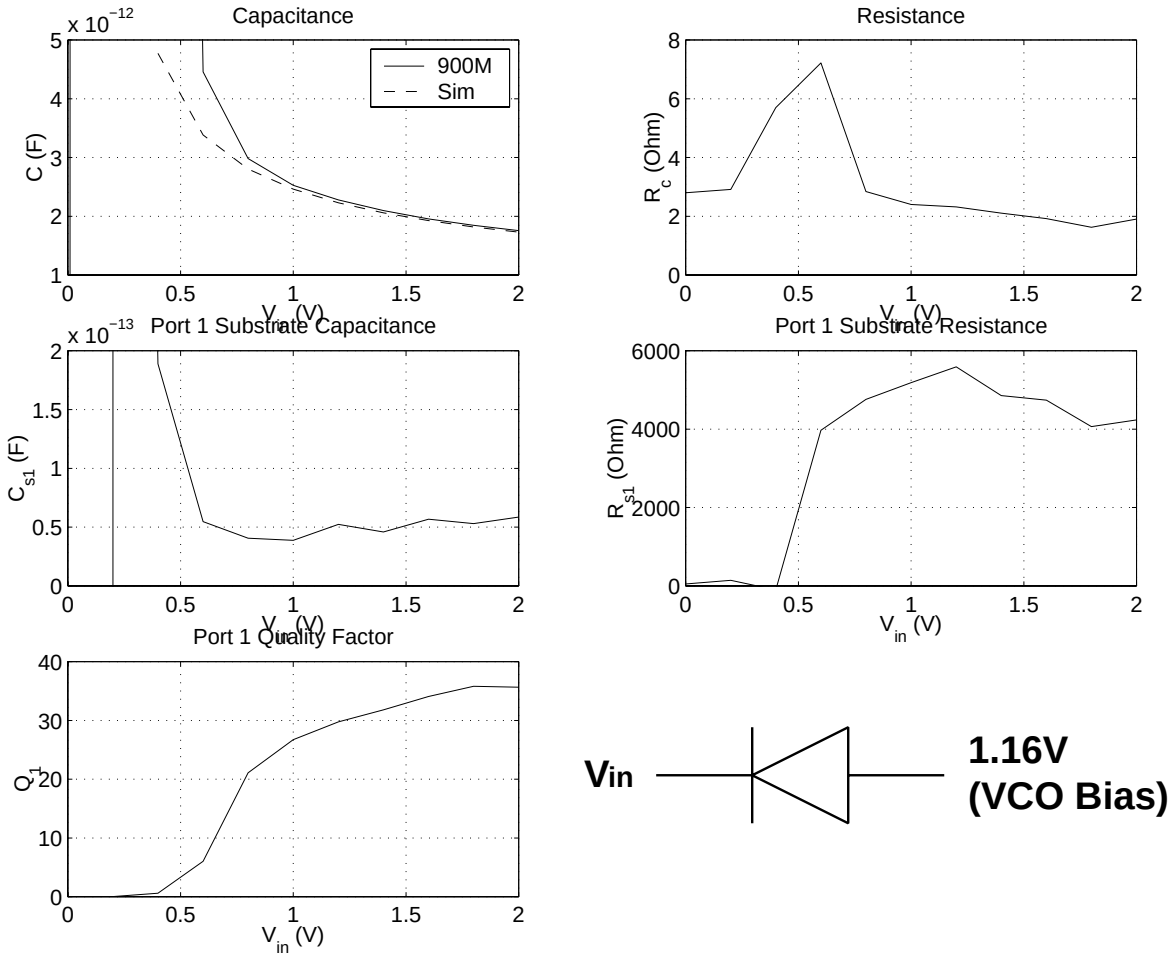


Figure 6.4 Measurement results and biasing condition of the pn-junction varactor.

6.2.2 LC oscillator

6.2.2.1 Test Setup for Phase-Noise Measurement

Figure 6.5 shows the test setup for the phase-noise measurement. It consists of a HP 8510C spectrum analyser, a pair of on-chip NMOS transistors M_{buf}, a pair of bias-Ts and a power combiner. The transistors M_{buf}, which are biased by the bias-Ts, sense the LC-oscillator output. Then the signal is ac-coupled by the bias-Ts and finally is converted to single-ended output by the power combiner. The gain of the output buffer needs not be large since the phase noise does not depend on the signal amplitude. However, the buffer gain should be large enough to ensure the phase-noise level is 10 dB over the noise floor of the spectrum analyzer.

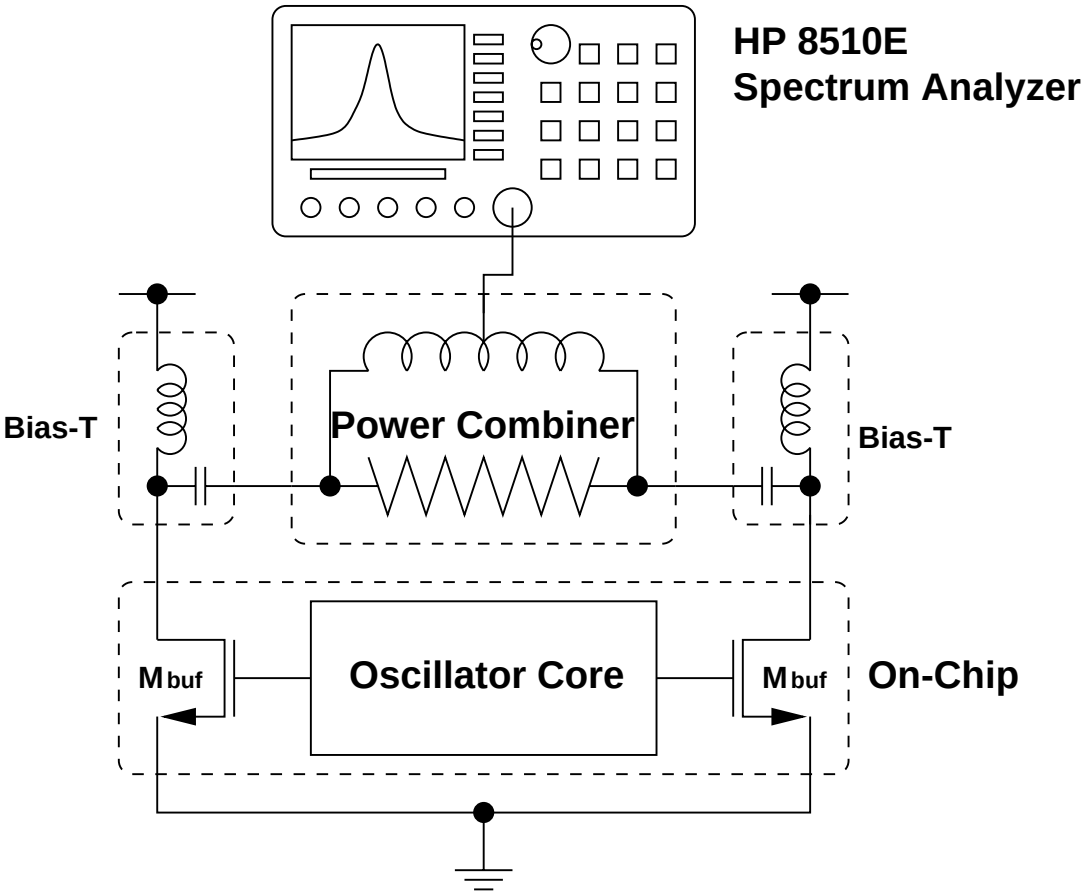


Figure 6.5 Test setup for the phase-noise measurement.

Direct Phase Noise Measurement is adopted to characterize the phase-noise performance of the oscillators [27]. First, the carrier power is determined at large video (VBW) and resolution bandwidths (RBW). Then, the resolution bandwidth is reduced until the noise edge and not the envelope of the resolution filter are displayed. Finally, phase noise is measured at 600-kHz frequency offset from the carrier. To make sure that the measured phase noise is valid, the display values must be at least 10 dB above the intrinsic noise of the analyser.

6.2.2.2 Phase-Noise Measurement Results

Figure 6.6 shows the measurement results of the LC oscillator VCO2. Due to the quality-factor degradation of the spiral inductor, bias current is increased from 6.8 mA to 8.0 mA to achieve the same phase noise specification (-121 dBc/Hz@600kHz). With bias current of 8.0 mA, operating frequency is between 725.0 MHz and 940.5 MHz. Comparing to the

simulation results, oscillation stops when VCO control voltage is below 0.6 V. The oscillation stops because the diodes (varactors) are turned on such that oscillation start-up condition is violated. At the desired frequency range between 865.2 MHz and 889.8 MHz, the phase noise is below -121 dBc/Hz@600kHz.

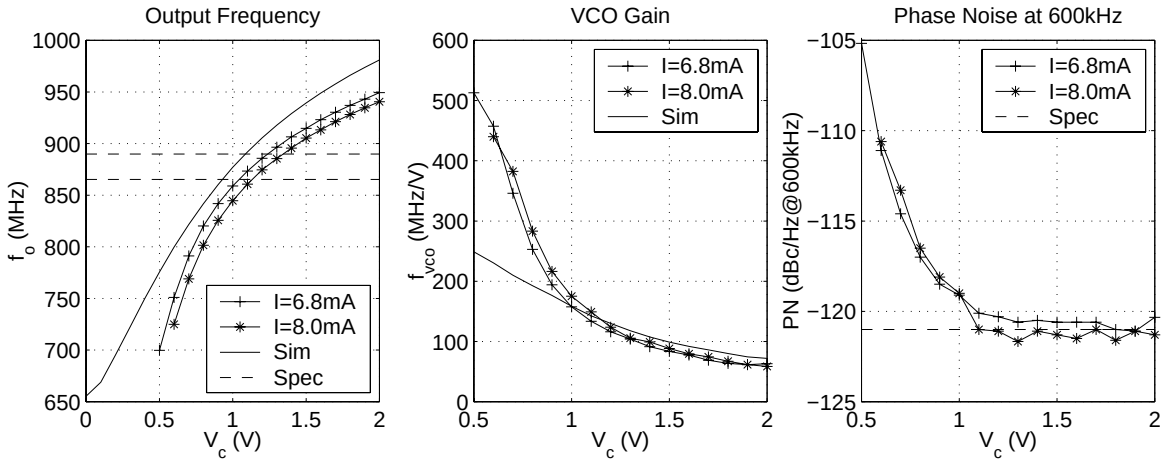


Figure 6.6 Measurement results of the LC oscillator VCO2.

6.3 Ring Oscillator VCO1

Since the ring oscillator VCO1 only utilizes device parasitic capacitance, oscillating frequency f_o can deviate up to 200 MHz. Therefore, a 2-bit capacitor array is added to the ring oscillator core for coarse frequency tuning. Figure 6.7 shows the measurement results of the ring oscillator. It is found that desired frequency range can be achieved either without the capacitor array or with only one capacitor from the array. Although the case with 1 additional capacitor achieves a V_c-to-f_o characteristic closer to the simulation results, the case with zero additional capacitor is adopted in the frequency-synthesizer measurement because of its linear V_c-to-f_o characteristics. The operating frequency is between 324.0 MHz and 642.2 MHz. Similarly to the LC oscillator, the phase noise of the ring oscillator is measured by direct-phase-noise-measurement method. Within the desired frequency range, phase noise is between -112 and -108 dBc/Hz@600kHz.

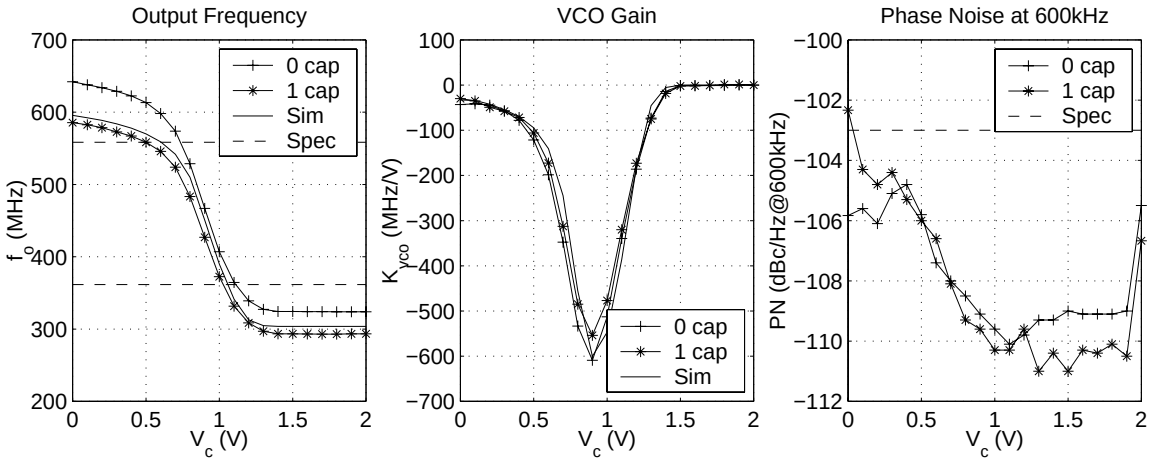


Figure 6.7 Measurement results of the ring oscillator VCO1.

6.4 Frequency Dividers N_1, N_2 & N_3

The measurement setup of the frequency dividers consists of a HP 80000 data generator, a Picoprobe coplaner ground-signal GS probe, a Picoprobe high impedance probe and a Tektronix 11403A digitizing oscilloscope. High frequency full-swing signal (up to 1 GHz) is applied through the GS probe to the frequency divider, then divider output is sensed by the high impedance probe and observed by the digitizing oscilloscope.

6.4.1 Frequency Divider N_1

At supply voltage of 2V, the frequency divider N1 is fully programmable between 226 and 349. The maximum operating frequency is 650 MHz which is larger than that of the ring oscillator. The minimum operating frequency is 25 MHz since the slowest stage is operating at 70 kHz. Figure 6.8 shows the waveforms that the frequency divider N_1 operates at 600 MHz with N_1 = 226 and 349.

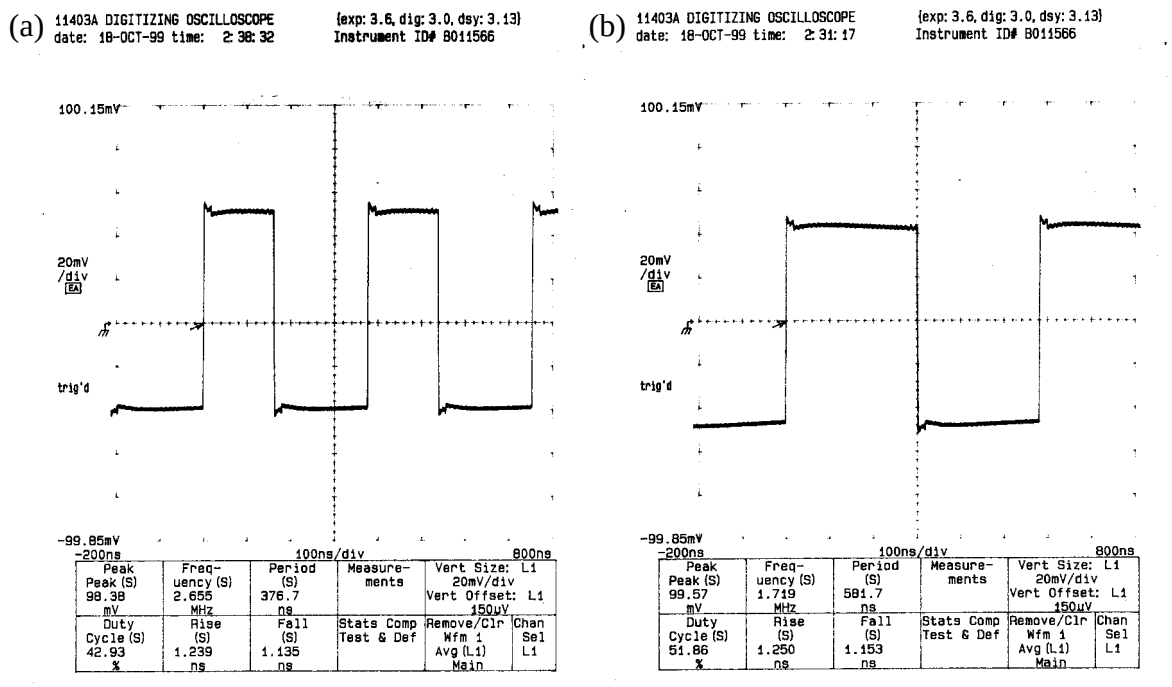


Figure 6.8 Output waveforms of the programmable-frequency divider N_1 at 600 MHz with (a) N_1 = 226 and (b) N_1 = 349.

6.4.2 Frequency Divider N_2

The frequency divider N_2 is tested in a similar way. At 2-V supply voltage, the maximum operating frequency is 640 MHz which is larger than that of the ring oscillator VCO1. The minimum operating frequency is less than 1 MHz. Figure 6.9 shows the waveforms of the divider N_2 operating at 600 MHz.

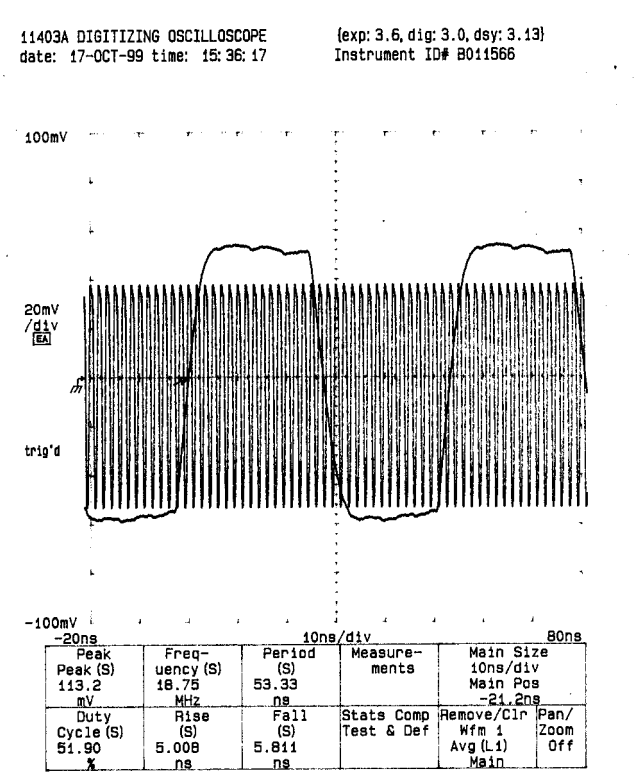


Figure 6.9 Waveforms of the divide-by-32 frequency divider N_2 at 600 MHz.

6.4.3 Frequency Divider N_3

Since frequency divider N_3 senses the sinusoidal output signal of the LC oscillator VCO2, a HP E4422B signal generator and a bias-T are used to generate sinusoidal input signal with dc bias. Under 2-V supply voltage, the operating frequency is larger than 1 GHz which is larger than that of the LC oscillator. With input voltage of 0.5 V, input dc voltage can be between 0.62 V and 1.32 V. With input dc bias of 1.1 V, which is the dc bias of the LC-oscillator core, the minimum requirement input amplitude is 0.24 V. Figure 6.10 shows the waveforms of the divider N_3 operating at 1 GHz.

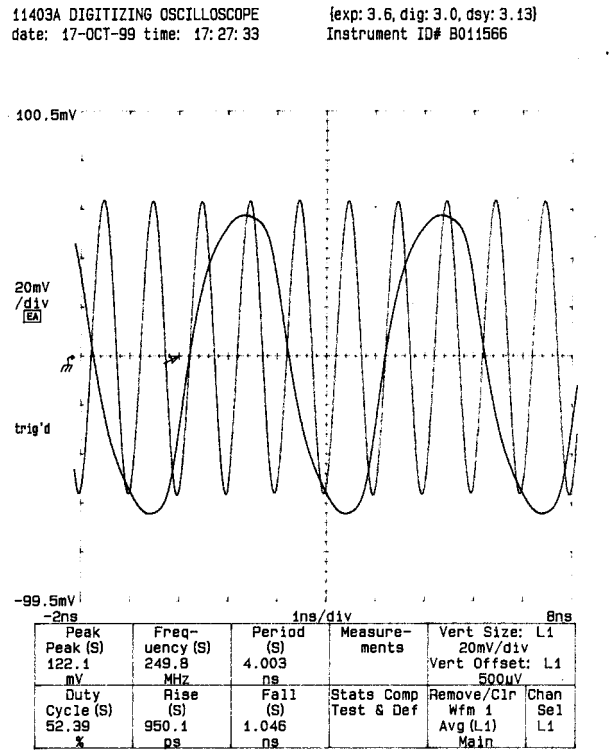


Figure 6.10 Waveforms of the divide-by-4 frequency divider N_3 operating at 1 GHz.

6.5 Dual-Loop Frequency Synthesizer

6.5.1 Loop Filters

Loop filters are measured by a HP 4284A precision LRC meter and a pair of dc probes. Figure 6.11 shows the magnitude and phase plots of the loop-filter impedance of both the low-frequency loop and high-frequency loop. Magnitude and phase plots show a response the same as the second-order loop filter in Figure 4.53. Comparing to the simulation results, the phase derivation is less than 5°. Therefore, loop stability, phase-noise and spurious-tone filtering transfer functions can be preserved. At frequency close to 1 MHz, some glitches can be observed in the phase characteristics. The glitches may be caused by the defects of the measurement setup since it is close to the measurement-frequency limit.

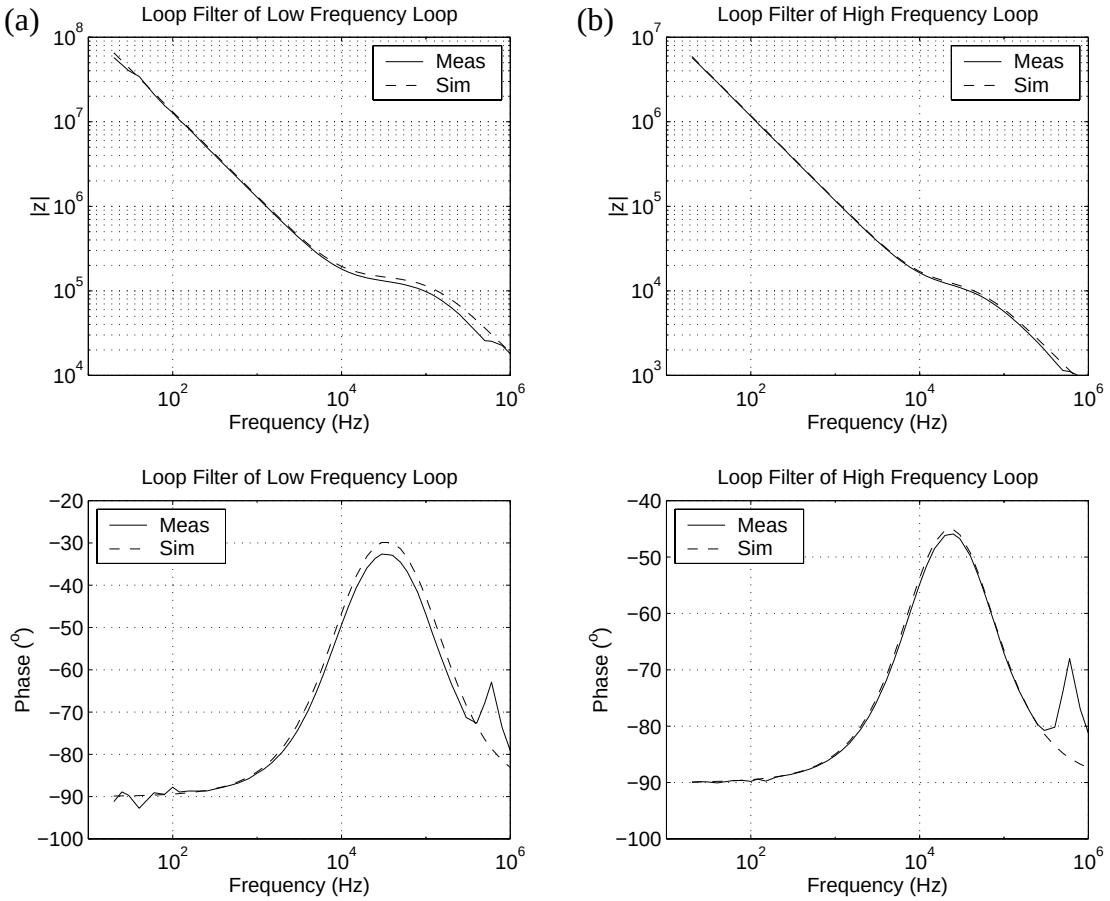


Figure 6.11 Measurement results of the loop-filter impedance of the (a) low-frequency loop and (b) high-frequency loop.

6.5.2 Spurious Tones

The worst-case spurious tones can be observed at the minimum channel frequency as the input frequency of the high-frequency loop is 11.3 MHz (17.45 MHz for maximum channel). As shown in Figure 6.12, spurious levels are -79.5 dBc@1.6MHz, -82.0 dBc@11.3MHz and -82.83 dBc@16MHz. At 11.3 MHz, the spurious level is 6 dB only above the specification (-88 dBc@11.3MHz). However, the predicted spurious level at 1.6 MHz should be below -90 dBc and the spur at 16 MHz should not exist. In fact, the first reference signal at 1.6 MHz is generated by a crystal oscillator at 16 MHz divided by a decade counter. Therefore, the spur at 16 MHz is caused by substrate coupling between crystal oscillator and the high frequency loop.

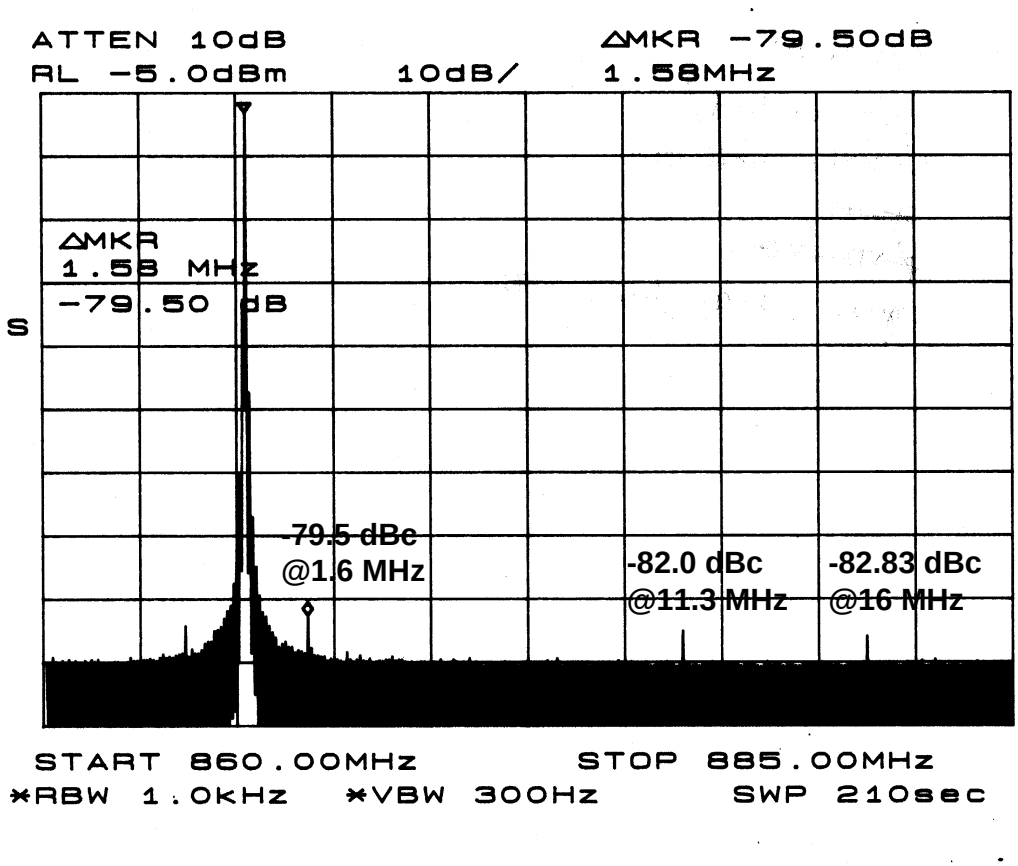


Figure 6.12 Measurement results of the spurious tones at f_o = 865.2 MHz.

Since there exists substrate coupling between the crystal oscillator and the high-frequency loop, it is suspected that the large spurious level at 1.6 MHz is caused by substrate coupling between the decade counter and the high-frequency loop. To verify the assumption, the low-frequency loop is turned off and external input signal at 11.3 MHz is applied to the high-frequency loop. Figure 6.13 shows that spurious level is -75.1 dBc@1.6MHz and it implies the increase in spurious level at 1.6 MHz is due to the substrate coupling.

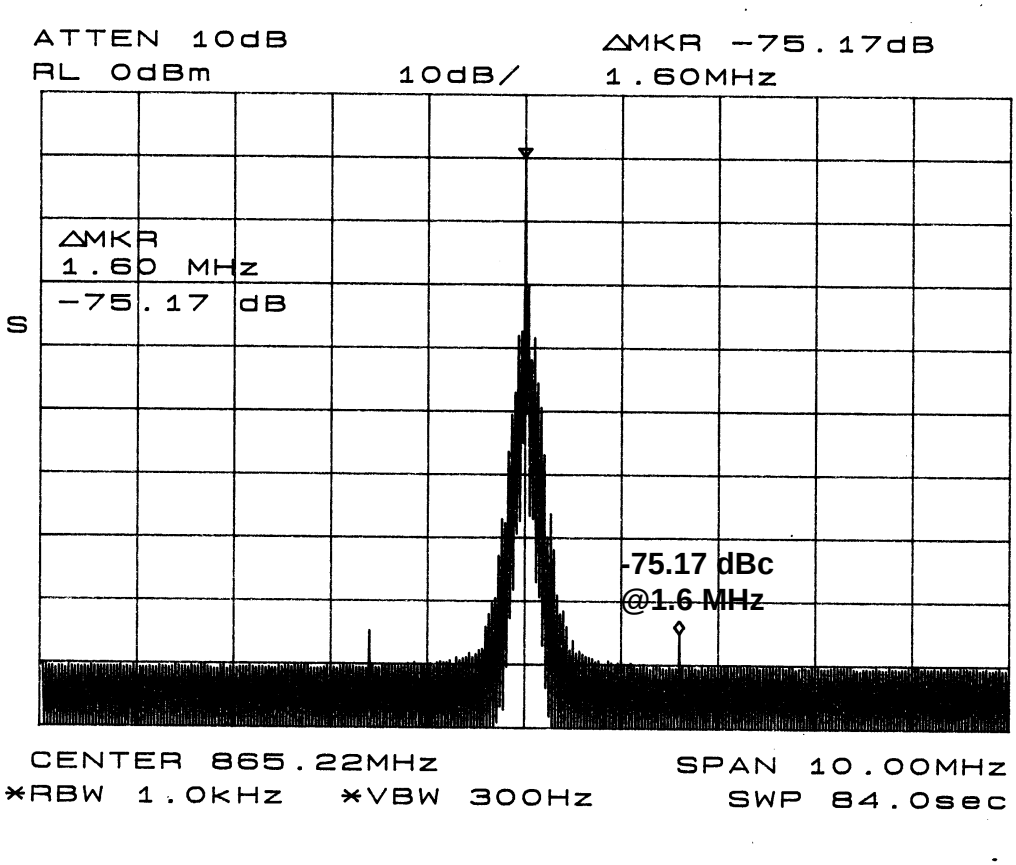


Figure 6.13 Spurious level at 1.6 MHz when the low-frequency loop is turned off.

6.5.3 Phase Noise

The worst-case phase noise happens at the maximum channel frequency as reference and charge-pump phase noise are multiplied by the frequency division ratio N_1 = 349. Figure 6.14 shows the phase noise at the maximum channel frequency f_o = 889.8 MHz. The phase noise is -121.8 dBc/Hz@600kHz which meets the specification. The close-in phase noise is measured to be about -81 dBc/Hz. At offset frequency between 10 Hz and 100 Hz, the rise in phase noise may be due to the flicker noise of charge pump since the phase noise drops about 10 dB per decade. However, the peak phase noise is only -65.67 dBc/Hz which is over 20 dB above the predicted performance in Figure 4.66.

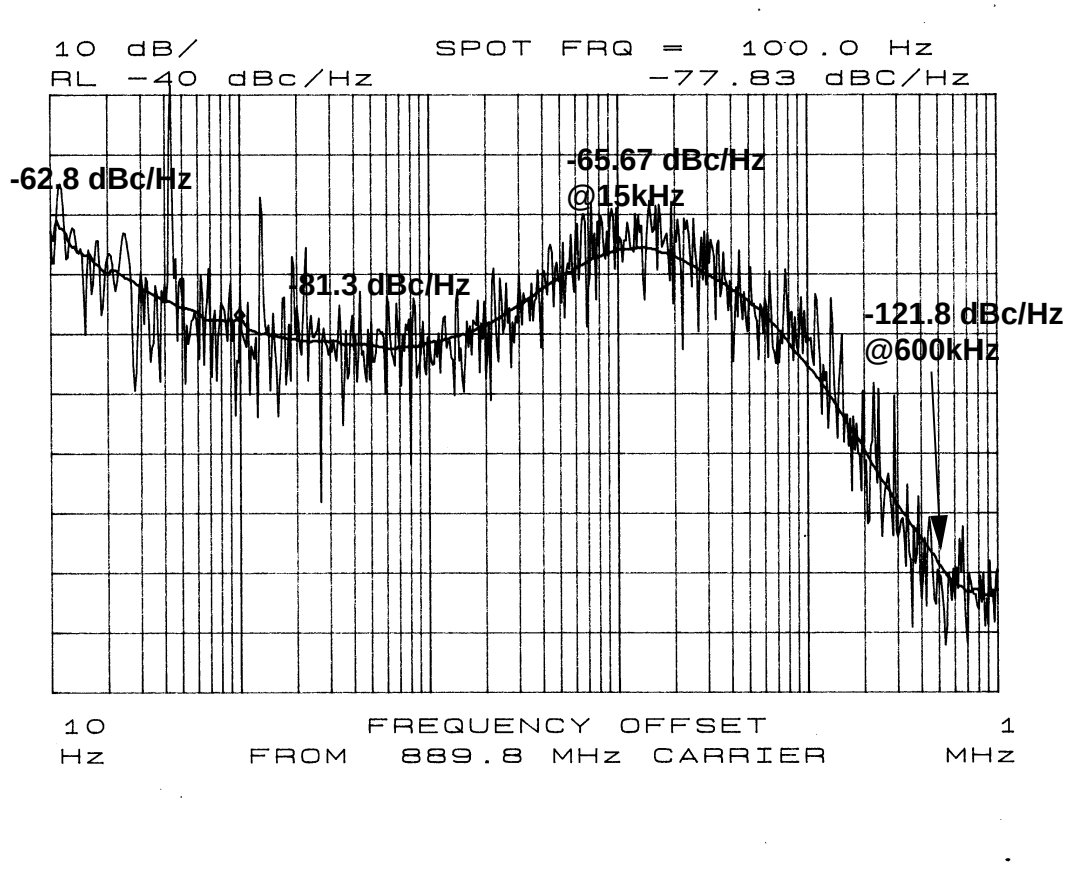


Figure 6.14 Measurement results of the phase noise at f_o = 889.8 MHz.

6.5.4 Switching Time

6.5.4.1 Test Setup for Switching-Time Measurement

The test setup for switching time measurement is shown in Figure 6.15. It consists of a SRS DS345 synthesized function generator, two Philips 74HC157D 4-bit multiplexers, two dc probes and a HP 54520A general-purpose oscilloscope. The function generator applies clock signal to the 4-bit multiplexers in order to program the frequency division ratio N_1. When the synthesizer switches between two channels at a very low frequency (e.g. 1 Hz), the switching can be observed in the spectrum analyzer.

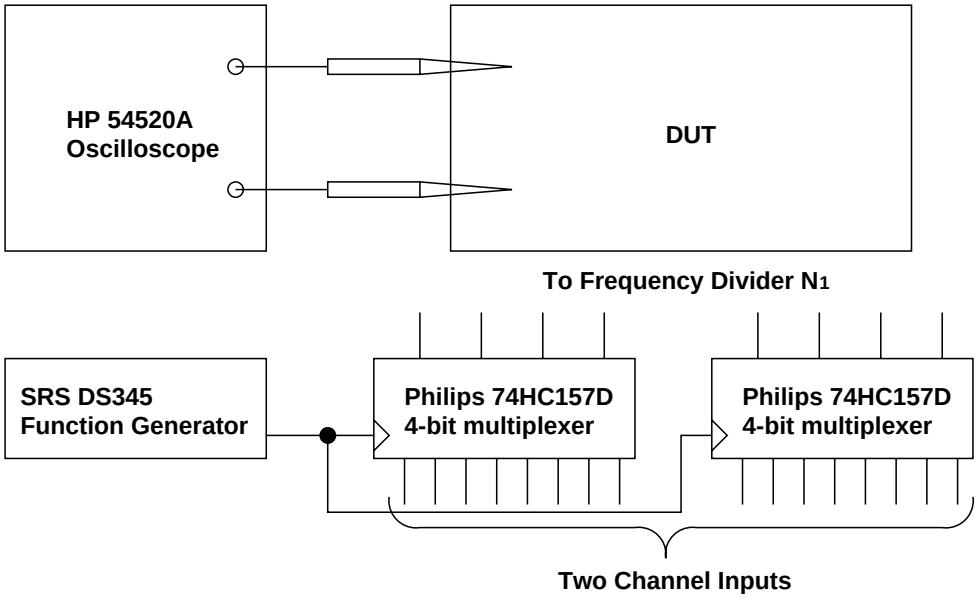


Figure 6.15 Measurement setup for the switching-time measurement.

6.5.4.2 Switching-Time Measurement Results

To determine the switching time, VCO-control voltage of both the low-frequency and high-frequency loops are observed by the digitizing oscilloscope. To prevent the probe and oscilloscope parasitics from loading the loop filter, an unity-gain amplifier is used to buffer the VCO control voltages of both loops. Figure 6.16 shows the switching times of VCO control voltage of both low-frequency and high-frequency loops when the synthesizer is switching between the minimum and maximum channels. The worst-case settling time of the synthesizer is 830 μs.

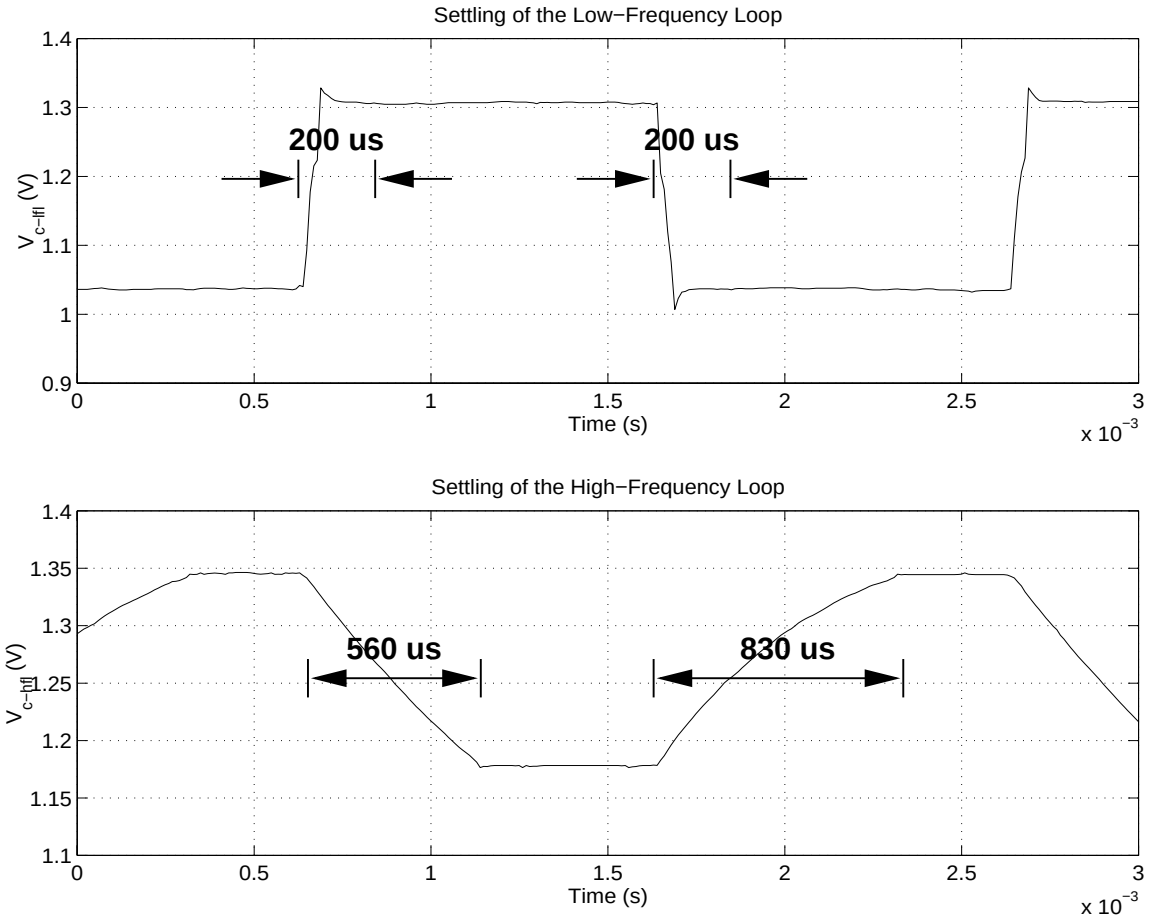


Figure 6.16 VCO control voltages of the low-frequency and high-frequency loops switching between the minimum and maximum channels.

6.6 Performance Comparison

After the measurement of the whole dual-loop frequency synthesizer, Table 6.1 summaries the performance of different monolithic frequency synthesizer design published in recent years for comparison purpose. For fair phase-noise comparison, all the phase-noise performance is recalculated to an equivalent offset frequency of 600 kHz, assuming a dependence of 20 dB per decade on offset frequency.

Design (1) is designed for the application of DCS 1800 which has similar specification to GSM 900 except that the synthesizer operates at 1.8 GHz. By using fractional-N architecture, input frequency can be designed at 26.6 MHz which is twice of the input frequency of the high

frequency loop. Therefore, loop bandwidth can be designed at 45 kHz to achieve a switching time of 250 μs. However, the loop filter is implemented by two layers of polysilicon, which the unit capacitance is only 1.5 fF/μm^2, the chip area is larger the dual-loop design. Moreover, design (1) operates at 3-V supply, so its power consumption is around 33% larger than this work.

Design (2) also adopts fractional-N design with input frequency of 9.6 MHz. This design achieves the best spurious level below -110 dBc. However, the chip area is the biggest one (5.5 mm^2) although external loop filter is adopted. Moreover, the power consumption is around 33% larger than this work since it operates at 2.7-V supply voltage.

Design (3) also adopts fractional-N architecture. Since this design only aims to achieve 600-kHz channel spacing, 61.6-MHz input reference is adopted and the loop bandwidth is designed at 200 kHz which is 7 times larger than the dual-loop design. However, this design has larger current consumption but its phase-noise performance is even worse than the dual-loop design.

From the above comparison with the other existing monolithic frequency-synthesizer solutions, it is found that the dual-loop frequency synthesizer satisfies the phase-noise specification at 600-kHz frequency offset and switching-time specification for GSM 900. Spurious level is limited to be -79.5 dBc because of substrate coupling of reference signal, which also exists in design (1) and (3). Since the dual-loop design operates under 2-V supply, its power consumption is at least 33% lower than the other designs. According to the design optimization in Figure 4.63 and Figure 4.65, the loop-filter area of the low-frequency loop is only one-tenth of that of the high-frequency loop. Therefore, the chip area of the dual-loop design is just the average among the designs mentioned above with the help of linear capacitor, where unit capacitance is 2.4 fF/μm^2.

Design	(1) Ref. [3]	(2) Ref. [28]	(3) Ref. [29]	(4) This Work
System	DCS 1800	N. A.	N. A.	GSM 900
Carrier Frequency	1.8 GHz	900 MHz	1.6 GHz	900 MHz
Channel Spacing	200 kHz	600 kHz	600 kHz	200 kHz
No. of Channel	124	41	N. A.	124
Process	0.4-µm CMOS	25-GHz BJT	0.6-µm CMOS	0.5-µm CMOS
Architecture	Fractional-N	Fractional-N	Fractional-N	Dual-Loop
Supply Voltage	3 V	2.7 to 5 V	3 V	2 V
Reference Frequency	26.6 MHz	9.6 MHz	61.5 MHz	1.6 MHz 205 MHz
Chip Area	3.23 mm^2	5.5 mm^2	1.6 mm^2	2.64 mm^2
Loop Filter	On Chip	Off Chip	On Chip	On Chip
Loop Bandwidth	45 kHz	4 kHz	200 kHz	40 kHz 27 kHz
Close-In Phase Noise	-80 dBc/Hz	N. A.	N. A.	-65.7 dBc/Hz
Phase Noise at 600-kHz Offset	-121 dBc/Hz	-116.6 dBc/Hz (recalculated)	-115 dBc/Hz	-121.83 dBc/Hz
Spurious Level	-75 dBc @ 26.6 MHz	< -110 dBc	-83 dBc @ 61.5 MHz	-79.5 dBc @1.6 MHz -82.0 dBc @11.3 MHz -82.88 dBc @16 MHz
Switching Time	< 250 µs	< 600 µs	N. A.	< 830 µs
Current Consumption	17 mA	18.5 mA	30 mA	17 mA
Power Consumption	51 mW	50 mW	90 mW	34 mW

Table 6.1 Performance comparison between different monolithic implementation of the frequency synthesizer.

Chapter 7

Conclusion

This master thesis presents the design of a 2-V 900-MHz monolithic CMOS dual-loop frequency synthesizer for GSM receivers with good phase-noise performance.

Designing fully integrated frequency synthesizers for system integration is always desirable but most challenging. This first requirement is to achieve high frequency operation with reasonable power consumption. However, the most critical challenges for the frequency synthesizer are the phase-noise and spurious-tone performance. Finally, small chip area is essential to monolithic system integration.

The dual-loop design consists of two reference signals and two phase-locked loops (PLLs) in cascode configuration. Because of the dual-loop architecture, input frequencies of the two PLLs are scaled from 200 kHz to 1.6 MHz and 11.3 MHz. Therefore, the loop bandwidths of both PLLs can be increased, so that both switching time and chip area can be reduced.

Measurement of the on-chip spiral inductor shows the quality factor drops from 3 to 1.6. The quality-factor degradation is mainly due to additional eddy current induced in the N-well fingers under the inductor, which is proven by the measurement results of the inductors with laminated polysilicon and with only P-substrate.

Because of the quality-factor degradation of inductor, bias current of the LC oscillator is increased from 6.8 mA to 8.0 mA in order to satisfy the phase-noise requirement. The

phase-noise performance of the whole dual-loop frequency synthesizer is close to the estimation except that the peak-close-in phase noise is 15 dB worse than the specification.

The spurious tones are -79.5 dBc@1.6MHz, -82.0 dBc@11.3MHz and -82.88 dBc@16MHz, which are limited by substrate coupling. This assumption is verified by turning off the low-frequency loop and spurious tones are still observed at with similar spurious level at these frequencies.

Implemented in a 0.5-μm CMOS technology and at 2-V supply voltage, the dual-loop frequency synthesizer has a low power consumption of 34 mW. At 900 MHz, the phase noise of the dual-loop design is less than -121.83 dBc/Hz at 600-kHz frequency offset. The spurious tones are -79.5 dBc@1.6MHz, -82.0 dBc@11.3MHz and -82.88 dBc@16MHz. The worst-case switching time is less than 830 μs. The chip area is 2.64 mm^2. However, the peak close-in phase noise is -65.67 dBc/Hz at 15-kHz frequency offset which is 15 dB worse than the specification of GSM 900.

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