A 1.5-V 900-Mhz Monolithic CMOS Fast-Switching Frequency Synthesizer for Wireless Applications

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By

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ABSTRACT

In modern transceiver designs, a frequency synthesizer with good phase-noise performance is very important because it affects the efficiency of valuable air channel usage and sensitivity of small signals under the presence of large interference. Fast frequency switching is also required in many TDMA systems and frequency-hopping spread-spectrum systems. Other than these, low supply voltage, low power consumption and monolithic design are three important features of any modern analog circuits.

However, the above requirements are difficult to be achieved in traditional frequency synthesizer designs. To solve these problems, a new design of phase-locked loop frequency synthesizer is proposed. Instead of voltage or current domain, some signals in the phase-locked loop are manipulated in capacitance domain. A binary-weighted switchable-capacitor array is used to replace the digital-to-analog converter while two varactors connected in parallel replace the voltage adder. This design provides many advantages, including simplified analog circuitry, low supply voltage, low power consumption, small chip area, fast frequency switching and high immunity of substrate noise.

A prototype of a 1.5-V 900-Mhz monolithic CMOS fast-switching frequency synthesizer based on GSM specifications is designed and fabricated to demonstrate the idea. It consumes 30mW. The total chip area is 0.9 x 1.1 mm^2. The settling time is within 150us and phase noise is –118dBc/Hz at 600kHz offset. The ability of direct-digital modulation is also provided with the sigma-delta fractional-N architecture.

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Table of Contents

List of Tables

List of Figures

Page

Chapter 1 Introduction

Background

Wireless communication is replacing the cable communication to become the most important part of the modern world. The most familiar wireless communication is the mobile phone. It links all people anywhere anytime. Starting from the bulky analog mobile phones to digital mobile phones, the size, the weight and the price become lower and lower while the performance becomes better and better.

Inside a mobile phone, there is basically a wireless transceiver. In the past, most of the transceivers were implemented by bulky and expensive discrete components. As the technologies are improved, some building blocks can be implemented by low-density integration technologies, e.g. BJT, GaAs, to reduce the cost and size of the transceivers. However, this is not enough to satisfy people's desire of low cost, small size and good performance. Due to the rapid development of the microprocessor and computer industries in the past years, the digital CMOS process becomes very mature. Compared to other available processes, the digital CMOS process has the strong advantages of low cost and high density. The growing density and performance of the sub-micro CMOS process make the process to be a very attractive candidate for the radio-frequency integrated circuits.

In this research, we are trying to demonstrate the possibility to implement wireless receiver and transmitter with the digital CMOS process. The first step is to implement a monolithic wireless receiver for the GSM system, which is the most popular in the

world. All the building blocks of the wireless transceiver, including low-noise amplifier, RF image-rejection filter, mixer, frequency synthesizer, IF channel-selection filter and the IF analog-to-digital converter will be implemented on the same chip.

One of the major building blocks is the frequency synthesizer. The frequency synthesizer is to generate the LO frequency for the mixer to down-convert the RF signal to the IF filter. Unlike other building blocks in the receiver, the frequency synthesizer itself is already a small system including many building blocks. This makes the frequency synthesizer to be a very challenging project because the project involves system design, RF circuit design, high speed digital circuit design and low noise analog circuit design.

In this project, a monolithic frequency synthesizer is designed with a lot of efforts on both system and circuit implementation to solve the problems encountered with existing deigns.

Challenges

In modern transceivers, a good frequency synthesizer to provide a pure local oscillator frequency is very important because of the valuable bandwidth available. Phase noise is the most basic requirement of performance for a frequency synthesizer. It affects the efficiency of air channel usage and sensitivity of small signal under the presence of large interference.

Fast switching between different frequencies is also important in TDMA and spread spectrum systems. Spread spectrum is especially important in modern wireless

applications because it can provide immunity to multipath interference and fading, and provide robust multiple access capability.

Other than phase noise and switching performance, low supply voltage, low power consumption and monolithic design are three essential features of any modern analog circuits. Low supply voltage, especially 1.5 volt from a single battery, is very important in portable applications. It allows the design to integrate with modern low-voltage digital circuits easily, reduce the weight and size of battery, and usually reduce the power consumption. Monolithic design is also important because it has lower manufacturing cost, smaller size and lower power consumption.

Most of the common frequency synthesizers are based on phase lock loop (PLL) design. Compared to direct analog synthesizer and direct digital synthesizer, it has the advantages of simpler design and smaller power consumption. But it still has its own difficulties to meet the above requirements for modern wireless applications.

Noise

In monolithic design, the phase noise performance of the synthesizer is degraded not only by the phase noise of the voltage-controlled oscillator itself and the noise from the loop filter but also by the substrate noise. Since the substrate is conductive, any noise from other noisy circuits e.g. digital circuit, will couple through the substrate to the voltage-controlled oscillator (VCO) and degrade the phase noise. This noise source is difficult to predict and cannot be prevented or reduced by increasing power consumption. Large separation from noise sources and guard ring can only improve the problem a bit.

Switching speed

Switching speed is limited in PLL based synthesizers. In conventional design, the finest frequency resolution equals to the reference frequency. However, in order to fulfill the requirement of stability, the larger loop bandwidth is limited to approximately 1/10 of the reference frequency [1]. As a result, PLL synthesizers with a fine frequency resolution have a small loop bandwidth and thus a low switching speed. Moreover, at different output frequencies, the varactor of the VCO is biased with different voltages and has different gains. The loop gain is therefore not constant through out the whole output frequency range. In some frequency range, the loop bandwidth and speed are smaller than the optimum because the stability of the loop has to be ensured in all cases. Although some linearization techniques can be used[2], they require the characteristic of a pre-measured varactor and thus can only provide limited linearization.

Supply voltage

To compensate the center frequency variation in voltage controlled oscillator, a large tuning range is required. In this case, large voltage range is required to bias the varactor for large frequency range. Thus, large supply voltage is needed.

Monolithic

To meet the tough phase noise specification, huge capacitors are needed to reduce the thermal noise in the charge-pump and loop filter. The capacitors are usually so large that they will either occupy a very large chip area or have to be put off-chip.

Thesis overview

In this work, we will try to solve the problems mentioned above including substrate noise, frequency switching speed, supply voltage and chip area, which are faced by

existing monolithic frequency synthesizers. The main emphasis of the research relies on the system improvement of the frequency synthesizer in order to solve the above problems and to relax the requirement on the circuit performance. In chapter 2, the specifications of the frequency synthesizer are discussed. In chapter 3, the proposed system and its advantages are discussed. Some detailed system parameters are also determined. Chapter 4 deals with the circuit implementations of different building blocks of the frequency synthesizer. Chapter 5 is special for the discussion on the quadrature phase and amplitude matchings in coupled-LC oscillators. In chapter 6, some layout considerations are discussed. The testing methods and experimental results are discussed in Chapter 7. Finally Chapter 8 provides a conclusion of the whole research and the contribution.

Chapter 2 Specifications

Frequency range and resolution

In a wireless receiver, as shown in Fig. 1, the radio-frequency (RF) signal is received through the antenna and amplified by the low-noise amplifier (LNA). Since the output frequency of the down-convert mixer is the absolute value of the difference of the two input frequencies, both the desired signal RF and the image signal RF-2IF can be mixed down to IF. Therefore RF signal is filtered by the RF image-rejection filter in order to remove the RF-2IF signal before it is down-converted as shown in Fig. 2. As the mixer performs the frequency subtraction, resultant signal of the mixer RF-LO which equals to the intermediate-frequency (IF) will pass through the channel selection filter. Only the desired channel is remained and sampled by the analog-to-digital converter.

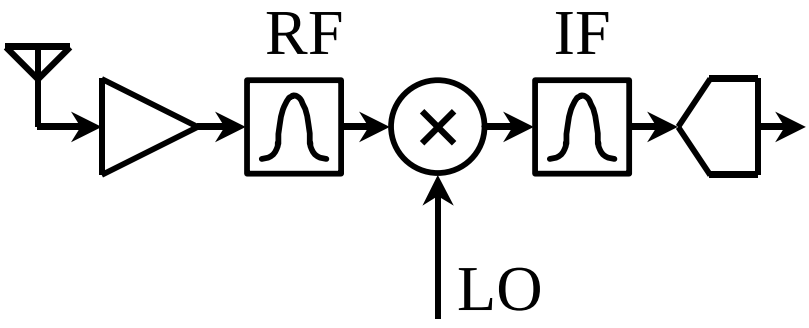

Fig. 1 Block diagram of a receiver

As shown in Fig. 3, the mixer will mix down the desired channel within receiver frequency band (935MHz – 960MHz) to exactly 70MHz and let the IF channel selection filter which is centered at 70MHz to filter out all other unwanted channels. As

the receiver frequency band is from 935MHz to 960MHz and the IF is 70MHz, the output frequency range of the frequency synthesizer will be from 865MHz to 890MHz. The channel spacing in the receiver band is 200kHz and therefore the frequency resolution of the frequency synthesizer is 200kHz.

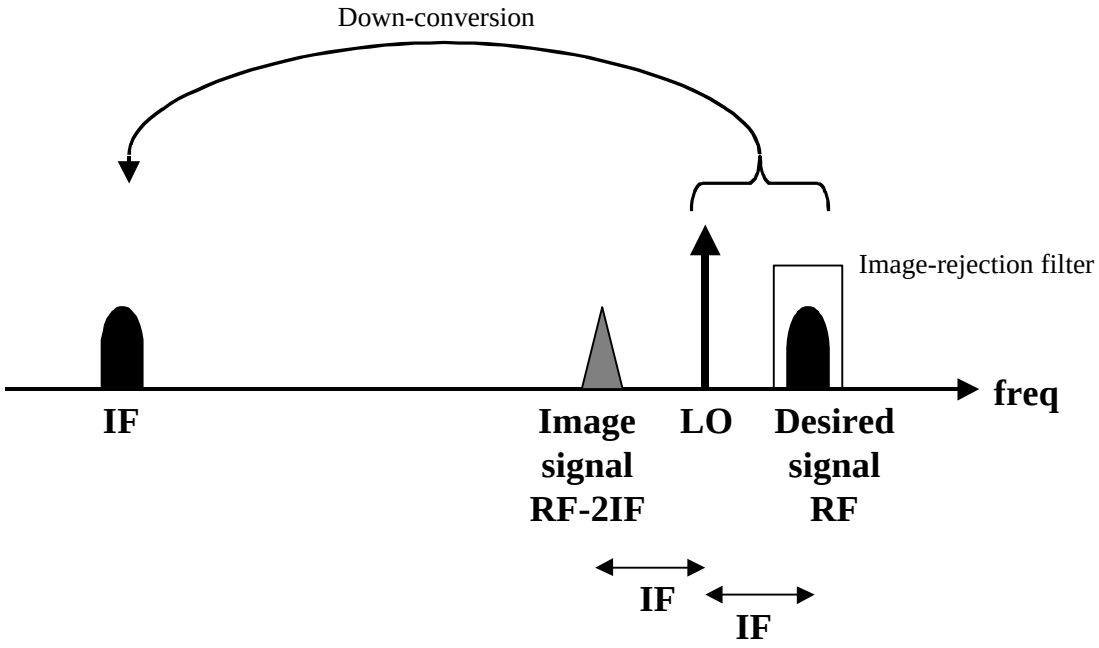

Fig. 2 Frequency domain representation of the down-conversion and the relationship between RF, image, LO, and IF signals

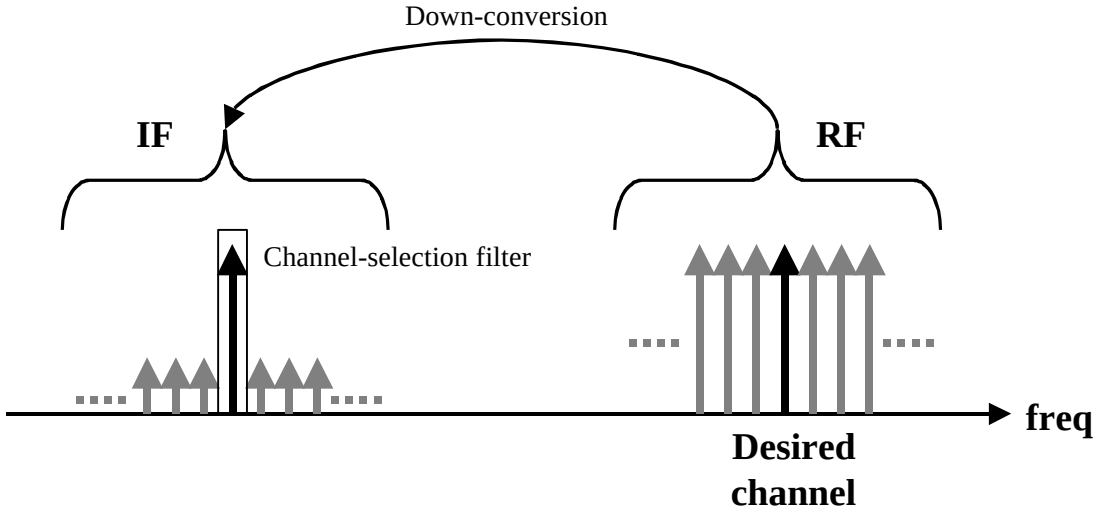

Fig. 3 Frequency domain representation of the channel selection

Phase noise

In the specification of GSM 900[3], around the received signal, there is a lot of interference due to the adjacent signals.

Fig. 4 shows the profile of the maximum interference signals defined in the specifications. The power of nearest adjacent channel at 200kHz offset from the received signal can be as large as –93dBm and the maximum interference powers at 400kHz, 600kHz, 1.6MHz and 3MHz offsets are –61dBm, -43dBm, -33dBm and -23dBm. The maximum interference powers at frequency larger than 980MHz or smaller than 915MHz can be as large as 0dBm. However, since these two interference signals are outside the receiver band, most of them can be filtered out by the RF filter and they can be ignored in this case. The GSM specifications also define the minimum power level of the received signal to be –102dBm.

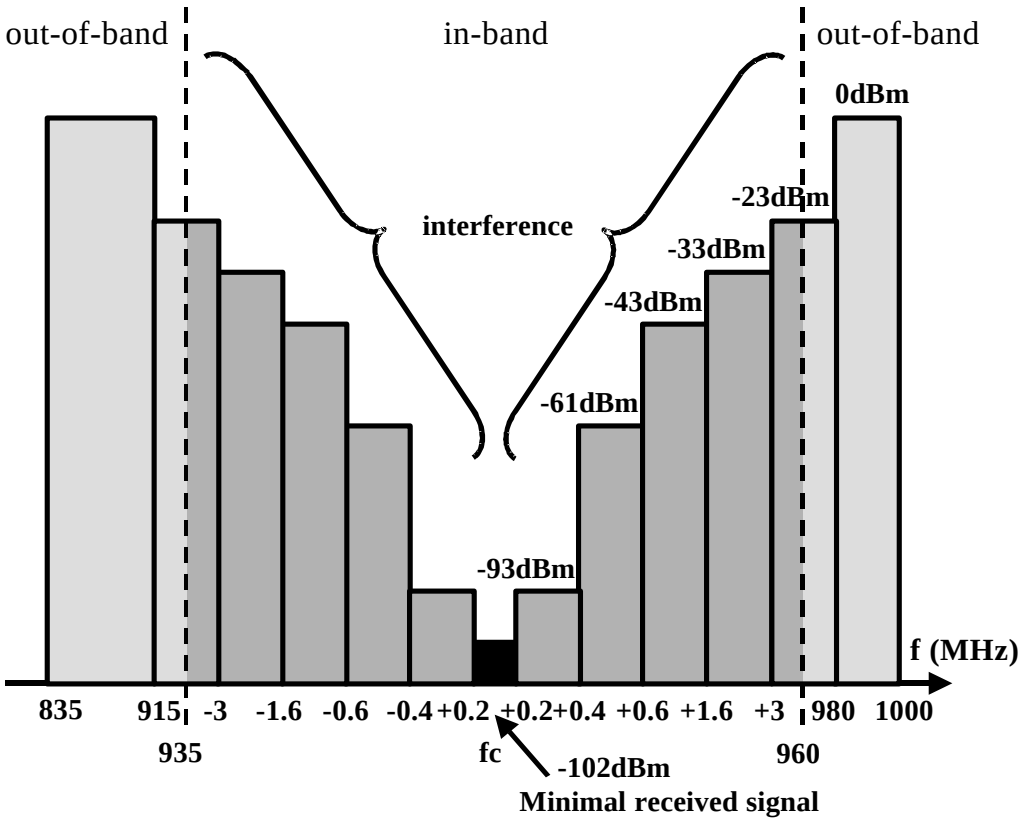

Fig. 4 Profile of interference signals

Ideally, the output of the frequency synthesizer should be a pure tone. However, due to the thermal noise of the resistors and transistors in the oscillator or some noise at the frequency tuning input of the oscillator, the phase of the oscillation will fluctuate. In frequency domain, the phase fluctuation forms a skirt of noise power around the carrier impulse as shown in Fig. 5. The phase noise is defined as the difference between the carrier power and the total noise power within 1Hz at some frequency offset Δf from the carrier frequency. If the noise source is white, the phase noise in the frequency domain is proportion to $1/\Delta f^2$.

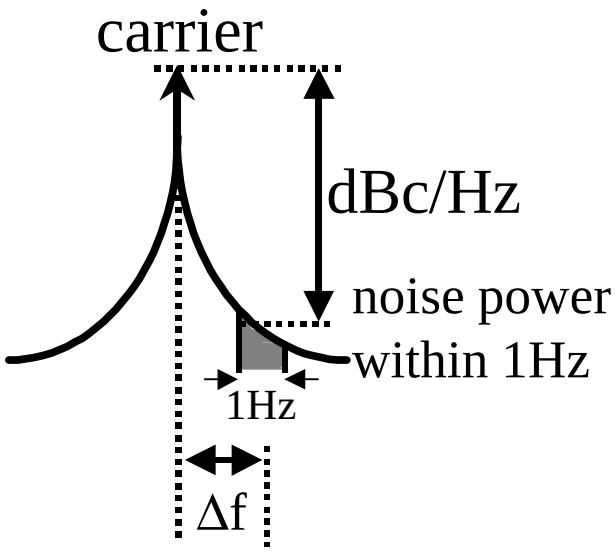

Fig. 5 Frequency domain representation of phase noise

As shown in Fig. 6, if there is a large interference signal near the small desired signal and the LO signal has a phase noise skirt, both the desired signal and the interference will be mixed down to the IF. However, both signals will also have the same noise skirt as the one of the LO signal because the down-conversion is actually a convolution in frequency domain. Since the powers of the interfere signals are generally large, the noise down-converted to the frequency of the desired signals can significantly degrade the signal-to-noise ratio (SNR) of the desired signals.

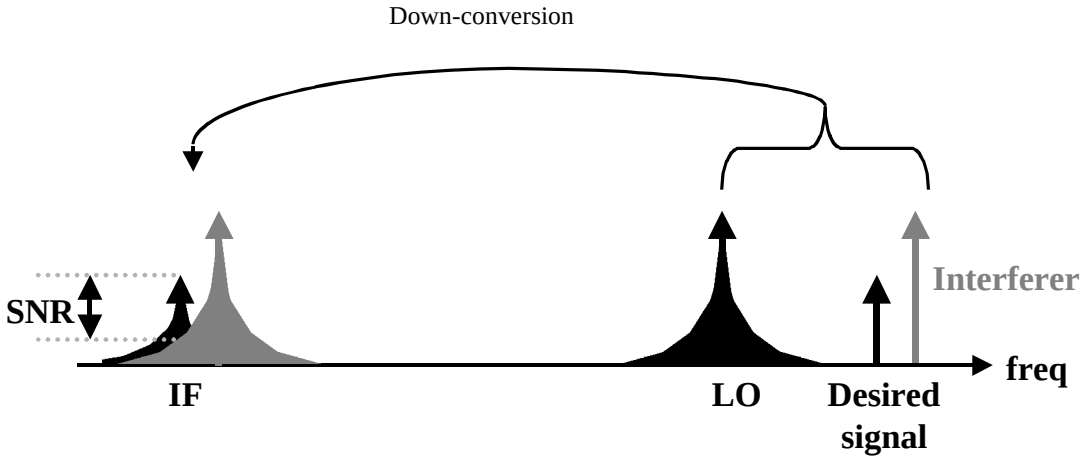

Fig. 6 Effect of phase noise of LO signal

Based on the maximum interference, minimum received signal and the minimum required signal-to-noise ratio defined in the GSM specifications which is 9dB, the maximum phase noise accepted of the LO signal at different frequency offset can be calculated as following.

$$\text{required SNR} < \frac{\text{minimum received signal power}}{\text{maximum noise power}}$$

$$\text{required SNR} < \frac{\text{minimum received signal power}}{\text{maximum interference power} \times \text{LO phase noise} \times \text{signal bandwidth}}$$

$$\text{LO phase noise} < \frac{\text{minimum received signal power}}{\text{maximum interference power} \times \text{signal bandwidth} \times \text{required SNR}}$$

For example, at 600kHz frequency offset,

$$\text{LO phase noise} < \text{-102dBm} - (\text{-43dBm}) - 9\text{dB} - 53\text{dB} = \text{-121 dBc/Hz}$$

Based on this calculation, the phase noise requirements at different frequency offsets are –103dBc/Hz at 400kHz, -121dBc/Hz at 600kHz, -131dBc/Hz at 1.6MHz and -141dBc/Hz at 3MHz as shown in Fig. 7. The phase noise requirements at different frequency offset from the carrier can be compared easily by normalizing them to the same frequency offsets because the phase noise in this frequency range is proportion to $1/\Delta f^2$. The phase noise requirements for GSM specifications at larger frequency offsets are tougher than the ones at smaller frequency offsets. Due to the limitation of on-chip oscillators, it is impossible to meet the all the phase noise requirements. Usually, only the requirements at the two closer frequency offsets 400kHz and 600kHz are considered which is equivalent to –121dBc/Hz at 600kHz offset[4].

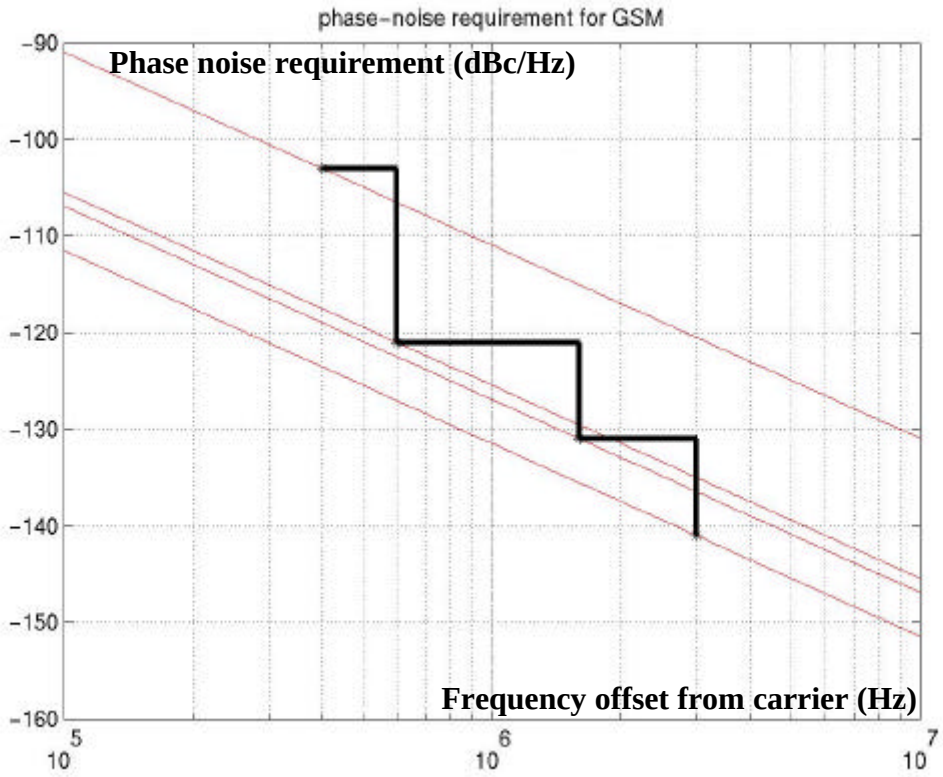

Fig. 7 Phase noise envelope for local oscillator signal in GSM receiver

Spurs

Other than the phase noise due to the internal thermal noise and external input noise, the oscillator can also be modulated by some noise of fixed frequencies due to the switching of other circuits in the synthesizer. One of the main noise sources is the switching noise of the charge pump at the reference frequency. The input noise will modulate the oscillator and be up-converted to the carrier. Two tones will appear at the upper and lower sideband of the carrier as shown in Fig. 8. These tones are called spurs and measured by the difference between powers of the carrier and the spurs at some frequency offset in the units of dBc.

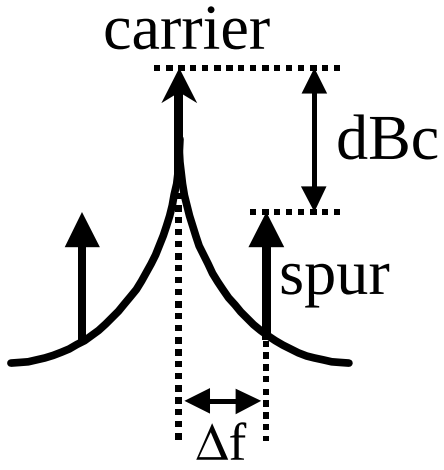

Fig. 8 Frequency domain representation of spurs

Similar to the case of phase noise, as shown in Fig. 9, if there is a large interference signal near the small desired signal and the LO signal has spurs, both the desired signal and the interference will be mixed down to the IF. However, both down-converted signals will also have the spurs as the ones of the LO signal. If the spur of the down-converted inference is at the same frequency of the desired signal, it degrades the SNR of the desired signal.

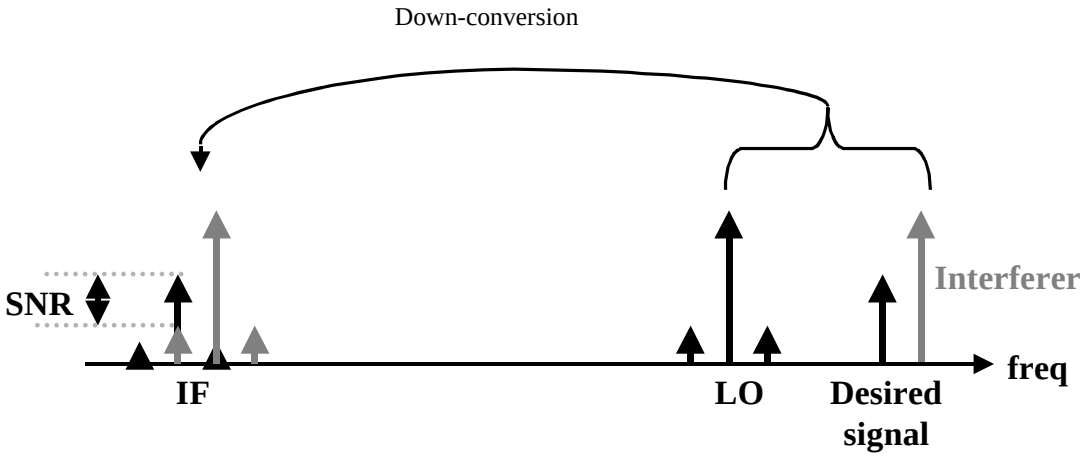

Fig. 9 Effect of spurs of LO signal

Also based on the maximum interference, minimum received signal and the minimum required signal-to-noise ratio defined in the GSM specifications, the maximum spurs accepted of the LO signal at different frequency offset can be calculated as following.

$$\text{required SNR} < \frac{\text{minimum received signal power}}{\text{maximum noise power}}$$

$$\text{required SNR} < \frac{\text{minimum received signal power}}{\text{maximum interference power} \times \text{LO spur power}}$$

$$\text{LO spur power} < \frac{\text{minimum received signal power}}{\text{maximum interference power} \times \text{required SNR}}$$

For example, at 600kHz frequency offset,

$$\text{LO phase noise} < \text{-102dBm} - (\text{-43dBm}) - 9\text{dB} = -68\ \text{dBc/Hz}$$

Based on this calculation, the spur requirements at different frequency offsets are –50dBc/Hz at 400kHz, -68dBc/Hz at 600kHz, -78dBc/Hz at 1.6MHz and -88dBc/Hz at 3MHz as shown in Fig. 10

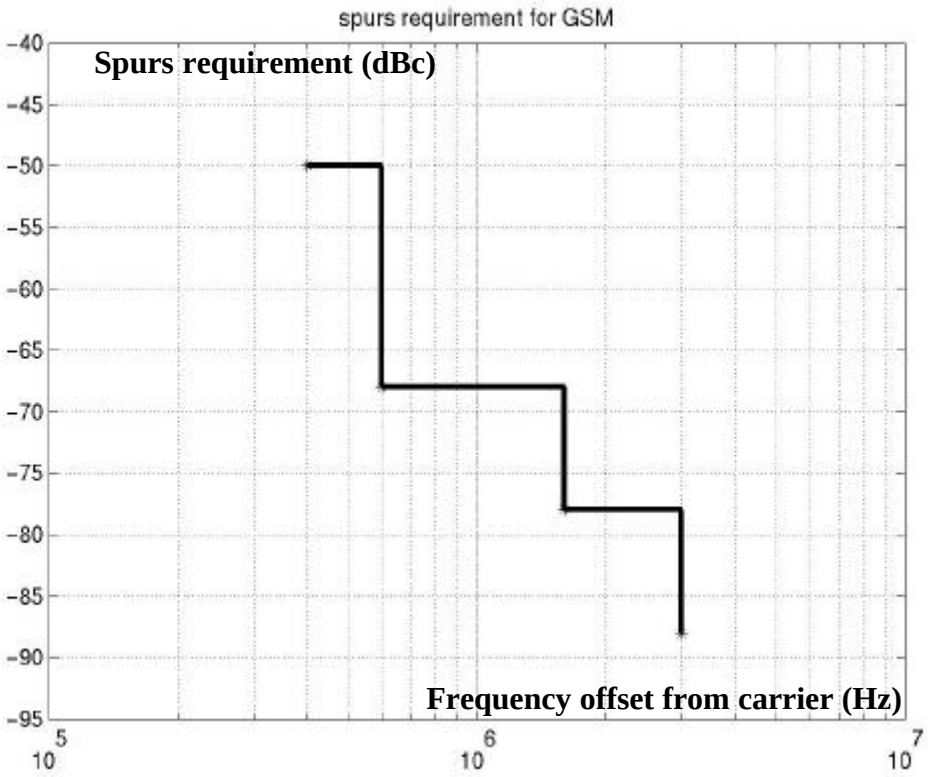

Fig. 10 Spur envelope for local oscillator signal in GSM receiver

Frequency switching time

GSM uses a combination of time-division-multiple-access (TDMA) and frequency-division-multiple-access (FDMA) schemes to provide base stations with simultaneous access to multiple users. The available frequency bands are divided into 200kHz wide channels called absolute radio frequency channel numbers (ARFCNs). Each channel is time shared among as many as eight subscribers using TDMA.

As shown in Fig. 11, the signal is received in the first time slot and the signal is transmitted in the fourth time slot. The time slot between R6 and R7 is used for system monitoring. Usually only one frequency synthesizer is used in the transceiver for both up-conversion and down-conversion in the transmitter and receiver. The minimum switching time is limited by the time to switch between the time slot for transmission

and the time slot for system monitor, in which case the frequency switching has to be finished with 1.5 time slots which is 870μs. The corresponding minimum loop bandwidth for the settling time within 870μs is around 3kHz.

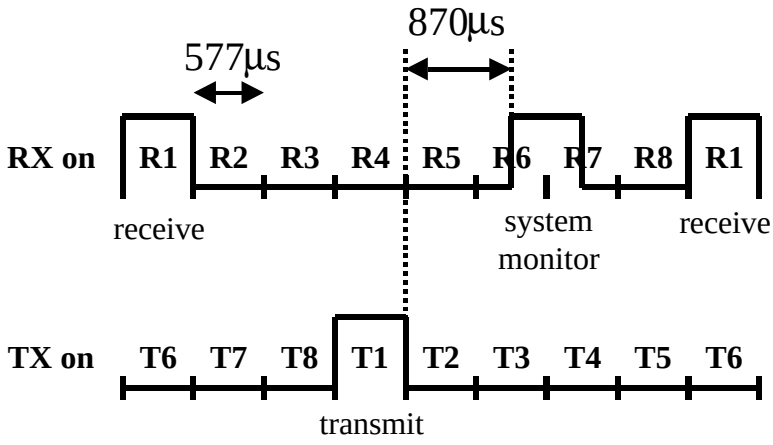

Fig. 11 GSM Receive and transmit time slots

When the wireless signals are transmitted between the base station and the handsets, the signals will undergo different paths due to multi-reflection in order to reach the destination. Different paths will have different delays. The signals with different delays will interference each other constructively or destructively depended on the frequency of the signals. In this case, the wireless signals will undergo frequency selective channel as shown in Fig. 12. Signals at different frequencies will have different fading. Moreover, there are some narrowband fixed-frequency interference signals due to some near-by electronic applications.

Under the frequency selective fading and narrowband interference, some frequency slots are in deep fades or subject to large interference. One of the solutions is frequency diversity which can avoid deep-fade and narrowband interference. It is because deep-fading and interference occurs only when all the paths are in deep fades and jammed by interference.

The frequency diversity can be performed by frequency hopping. In a frequency hopping system, the frequency for the wireless signal changes from time to time. In this case, the LO signal provided by the synthesizer is required to switch between different frequencies rapidly. The switching speed of the frequency depends on different systems and purposes. In Bluetooth system[5], the frequency changes around 1600 times per second.

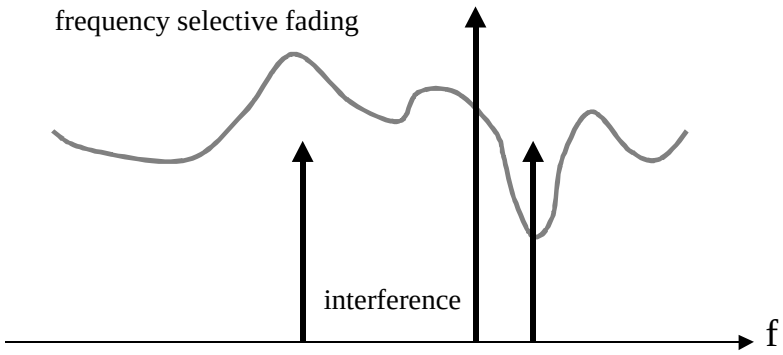

Fig. 12 Frequency selective fading and narrowband interference

Loop bandwidth

In addition to generating the LO signals for up-conversion or down-conversion in a receiver. The frequency synthesizer can also be used as a frequency-shift-key (FSK) transmitter[6]. As shown in Fig. 13, by inputting different division ratio into the prescalar of the frequency synthesizer, the output frequency of the synthesizer will changed accordingly. The output of the synthesizer can directly drive the power amplifier and the antenna. In order to directly modulating the synthesizer and using it as a transmitter, the loop bandwidth has to be larger than the bandwidth of the transmitted signals or some compensation is needed to provide a flat response for the transmitted signals [6].

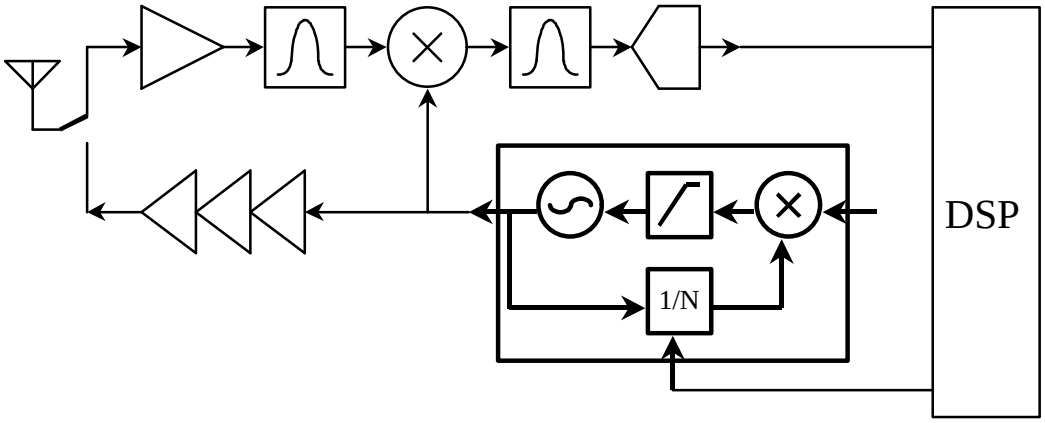

Fig. 13 System diagram of the proposed transceiver

Summary of specifications

Most of the specifications of this project are based on specifications for the GSM receiver. Also some additional specifications, e.g. loop bandwidth and settling time, are partly based on specifications of the GSM transmitter and some frequency hopping systems in order to demonstrate some ideas in the frequency synthesizer. The tough specifications of supply voltage, power consumption and area are also designed to make the project challenging. Table 1 summarizes the specifications.

Table 1 Summary of specifications

Frequency range	865-890MHz (70MHz IF receiver)
Frequency resolution	200kHz (or finer for directly modulated transmitter)
Phase noise	-119dBc/Hz @ 600kHz
Spurs	<-88dBc (in band)
Settling time	<865μs (or smaller for frequency hopping)
Loop bandwidth	80kHz
Supply voltage	1.5V
Power consumption	<50mW
Area	< 2mm x 2mm

Chapter 3 System Design

Phase-locked loop synthesizer

There are many methods to synthesize a required frequency from a frequency reference source. The most common methods are direct analog synthesis, direct digital synthesis and phase-locked loop synthesis[7, 8]. However, most of the frequency synthesizer designs are dominated by phase-locked loop designs because they are simpler, smaller and less power-consuming.

The basic block diagram is shown in Fig. 14. The voltage-controlled oscillator outputs a signal of frequency f_{out}. Then the signal f_{out} will be divided by a programmable digital counter. The frequency and phase of the resultant signal is then compared to the frequency and phase of the reference signal f_{ref} by a mixer or a frequency-phase detector. The output signal of the mixer or frequency-phase detector is filtered out by a low-pass filter. The signal at the filter output is an error signal which represents the difference of phase and frequency of the reference signal f_{ref} and the divided signal f_{out}/N and is used to control the voltage-controlled oscillator such that the signal f_{out}/N equals to f_{ref}, or f_{out} equals to $N \times f_{ref}$.

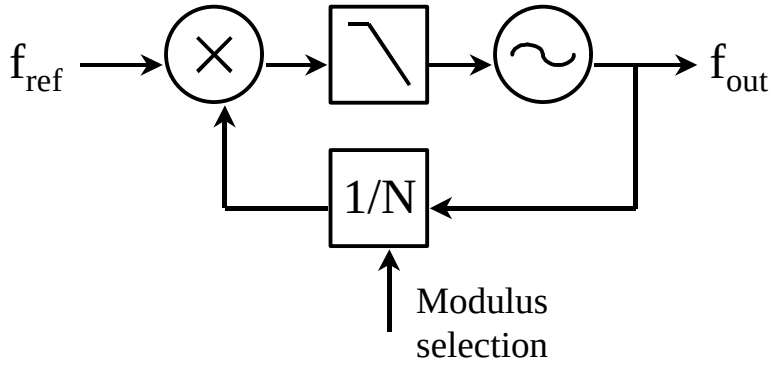

Fig. 14 Block diagram of phase-locked loop frequency synthesizer

However, since the closed loop response of the phase-locked loop synthesizer is low-pass, the response of the phase-locked loop synthesizer for any change of the frequency of the output signal is quite slow. The fast change of the output frequency is very important in time-division dualplex and frequency-hopping systems. The change of the output frequency is done by the change of the modulus selection word.

Existing architecture

There are many different approaches to increase the frequency switching speed of the phase-locked loop synthesizer. One approach is to predict the settled tuning voltage of the VCO. By adding the predicted voltage offset from a digital-to-analog converter (DAC) to the charge pump or loop filter output as shown in Fig. 15a, the capacitance of VCO's LC tank and output frequency change immediately because the loop does not need to change and to settle down[7]. Although the capacitance-to-frequency relationship, which is governed by the equation $f = 1/\sqrt{LC}$, is quite linear within a small range, the voltage-to-capacitance relationship of the varactor, which depends on doping and geometry, is non-linear and difficult to be predicted. Therefore, it is difficult to generate the required voltage to tune the VCO to the correct frequency. Consequently, only

coarse tuning can be provided by the DAC. The loop still has to change a lot and settle down before the desired output frequency reaches. Moreover, in order to reduce the noise from the DAC and voltage adder to the VCO, the voltage summation has to be placed before the loop filter instead of directly before the VCO. As a result, the predicted tuning voltage still has to pass through the loop filter and take time to reach the VCO.

Proposed architecture

Based on the above approach, a new architecture is proposed in this work. Instead of doing the addition in voltage domain, the addition is done in capacitance domain. The addition is implemented as easily as putting two capacitors in parallel. Originally, the voltages from the DAC and charge pump is added by a voltage adder and the resultant voltage controls the capacitance of the LC tank of the VCO through a varactor with an unknown and non-linear characteristic. In the proposed architecture, the DAC is replaced by a binary-weighted switchable-capacitor array (SCA), and the voltage adder is replaced by a parallel connection of the switchable-capacitor array and the varactor, as shown in Fig. 15b.

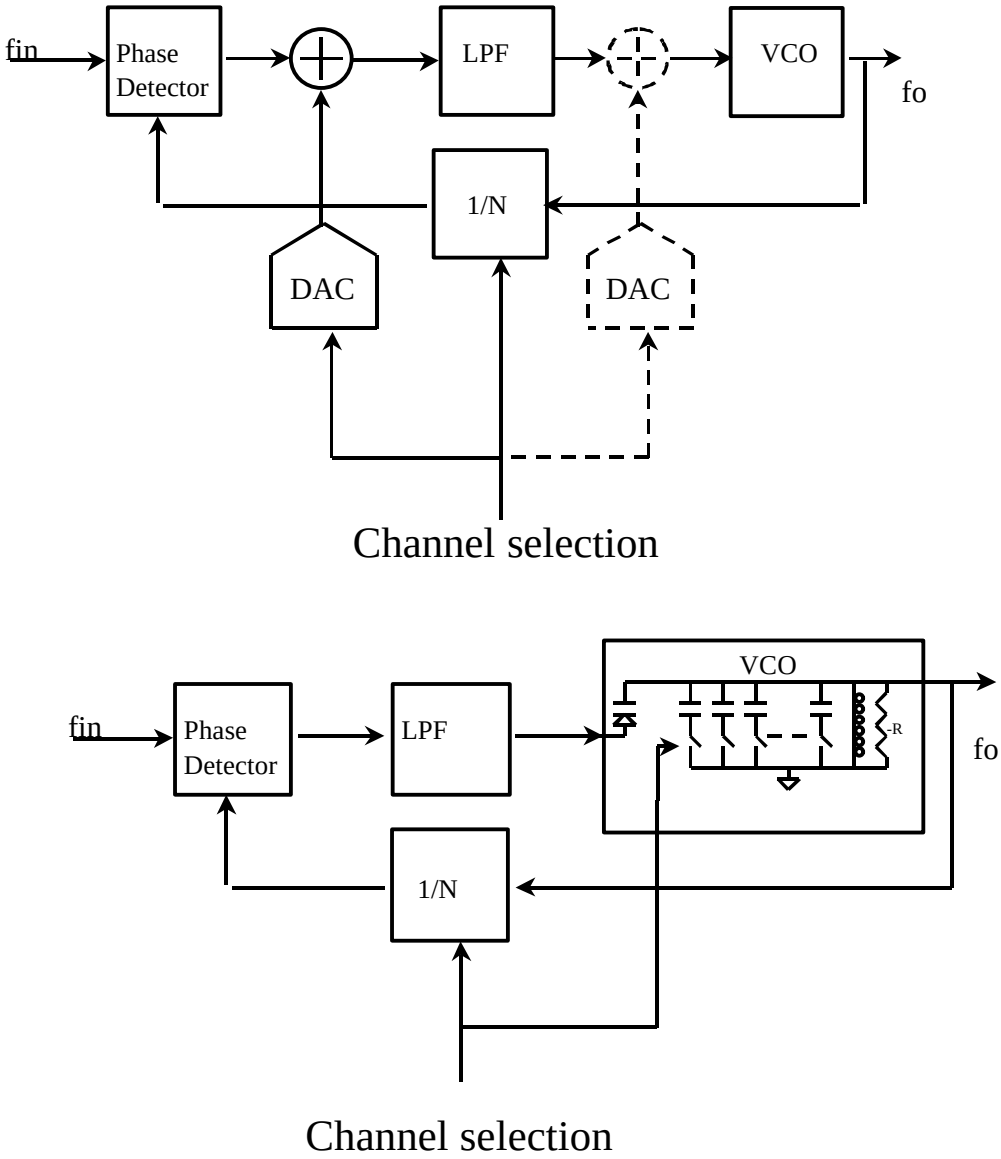

Fig. 15 The evolution of fast-switching PLL frequency synthesizer – a) two possible configurations employing DAC to increase frequency switching speed; b) employing switchable-capacitor-array to increase frequency switching speed

Advantages

In the proposed approach, the capacitance of the varactor controlled by the loop and the capacitance of the switchable-capacitor array are added. The capacitance of the switchable-capacitor array is controlled directly and linearly without through a varactor which has a non-linear voltage-to-capacitance characteristic. As a result, the output frequency can be controlled quite linearly and fine tuning from the switchable-capacitor

array is now possible. Moreover, the addition of capacitance is simply by connecting two capacitors in parallel and no voltage adder is needed.

Since the tuning of frequency is mainly done by the switchable-capacitor array, the gain of the varactor and the change of the tuning voltage can be very small. These two features provide many other advantages of this approach.

Faster switching speed

Due to the linear control of the capacitance in the switchable-capacitor array, fine tuning from the switchable-capacitor array is possible. The accurate amount of capacitance added can change the output frequency close enough to the desired value and the loop can settle quickly. Moreover, the frequency change by adding of the extra capacitance is faster because the control of the addition bypasses the loop filter.

The small variation in the tuning voltage of the varactor results in a constant bias condition and gain of the varactor. The constant and optimal loop bandwidth for speed is obtained without any linearization technique.

Lower supply voltage

In order to compensate the center frequency shift due to process variations, the tuning range of the voltage-controlled oscillator usually has to be very large and a large range of tuning voltage is required for the large tuning range. As a result, a large supply voltage is needed.

In the proposed architecture, as most of the tuning is done by the switchable-capacitor array and the variation of the tuning voltage of the varactor is very small, the tuning range of the voltage-controlled oscillator is independent of the supply voltage. Therefore, a small supply voltage can be used. The small-variant tuning voltage also

prevent the PN junction varactor used from being forward biased and simplifies the circuit design of the analog signal path due to the small required dynamic range.

Smaller chip area

As most of the tuning is by the switchable-capacitor-array, the required tuning range and the gain of the varactors is very small. More noise from the loop filter can be tolerated in the proposed architecture because any change in the tuning voltage has very small effect on capacitance of the varactor and the frequency of the VCO. As a result, much smaller on-chip capacitors of the loop filter can be used to filter out the noise.

Low phase noise

Since the capacitance of the switchable-capacitor array is quite constant when the NMOS switches is fully turned on or off and the gain of the varactor is very small, the substrate noise can only change the total capacitance and the output frequency of the LC voltage-controlled oscillator very little through the varactor and switchable-capacitor array. This can reduce the phase noise of the voltage-controlled oscillator due to unpreventable substrate noise and larger tolerance to substrate noise is obtained.

In addition to smaller power consumption, the absence of the noisy digital-to-analog and voltage adder can also reduce thermal noise added in the tuning voltage which would modulate the voltage-controlled oscillator and degrade the phase noise.

Fractional-N synthesizer

The above-proposed architecture provides a simple solution to increase the frequency switching speed of phase-locked loop frequency synthesizers. There are also many variations of the basic phase-locked loop frequency synthesizer to increase the

performance of the synthesizer [9]. One of the variations is the multi-loop phase-locked loop frequency synthesizer which employs two or more phase-locked loop frequency synthesizers. The most common design is dual-loop phase-locked loop frequency synthesizers. There can be a number of different configurations. One of the frequency synthesizer can generate the reference frequency to the other frequency synthesizer, as shown in Fig. 16a. Or, one of the frequency synthesizer can generate a frequency offset added or subtracted from the other frequency synthesizer, as shown in Fig. 16b.

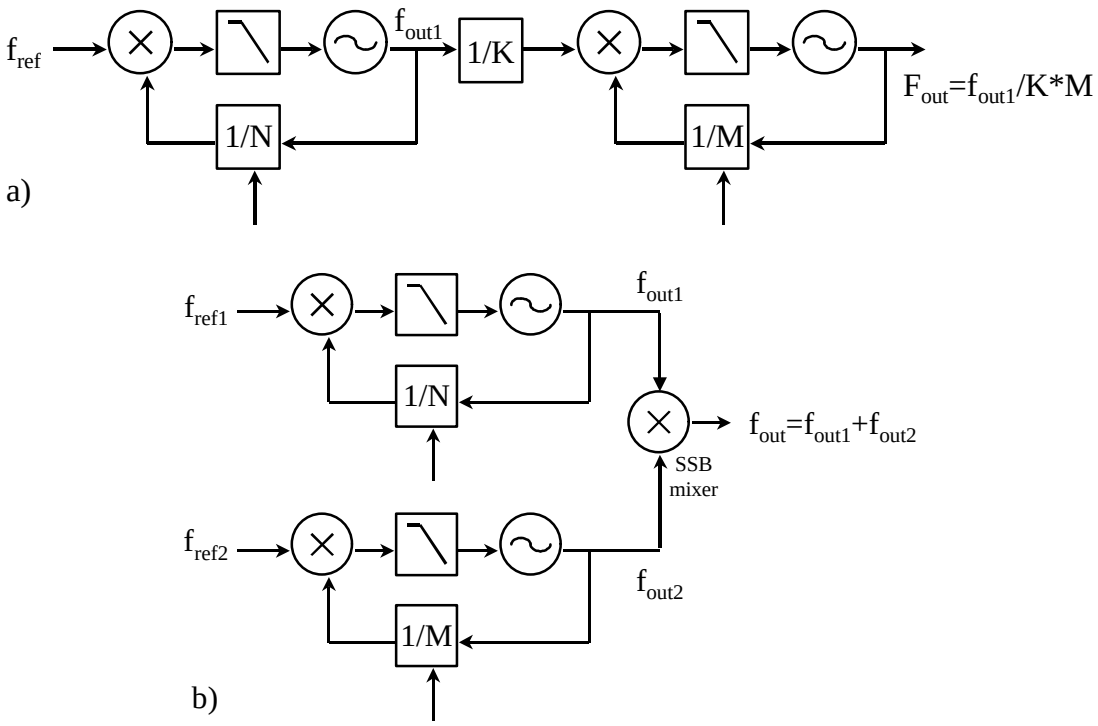

Fig. 16 Block diagrams of some dual-loop synthesizer designs

In the original phase-locked loop frequency synthesizer (Integer-N frequency synthesizer), the output frequency f_{out}, which equals to N x f_{ref}, is an integral multiple of the reference frequency f_{ref} because the frequency divider can only have integer division ratio. However, by continuously changing the division ratio of the frequency divider, it is possible to have an average division ratio which is a fractional number. For example, if a frequency divider have the division ratio 4 in 50% of time and the division

ratio 5 in the other 50% of time. The average division ratio will be 4.5. This is referred to a fractional-N frequency synthesizer.

The fractional-N frequency synthesizer is actually an integer-N frequency synthesizer with a changing division ratio in the frequency divider. Only some additional digital circuits are needed to generate a continuously changing division ratio. This makes the design to be more simple and robust than the multi-loop frequency synthesizer as multiple hardware of the multi-loops, filters and mixers are needed in multi-loop frequency synthesizer. Therefore, this design is based on fractional-N PLL architecture.

Design criteria

One drawback of the fractional-N synthesizer is that quantization noise is added to the loop because there are only a few division ratios (quantization level) in the frequency divider but they will represent the division ratios in between. In the case of a constant fractional division ratio required, the quantization noise generated is a single frequency tone, as shown in Fig. 17a, in which the frequency depends on the fractional division ratio. In case of a random changing division ratio required, the quantization noise generated has a white noise spectrum as shown in Fig. 17b. To solve the problem, a sigma-delta modulator can be used before the divider [10]. For a fractional number input (Fig. 18a), the sigma-delta modulator can redistribute the quantization noise such that the most of the noise is located at higher frequencies (Fig. 18b). The resultant high frequency noise can be filtered out by the low-pass response of the loop (Fig. 18c), and very little noise is left.

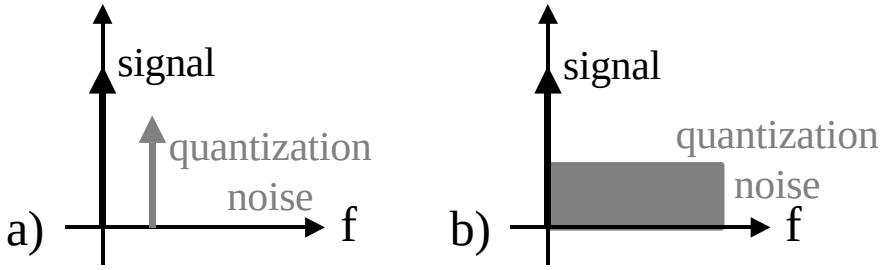

Fig. 17 Quantization noise in frequency domain

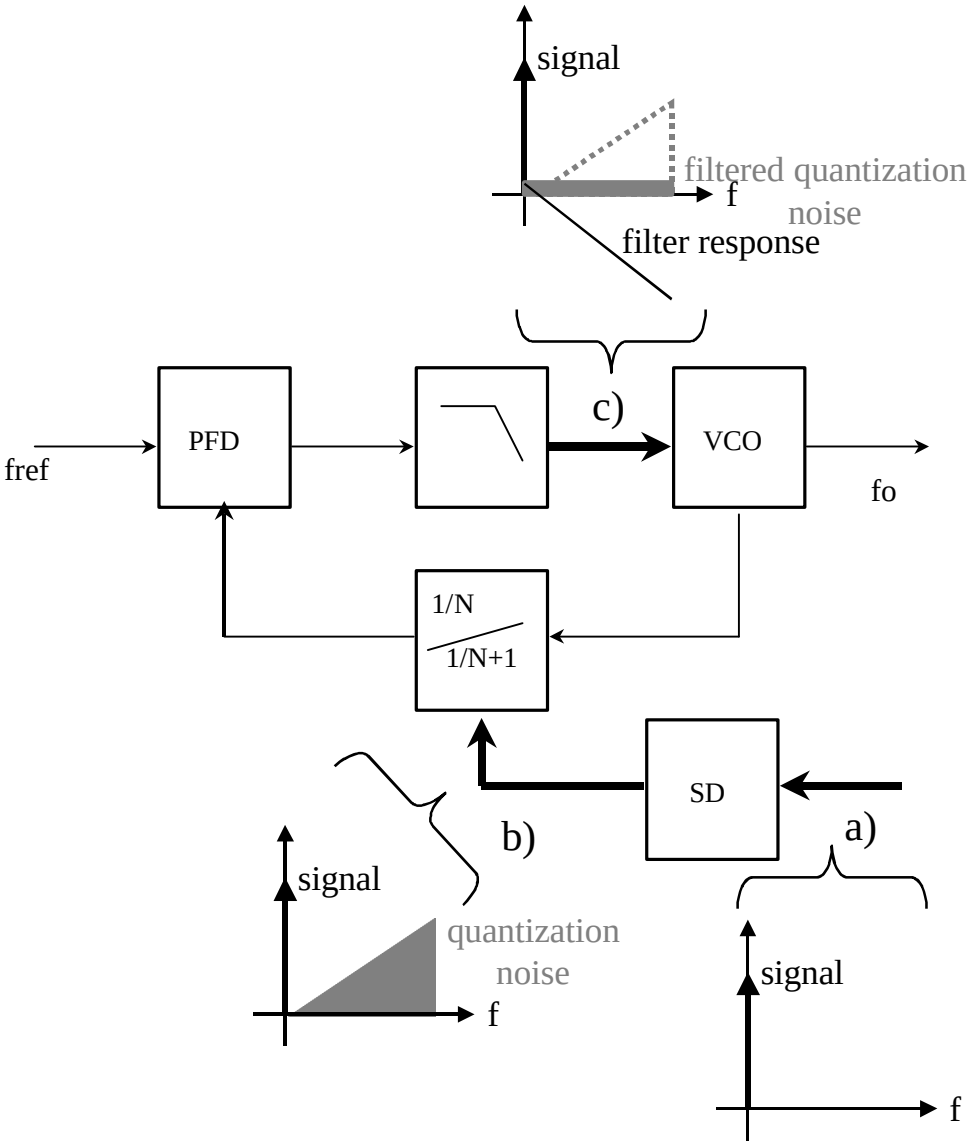

Fig. 18 Quantization noise in a sigma-delta Fractional-N synthesizer

To design a fractional-N PLL synthesizer, three parameters, including reference frequency, loop bandwidth, number of orders of the sigma-delta modulator, have to be

determined. These parameters mainly determine the switching speed, spurs and noise of the loop.

Quantization noise

Higher clock frequency (reference frequency of the phase-locked loop) and order of the sigma-delta modulator can force more noise at higher frequencies. Lower loop bandwidth can filter out more noise at high frequencies. For the phase noise requirement of –121dBc/Hz @ 600kHz offset, the required maximal loop bandwidths and minimal reference frequencies are shown in Fig. 19 for second, third and fourth-order sigma-delta modulators used. In this design, reference frequency of 25.6MHz and third-order sigma-delta modulator can provide maximal 300kHz loop bandwidth for the required phase noise performance. The reference frequency of 25.6Mhz is used because it can simplify the design of the modulator if the channel spacing (e.g. 200kHz in GSM) is the reference frequency divided by 2^N. Moreover, since the reference frequency is 25.6MHz, any spurs in the output of the frequency synthesizer will be multiple of 25.6MHz which is already located outside the receiver band. Only the out-of-band noise which is already attenuated a lot by the RF image rejection filter can be mixed down to IF by the spurs at 25.6MHz offset.

System parameters

The frequency synthesizer is designed for a GSM receiver. The phase noise requirements are –103dBc/Hz at 400KHz and –121dBc/Hz at 600KHz offset, respectively. The frequency range is 865-890MHz for a 70-MHz IF with 200KHz

resolution. The loop bandwidth is 80KHz. The whole synthesizer is operated with a single 1.5-V supply.

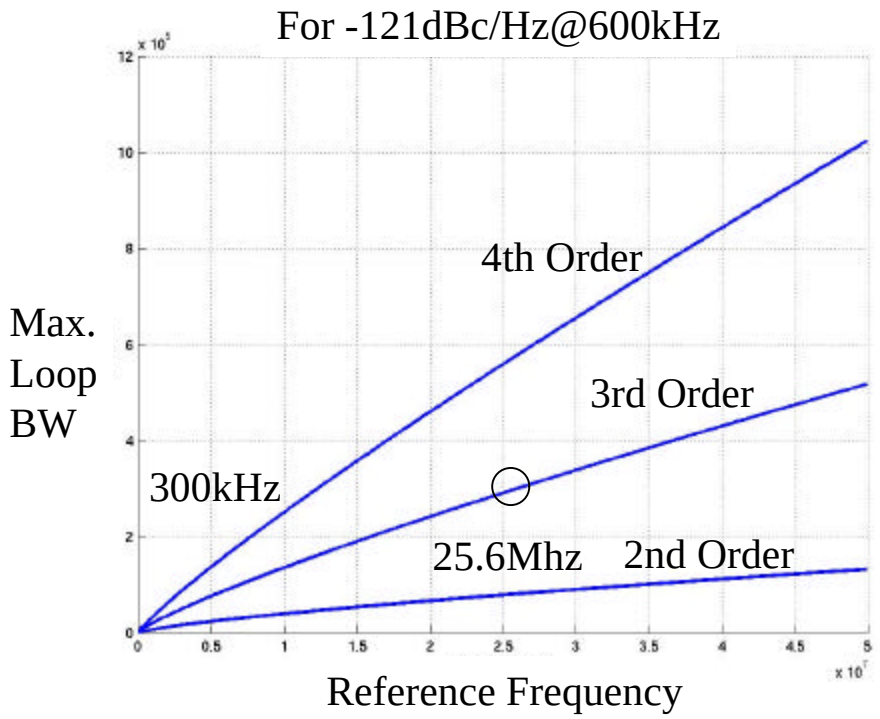

Fig. 19 Maximal loop bandwidths and minimal reference frequencies for second, third, fourth-order sigma-deltra modulators for phase noise requirement of –121dBc/Hz @ 600kHz offset

The complete system includes a fractional-N phase-locked loop synthesizer, and gain and offset adjustment circuits for the switchable-capacitor array as shown in Fig. 20. The PLL synthesizer includes a LC VCO with switchable-capacitor array, an improved loop filter, a charge-pump, a frequency-phase detector, a multi-modulus prescalar, and a third-order digital sigma-delta modulator.

The fractional-N phase-locked loop synthesizer is based on third-order sigma-delta fractional-N design with a 25.6-MHz reference frequency. The fractional-N synthesizer includes an integer-N phase-locked loop synthesizer and a digital sigma-delta modulator. Since a 25.6-MHz reference frequency and a prescalar with the division ratios from 32 to 39.5 are used, the output frequency range is from 25.6MHz x 32 =

819.2MHz to 25.6MHz x 39.5 = 1011.2MHz and the minimal frequency resolution is 25.6MHz x 0.5 = 12.8MHz. The 16 division ratios are controlled by a 4-bit digital signal. In order to generate the channels with a 200-kHz spacing, a digital sigma-delta modulator of at least 6 bits is needed because 12.8MHz / 2^6 = 200kHz. Each least significant bit of the 6-bit sigma-delta modulator represents a 0.5 / 2^6 in the division ratio of the prescalar. Including the four bits to directly control the prescalar, a 10-bit channel selection word is required to control the output frequency.

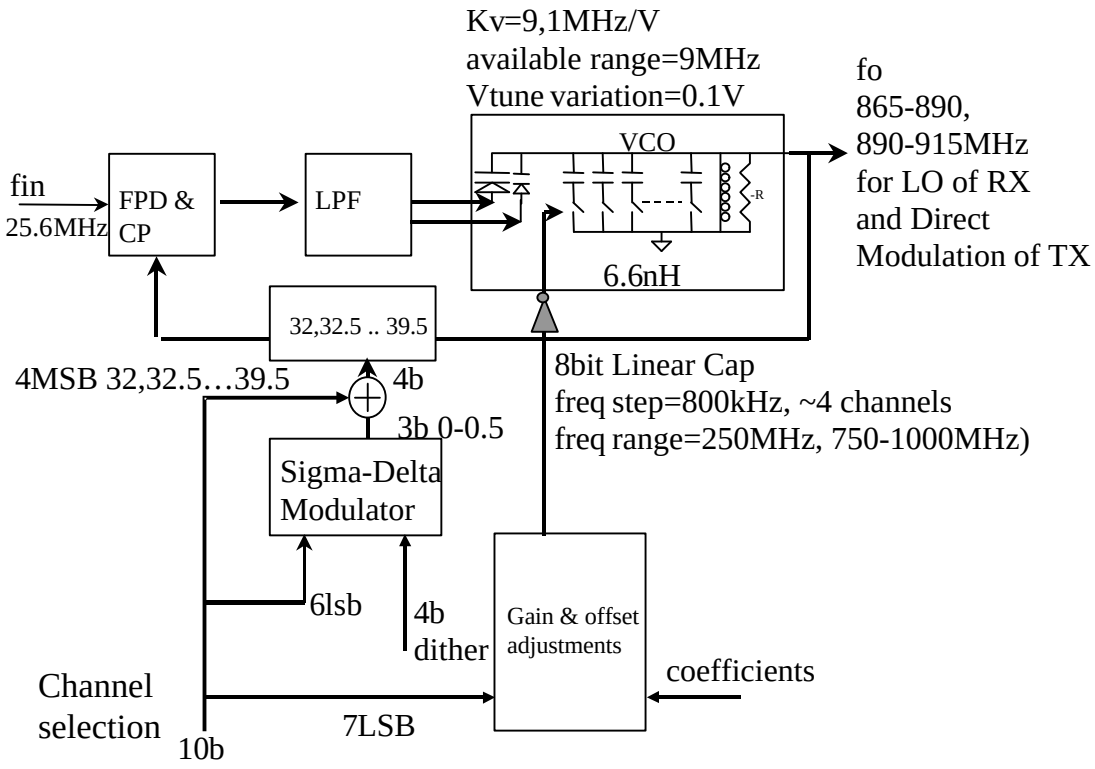

Fig. 20 Detailed system diagram of this design

Extra four bits added in the sigma-delta modulator are for the dither signal to random the input of the sigma-delta modulator in order to prevent the problem of pattern noise at the output of the sigma-delta modulator.

In a higher-order digital modulator, the output signal swing is larger than the available output value (it will be discussed more in Chapter 4). For a third-order modulator with

the output value between 0 and 0.5, the signal swing can be up to –1 and 2. Due to the extra signal swing required, the available division ratios will be reduced. As a result, this prescalar with extra division ratios is used. The minimum and maximum division ratios with this prescalar will become 32-(-1)=33 and 39.5-2+0.5=38 which corresponds to the output frequency 25.6MHz x 33 = 844.8MHz and 972.8MHz. The available output frequency range can still cover the required frequency range (865-915MHz) in both receiver and transmitter systems.

The lower seven bits of the channel selection word represents the 125 channels. These seven bits are used to control the switchable-capacitor array to obtain the correct output frequency. Since these seven bits only represent the channel number but not the exact frequency of the channel, a frequency offset is added to obtain the correct frequency for the channels. Moreover, the frequency change due to a change in the least significant bit in the switchable-capacitor array does not represent exactly a channel. A gain adjustment is required to relate the channel number and the corresponding number of the switchable capacitors.

A 8-bit switchable-capacitor array is used to provide around 300-MHz tuning range (from 800MHz to 1100MHz) and 800-kHz frequency step. The varactors in the voltage-controlled oscillator can provide about 9MHz/V. As a result, the tuning voltage of the varactors will vary within 0.1V.

Chapter 4 Circuit Implementation

Voltage-controlled oscillator

Quaduature LC oscillators

The voltage-controlled oscillator, as shown in Fig. 21, includes two identical differential LC oscillators which are mutually coupled by four coupling transistors to provide quadrature phase outputs[11]. The LC oscillator employs two-layer (metal 2 and metal 3) spiral inductors. Each oscillator contents an 8-bit switchable-capacitor-array as the main frequency tuning and two small varactors as the fine frequency tuning.

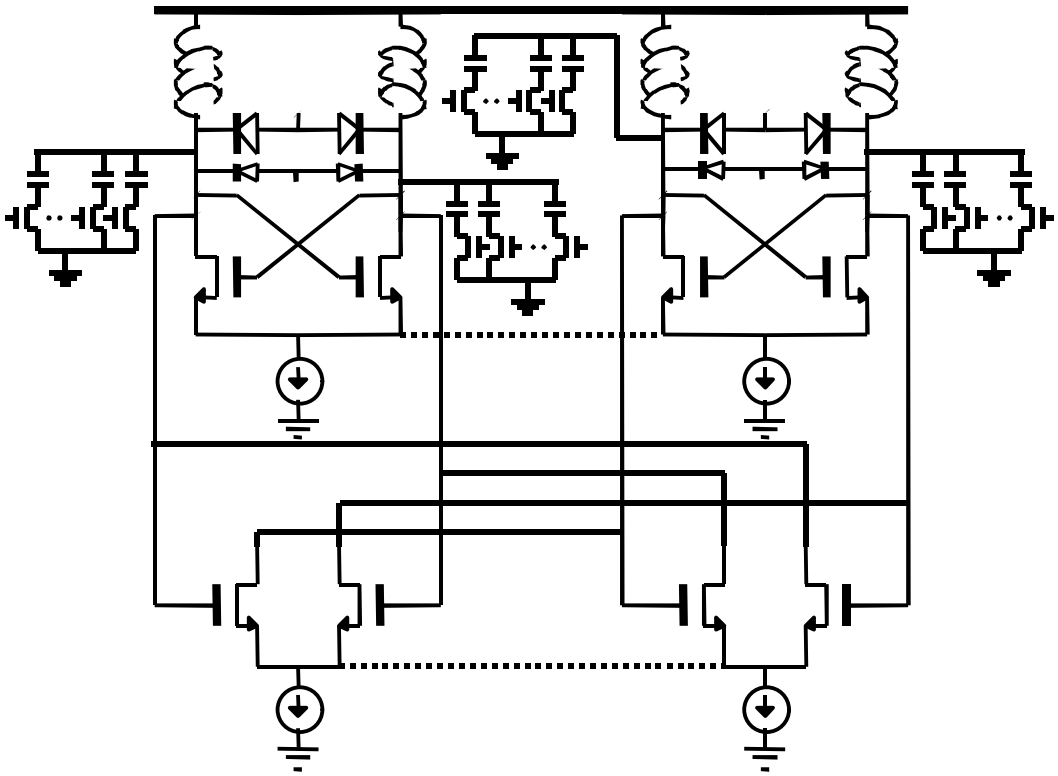

Fig. 21 The schematic diagram of the voltage-controlled oscillator with switchable-capacitor-array

The coupled-LC oscillators can be viewed as two LC oscillators put in a four-stage ring oscillators, as shown in Fig. 22. Each stage of the ring oscillator has a phase shift of 90 degrees. Inside this frame of the ring oscillator, the two LC oscillators will have a 90-degree phase difference between their outputs. As the noisy ring oscillator maintains the quadrature phases, the two LC oscillators maintain the purity of frequency. By sharing the current sources, both amplitude and phase matchings of the outputs of the two oscillators are even better maintained[12] (more discussions in the coupled-LC oscillators will be in Chapter 5).

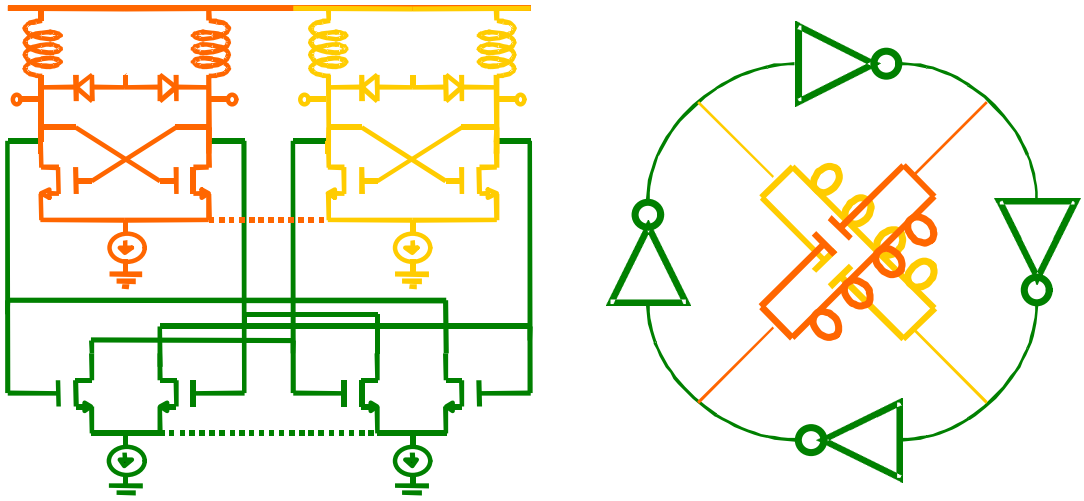

Fig. 22 Another view of coupled LC oscillators

Switchable-capacitor-array

The frequency of oscillator is mainly controlled by the switchable-capacitor array. The switchable-capacitor array is used to directly control the center frequency of the oscillator for fast switching between frequencies. It should also have a large tuning range to compensate the center frequency shift of the oscillator due to the process variation and inaccurate modeling. Moreover, it can reduce the required tuning range and gain of the varactors. The most important is that it should not degrade the overall performance compared to the case of using a varactor for tuning.

The finest tuning resolution by the switchable-capacitor array depends on the non-linearity of the relationship between the frequency and the capacitance. The relationship between the frequency and the capacitance of the switchable-capacitor array is governed by the simple relationship,

$$f = \frac{1}{\sqrt{LC}}$$

$$f + \Delta f = \frac{1}{\sqrt{L(C + \Delta C)}} = f\left(1 - \frac{1}{2}\frac{\Delta C}{C} + \frac{3}{8}\left(\frac{\Delta C}{C}\right)^2\right)$$

$$\frac{\Delta f}{f} = -\frac{1}{2}\frac{\Delta C}{C} + \frac{3}{8}\left(\frac{\Delta C}{C}\right)^2$$

As $\frac{\Delta f}{f} = \frac{25Mhz}{890Mhz}$,

$$\frac{\Delta C}{C} = -0.054$$

For convenience, we assume the change in frequency proportional to the change in capacitance. This assumption is valid because the relationship between the frequency and the capacitance is quite linear within a small range. In this case, a binary-weighted switchable-capacitor array can be used to change the oscillation frequency in a linear fashion.

The maximal frequency deviation between the actual frequency (the solid line in Fig. 23) and the linear approximation (the dashed line) occurs when half of the capacitors are turned on.

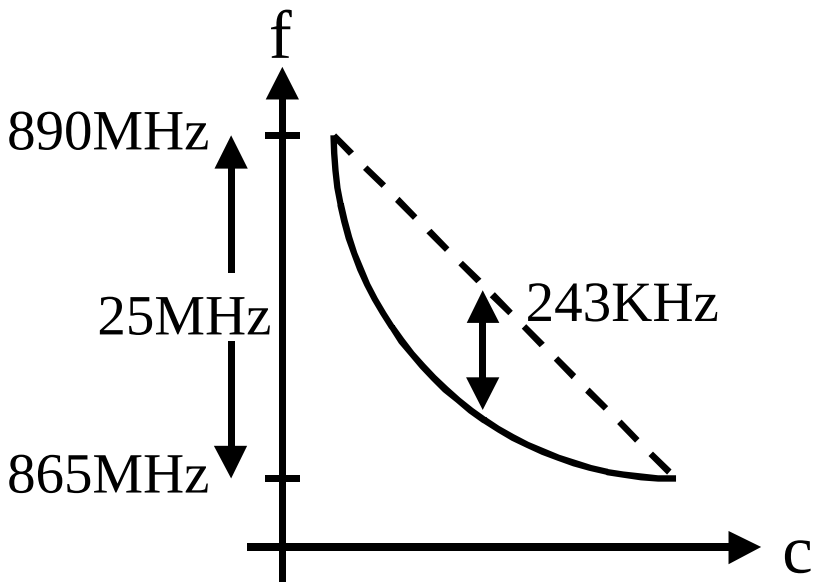

Fig. 23 Tuning curve of the oscillator by switchable-capacitor-array

As half of the capacitors in the array is turned on,

$$\frac{\Delta C}{C} = \frac{-0.054}{2} = -0.027$$

Maximal frequency deviation

$$= 12.5Mhz - f\left(-\frac{1}{2}\frac{\Delta C}{C} + \frac{3}{8}\left(\frac{\Delta C}{C}\right)^2\right)$$

$$= 12.5Mhz - 12.257Mhz$$

$$= 243Khz$$

The maximal frequency deviation due to the non-linear relationship between the frequency and the capacitance is 243KHz at the frequency around 890MHz. The frequency deviation is equivalent to around 1.2 channel of 200KHz. This deviation can be compensated by the change of the capacitance of the varactor when the loop is locked.

The finest tuning resolution also depends on the minimal size of the switchable capacitor. The switchable-capacitor-array employs linear capacitors and donut NMOS transistors as the switches, as shown in Fig. 24a. The donut transistor is used because of the smaller drain parasitic capacitance[13]. The switchable-capacitor-array includes a 7-bit binary-weighted array of unit switchable-capacitor and an extra half-size switchable-capacitor as the least significant bit. Totally, this 8-bit array can provide around 300MHz tuning range (from 800MHz to 1100MHz) and 800kHz frequency resolution which is equivalent to 4 frequency channel spacings. The available tuning range should be good enough to compensate the center frequency shift due to the process variation or the inaccurate modelings of the inductor and capacitors. Each of switchable-capacitors in the 7-bit binary-weighted array includes a 26.7fF linear capacitor and a 11.5u/0.5u donut transistor while the half-size switchable-capacitor includes a 14.3fF and a 8.5u/0.5u donut transistor. When the switches are off, there are about (2.8fF+2.8fF+3.95fF)=9.55fF and (1.5fF+1.9fF+2fF)=5.4fF remained in the normal-sized and half-sized unit switchable-capacitors due to the drain parasitic capacitance (Cd), the gate-to-drain overlap capacitance (Cov) and the Nwell-to-substrate capacitance of the linear capacitors (Cwell) respectively, as shown in Fig. 24c. The changes of capacitance are about 63% of the maximum value for both switchable-capacitors of different sizes. Higher resolution of the switchable-capacitor array is also possible by using smaller unit linear capacitors and switches. However, the increase in the parasitic capacitance will limit the overall tuning range of the array.

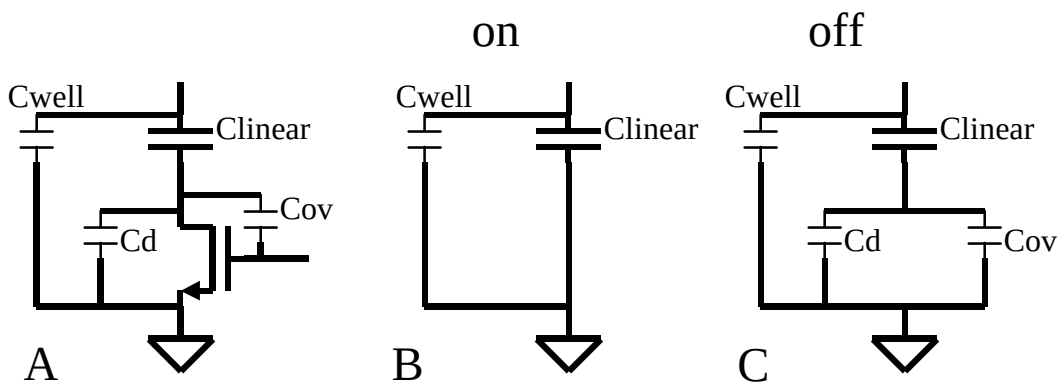

Fig. 24 Models of an unit switchable-capacitar (A) general case (B) turn-on (C) turn-off

The quality factor of the linear capacitor is very good (>50) because it is just a parallel plate capacitor with N+ active and silicide poly of low resistance as the two plates. The quality factor of the switchable-capacitor array is mainly limited by the turn-on resistance of the transistor. There is a trade-off between the quality factor and the tuning range of array because larger switches can reduce resistance but increase parasitic capacitance at the same time. For a 11.5u/0.5u NMOS switch, the turn-on resistance with a 1.5V supply is 340ohms. The quality factor of a turn-on switchable-capacitor is designed to be 19 which does not degrade the overall quality factor of the LC tank too much because it is about 5-10 times larger than the quality factor of the spiral inductor. Further increase of the quality factor of the switchable-capacitor array by increasing the switch size has little effect on the overall qualify factor, but the increase of the parasitic capacitance will reduce the available tuning range.

Varactor

As the minimal frequency resolution of the switchable-capacitor array is 800kHz, the small varactors have to provide the remaining 800kHz tuning. Since only very small tuning range is needed, the voltage-controlled oscillator with small gains of 9Mhz/V can already cover the whole range while the tuning voltages need to vary by only 0.1V

for 800KHz frequency deviation. The voltage-controlled oscillator is turned by the two varactors based on parasitic PN junction diode of P+ active and N-well, as shown in. There are totally 18 and 186 unit PN junction diodes for the two varactors. Each diode has around 2.1fF at 1V reverse bias and the capacitance changes around 15% per volt. Each diode also shares around 1.5fF Nwell-to-substrate parasitic capacitance which further reduces the tuning range of the varactor. The overall tuning range of the varactors is only about 9% per volt, from 0.74pF to 0.8pF.

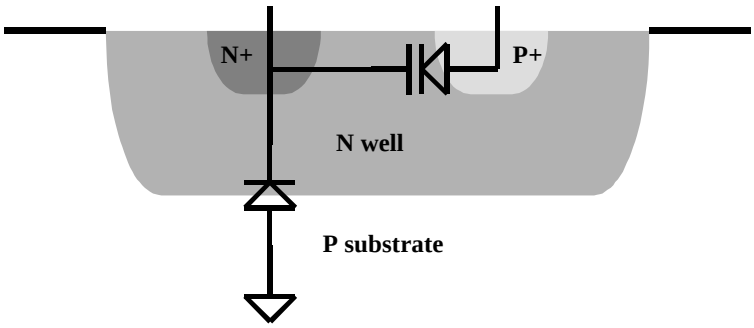

Fig. 25 Cross section of the parasitic PN junction varactor

This parasitic PN junction varactor has the quality factor of around 30 by minimizing the size of unit diode in the array. As the quality factor of the diode degrades a lot when the diode is forward-biased, the available biasing range of the diode is very limited as the cathode is connected to the large-swing output. However, it is not a problem in this design because the diode is always 1V reversed-biased with variation of only 0.1V.

Inductor

The inductors used are double-layer (Metal 3 and Metal 2) circular spiral inductors. The spiral inductor is designed and simulated by the ASITIC program [14]. The inductance is 6.6nH and the parallel parasitic capacitance is 0.6pF. However, since the program ignores loss due to the substrate eddy current, the quality factor of the inductor calculated by the program is totally incorrect. From previous trials, the quality factor of

spirals of similar sizes is around 2-2.5 which will dominate the overall quality factor of the whole LC tanks and limit the phase noise performance of the oscillator.

Phase noise performance

The phase noise of a LC oscillator can be calculated by the equation,

$$L(\Delta\omega) = \frac{kTR_s(1+A)\left(\frac{\omega_o}{\Delta\omega}\right)^2}{V^2/2}$$

where Rs is the equivalent series resistance of the LC tank, V is the oscillation amplitude and A is the excess noise factor of the oscillator. The phase noise depends on the power of the carrier ($V^2/2$), the noise power of the lossy resistance (kTRs), and the noise power of the compensation (kTRsA).

To determine the phase noise, the power of the carrier, the noise power of the lossy resistance, and the noise power of the compensation. The noise power due to the lossy resistance in the LC tanks depends on the resistance in the inductor and the varactor which is process-dependent. The carrier power (or the amplitude of oscillation) and the compensation can be calculated based on the criterion for oscillation. The simplest criterion for oscillation is:

"Loop gain is larger than one when 360^o phase shift."

In a most simple LC oscillator, as shown in Fig. 26, the criterion can be explained as follow:

"The product of Gm and Req is larger than one" where the Gm is the tranconductance to compensate the loss in the LC tank, and Req is the equivalent parallel resistance of LC tank at resonance. The product of Gm and Req is the loop gain at 360^o phase shift.

There is another theory of LC oscillator based on negative conductance to describe the oscillation. The criterion for oscillation ***is "The magnitude of the negative conductance Gm is larger than the positive conductance 1/Req"***.

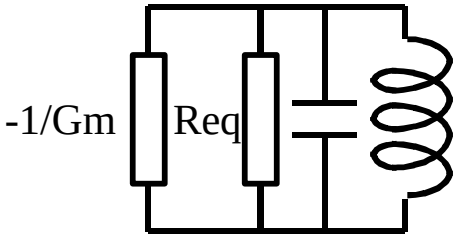

Fig. 26 Model of a simple LC oscillator

Both theories explains the oscillation but in different views. To apply these theories to determine the oscillation amplitude and the required compensation, a generalized criterion can be used – ***"The average product of Gm and Req is larger than one"*** or ***"The average magnitude negative conductance Gm is larger than the positive conductance 1/Req"***. The region where the criterion is true determines the oscillation amplitude. The graphical representations of the criterion in the two theories are shown in Fig. 27. Based on loop gain theory, the oscillation stops when the average loop gain is smaller than one. The amplitude of oscillation will be the voltage where the loop gain (Vout/Vin) cuts the line of unity slope. Based on negative conductance, the oscillation stops when the average negative conductance ($\int_0^V GmdV \big/ V$) is smaller than the reciprocal of the resistance (1/R). The voltage (Vin=Vout when oscillation) where the average negative conductance cuts the reciprocal of resistance is the oscillation amplitude. Although there are different loop gains and different negative conductance

in Fig. 27a and Fig. 27b, the same oscillation amplitude can be obtained if their average values within the oscillation range are the same. As the loop gain and the negative conductance are usually decreasing, the loop gain and the negative conductance at the center point have to be larger than 1 and 1/R in order to start the oscillation.

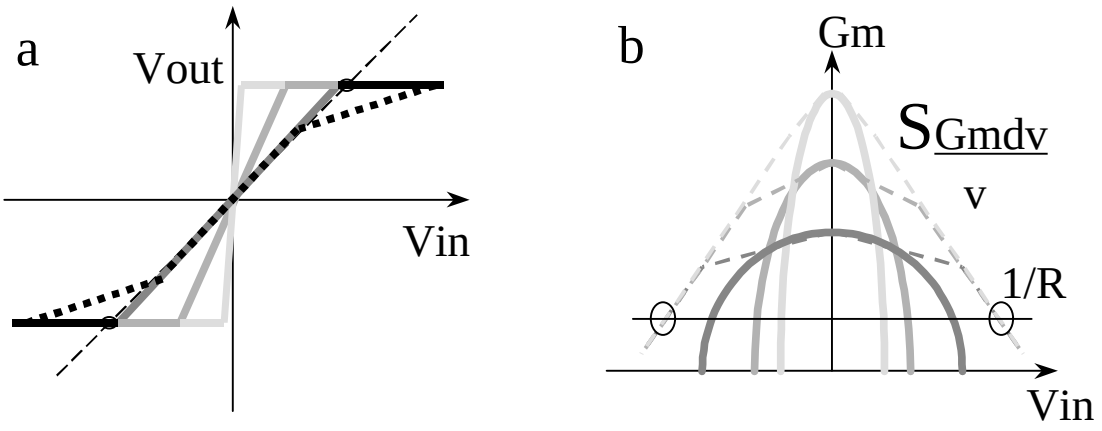

Fig. 27 Graphical representations of the generalized criterion for oscillation a) based on loop gain b) based on negative conductance

Surprisingly, in the most common differential LC oscillator shown in Fig. 28, the criteria results in a very simple relationship between the amplitude of oscillation and the bias current. ***"The single-ended peak-to-peak amplitude of oscillation is "usually" equal to the product of the tail current in a carefully designed oscillator and the equivalent parallel resistance of one of the LC tanks at resonance."*** Or the relationship can be called Ohm's law (V=IR). ***"The voltage at resonance frequency equals to the product of bias current and the equivalent resistance at resonance of the LC tank."***

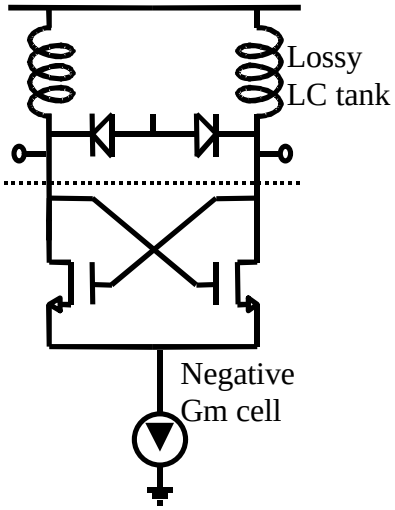

Fig. 28 Schematic diagram of an LC oscillator

The noise power due to the lossy resistance is proportional to kTRs, and the noise power of the compensation is proportional to kTRsA. The excess noise factor (A) is the ratio between the noise power generated by the compensation and the lossy resistance. Based on negative conductance theory, the average compensation should be equal to the loss of the resistance. The voltage noise power of a resistor is 4kTR. The voltage noise power of a MOS transistor is 4kTγ gdo where gdo is the channel conductance and γ is usually in between 2/3 and 1. Assuming γ is equal to one for simplicity and gdo is equal to gm when the transistor is in saturation region, the noise powers of the resistor and the compensation using transistors are the same. The excess noise factor (A) is equal to 1.

However, when the transistor is in linear region, gdo is proportional to the Vgs – Vt. The corresponding channel conductances (gdo) for different negative conductances (Gm) are shown in Fig. 29. Although all the negative conductances have the same average value and provide the same oscillation amplitude, the channel conductances are different and depend on the peak values of the negative conductances. As a result, excess noise factor (A) is approximately equal to the ratio between the peak negative

conductance (Gm) and the reciprocal of the resistance (1/R) if the amplitude of oscillation is not too large. If the amplitude of oscillation is larger, the excess noise factor will be even larger.

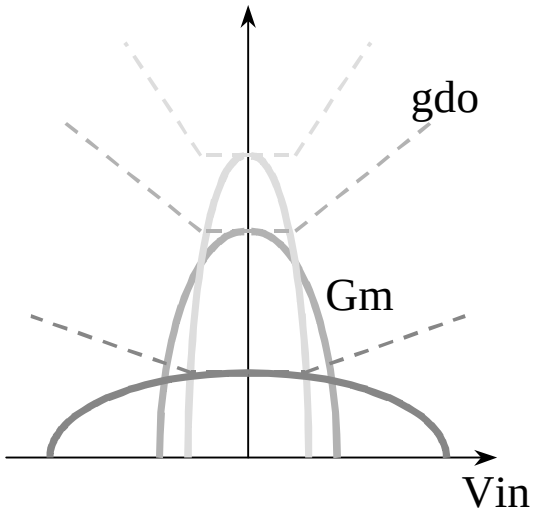

Fig. 29 gdo for different negative conductances

Since the oscillation amplitude only depends on the tail current of the negative Gm cell and the parallel equivalent resistance, by designing a Gm cell with the smallest peak Gm will give the best phase noise performance. The Gm should be always a bit larger than 1/R within the oscillation range. This can be done by using the transistors with a small W/L ratio to implement the negative Gm cell. However, since the negative Gm is just a bit larger than the 1/R. When the loss of the LC tanks is larger due to incorrect modeling of the inductor or varactor, the oscillator cannot oscillate. For example, as shown in Fig. 30, for an oscillator with optimal W/L transistors, if the loss is double, then four times of the original current is needed to compensate the loss. It is because the peak tranconductance of the transistor is proportional to the square root of the current. As a result, at least four times of the original current is required for the double compensation and provide an unexpected double amplitude. However, if the designed negative conductance has a larger peak value, only double of current are need to

compensate the double loss and provide the same oscillation amplitude. To design the negative conductance cell, there is a trade-off between the phase noise performance and the freedom to use.

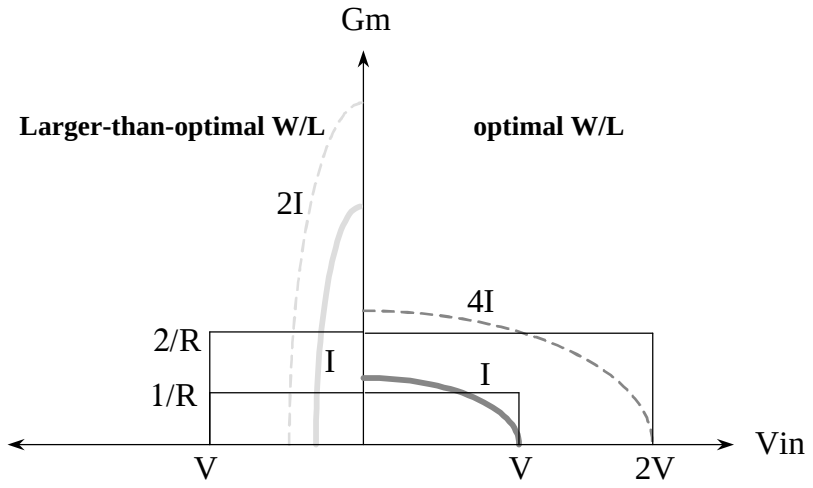

Fig. 30 Transconductance vs input voltage of transistors of different W/L ratios

Since in this design, the spiral inductor limits the overall quality factor of the LC tank, the equivalent series resistance of the inductor is Rs which is about 15ohms for the 6.6nH inductor with the quality factor 2.5. To improve the phase noise, we can increase the amplitude of oscillation. However, in this differential LC design, the transistors will be in deeply linear region if the differential amplitude is much larger than Vt about 0.7V. The small output resistance of the transistors in linear region will degrade the quality factor of the LC tank. Therefore, the differential oscillation amplitude is designed to be 0.8V in this case. The excess noise factor A is the ratio between the noise generated from the tranconductance for compensating the loss due to the resistance of the LC tank and the noise generated from the resistance itself. To ensure the oscillation can start, the compensation is designed to be about twice of the required. In the case, the excess noise factor is about 2 to ensure the startup of oscillation.

Then the phase noise of a LC oscillator is,

$$L(600KHz) = \frac{0.0259 \times 1.6 \times 10^{-19} \times (2 \times 15) \times (1+2)\left(\frac{900M}{600KHz}\right)^2}{0.8^2/2} = -116dBc/Hz$$

However, due to two LC oscillators are used and coupled, the noise power is averaged and reduced by half. Then the overall phase noise is –119dBc/Hz

Novel idea of zero excess noise factor

The criterion for a stable oscillation is that the average negative Gm is larger than the reciprocal of the resistance. Usually, as the loop gain and the negative conductance are decreasing, the loop gain and the negative conductance at the center point have to be larger than 1 and 1/R respectively in order to start the oscillation. However, if some methods are used to start the oscillation, it is not necessary to have a large loop gain or negative conductance at the center point.

For example, the LC oscillator shown in Fig. 31a, two voltage sources are used to shift down the voltage applied to the gates of the two transistors. In this case, the transistors are only turned on when the drain voltages are very large. The corresponding negative conductance provides by the transistors is shown in Fig. 31b (solid line). Instead of a decreasing negative conductance in other normal Gm cells (dashed lines), the negative conductance increases when the voltage is large. If the areas under the curves of the negative conductances in these different Gm cells are the same, the same oscillation amplitude can be obtained.

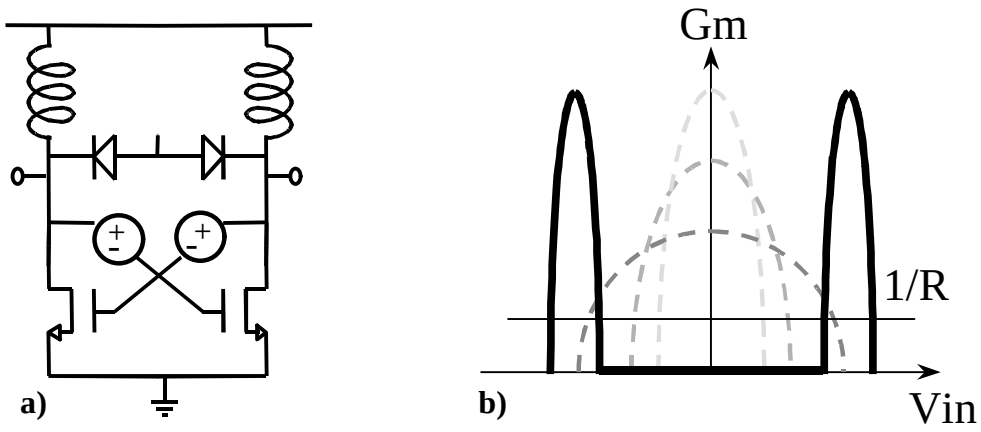

Fig. 31 a) Proposed LC oscillator and b) the corresponding Gm

The resultant channel conductance Gdo is shown in Fig. 32. Since the transistors in the proposed design are turned on only when the voltage is large, there is no channel conductance at the center compared to the normal case. To relate the thermal noise due to the channel conductance to the phase noise of the oscillator, impulse sensitivity function can be used [15]. The idea of the impulse sensitivity function is that the voltage noise can only change the phase of the oscillation during the voltage is in transition. Therefore, the function has a maximum at the center point and is zero at the peak amplitude. The product of the noise power from the channel conductance and the impulse sensitivity function gives the phase noise contribution function shown in Fig. 34. Due to the absence of noise power at the central range in the proposed Gm cell, the total phase noise contribution is much lower than the normal designs. In this proposed design, the gain and the noise are shifted to the two ends. The available gain can still keep the same oscillation but the noise is now located at some regions which is not important to phase noise. If the gain is two impulses located at the two ends, it is possible to have zero excess noise factor due to the zero impulse sensitivity function there. As a result, half of the phase noise can be reduced. This novel proposal of a LC oscillator is still under investigation and some more analysis will be done.

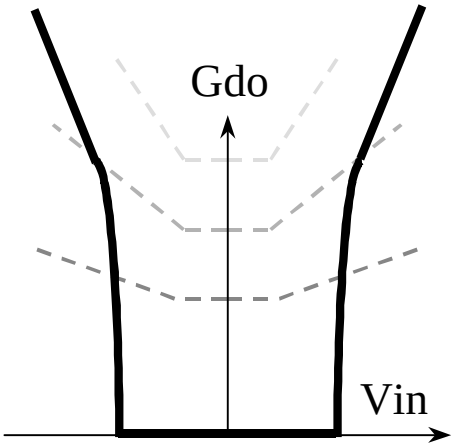

Fig. 32 Gdo of the proposed LC oscillator

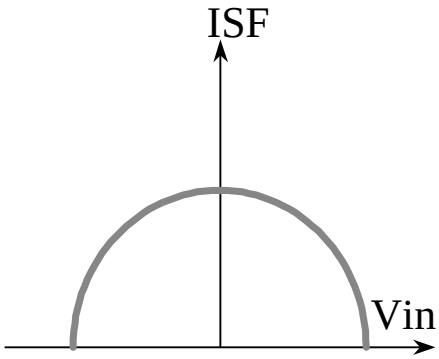

Fig. 33 Impulse sensitivity function

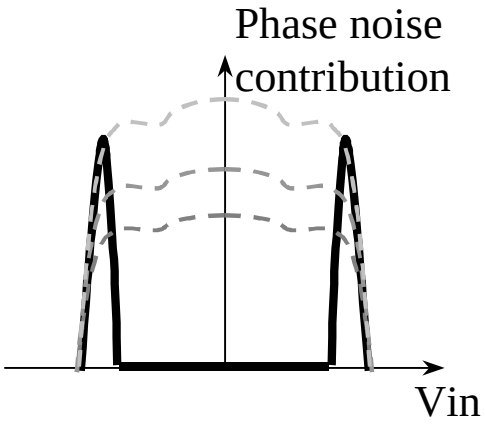

Fig. 34 Phase contribution of the proposed oscillator

Loop filter

Dual-path filter

In a type-2 PLL, a zero in the open loop transfer function is required to maintain the loop stability. It can be implemented by a resistor in series with a capacitor in the feedback path of a active filter, as shown in Fig. 35a. However, the resultant capacitor Cz will be too large (a few nF) because of the large ratio between the Cz and Cp. As Cp is determined by the noise requirement, Cz will become very large due to the large ratio to Cp. Another way to implement the required zero with smaller capacitors with a dual-path filter[2]. By adding the outputs of a integrator and a low pass filter, as shown in Fig. 35b and Fig. 36, the zero is formed. In this case, there is no dependency between the Cz and Cp, both of them can take the minimal value for the required noise contribution.

Dual-path filter based on capacitance domain operation

Similar to the case of adding predicted offset from the switchable-capacitor array, this addition can also be done in capacitance domain. Instead of using a voltage adder which consumes power and generates noise to add the voltages, the two voltages are added by directly controlling two weighted varactors in the oscillator, as shown in Fig. 35c. As a result, the summation is implemented in capacitance domain as two capacitors are in parallel. When the loop is locked, the output of the integrator is constant and no net current from the charge pumps. The DC voltage generated by the low-pass filter is always zero and it cannot provide any tuning range from the varactor. Therefore, we can use an even smaller varactor for the path of the low-pass filter. In this case, the varactors used for the two paths of the integrator and low-pass filter have the gain of 9MHz/V and 0.9MHz/V respectively.

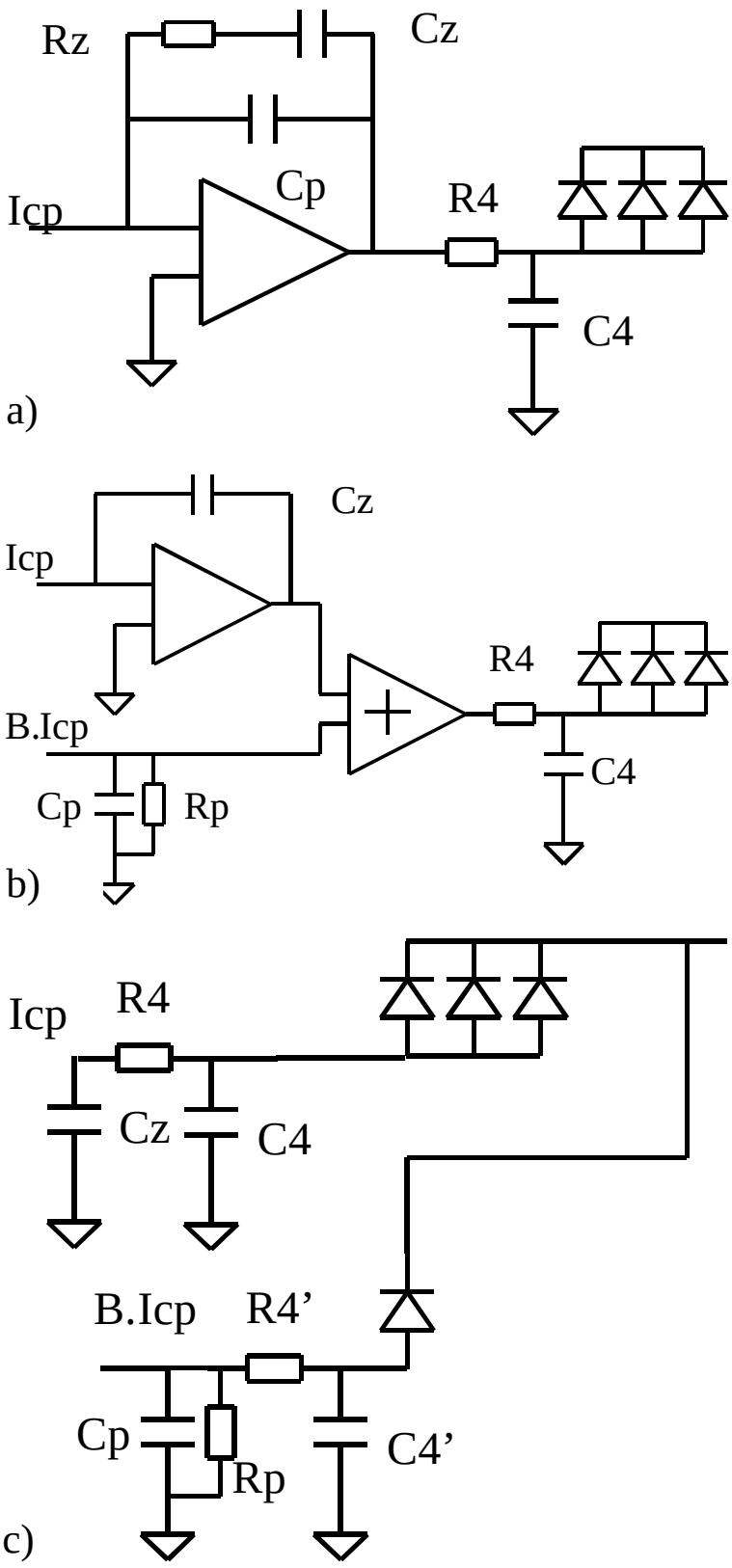

Fig. 35 Evolution of the loop filter – a) simple active filter b) dual-path filter by adding the outputs of the integrator and LPF with a voltage adder; c) dual-path filter by adding the outputs in capacitance domain

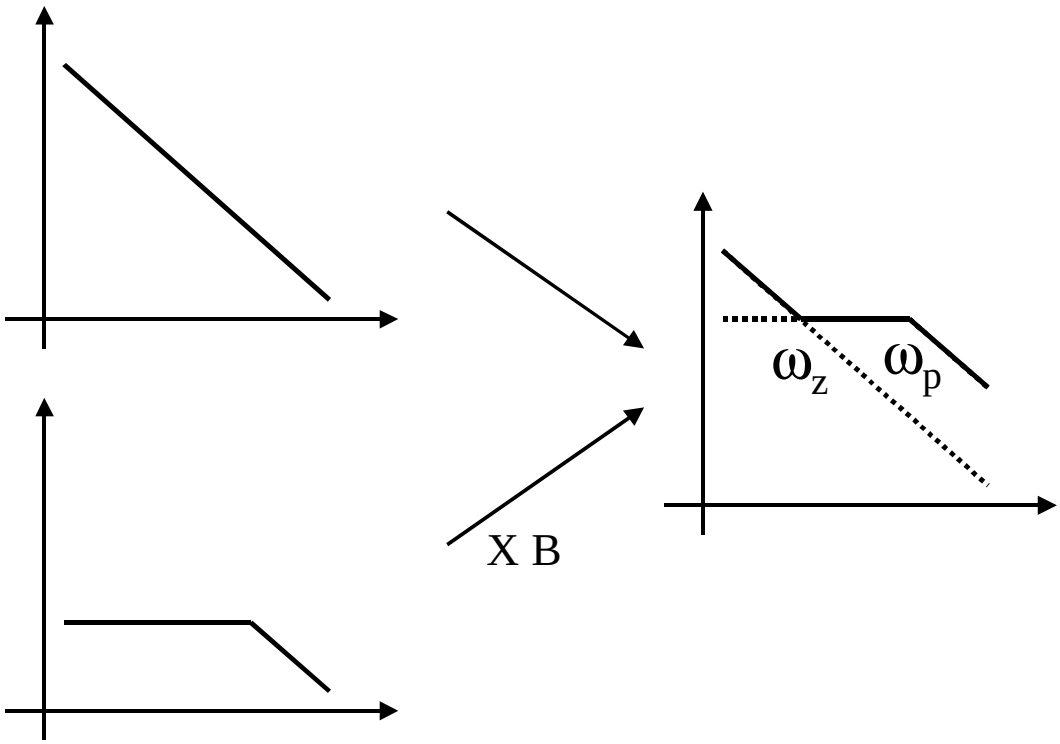

Fig. 36 Dual-path loop filter principle

Noise from the filter can modulate the voltage-controlled oscillator to generate phase noise. However, since most of the frequency tuning is done by the switchable-capacitor array, the required gain and tuning range of the varactors are very small. Due to the small varactors in the oscillator used, less noise from filter and charge-pump is converted into phase noise of VCO. Thus, larger resistance and smaller capacitors can be used in the filter.

In this proposed filter, the path of the integrator which can provide frequency tuning and the path of the low-pass filter are separate. An even smaller varactor can be used with the low-pass filter path. As a result, even more noise can be tolerated in this path and much smaller capacitors can be used there. This proposed filter design can further reduce the required capacitors by almost half.

Usually, capacitors in the filter occupy most of the chip area or even have to be off-chip. However, due to the use of switchable-capacitor array and the proposed dual-path filter, the resultant total capacitance occupies less than 10% of the core area of the synthesizer. For 80kHz loop bandwidth, the parameters of the filter is summarized as the following:

Table 2 Summary of filter parameters

Cz	54pF
R4	24.7kohms
C4	67.5pF
Cp	2.25pF
Rp	740kohms
R4’	247kohms
C4’	6.75pF
Icp	2.9uA
B.Icp	29uA

In order to use the frequency synthesizer as a GSM transmitter, the required loop bandwidth has to be at least 200kHz. However, a larger bandwidth will let much more noise to the voltage-controlled oscillator and much larger capacitors are needed to filter out the noise. For example, in a second-order low-pass filter, 200-kHz bandwidth (which is 2.5 times of 80kHz) requires about 39 times of the original capacitor (2.5^4 = 39.0625). Due to the capacitors occurring too much area for the 200-kHz loop bandwidth, a smaller loop bandwidth is used to demonstrate the idea of direct-modulated transmitter.

Implementation

In this design, all capacitors are implemented by linear capacitors. Silicide-blocked poly is used to implement most of the resistors while NMOS transistors are used to implement the largest resistor, as shown in Fig. 37. This non-linear resistor by NMOS transistors can be used because of the small variation of the tuning voltage. This resistor is designed to be the largest and the loop gain is the largest in the normal operation region, 0.55V, as shown in Fig. 38. The 1/gm of the upper transistor will become smaller if input is smaller than 0.55V while the 1/gm of the lower diode-connected transistor will become smaller if input is larger than 0.55V. This can guarantee the stability of the loop even out of the normal operation region.

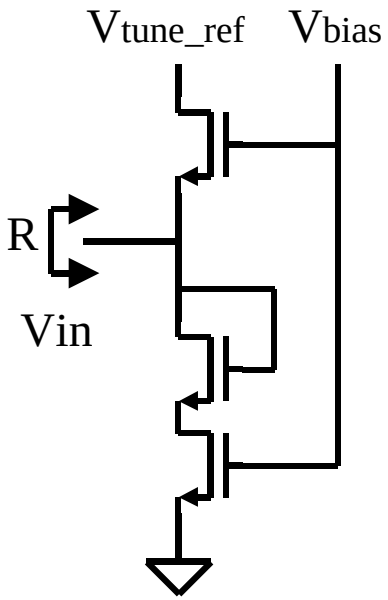

Fig. 37 Schematic of the largest resistor implemented by NMOS transistors

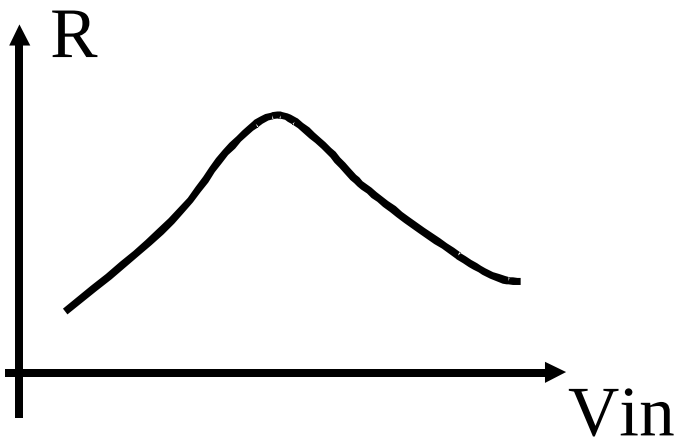

Fig. 38 Resistance of NMOS resistor vs. input voltage

Charge pump

In order to provide the two paths with different gains, two charge-pumps of different sizes used. The charge-pumps are simple current steering charge-pumps with transistor switches in saturation region for large output impedance. The output voltage range of the charge-pumps can be very small because of the nearly constant tuning voltage of the VCO, around 0.55V. In order to maintain the switches in the charge-pumps in saturation region, around 1V is needed to turn on the NMOS switches. Usually a resistive potential divider can generate the required 1V for the switches. However, since a resistive potential divider requires small impedance for fast switching, it consumes a lot of DC power. A simple switch capacitor driving stage, as shown in Fig. 40, is designed to drive the saturated transistor switches. When the input is high, all the NMOS switches are turned on and discharge all the capacitors to zero. When the input is low, the PMOS switch is turned on and charge up the two capacitors in serial. Due to the ratio between the two capacitors, when the upper electrode of the upper capacitor is charged to 1.5V, the middle point between the two capacitors will become 1V. This

capacitive potential divider can quickly switch to the required voltage from the reset state without consuming any DC power.

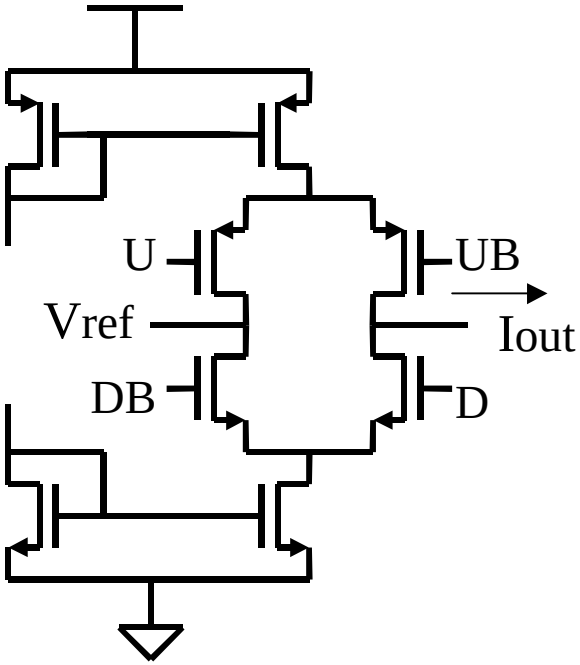

Fig. 39 Schematic of current steering charge-pump

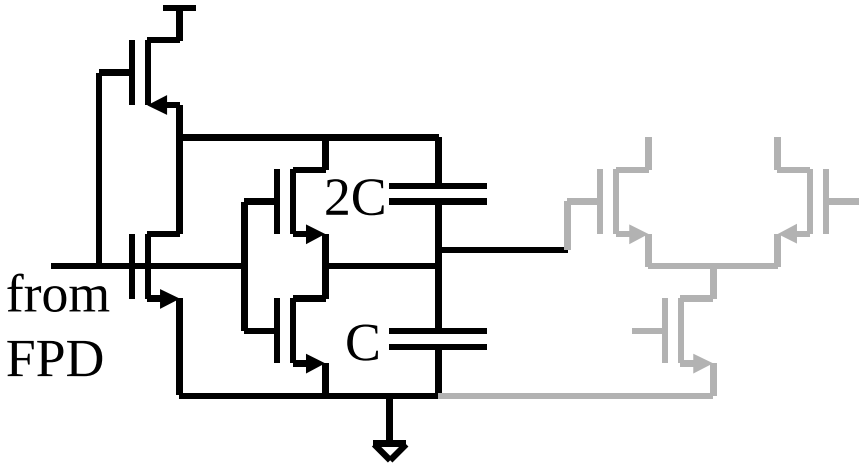

Fig. 40 Schematic diagram of the current steering charge-pump (pump-down current branch only) and the switch capacitor driving stage

Frequency-phase detector

A traditional frequency phase detector implemented by two D-type flip-flops and a NOR gate , as shown in Fig. 41, is used. A slow NOR gate provides delay in the

feedback path to prevent the problem of dead zone. A true-single-phase-logic D-type flip-flop[16], as shown in Fig. 42, is used because of the simple design. Since the input of the D-type flip-flop is always connected to high, the first stage of the true-single-phase-logic D-type flip-flop is omitted. A chain of inverters is used to generate a pair of matched differential signals to drive the differential inputs of the current steering charge pumps.

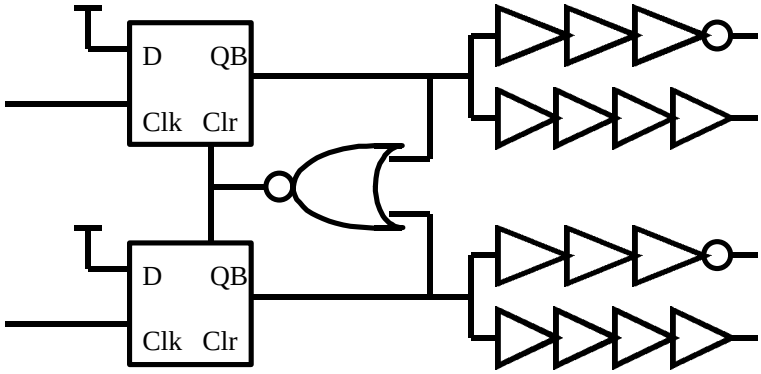

Fig. 41 Schematic of frequency phase detector

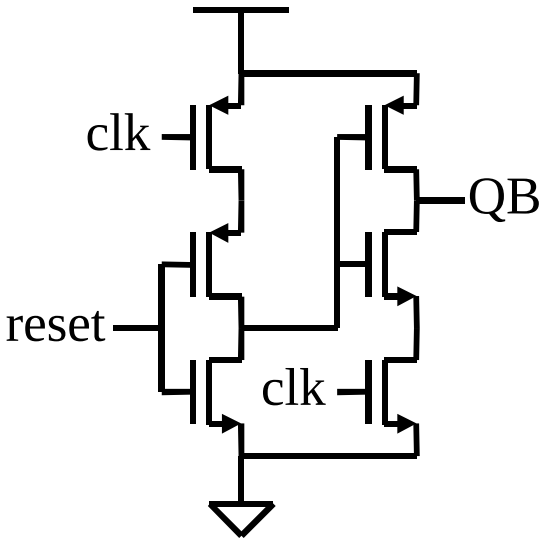

Fig. 42 Schematic of simplified TSPL D F/F

Gain and offset adjustment for the switchable-capacitor-array

Specification

The switchable-capacitor-array is controlled by the channel selection word with gain and offset adjustments, as shown in Fig. 20. The offset adjustment is used to compensate the center frequency shift due to the process variation and the inaccurate modeling of the passive components. The gain adjustment is used to compensate the variation of the gain of the switchable-capacitor array due to the process variation and the different gains in different frequency ranges. The gain and offset adjustments are only digital multiplier and adder. They can be also implemented as a few extra lines of codes in DSP chip. The self-calibration of the gain and offset adjustments can be done by monitoring the tuning voltage of the VCO using a simple voltage comparator. It can be done once at the most beginning or occasionally during operation by a simple finite state machine or DSP codes. The calibration criterion is to maintain the tuning voltage of the voltage-controlled oscillator to be around 0.55V.

Due to the finite resolution in digital multiplier, the gain adjustment is not perfect. As shown in Fig. 21, the maximal frequency deviation due to the finite gain resolution is the product of the frequency range (25Mz) and half of the minimal gain resolution.

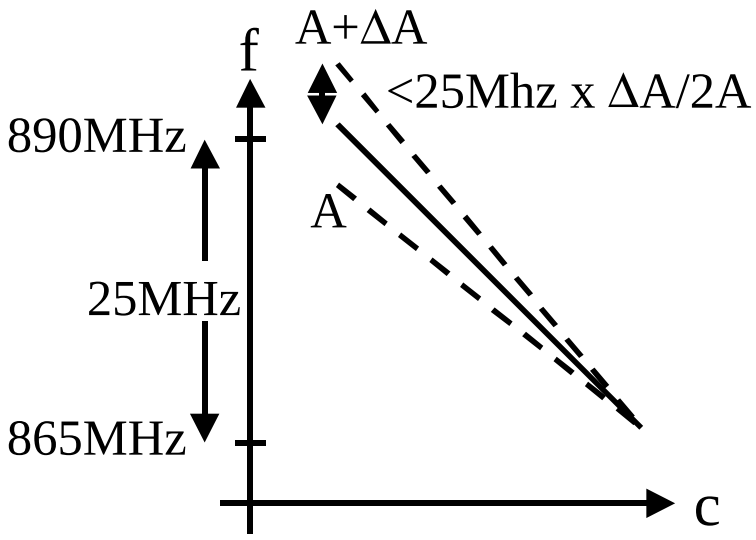

Fig. 43 Tuning curve by switchable-capacitor-array with gain adjustment of finite resolution

By using a digital multiplier with the minimal resolution of 1/16, the maximal frequency error due to the imperfect gain compensation is 781kHz. To avoid the deviation of the value of the unit switchable capacitor in the array due to process variation, a 6-bit multiplier is used to provide the gain adjustment from $\frac{1}{16}$ to $3\frac{15}{16}$.

Circuits

Due to the complexity of a digital multiplier proportional the product of the numbers of bits of the two inputs, an extra adder is added before the multiplier, as shown in Fig. 44, to reduce the number of bits of one input of the multiplier from 7 bits to 5 bits. The first adder is used to subtract the channel selection word, which is also the input of the prescalar and sigma delta modulator, to be the information of the channel number only (from channel 0 to channel 124). Since the switchable-capacitor array has the minimal resolution about 4 channels, only the group number of four channels (group 0-3, 4-7, …) will go into the gain adjustment. After the gain adjustment, a 8-bit frequency offset is added to adjust the center frequency within the 300MHz tuning range. Finally,

inverters are needed to invert all the signals to the switchable-capacitor array because the frequency reduces as the capacitors are turned on.

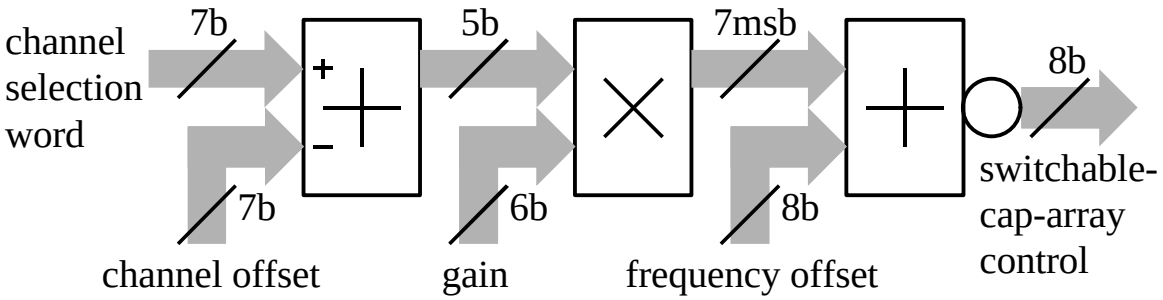

Fig. 44 gain and offset adjustments for the switchable-capacitor-array control

Prescalar

Architecture

A prescalar with division rate of 32, 32.5 … 39.5 is used for the fractional-N synthesizer. The input frequency is around 900MHz and the output is always 25.6MHz when the loop is locked. The prescalar is a cascade of a high speed divide-by-2,2.5,3,2.5 multi-modulus divider, two divide-by-2,3 dual-modulus dividers and two divide-by-2 dividers. Based on the combinations of the inner status of the prescalar, the dividers are controlled to provide the overall division ratio from 32 to 39.5 with 0.5 step size.

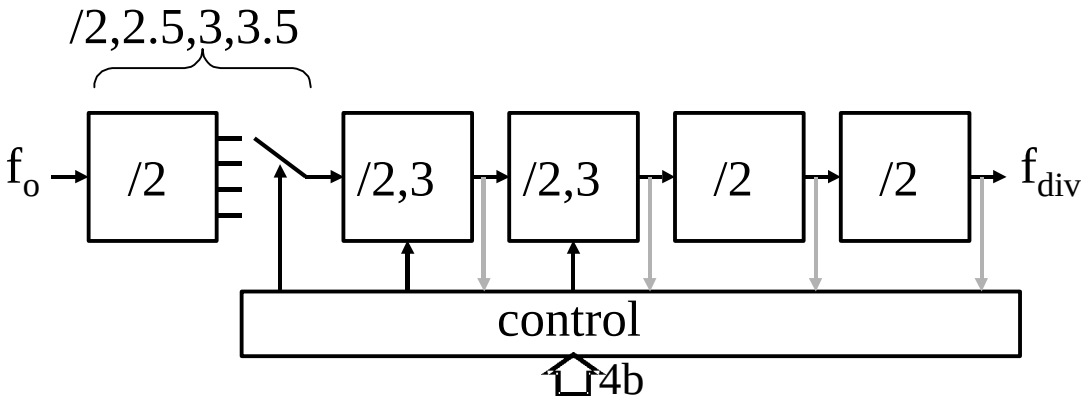

Fig. 45 System diagram of the multi-modulus prescalar

High-speed multi-modulus divider

The high-speed multi-modulus divider is based on phase selection design[2, 6], as shown in Fig. 46. By selecting the four phase outputs of a divide-by-2 divider, the different division ratio from 2 to 3.5 can be obtained. The time diagram in Fig. 47 shows that if the output of 90^o phase lag is selected in the next cycle, +0.5 in the division ratio is obtained. In this way, selecting the outputs of 90^o, 180^o, 270^o phase lag in the next cycle can provide the division ratio of 2.5, 3, 3.5 respectively, while staying in the current output can provide the division ratio of 2.

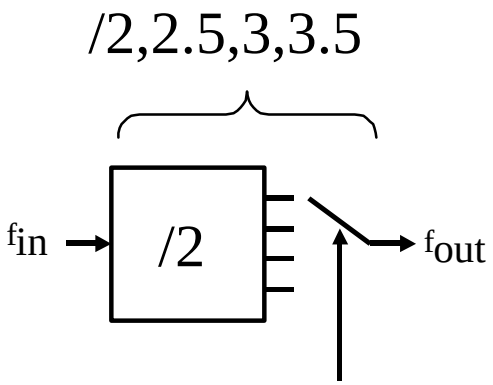

Fig. 46 Schematic of high speed divide-by-2,2.5,3,3.5 multi-modulus divider

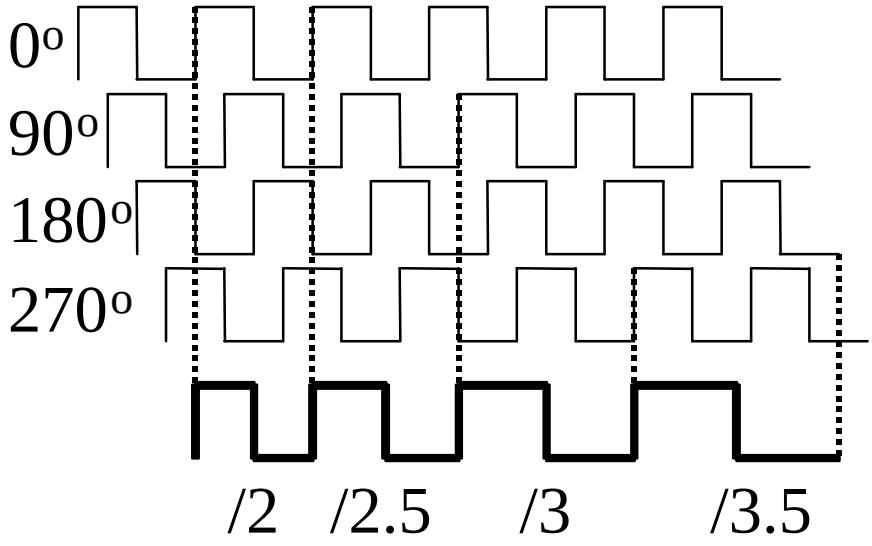

Fig. 47 Timing diagram of the high-speed divide-by-2,2.5,3,3.5 multi-modulus divider

The high-speed divide-by-2 divider is driven by the voltage-controlled oscillator output. Since the input DC level of the divider and the output DC level of the voltage-controlled oscillator are not matched, the input of the divider is AC-coupled from the output of the voltage-controlled oscillator and biased by external voltage reference by the circuit in Fig. 48. The circuit includes two linear capacitors and two NMOS transistors in linear region as large resistors.

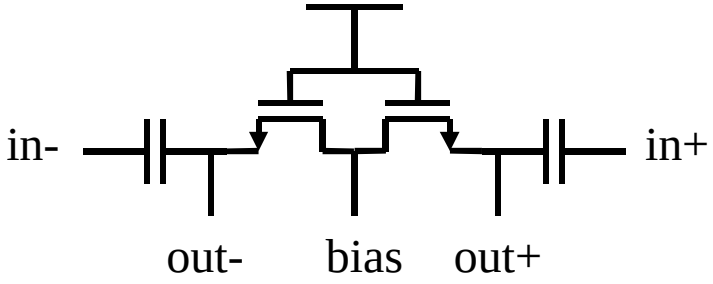

Fig. 48 AC couple and biasing for the input of the prescalar

The divider is a loop of two D-type latches clocked by a pair of complementary clocks, as shown in Fig. 49. The high-speed D-type latches have full swing output and can provide a robust performance. Except the clock inputs, all the transistors in the latch are NMOS without any stacking, as shown in Fig. 50 to increase the speed of operation. Once the clock input is low, the latch will store the input value.

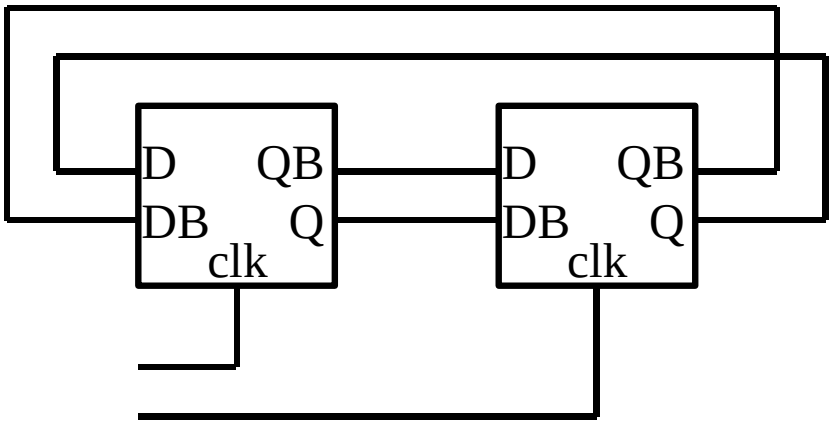

Fig. 49 Schematic diagram of the high speed divide-by-2 divider

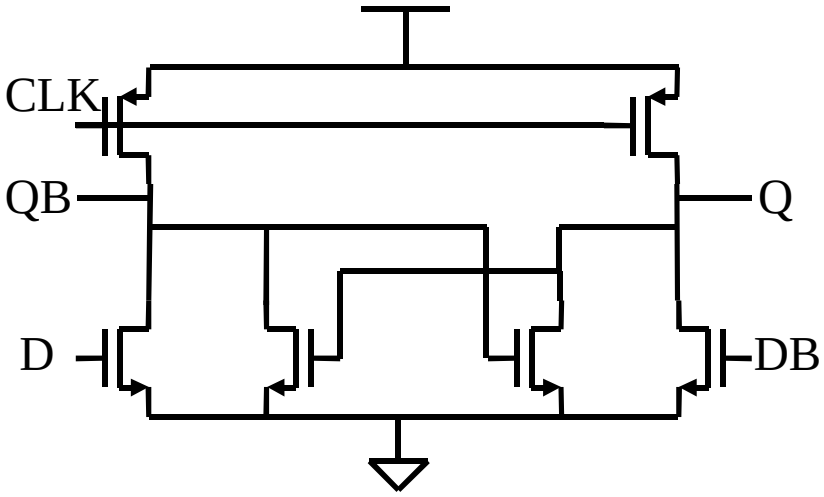

Fig. 50 Schematic diagram of the high speed D latch

Phase select circuit

The phase select is done by AND-OR gate array, as shown in Fig. 51. The inverted output from the divider will apply to the OR gate with its select signal. If the select signal is low, the phase is selected and passed to the output through the wired AND gate. For high-speed operation, all logic gates are pseudo-NMOS design. In Fig. 52, a) the pseudo-NMOS inverter a) inverts the input and pass the output to b) the pseudo-NMOS OR gate and all the outputs of the OR gate will be connected to a common pull-high NMOS to form c) a wired-AND gate.

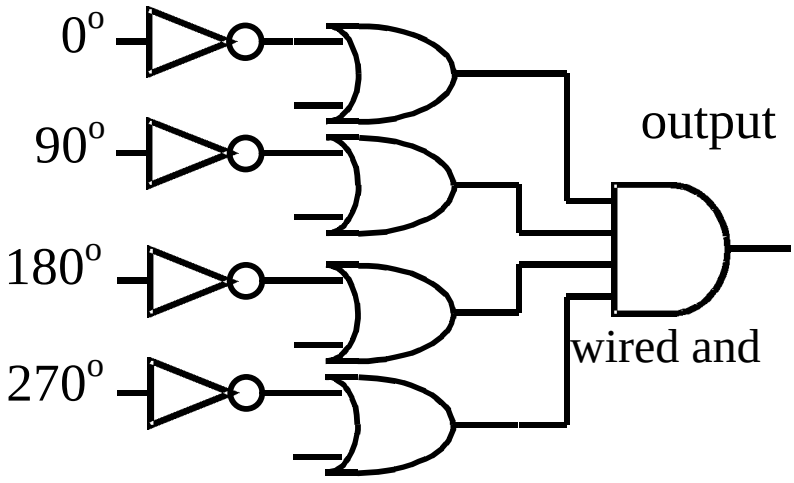

Fig. 51 Schematic of the phase select circuit

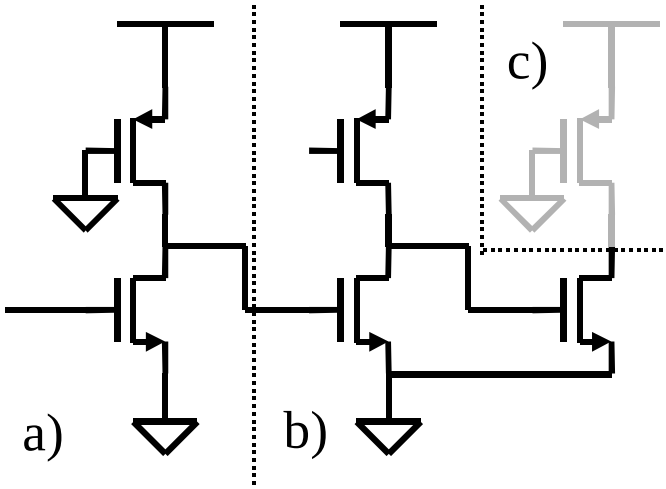

Fig. 52 Schematic of the pseudo-NMOS a) inverter, b) OR gate, c) wired-AND gate

Low-speed dual-modulus dividers

The low-speed divide-by-2, 3 dual-modulus dividers are based on the common configuration, as shown in Fig. 53. The divider includes two D-type flip-flops, two AND gates and some inverters. True-single-phase-logic D-type flip-flop is used because of the simplicity. The AND gate is also embedded in the D-type flip-flop as shown in Fig. 54.

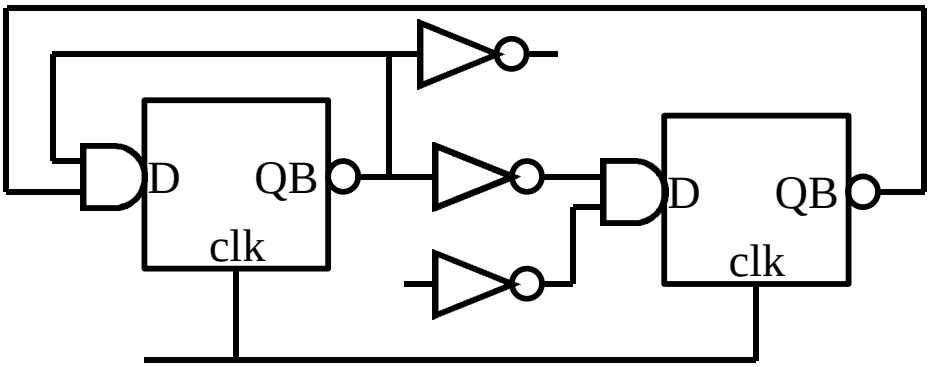

Fig. 53 Schematic diagram of the dual-modulus divider

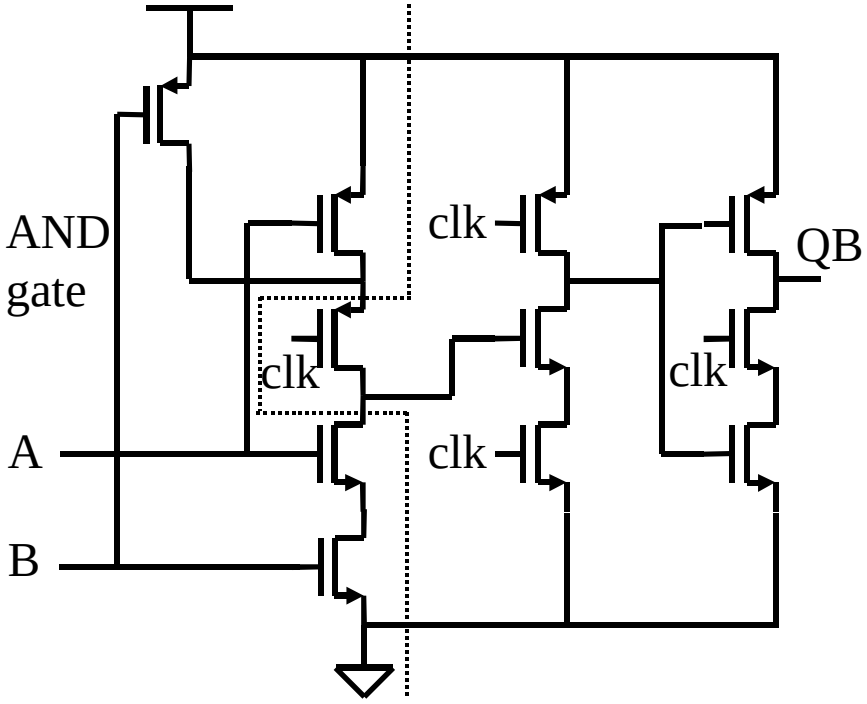

Fig. 54 Schematic diagram of the TSP D F/F with AND gate embedded

Low speed divide-by-2 divider

Shown in Fig. 55 and Fig. 56, a true-single-phase-logic D-type flip-flop with the inverted output feedback to its input forms the divide-by-2 divider.

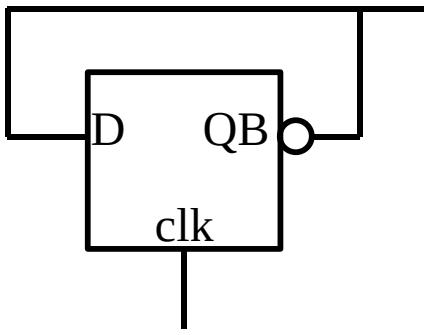

Fig. 55 Schematic diagram of the low speed divide-by-two divider

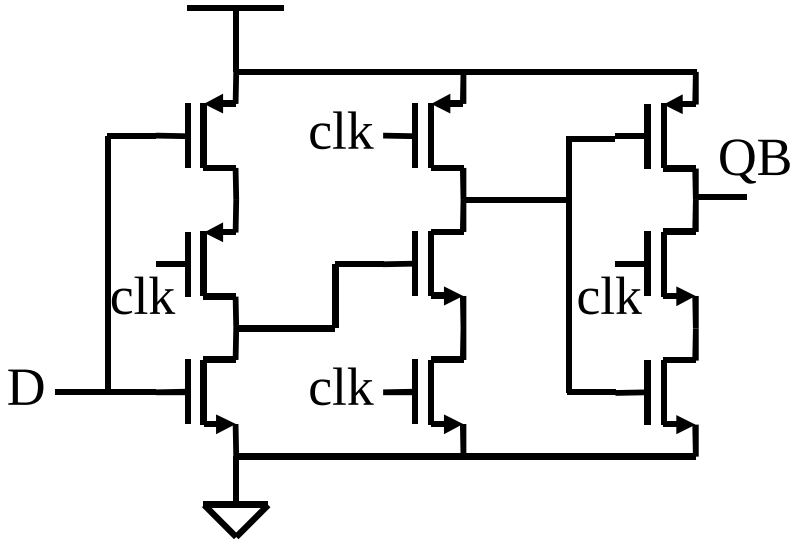

Fig. 56 Schematic diagram of the TSP D F/F

Control logic

Based on the combination of the inner status of the prescalar and the 4-bit modulus select input, the control logic controls the multi-modulus and dual-modulus dividers to perform the required overall division ratio. Some combination logics are used to determine the events for changing the modulus of the dividers by checking the combination of the internal status and the modulus select input. The outputs of the combination logics directly control the two dual-modulus dividers. Since the outputs of different phases have to be selected sequentially in order to have different modulus, a divide-by-4 divider is used to shift the output phase, as shown in Fig. 57. The divide-by-4 divider is implemented by four D-type latches as in Fig. 57. However, due to the possible silent input to the divide-by-4 divider, static D-type latches as shown in Fig. 58 have to be used.

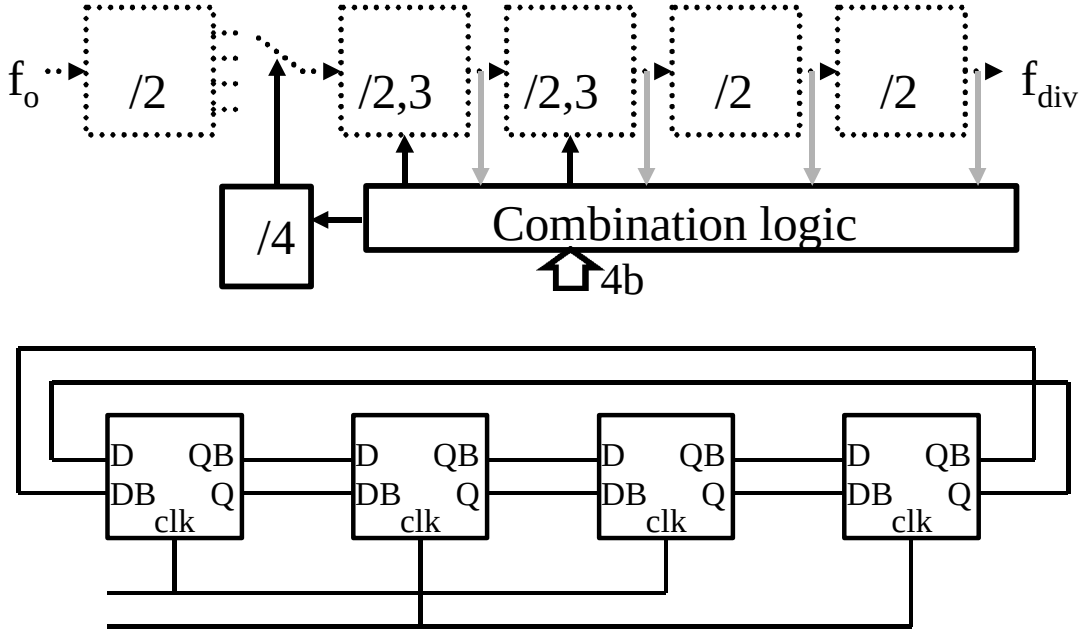

Fig. 57 Schematic diagram of the state machine of the phase select

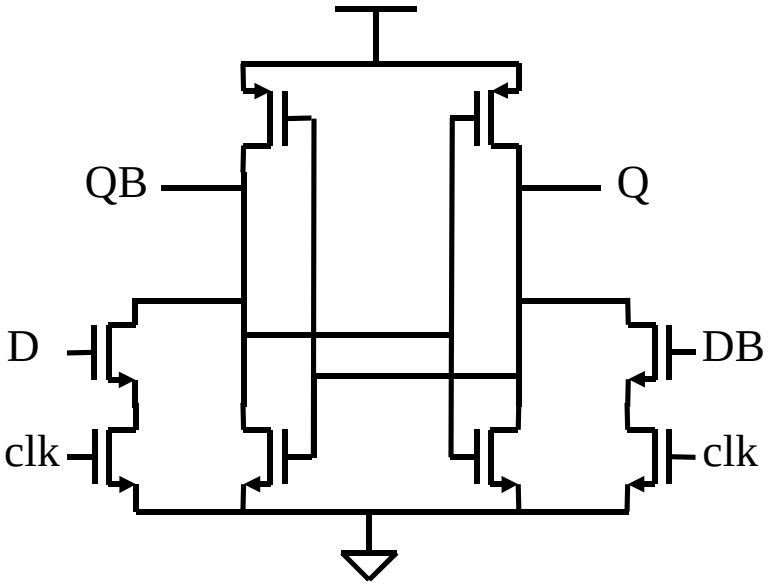

Fig. 58 Schematic diagram of the static D latch

Sigma-Delta Modulator

Architecture

A 10-bit digital third-order sigma-delta modulator is used to generate the outputs with the average value between zeros and one with the minimal resolution of $1/2^{10}$ and some third-order high-pass quantization noise. The output of the sigma-delta modulator will

control the multi-modulus prescalar. In this case, the multi-modulus prescalar with step size of 0.5 can have the average division ratio from 32 to 39.5 with the minimal step size of 0.5 x $1/2^{10}$. For a 25.6Mhz reference frequency used, the output frequency of the synthesizer can have the minimal frequency resolution of 25.6Mhz x $1/2^{11}$ = 12.5kHz.

There are different ways to implement high-order sigma-delta modulators such as high-order loop modulators and cascade-type modulator. High-order modulators can suffer from the problem of instability while cascades of first-order modulators are always stable. Both high-order loop and cascade-type modulators have the same problem that the difference between input and output range. As the number of orders increases, the high-order loop modulators will have decreasing input range while the cascade-type modulators will have increasing output range. In high-order loop modulators, since the signal range of the feedback signal increases as it passes through high-order digital filter, the input range decreases. In cascade-type modulators, the output range will increase as the output has to pass through high-order digital filter. A summary of the input and output ranges for different numbers of orders in both modulators is shown in Table 3.

Table 3 Summary of input and output ranges of high-order loop and cascade-type modulators

	High-order loop		*Cascade type*	
No. of orders	*Input range*	*Output range (no. of bits)*	*Input range*	*Output range (no. of bits)*
1	*1*	*1 (1b)*	*1*	*1 (1b)*
2	*½*	*1 (1b)*	*1*	*2 (2b)*
3	*¼*	*1 (1b)*	*1*	*4 (3b)*

MESH-3 Sigma-Delta modulator

In this design, a third-order cascade-type (MESH-3) modulator is used. It is a cascade of three first-order modulators with the quantization error of each stage as the input of

next stage, as shown in the Fig. 59. The outputs of the three stages will pass through some filters and be added together. For the three stages, their outputs will be the delayed version of their input and first-order high-pass quantization noise. For the input x, the outputs of the three stages are as the following:

$y= z^{-1} x+(1-z^{-1})e$ (first stage)

$y'= z^{-1} e+(1-z^{-1})e'$ (second stage)

$y''= z^{-1} e+ z^{-1}(1-z^{-1})e'+(1-z^{-1})e''$ (three stage)

By adding the filtered outputs of the three stages,

$z^{-2} y+ z^{-1}(1- z^{-1})y'+(1- z^{-1})^{2} y''$

$= z^{-3} x+(1- z^{-1})^{3} e''$

All of the quantization noise except the third-order high-pass filtered noise from the third stage will be cancelled. The final output will be the delayed version of the input x and the third-order high-pass quantization noise.

To implement the required first-order sigma-delta modulator, a digital adder and a D-type flip-flip can be used. The digital adder and the flip-flop form a digital accumulator, as in Fig. 60. The input of the adder is the input of the modulator, the carry-out of the accumulator is the output, and the accumulated value is the quantization error. To explain it, firstly, the digital adder can be modeled as Fig. 61a. It is normally an adder. However, since the adder will be overflow in the sum is too large, it will only provide

the residue and the carry-out signal in this case. Based on this, the accumulator can be modeled as Fig. 61b which has a delay at the residue output and the delayed residue is feedback to the input. Without affecting the performance, we can add an extra delay at the carry-out externally. Then we can shift the delays to the output of the adder, as shown in Fig. 61c. Finally, the feedback path splits into two and the accumulator becomes exactly the same as the first-order modulator, by comparing the model in Fig. 59 and Fig. 61d.

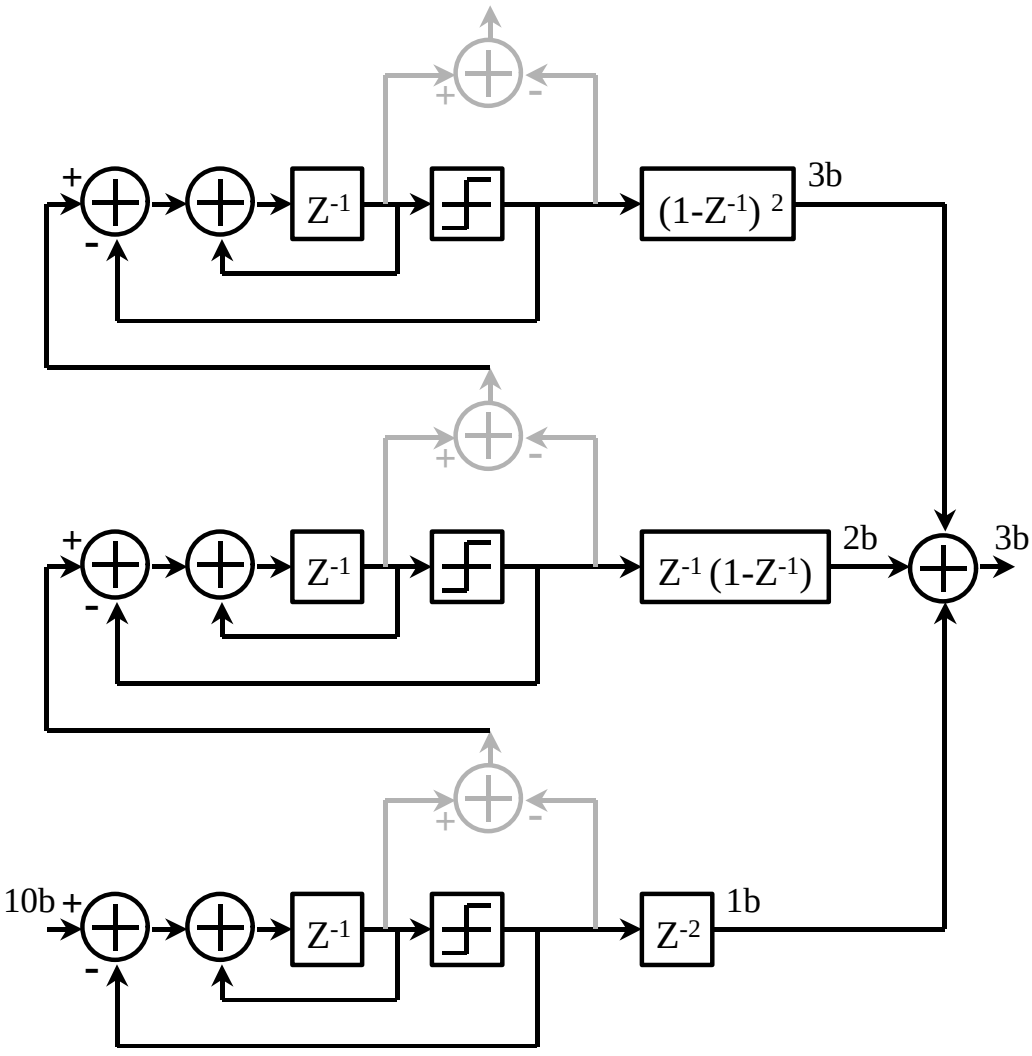

Fig. 59 System diagram of MESH-3 Sigma-Delta modulator

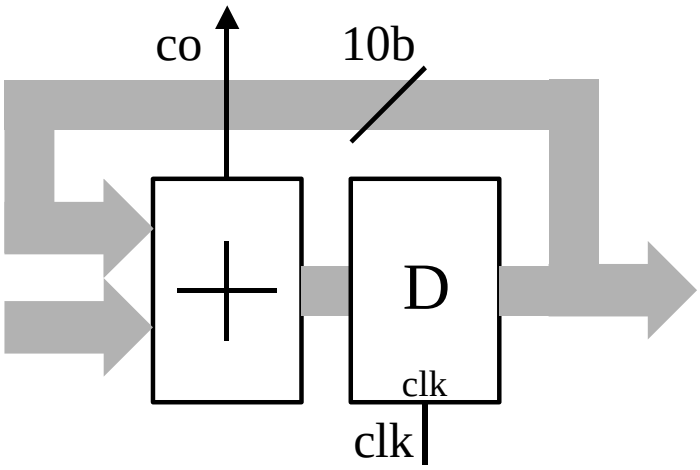

Fig. 60 Schematic of the accumulator

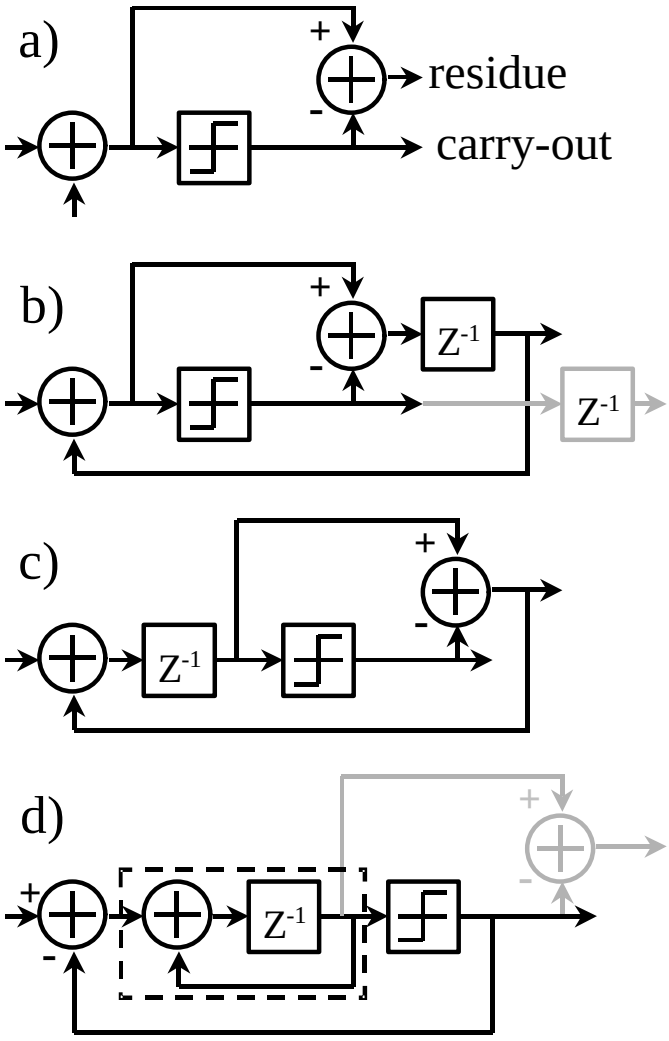

Fig. 61 Evolution of the digital accumulator a) System diagram of a digital adder b-d) Different views of system diagram of a digital accumulator

The schematic of the MESH-3 modulator is shown in Fig. 62. Three 10-bit digital accumulators connected in serial and the carry-out outputs are passed into the quantization noise cancellation circuit which filters the outputs and add them together. The output of the MESH-3 modulator will be 3-bit output represented the input fractional number with third-order high-pass quantization noise. However, to prevent the problem of pattern noise, a dither generator is used to generate dither signal. The dither signal is added to the input and randomizes the input.

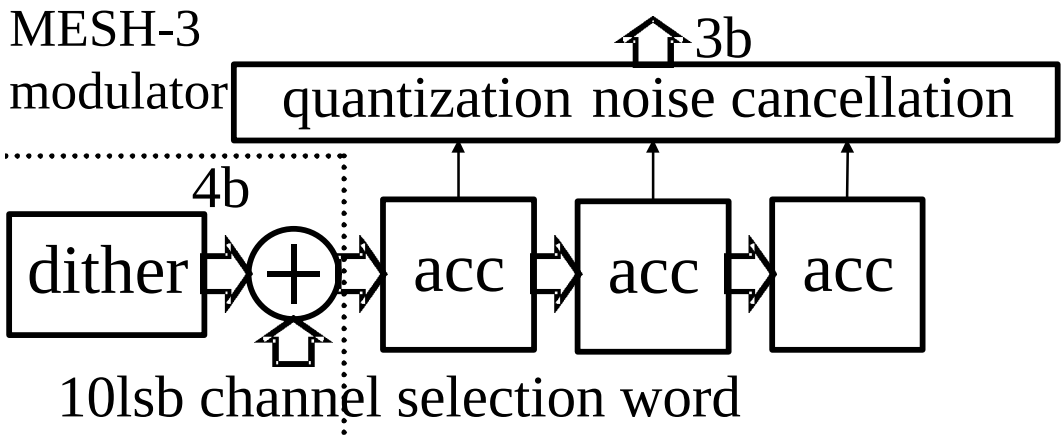

Fig. 62 Schematic of the 3-order digital Sigma-Delta modulator with a dither input

The quantization noise cancellation includes some digital filter and the adder to sum the outputs of the three first-order modulators. The digital filter can be implemented by adders and D-type flip-flop as the delay Z^{-1}. Then the quantization noise cancellation circuit is shown in Fig. 63.

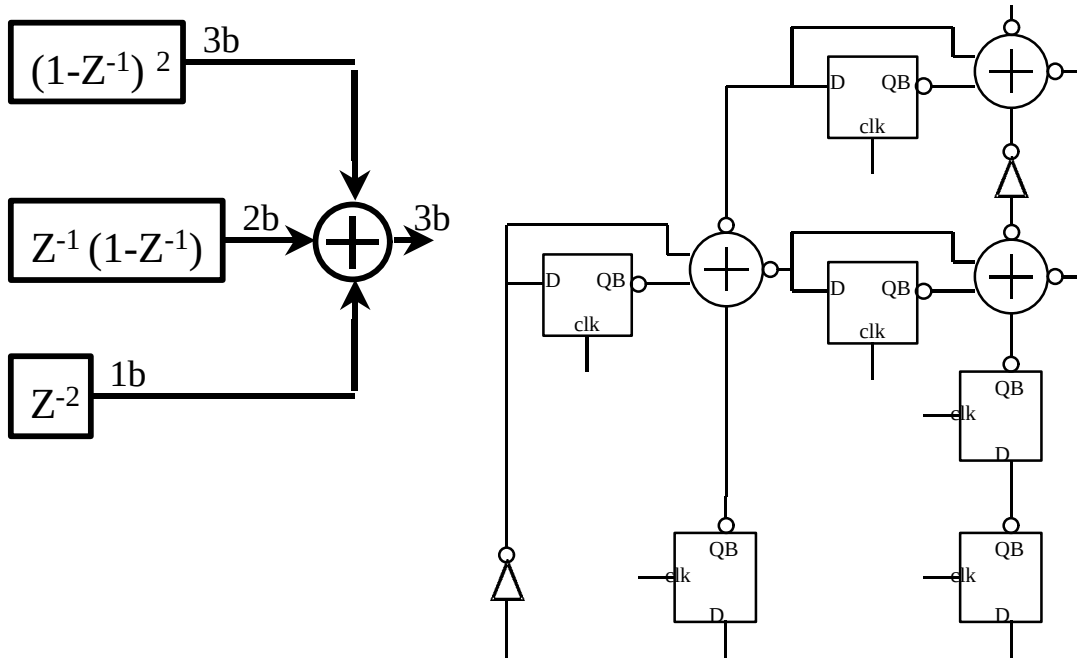

Fig. 63 System and schematic diagrams of the quantization noise cancellation

Dither generator

All types of sigma-delta modulators suffer from the problem of pattern noise if the input is silent or periodic. For example, in Fig. 64, if we input a constant DC of half of the full range into a first-order modulator, the output will oscillate between zero and one to provide the average value of 0.5. In this case, instead of having the high-pass quantization noise as Fig. 65a, the output will have some tones at fixed frequencies as Fig. 65b,. The magnitude and the frequency of the tones depends on the DC level and the period of the input. One way to solve the problem is by adding some random noise to the input to randomize it. However, since the extra noise added and the input signal will appear together at the output, the noise should have a matched shape of the quantization in order not to affect the overall performance, as shown in Fig. 65c. In all frequencies, the noise from the dither is always smaller than the quantization noise at the output.

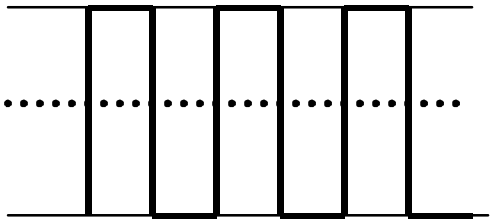

Fig. 64 Output of a first-order modulator with a half-range input

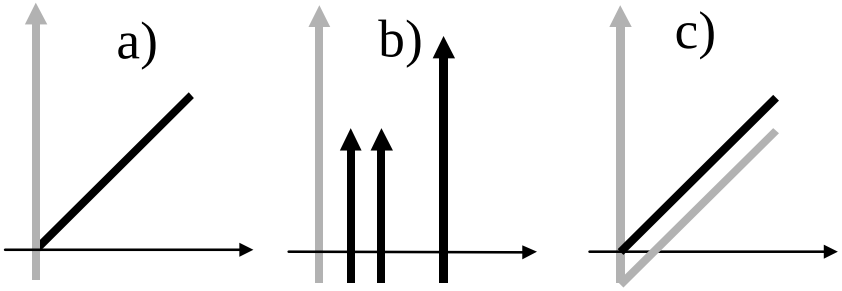

Fig. 65 Output spectrums of a sigma-delta modulator a) random input b) DC or periodic input c) DC or periodic input with dither

Since the sigma-delta modulator is used in a fractional-N frequency synthesizer, usually we want to have a constant DC input to provide a fixed ratio between the reference frequency and output frequency. Therefore, a dither is required. As a third-order sigma-delta modulator is used, the dither has to be third-order high-pass too. To generate the required dither, a pseudo random generator is used. 16 shift registers are put in serial and the product of the status of first two stages is feedback to the input, as shown in Fig. 66. Totally, it can provide 2^{16}-1 different patterns before repeating. Then a third-order digital high-pass filter is required to filter the white noise from the pseudo random generator into third-order high-pass noise. The digital filter can be implemented by adders and D-type flip-flops, as shown in Fig. 67. 4 NOR gates are used to disable the dither signal when the dither is not required.

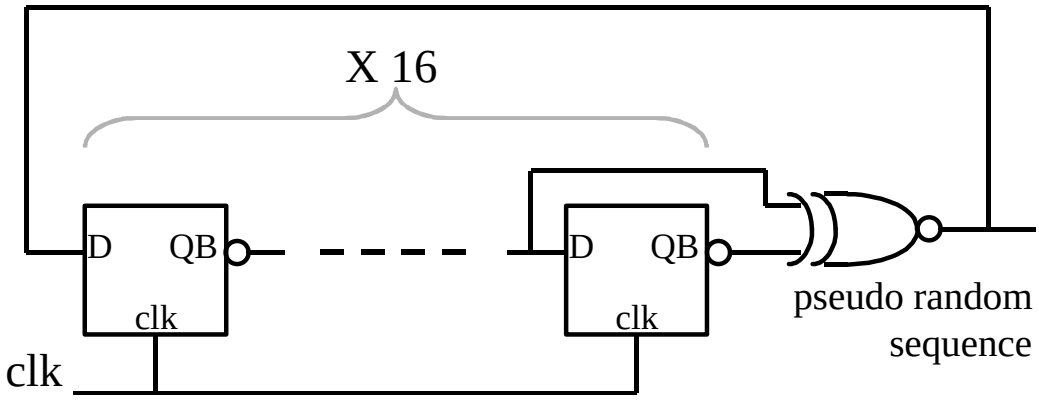

Fig. 66 Schematic diagram of the pseudo random sequence generator

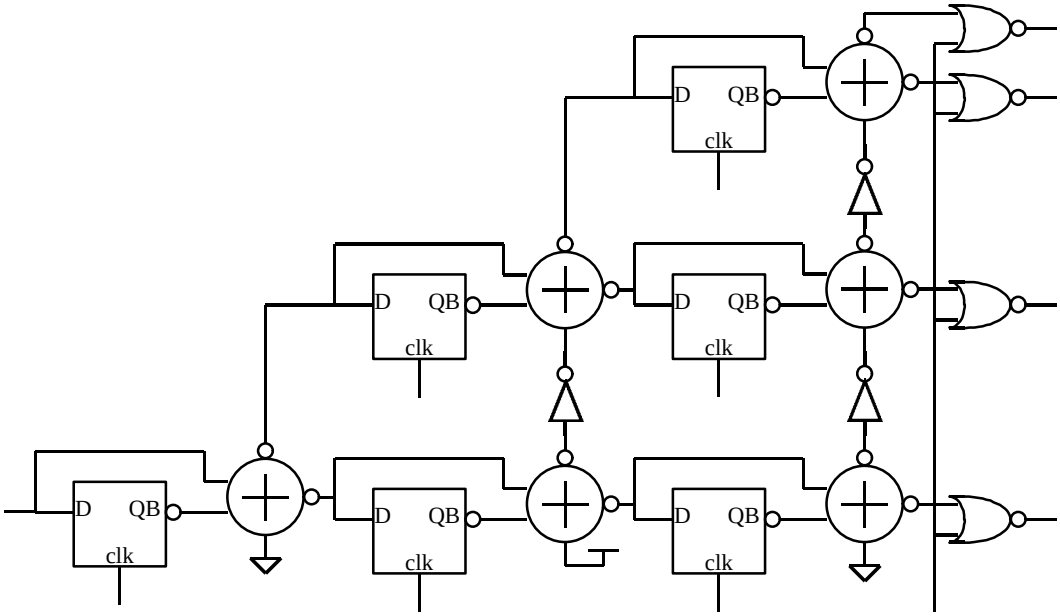

Fig. 67 Schematic diagram of the 3-order high pass digital filter

Chapter 5 Quadrature phase and amplitude matchings in coupled-LC oscillators

Introduction

As CMOS technology gets maturer, high performance CMOS monolithic transceivers become more and more feasible [17]. In order to get rid of bulky discrete RF filters, image-reject mixers are employed. One of the challenges is to implement on-chip low-phase-noise voltage-controlled oscillators with quadrature outputs for LO inputs of image-reject mixers [1, 18].

LC oscillators can satisfy the strict requirements of phase noise, power and output swing. In order to generate quadrature phase outputs, many methods, as shown in Fig. 68, are used, e.g. a) RC-CR network, b) Havens' technique, and c) frequency division, but they suffer from inaccurate phase, amplitude loss, and double frequency operation [19]. By using two identical LC oscillators with four coupling transistors as shown in Fig. 69, even quadrature outputs can be obtained [11, 20]. If the two oscillators are identical, they will oscillate at the same frequency with quadrature phase difference. However, as the mismatches in the two oscillators get larger, the amplitude will be deviated from each other, and phase difference will be further from 90 degrees. If the mismatch is large enough, the two oscillators will eventually oscillate independently at different frequencies.

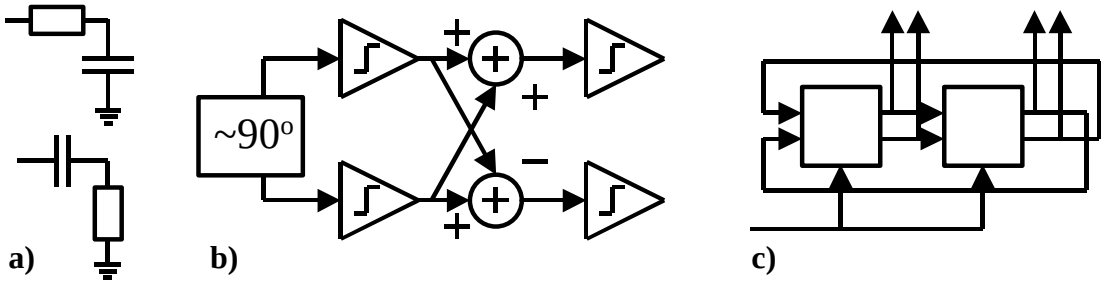

Fig. 68 Different methods to generate quadrature outputs.

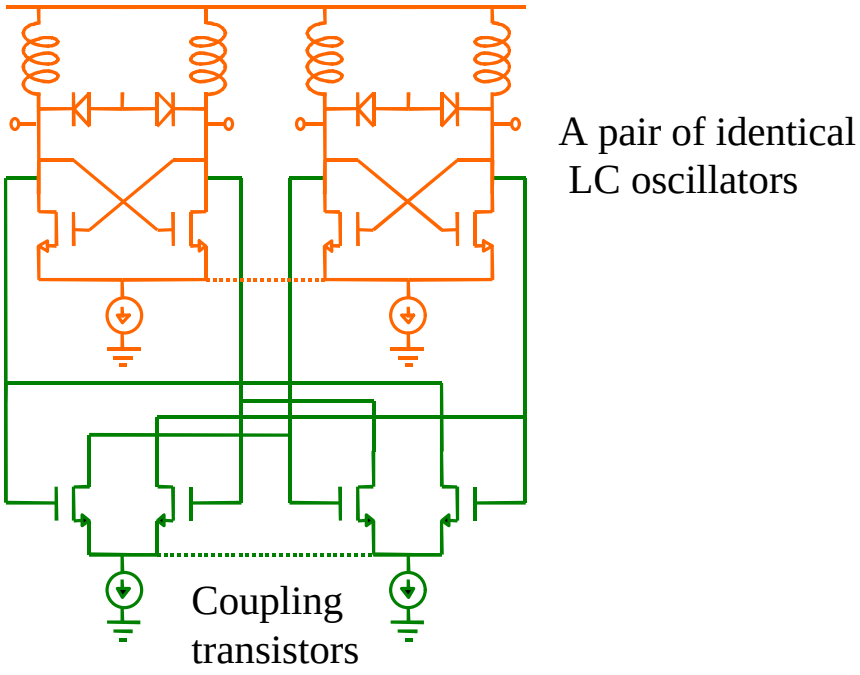

Fig. 69 Schematic of coupled LC oscillators with quadrature outputs

For LC oscillators, causes of mismatches include geometric error from the process, a large area of non-uniform substrate under the inductors and varactors, and nearby objects, which couple to the tanks both electrically and magnetically. Due to the large area of the LC resonant tanks, the mismatch problem of the two oscillators will be serious. Although larger coupling transistors with larger bias can force the two non-identical oscillations in a more quadrature way, they cannot control the output amplitudes of the two oscillations and will hurt the phase noise performance as well.

Additionally, the coupling transistors can maintain the quadrature phase well only when two oscillations have same output amplitudes.

As the two oscillators are connected only by four transistors, more mechanisms are needed to maintain both amplitude and phase matchings of quadrature outputs. As will be presented in this chapter, such a mechanism can be achieved simply and effectively by connecting the two bias current sources of the two oscillators together as shown in dotted lines in Fig. 69. This connection can provide an amplitude control, which is not available before, and enhance the phase control as well. About three times' improvement in amplitude and phase matching is observed.

Operational principles

Amplitude control

Consider a single LC-oscillator as shown in Fig. 70a. A negative-gm cell is used to compensate the loss in the LC-tank to maintain the oscillation. Typically, the common source of the two transistors of the differential pair is assumed to be a virtual ground. However, the assumption is no longer valid if the differential output signal becomes large. As one of two outputs of the oscillation is high and the other is low, one of the transistors is cut-off and the other becomes linear. The common source (node CS) of the two transistors will be pulled high by the linear transistor which acts as a small-value resistor. At this time, the cut-off transistor does not have tranconductance gain, gm, because it is off, and the linear transistor has a very small gm gain because the source node rises with the gate voltage. We can model the linear transistor as a transistor with source degeneration. The source degeneration reduces the gm gain when the differential output is large as shown in the flatten part of transfer curve of the gm cell in Fig. 70b

(dotted line). As the oscillation can only occur when the average loop gain is larger or equal to one, the intersection point of the loop transfer function with the line of unity slope line (light solid line) determines the amplitude of oscillation. Ideally, the differential amplitude can be as large as the product of the bias current and the equivalent parallel resistance of one LC tank.

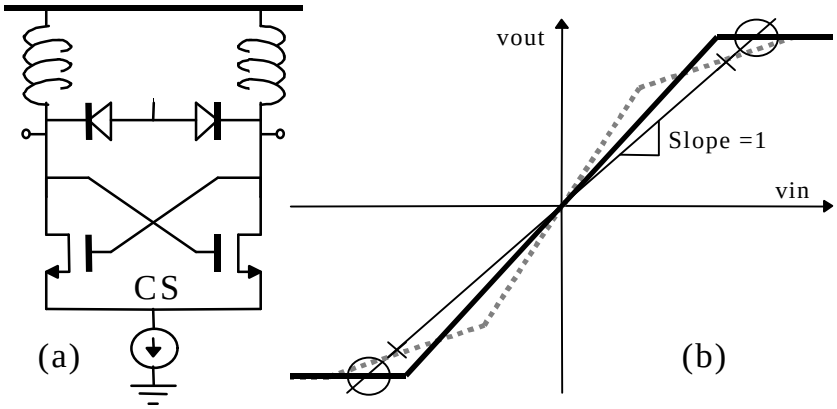

Fig. 70 (a) Schematic of LC oscillator; (b) Output-input characteristic of gm cell

However, since the transfer curve with degeneration (dotted one) cuts the line of unity slope at a point lower than the one without degeneration (darker solid line), the amplitude of the oscillation will be smaller than expected.

If a large capacitor is connected from the common source node to ground as shown in Fig. 71, the ac ground at the node would be maintained (curve 2 in Fig. 72b) and the gm gain would not be degraded. When the differential output of the oscillator is small, the gm cell does not require so much current from the current source and the extra current is stored in the capacitor. When the differential output of the oscillator is larger, the gm cell requires more current and draws current from the capacitor as shown in Fig. 71 and curve 2 in Fig. 72c. The transfer curve would be similar to the ideal one without source degeneration (solid line in Fig. 70b). According to the simulation, larger and closer-to-theoretical amplitude is obtained (curve 2 in Fig. 72a) with a large capacitor (e.g.

100pF). Better phase noise is also expected due to the absence of the noisy degeneration resistance. As a comparison, the corresponding waveforms for the original oscillator without a capacitor are shown as Fig. 72 curves 1.

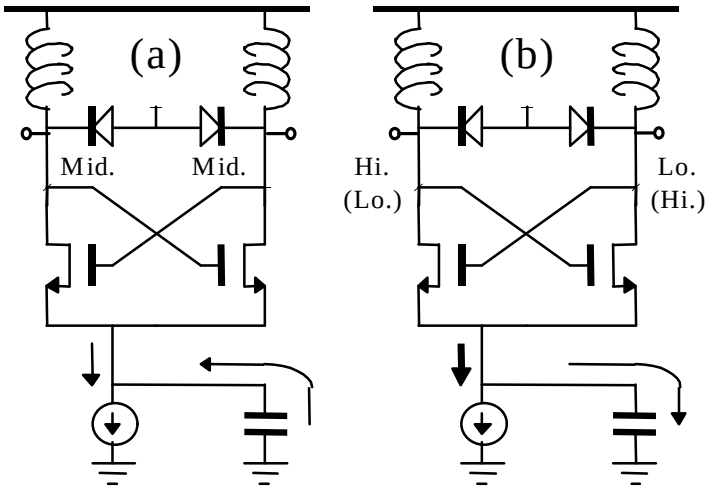

Fig. 71 (a) Less current flow in gm cell when small differential output; (b) More current flow in gm cell when large differential output

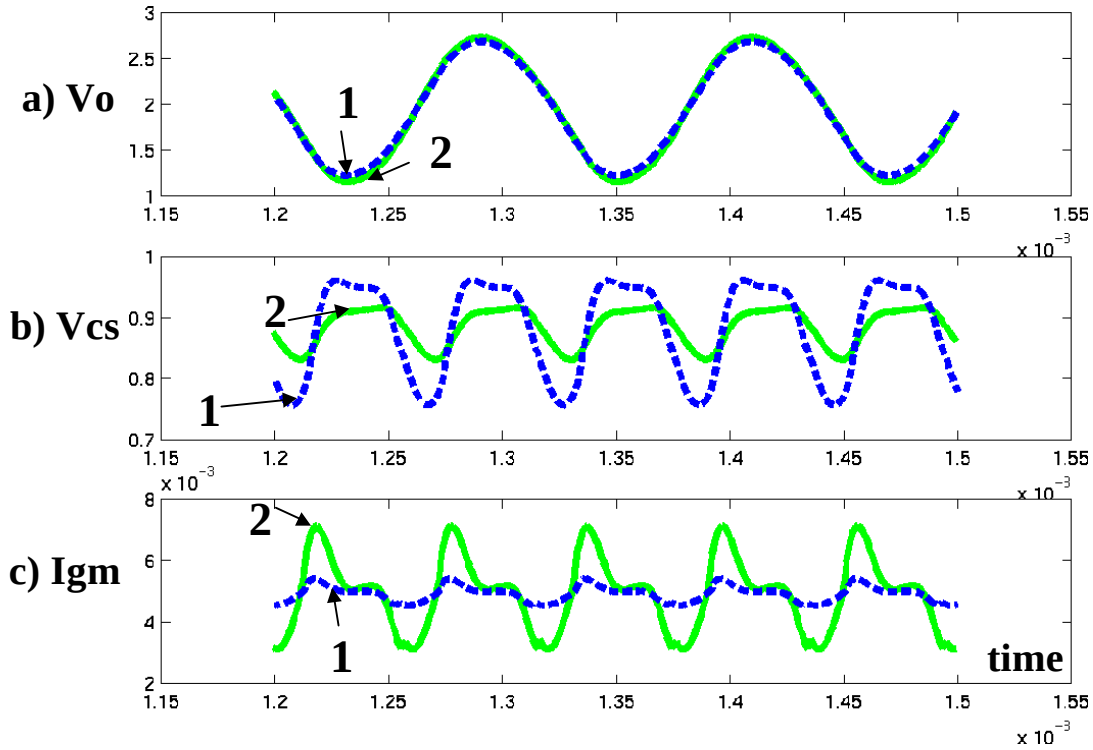

Fig. 72 (a) Single-ended output voltage of LC oscillator; (b) Common source voltage; (c) Current flow into gm cell. (1) without capacitor (2) with capacitor

In practice, it is not desirable to use such a huge capacitor in the circuit. In coupled LC oscillators, the similar effect and result can be achieved if their bias current sources are connected together (Fig. 73). For example, without loss of generality, let us assume that the differential output of oscillator A is small and the differential output of oscillator B is large. Oscillator A does not need much current while oscillator B wants more. Oscillator A can supply its extra current to oscillator B. One-fourth period later, oscillator B output becomes small, and oscillator A output becomes large. Oscillator B has extra current to return to oscillator A. For both oscillators, the other oscillator functions just like a capacitor connected to its common source node. Compared to circuit in Fig. 71, the circuit works the same way. As shown in Fig. 74, in the both cases of connected to a capacitor (2) and connected to the common source node (3), a larger and closer-to-theoretical output amplitude, a flatten common source voltage, and a gm cell current with extra current pulses can be observed.

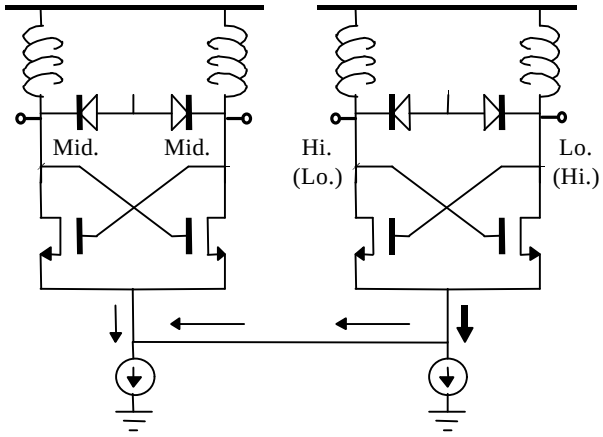

Fig. 73 Current flows in two oscillators with 90-degree phase difference

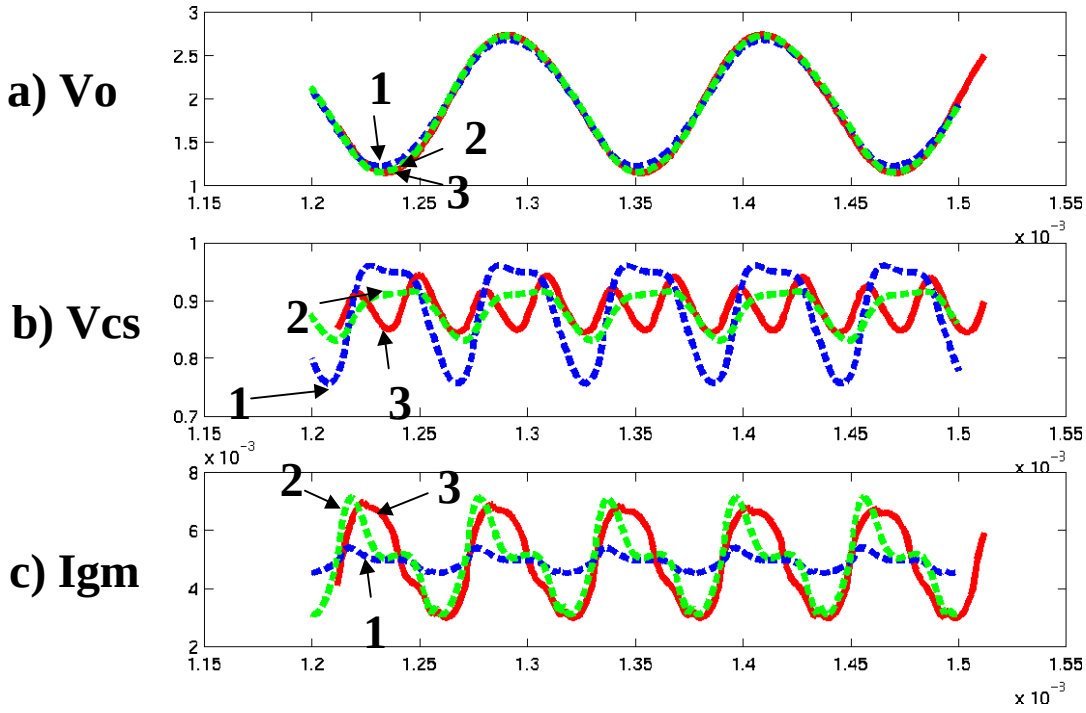

Fig. 74 (a) Output voltage of LC oscillator; (b) Common source voltage; (c) Current flow into gm cell. (1) without capacitor or common source node connection (2) with capacitor (3) with connection

In addition to providing larger amplitude and better phase noise, connecting the two current sources can also maintain the matching of the amplitudes of the two coupled oscillators. For example, oscillator A has larger output amplitude and oscillator B has smaller output amplitude due to the unmatched LC tanks. Since oscillator B has smaller amplitude, it cannot store and release too much current for oscillator A. Oscillator A will see oscillator B as a small-value capacitor as shown in Fig. 75. On the contrary, oscillator B will see oscillator A as a large-value capacitor. As shown in Fig. 76, when the differential output is large, smaller voltage ripples at the common source node and larger peak current pulse are observed for oscillator B (T2) as compared to those for oscillator A (T1). The amplitudes of both oscillators will be increased due to the parallel capacitors but the amplitude of oscillator B will be increased more due to a larger capacitor connected. This mechanism can reduce the amplitude mismatch of the oscillator due to the mismatch between the two LC tanks. Both increase in amplitude

and decrease in amplitude mismatch can be observed in simulation (Fig. 77). This amplitude control is a result of the parallel capacitor effect only because the average bias currents in two unmatched oscillators are the same, just like the case with a capacitor in parallel.

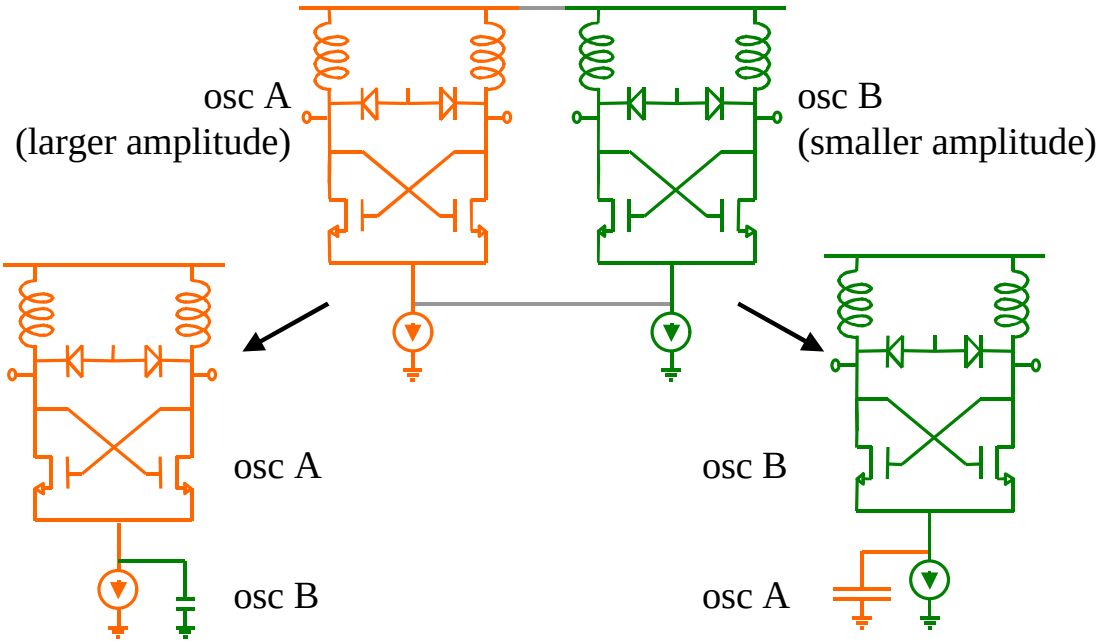

Fig. 75 Another view of a matched coupled-LC oscillators

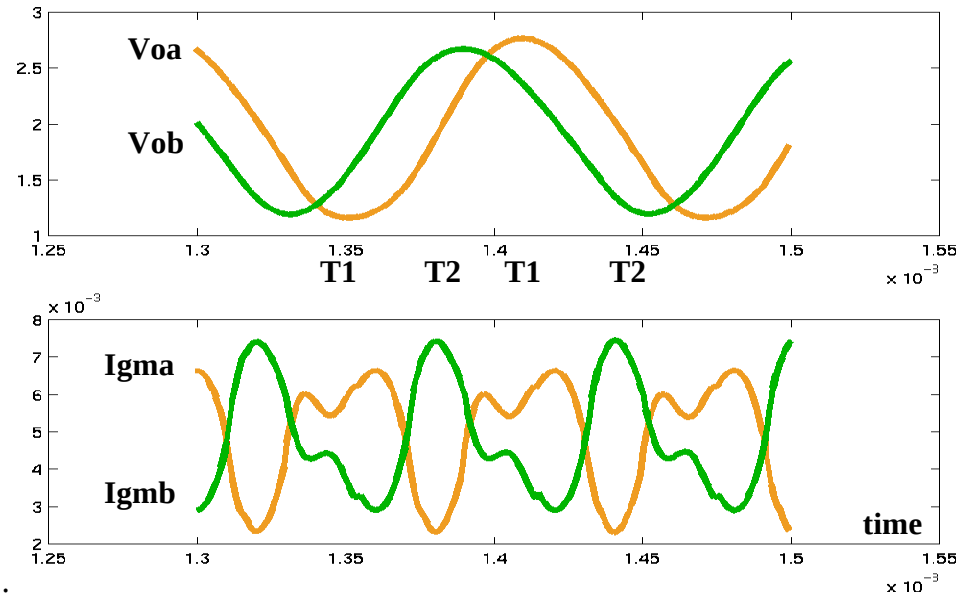

Fig. 76 Amplitudes and currents of the two mistmatched oscillators : T1: period when differential output is large in oscillator A; T2: period when differential output is large in oscillator B

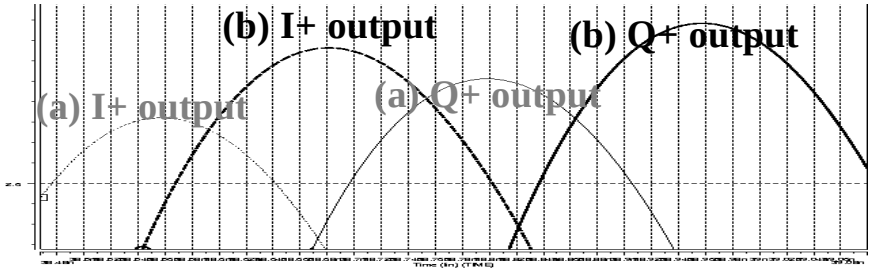

Fig. 77 IQ outputs of coupled LC oscillators (a) without common source connection and (b) with connection

Quadrature phase control

A better phase matching can be obtained for the quadrature outputs of the proposed LC oscillator due to the better-matched output amplitudes and the current interaction between the two oscillators.

Matched output amplitudes

The four coupling transistors force the two oscillators to oscillate at the same frequency and 90-degree out-of-phase. However, the quadrature phase can be maintained only if the amplitudes of the two oscillators are the same. A simple simulation using the circuit shown in Fig. 78 can show this. When the applied voltages at the coupling transistors are not matched, the quadrature phase difference cannot be maintained. Since the output amplitudes of the two oscillators, which share the same current source, are more matched, the four coupling transistors can maintain the quadrature phase better.

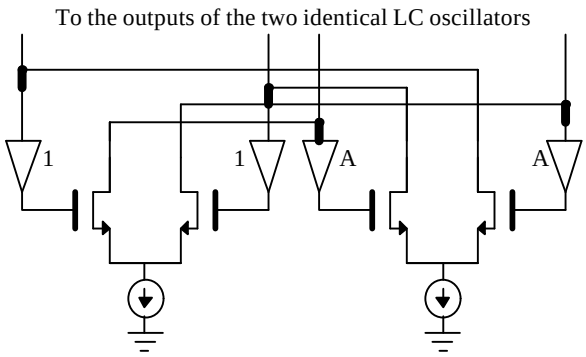

Fig. 78 Circuit to verify imperfect control of the phase for different IQ amplitudes

Current interaction

The two oscillators can supply extra current for each other when more current is needed to enhance both oscillations if they oscillate at the same frequency with quadrature phase difference. This effect favors them to oscillate at the same frequency and with a 90-degree phase difference than any other condition. This mechanism can be proved by two identical oscillators with only the current sources being connected together but without four coupling transistors. After startup, they can automatically oscillate with 90-degree out-of-phase (Fig. 79). Another evidence is that a pair of coupled oscillators with shared current source can always form the quadrature relationship between the outputs much faster as shown in Fig. 80.

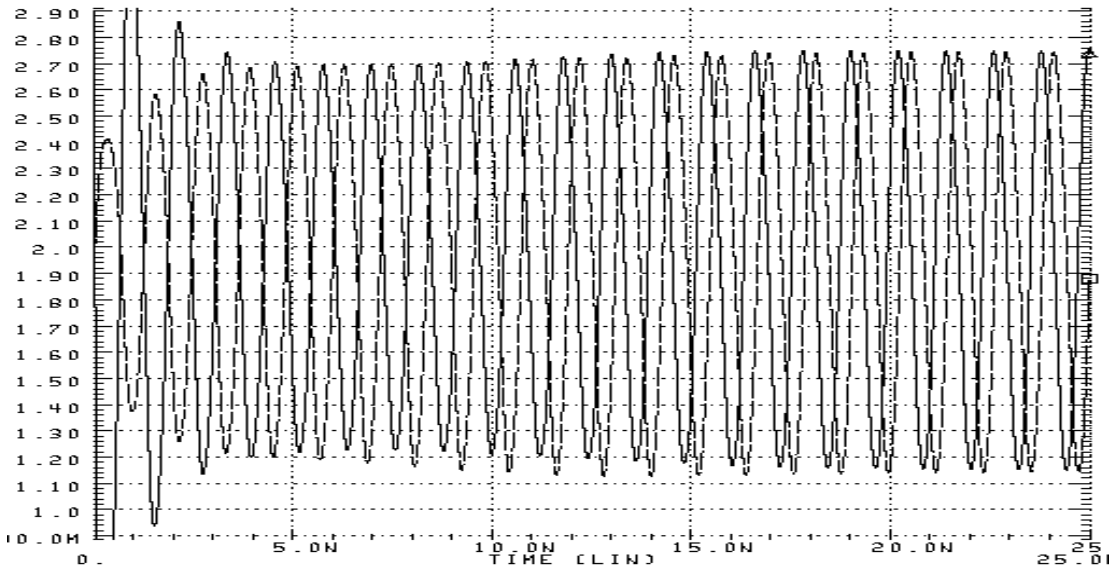

Fig. 79 Output voltage waveform of two LC oscillators with common source node connection only

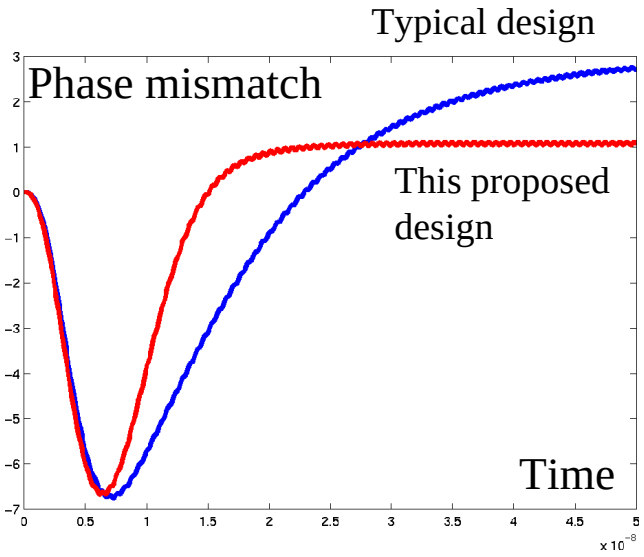

Fig. 80 Phase error with time of coupled LC oscillators without common source connection and with connection

Design considerations

In addition to the LC oscillator, the size of the four coupling transistors and their bias need to be designed. The four transistors form a 4-stage-ring-oscillator-like frame for the two LC oscillators to be put inside as shown in Fig. 81. The frame tries to maintain the quadrature-phase relationship between the two LC oscillators, while the two imperfectly matched LC oscillators try to oscillate at different frequencies and break the quadrature-phase relationship. At the same time, the LC oscillators maintain the purity of the frequency while the ring oscillator gives a poor phase noise. Thus, it is a tradeoff between the quadrature-phase maintenance and the phase-noise performance. The ratio of transistor sizes and biases of the coupling transistors (the ring oscillator) to the negative feedback transistors in LC oscillator determines whether the whole oscillator is closer to being either a ring oscillator with poor phase noise but good phase matching or a LC oscillator with poor phase matching but good phase noise. The tradeoff should be made based on the mismatches of the LC tanks, the quadrature phase, and phase noise

requirements. Fortunately, by connecting the two bias current sources together, the quadrature-phase relationship becomes stronger and the coupling transistors can be smaller to reduce the noise and increase the tuning range of the oscillator. Similar to the two negative gm cells, the common source nodes of coupling transistors are also connected together to increase the gain and improve the matchings. However, less significant effect is observed due to the smaller size and bias.

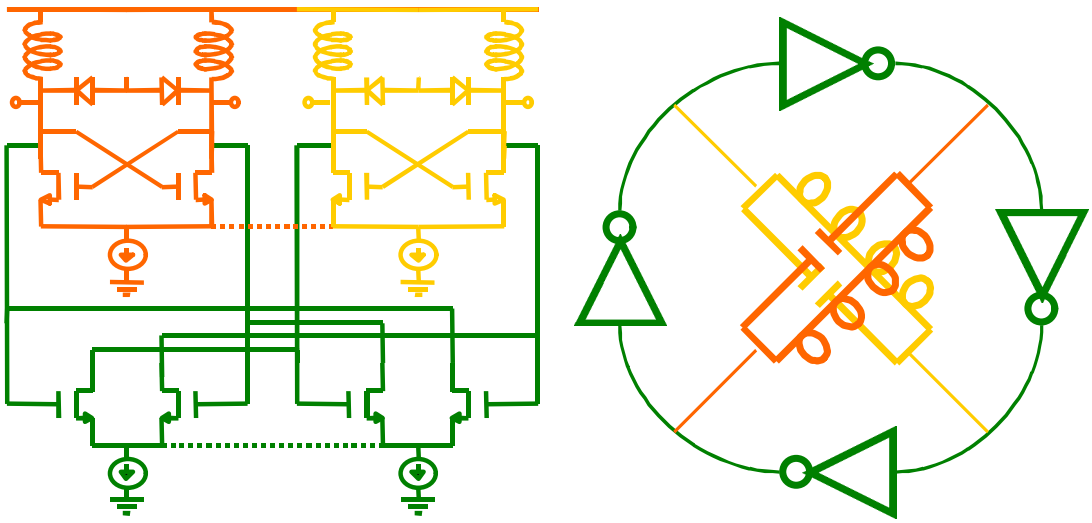

Fig. 81 Different views of the coupled-LC oscillators

Layout considerations

Good matching of the transistors is important to maintain a good quadrature outputs with amplitude and phase matchings. Instead of putting two identical oscillators together, they have to be considered and laid out as a whole. Instead of pairs of transistors, groups of four transistors have to be matched by layout techniques, such as interleaving, common centroid and rotational symmetry. A special floorplan technique is used to match two oscillators. For good IQ matching, every transistor is split into two to match with the transistors of 90-degree phase lag and 90-degree phase lead as shown

in Fig. 82. However, this floorplan technique will raise another problem. Due to the different orientations of the transistors, the mismatch between transistors will be larger.

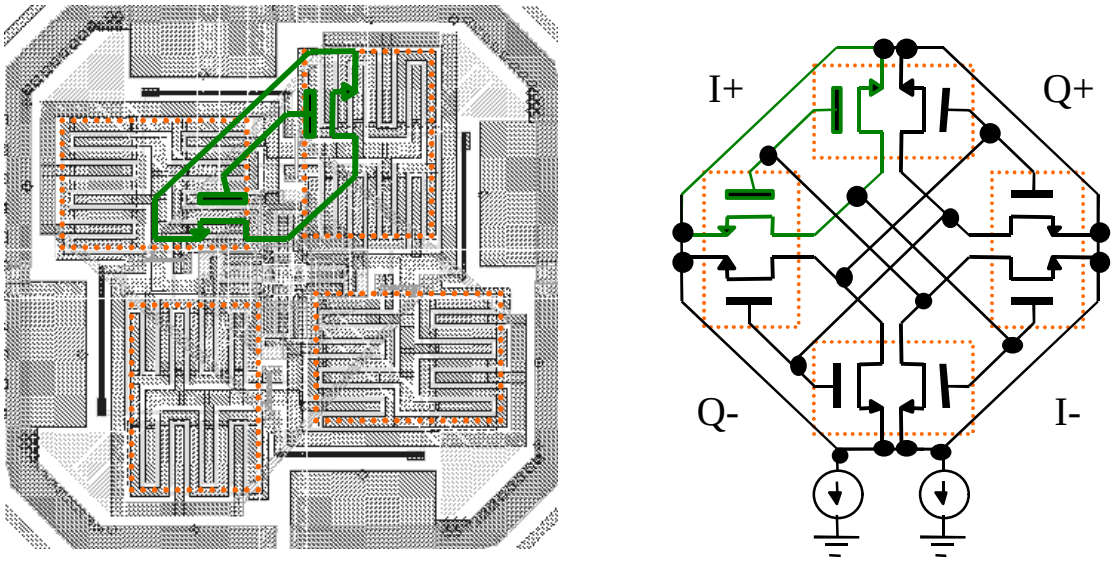

Fig. 82 Floorplan of the Gm cell transistors (matched pairs in dotted rectangles) and the corresponding schematic

Not only the positions but also the orientations of the inductors are important because of the mutual effects of the magnetic flux of the inductors. Different positions and orientations have been considered. The best arrangement is the one with rotational symmetry and common centroid as shown in Fig. 83a because the mutual effects of the inductors can still maintain the quadrature phase difference between outputs. However, this arrangement cannot be used because the connection to the outside and the near-by objects will always affect the symmetry. Any wirings or near-by objects will affect different inductors in different degrees.

If we cannot maintain the correct mutual influence between inductors for the relationship of the quadrature phase difference, we need to reduce the mutual influence between the two LC-coupled oscillators as much as possible. As a compromise, a floorplan with x- and y- mirror symmetries (Fig. 83b) is used in the prototype. The two

LC oscillators are put apart to reduce the mutual influence between them. The corresponding layouts for these two floorplans are shown in Fig. 84.

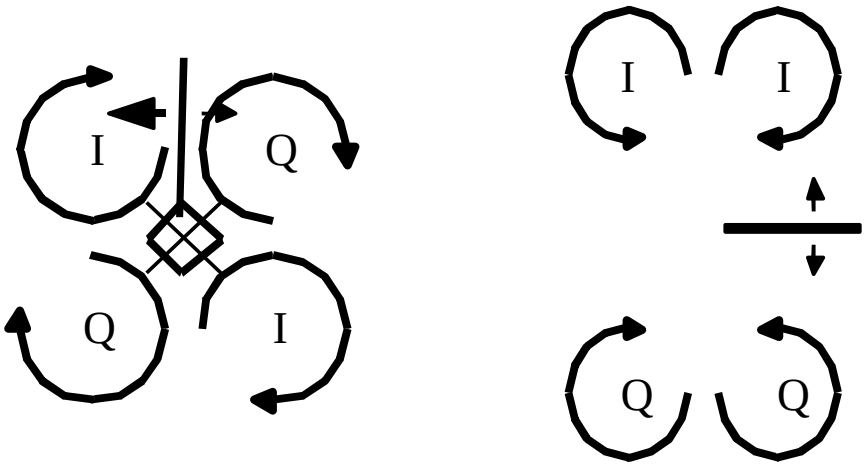

Fig. 83 a) Floorplan of four inductors with rotational symmetry b) Floorplan of the two pairs of inductors in the two oscillators with x-symmetry

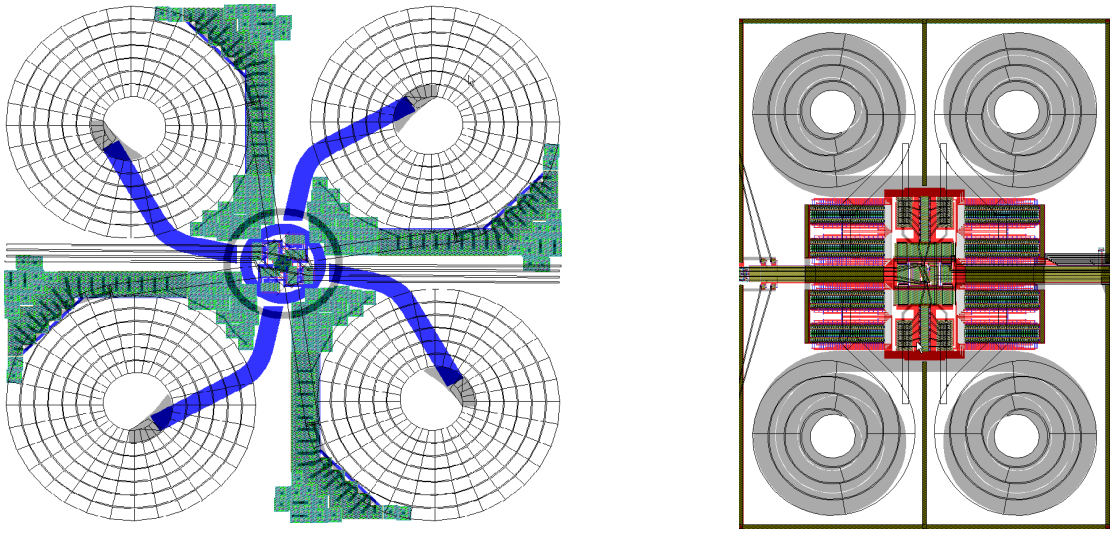

Fig. 84 Layouts of oscillators a) four inductors with rotational symmetry b) two pairs of inductors in the two oscillators with x-symmetry

There are other arrangements for the inductors. Fig. 85 shows one of the arrangements and the corresponding layout. However, due to the uneven influence between the inductors, the quadrature phase difference cannot be maintained.

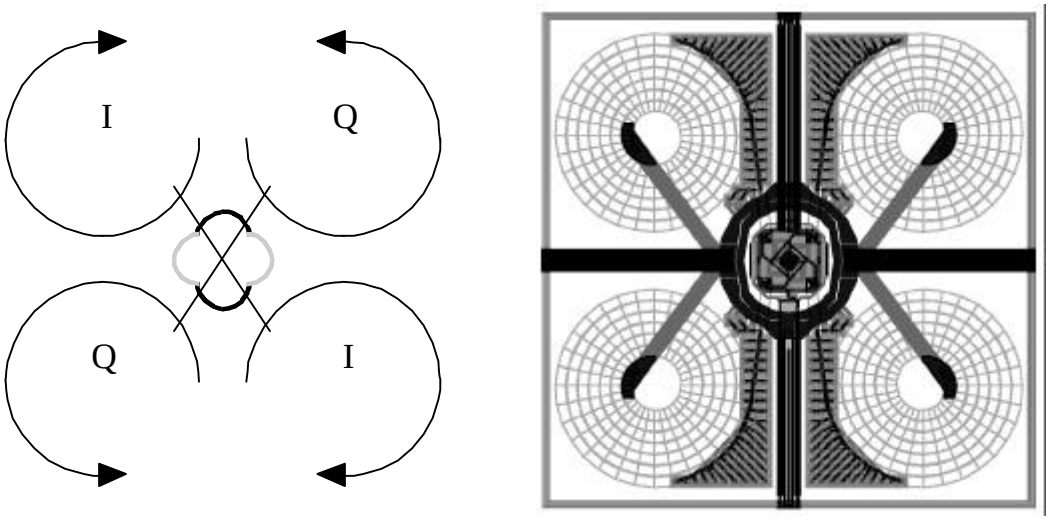

Fig. 85 Other alternative arrangement of inductors and the corresponding layout

Simulation results

Based on simulation, different degrees of mismatches of the resonant tanks are tested. For simplicity, cases with different values of mismatches of varactors in LC tanks are simulated. Simulation results show that there are about 3 times' improvement in both amplitude and phase matching (Fig. 86). In both original and our proposed design, the oscillators will malfunction when the phase and gain mismatches are larger than 15% and 5 degrees, respectively. However, for our proposal, the tolerance to degree of mismatch of the LC tank for stable single frequency oscillation and constant phase difference is improved by about 3 times (Fig. 86b) because the phase and amplitude mismatches are less for same LC tank mismatch. Similar improvements in amplitude and phase matchings are observed for mismatches from other sources, e.g. inductor values, quality factors, transistors' parameters.

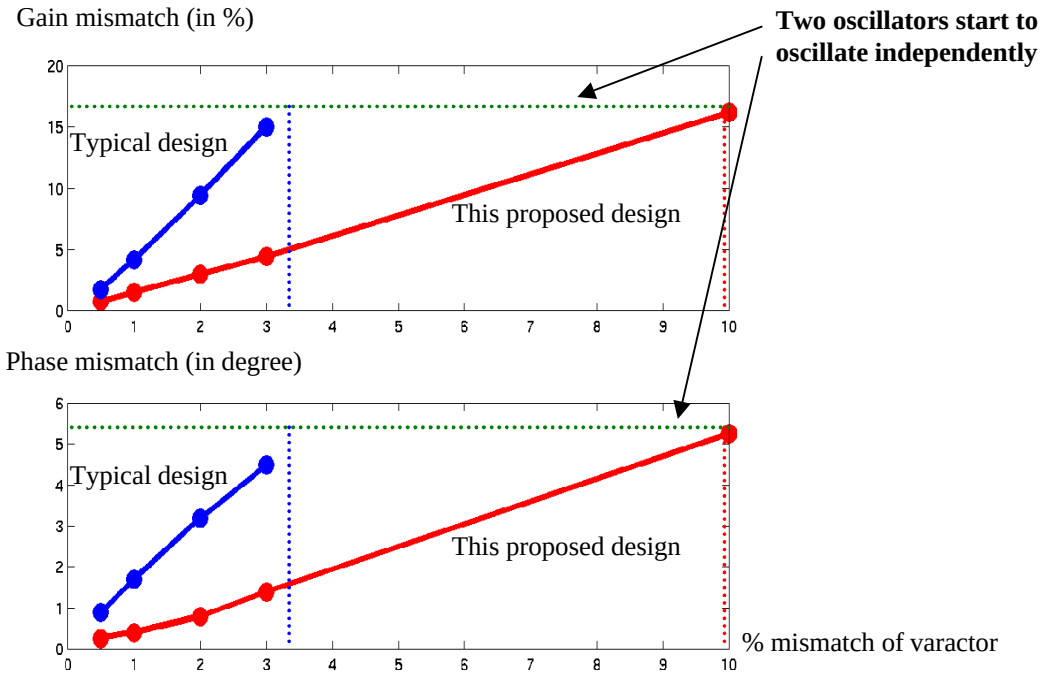

Fig. 86 a) Amplitude mismatch with mismatch error in varactors; b) phase mismatch with mismatch error in varactors

Limitations

The proposed feedback mechanism to control the amplitude is achieved by changing the effective capacitance in parallel to the source node. However, the capacitance in parallel can only lead the amplitude of oscillation to a closer-to-theoretical one. The feedback gain is finite and decreases as the amplitude increases, thus the amplitude control is not perfect and there will exist a non-zero steady-state error in the amplitude. We can only reduce the amplitude error but cannot eliminate it. Similarly, we can only enhance the phase control mechanism to reduce the phase error due to the circuit mismatches but cannot completely cancel it.

Chapter 6 Layout Considerations

Switchable-capacitor array layout

The switchable-capacitor array includes 63 unit switchable capacitor and a half-size switchable capacitor. Each switchable capacitor includes a donut NMOS transistor and a linear capacitor, as shown in Fig. 87 Layout of switchable-capacitor-array. The donut transistor is a transistor with the small drain surrounded by the circular gate and the gate is surrounded by the source. Although the source area is much larger and there is more source capacitance than the transistor with the normal layout, it is not important because the source is always connected to the ground. The importance is the smaller drain area and drain capacitance which can limit the available tuning range of the switchable-capacitor array.

The drain of the donut transistor is connected the poly electrode of the linear capacitor. All the linear capacitors share a common N well electrode in order to reduce the large redundancy and improve the matching.

All the capacitors are without a shape corner to prevent the over-etching at corners to increase the mismatch. The donut transistor and the linear capacitor have the same width 5.4μm. As a result, all the switchable-capacitors can be put side by side and form a compact layout as shown in Fig. 88. The height of the each unit capacitor is kept short (2.7μm) because the higher capacitor has a larger series resistance and larger capacitor. As a result, poor quality factor will be obtained because the quality factor of a capacitor

equals to $1/wRC$. By doubling the height, the quality factor will be degraded by 4 times.

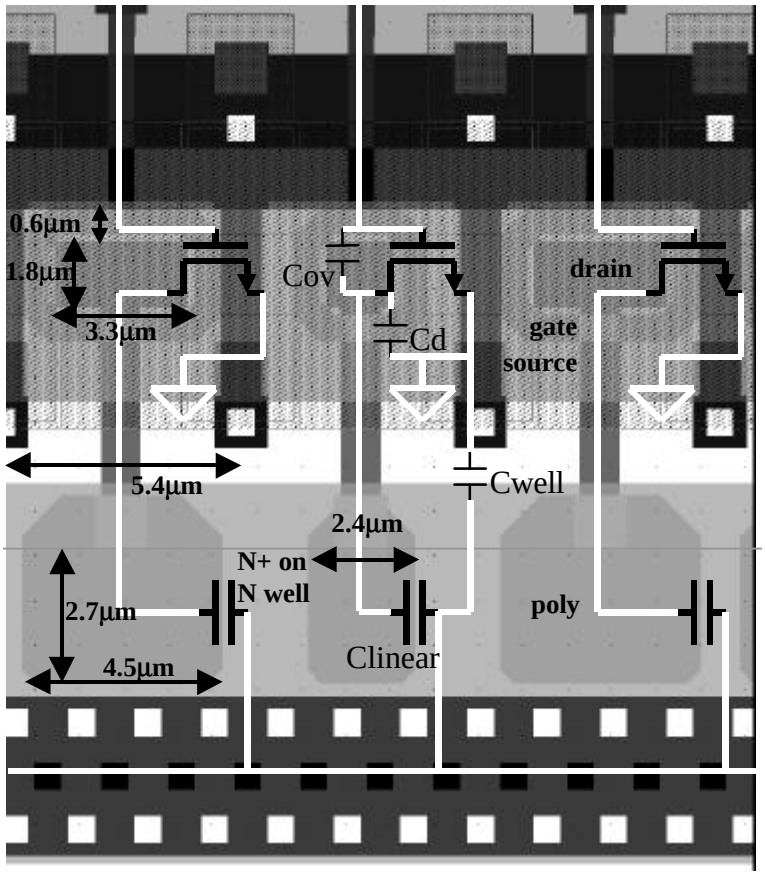

Fig. 87 Layout of switchable-capacitor-array

To reduce the mismatch between the unit switchable capacitors, the unit switchable capacitors are arranged as Fig. 88. The capacitors for the lowest five bits are labeled there. The unit capacitors corresponding to a single bit are evenly disturbed in the whole array. Moreover, all the bits except the lowest two bits are common-centroid.

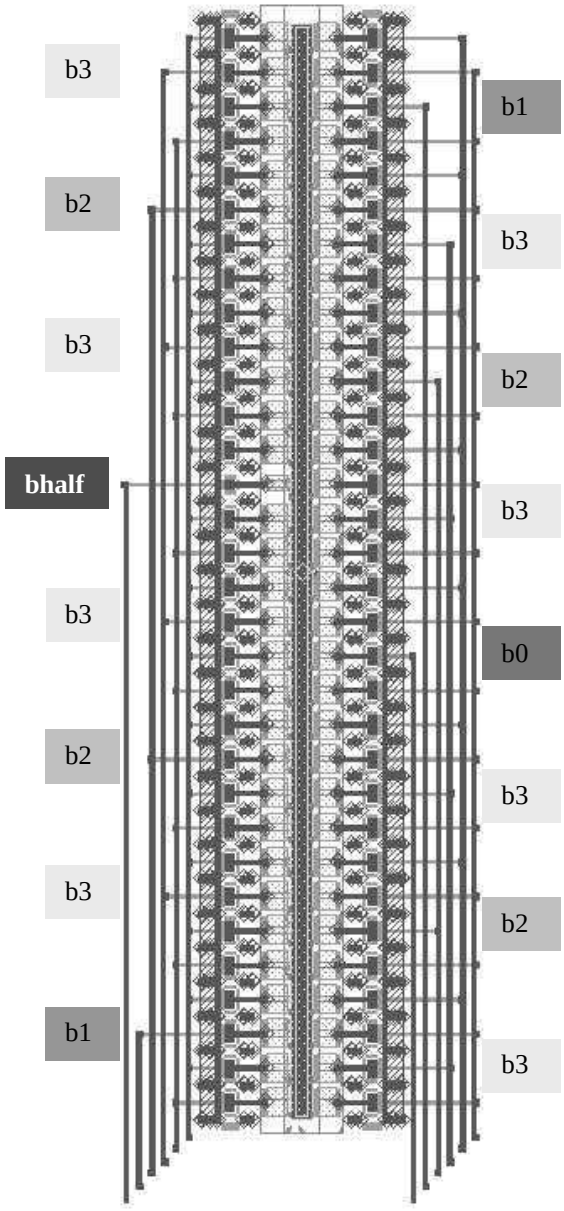

Fig. 88 Layout of half of the whole switchable-capacitor array

Varactor layout

The varactor employs parasitic PN junction diode between the P+ and N well, as shown in Fig. 89. There are totally 18 and 186 unit PN junction diodes for the two varactors used in the voltage-controlled oscillator. By minimizing the size of the unit diode and distance between the P+ electrode and N+ ohmic contact, the quality factor of around

30 is obtained. It is because the series resistance of the diode depends on the length of the high resistive N well. Reducing the distance (1.2μm) between the P+ electrode and the N+ ohmic contact can reduce the series resistance of the diode. Moreover, unit diodes of a smaller size (1.5μm x 1.5μm) can have smaller capacitance. Since the quality factor of a capacitor is $1/\omega RC$, smaller capacitance and smaller resistance can give better quality factor. For the same reason, octagonal unit diode is drawn because it keeps a smaller distance (1.2μm) between the P+ and N+ even at corners.

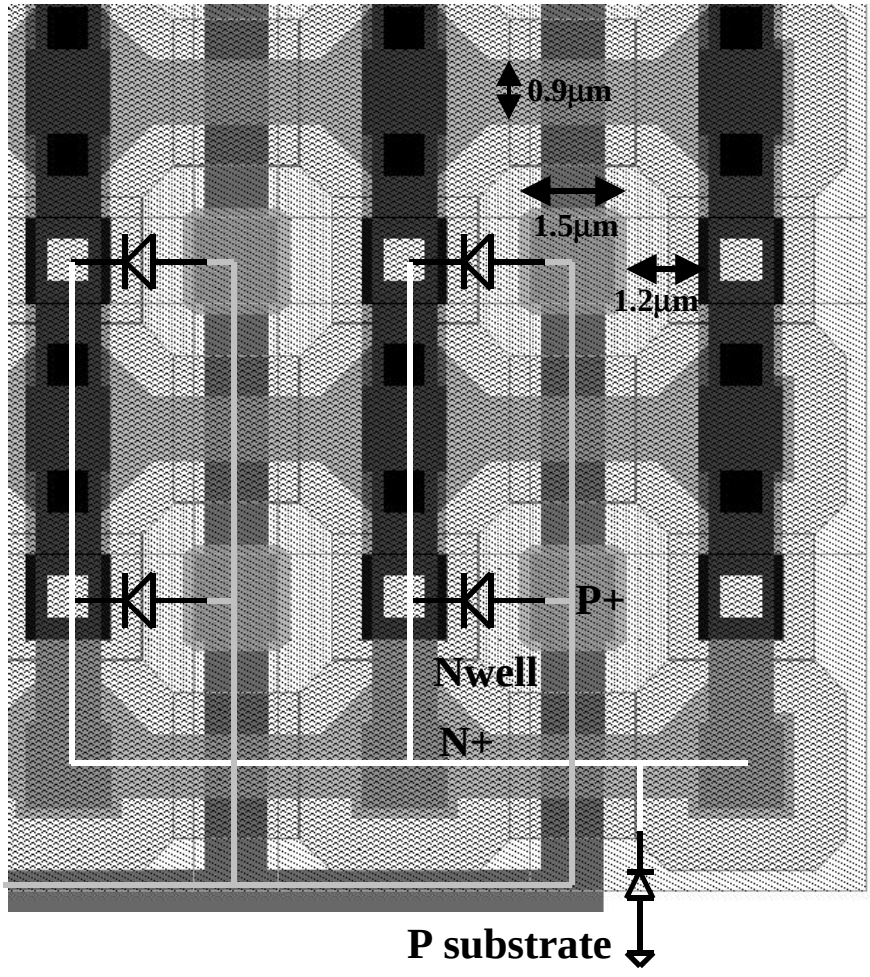

Fig. 89 Layout of P+ Nwell varactor

Inductor layout

The inductors used are double-layer (Metal 3 and Metal 2) circular spiral inductors. For the same inductance, circular spiral inductor has approximately pi/4 serial resistance and parasitic capacitance of a square spiral inductor. The smaller serial resistance (or larger quality factor) and parasitic capacitance can provide better phase noise performance and larger available tuning range of the voltage-controlled oscillator. Our previous trials show that single-layer and double-layer spiral inductors have a similar quality factor and parasitic capacitance. However, double-layer spiral inductor occupies about 1/4 area.

The diameter of the spiral inductor is 280um with a hollow hole of 75um diameter. The spacing between spirals is minimal, 1.8um. Since the sheet resistances of the two metal layers are different (0.05ohm for Metal 3 and 0.07ohm for Metal 2), the widths and numbers of turns of the spirals of two layers are designed to be different to maintain the same resistance per unit length, as shown in Fig. 90 and Fig. 91. In this case, the whole resistance will not dominate by the spiral on the layer of higher resistance. The width of the spirals in Metal 2 and Metal 3 layers are 36um and 26um while the number of turns are 2.5 and 3.5. These can keep the two spirals with the same resistance per length, the same diameter and the same hollow hole size, as shown in Fig. 92. As the two spirals overlap and connect at the most inner turn, the two spirals share the resistance there. The same resistance per unit length can be still maintained even if the width of the inner turn of two spirals reduces. This special connection, as shown in Fig. 93, can maximize the size of the hollow hole to improve the quality factor and reduce the parasitic capacitance.

The spiral inductor is designed and simulated by the ASITIC program. The inductance is 6.6nH and the parallel parasitic capacitance is 0.6pF. However, since the program ignores loss due to the substrate eddy current, the quality factor of the inductor calculated by the program is totally incorrect. From previous trials, the quality factor of spirals of similar sizes is around 2-2.5 which will dominate the overall quality factor of the whole LC tanks and limit the phase noise performance of the oscillator.

Fig. 90 Layout of metal-2 layer of the inductor

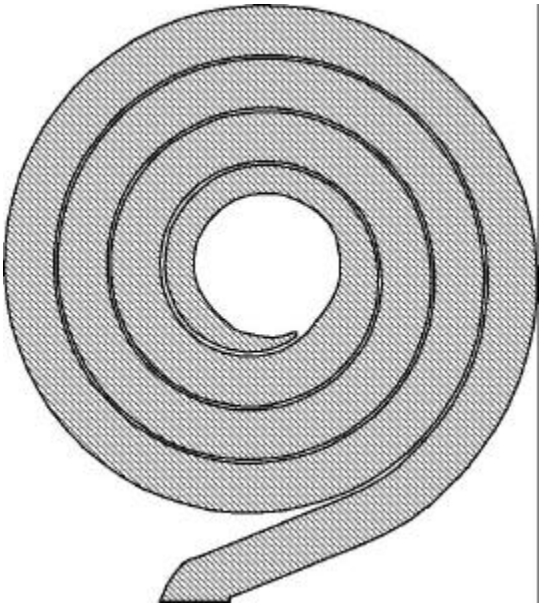

Fig. 91 Layout of metal-3 layer of the inductor

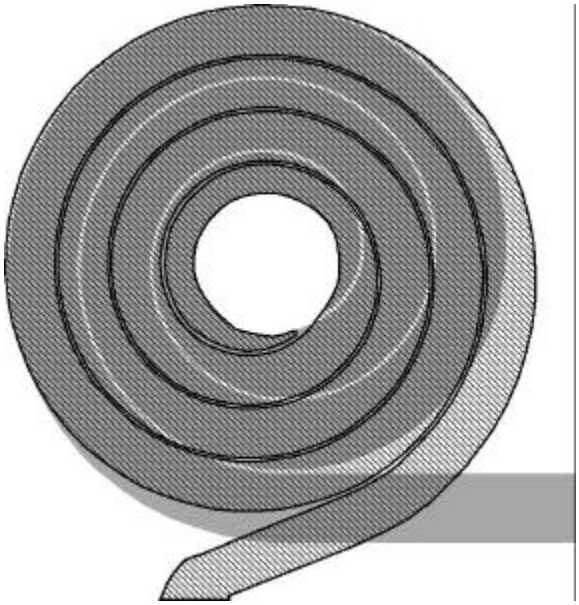

Fig. 92 Layout of the inductor

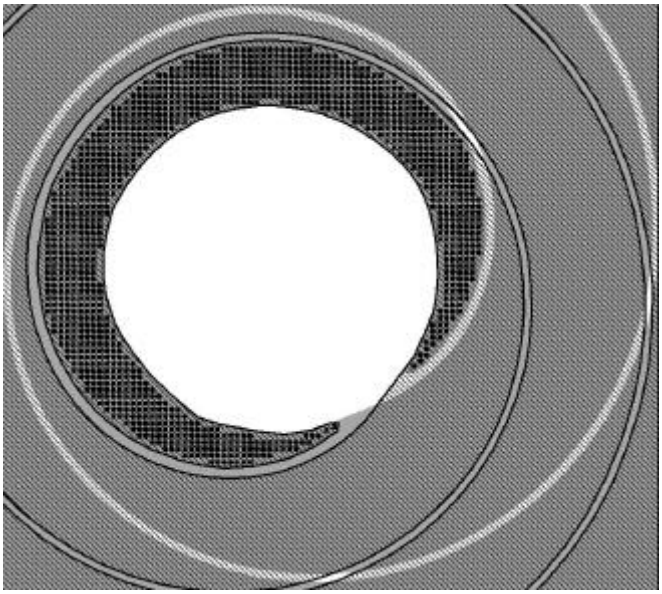

Fig. 93 Zoomed view of the interconnection of two layers of the inductor

Voltage-controlled oscillator layout

The most important building block of the frequency synthesizer is the voltage-controlled oscillator. The layout of the voltage-controlled oscillator and the corresponding schematic are shown in Fig. 94 and Fig. 95. The area of the layout is 0.65mm x 0.9mm. The voltage-controlled oscillator includes two identical LC

oscillators (shown in the upper and lower half of the layout). Each LC oscillator is also symmetrical about the vertical. In both Fig. 94 and Fig. 95, the switchable-capacitor array (a) which connects to the inductor (b) and varactor (c) to form the LC tank. The inductors of the two LC oscillators are put apart to reduce the magnetic coupling between them because the coupling will force the two oscillators oscillate in phase instead of with quadrature phase difference. However, the large separation may result in the poor matching between the two LC tanks in the two oscillators. The cross-couple differential pair (d) is used to compensate the loss of the LC tank. The shared current source (e) provides the current for both LC oscillators. There are a small coupling transistors as a ring oscillator (f) to keep the quadrature phase between the two LC oscillators. The arrow pointing into the center the voltage-controlled oscillator in the layout shows the biases, varactor tuning signal, digital control line of switchable-capacitor array, power supply line and ground. The arrow pointing out shows the outputs of the voltage-controlled oscillator. The whole voltage-controlled oscillator is surround by a p guard ring and a n-well ring (dashed line) in order to reduce the substrate noise from other circuits outside. There are also a SSB mixer (h) and output buffer to pad (i) for the quadrature phase and gain matching measurement and the phase noise measurement.

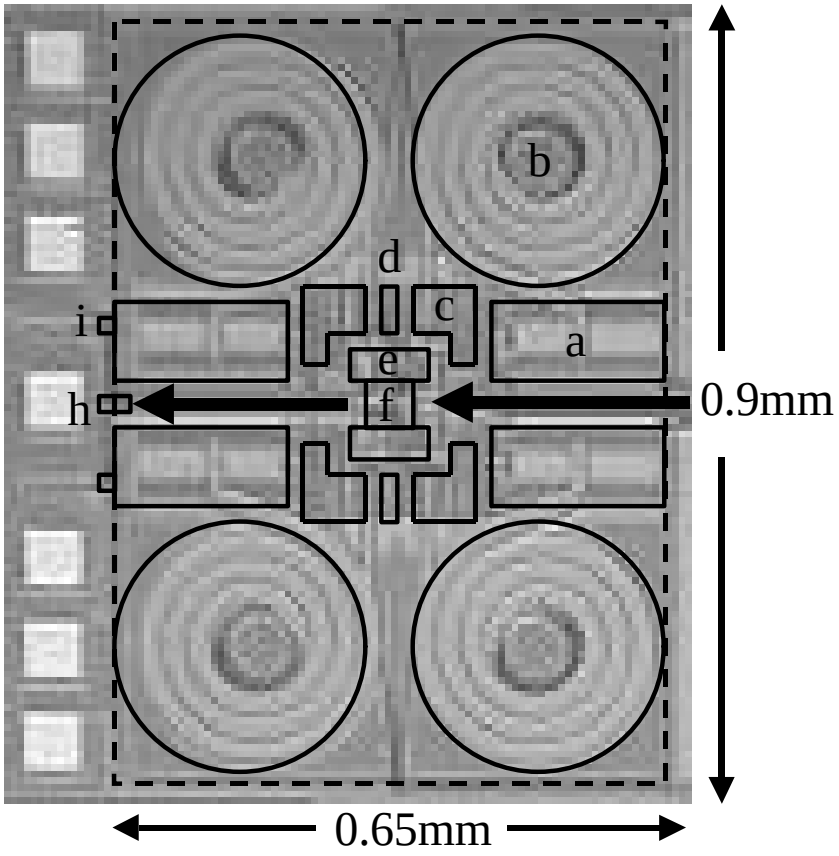

Fig. 94 Layout of the voltage-controlled oscillator

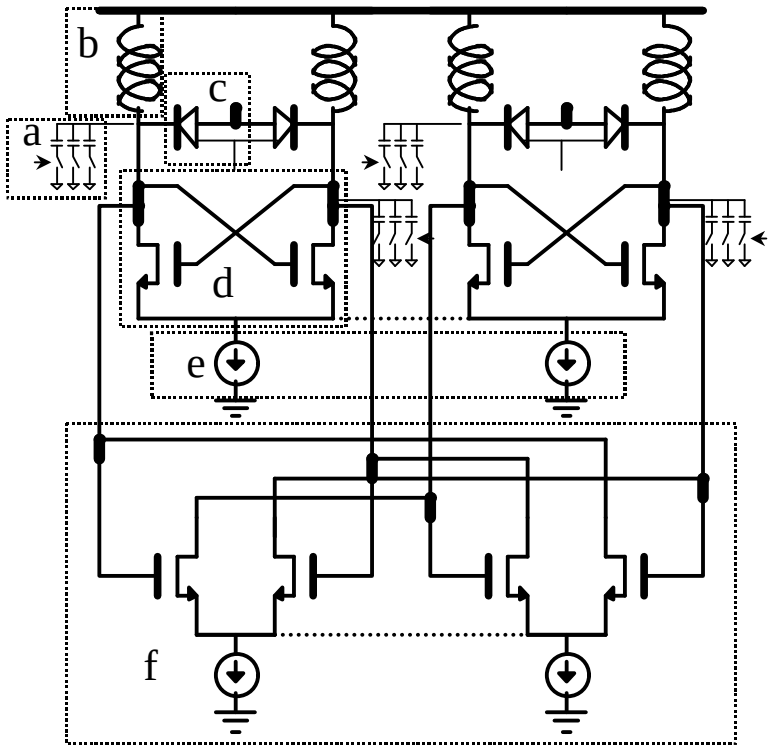

Fig. 95 Schematic of the voltage-controlled oscillator

Synthesizer Layout

The layout and the block diagram of the frequency synthesizer are shown in Fig. 96 and Fig. 97. The total area of the layout is 0.9mm x 1.1mm. The output of the voltage-controlled oscillator (a) drives the prescalar (b). Then the divided frequency from the prescalar are compared with the input reference frequency by the frequency phase detector (c). The frequency phase detector controls the charge-pump (d) to output the current to the loop filter (e). The error signal from the loop filter output will be used to control the voltage-controlled oscillator. In this case, the phase-locked loop is formed. In order to implement the fractional-N phase-locked loop frequency synthesizer, the prescalar (b) is also controlled by the sigma-delta modulator (f). Other than controlling from the loop, the voltage-controlled oscillator is also tuned by the switchable-capacitor array. The channel selection controls the switchable-capacitor array in the voltage-controlled oscillator (a) through the gain and offset adjustment circuit (g). In this layout, the noisy digital circuit, e.g. the sigma-delta modulator is tried to separate from the voltage-controlled oscillator and some guard rings (p guard rings and n-well rings) are put in between in order to reduce the effect of substrate noise coupling. However, due to the dense layout, the separation is only around 0.2mm.

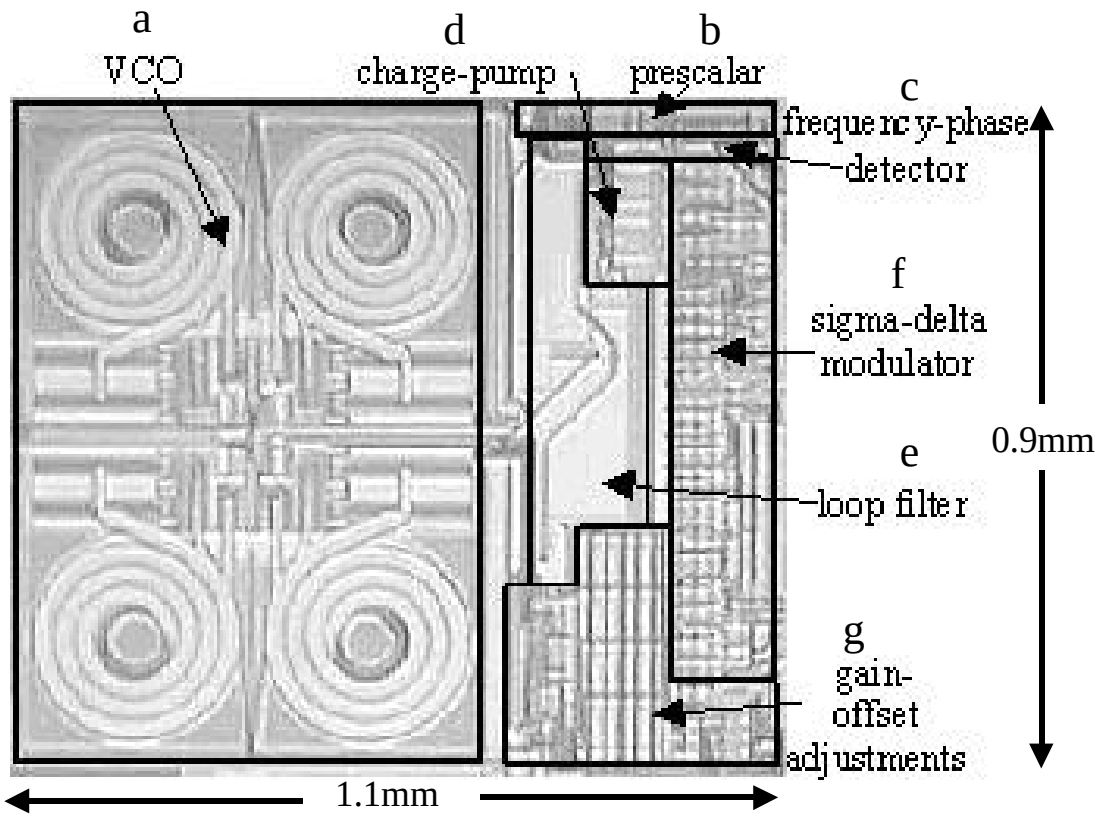

Fig. 96 Layout of the frequency synthesizer

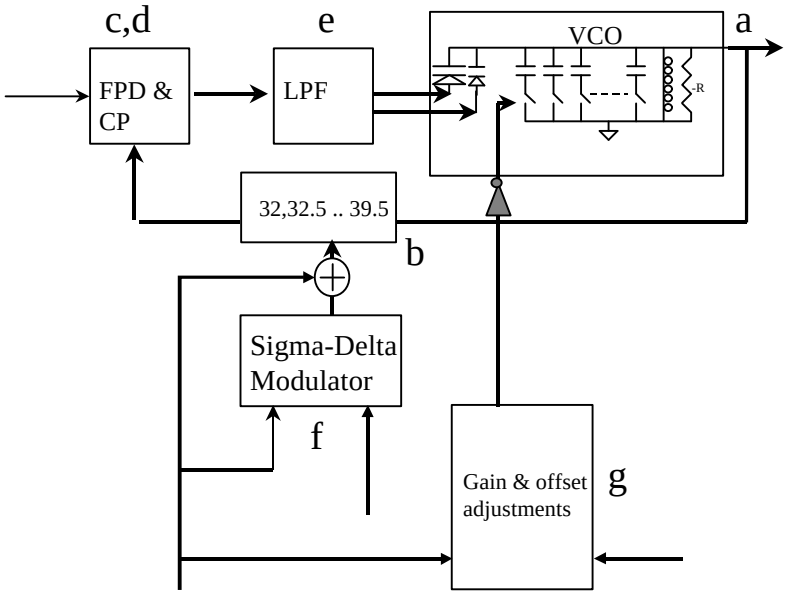

Fig. 97 Block diagram of the frequency synthesizer

Die Layout

Fig. 98 shows the die photo of the prototype. It is a 2mm x 2mm tiny chip. It includes the synthesizer and many test structures for the passive components. Due to the limited peripheral bonding pads, some of the digital inputs for the synthesizers are stored in a shift register while all the analog biasing inputs are connected to the bond pads. The reference frequency input at 25.6MHz is also connected to the bond pad directly. The output signals of the synthesizer at 900MHz are connected to some internal pads which are probed by a high-impedance probe. The test structures are connected to some internal pads which are probed by high-speed GSG probes.

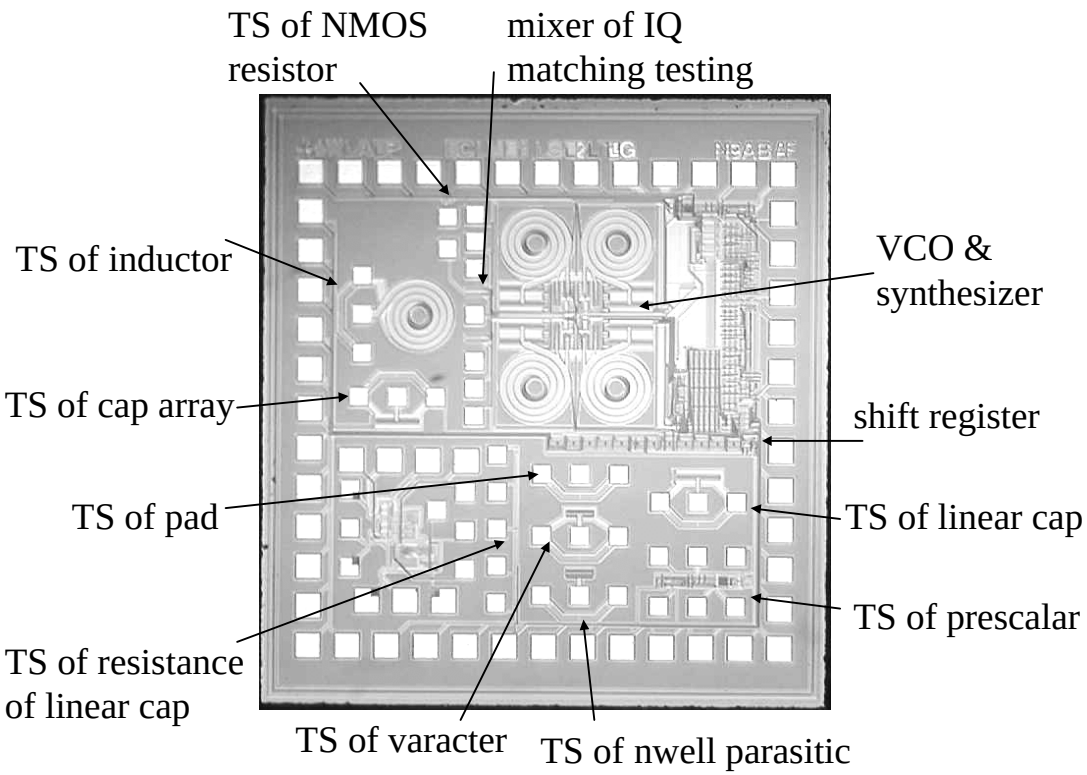

Fig. 98 Die photo of the frequency synthesizer and the test structures

Chapter 7 Measurement

Introduction

The frequency synthesizer is fabricated by a HP 0.5-μm single-poly-triple-metal N-well CMOS technology with N-well poly linear capacitor and silicide-blocked resistor options. The measurements include the passive components which dominate the performance of the frequency synthesizer, the voltage-controlled oscillator which is the most important building block in the frequency synthesizer, and the frequency synthesizer itself.

Passive components

In the voltage-controlled oscillator, there are many on-chip passive components including spiral inductors, switchable-capacitor arrays and varactors. The parameters of these passive components, including the extra value, the parasitics, tuning range and quality factor, determine the performance of the voltage-controlled oscillator, e.g. the phase noise performance, the center frequency, the tuning range, the amplitude and the power consumption. Unfortunately, the parameters of these components depend heavily on the process. Due the process variation and some conceal parameters of the process, the modeling of the passive components is not very accurate. Therefore, measurements on the passive components are necessary to verify the modeling and the performance of the frequency synthesizer.

Testing setup

The testing setup shown in Fig. 99 is used to measure the one-port S-parameter of the inductor, the switchable-capacitor array and the varactor. The measured one-port S-parameters are converted to Z-parameters to show the different parameters of the components including resistance, inductance or capacitance. All the passive components under test are connected to the pads as shown in the top of Fig. 99. The center-to-center distance between the pads is 150μm and the size of each pad is 75μm x 75μm. The two grounded pads of metal 3 are connected together and connected to the ohmic contacts on the substrate through metal 2 and metal 1. A calibrated high-speed GSG probe connected to a network analyzer is used to probe the components and the network analyzer will show the one-port S-parameter of the measured components. A DC power supply is connected to the network analyzer to bias the components for the measurements of the components under different bias conditions.

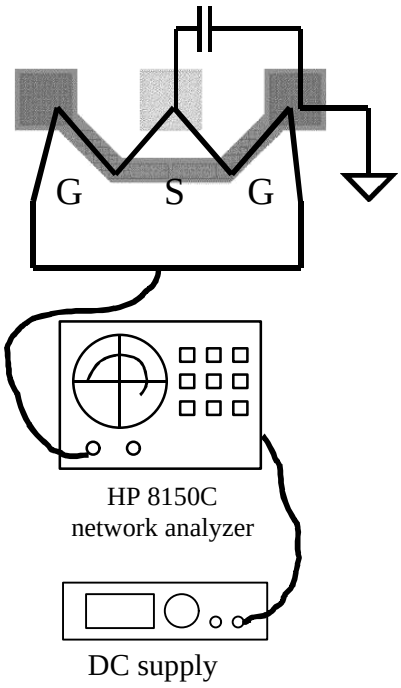

Fig. 99 Testing setup for the passive component measurement

Due to the parasitcs of the pads connected to the passive components, the measured parameters will be the combination of the pads and the components. Therefore, the pre-measurement of the pads is necessary to calibrate the measurement results due to the extra parasitics from the pads. Luckily, the parasitics due to the pads are not very large and the effect of the pads can be simply modeled as an extra capacitor in parallel to the component under test.

Fig. 100, Fig. 101 and Fig. 102 show the measured capacitance, the series resistance and the quality factor of the pads against frequency. Due the limitation of the network analyzer on measuring high-impedance devices, the measurement results fluctuate a lot. Especially at low frequency, the impedance of a small capacitor such as the pads is very high. However, at around 900MHz, the pads can still be modeled approximately as a 60fF capacitance in series to a 30ohms resistor. The quality factor of the pads is quite high which is about 100. Due to the good quality factor and the small capacitance of the pads, the measured result of the pads will not affect the accuracy of the measurements of other passive components too much.

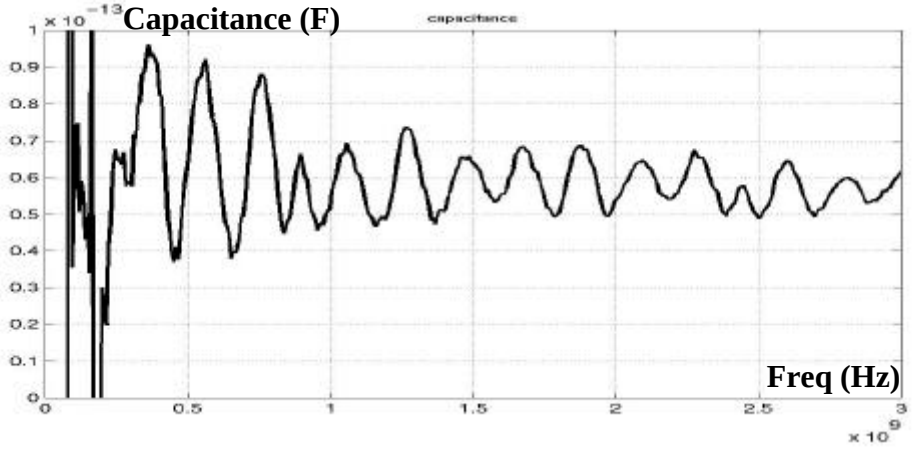

Fig. 100 Capacitance of the testing pads of the passive components vs. frequency

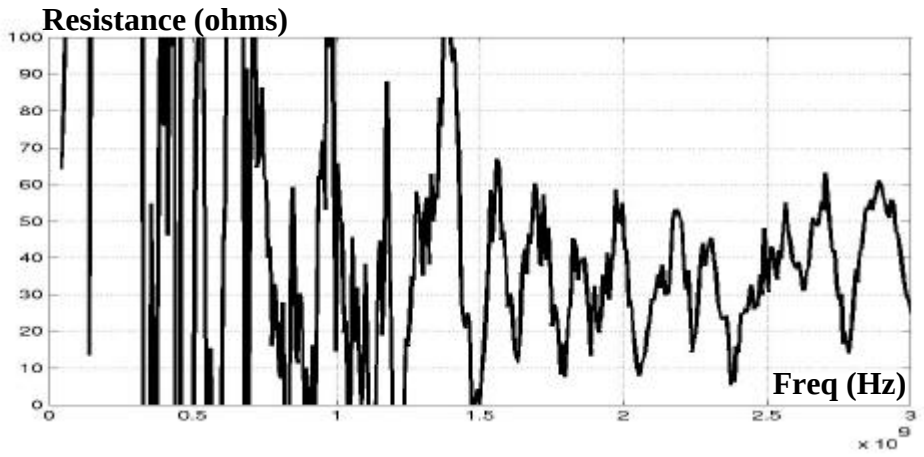

Fig. 101 Resistance of the testing pads of the passive components vs. frequency

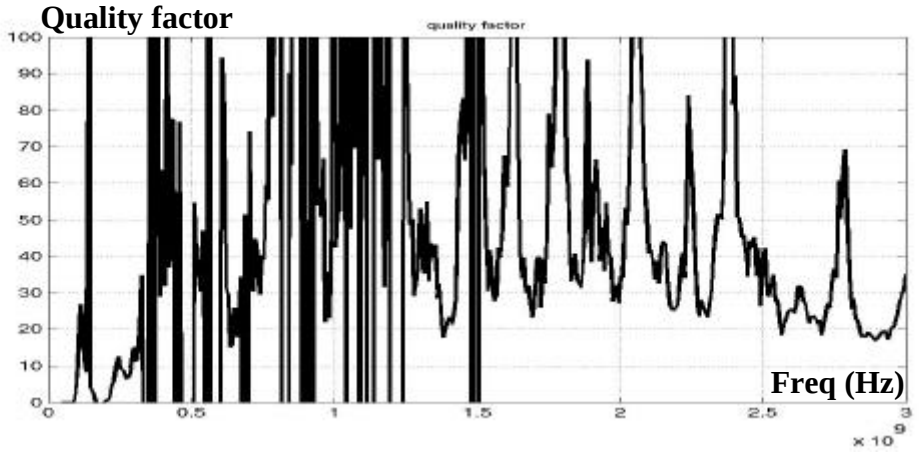

Fig. 102 Quality factor of the testing pads of the passive components vs. frequency

Inductor

Fig. 103 shows the testing structure of the spiral inductor. The lower layer of the inductor is connected to the ground pads as it is connected to VDD (which is also an AC ground) in the voltage-controlled oscillator.

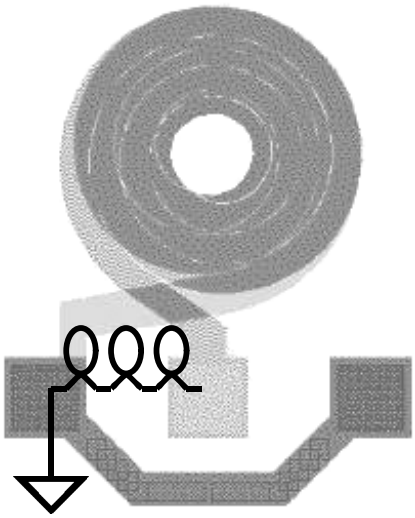

Fig. 103 Testing structure of the spiral inductor

After extracting the Z-parameter from the S-parameter, the inductance, resistance and quality factor of the inductor against frequency is shown in Fig. 104, Fig. 105 and Fig. 106. Similar to the prediction from the simulation, the parameters of the inductor strongly depend on the frequency. The inductance is quite constant at the low frequency because the skin effect of the metal, the parasitic capacitance to the substrate and the eddy current in the substrate have little effects until around 1GHz. After 1GHz, the quality factor becomes decreasing instead of increasing. The quality factor at 900MHz is about 2.1. The self-resonance frequency of the inductor is around 2.3GHz where the inductor becomes capacitive.

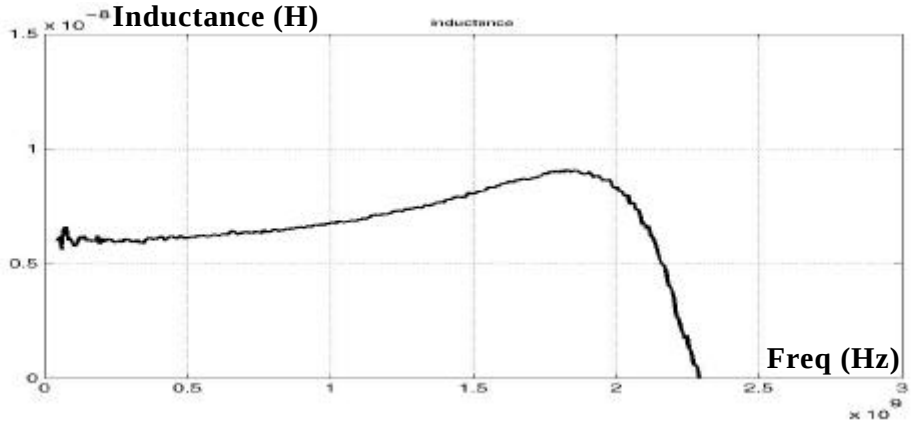

Fig. 104 Inductance of the inductor vs. frequency

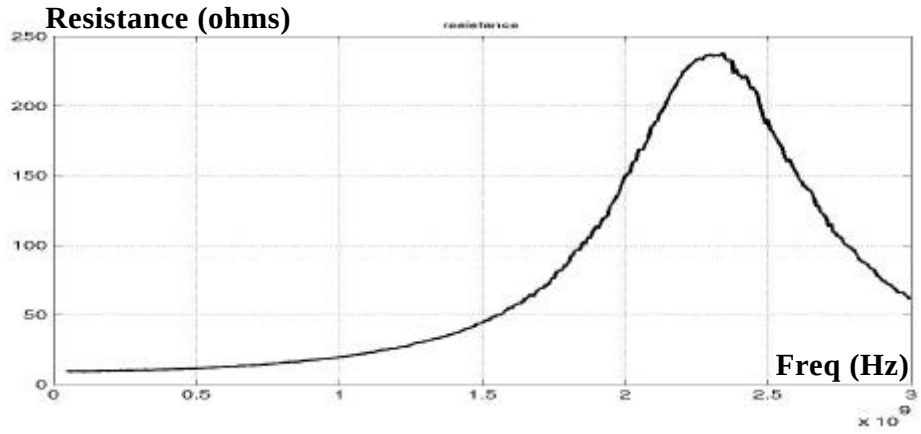

Fig. 105 Series resistance of the inductor vs. frequency

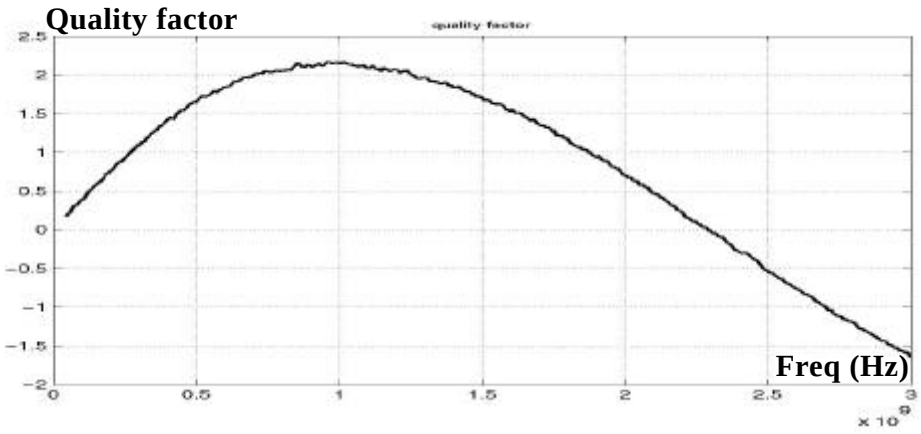

Fig. 106 Quality factor of the inductor vs. frequency

Fig. 107 shows the one-port S-parameter of the inductor. By curve fitting for the frequency between 700MHz and 1GHz, the parameters of the narrow-band model of the inductor, as shown in Fig. 108, can be determined. Both measured inductance and capacitance of the inductor are very close to the simulated values from the ASITIC program used because they are mainly determined by the geometry only. However, the resistances of the inductor are incorrectly predicted by the program due to the ignorance of the loss from the substrate eddy current. Table 4 summarizes the calculated and measured parameters.

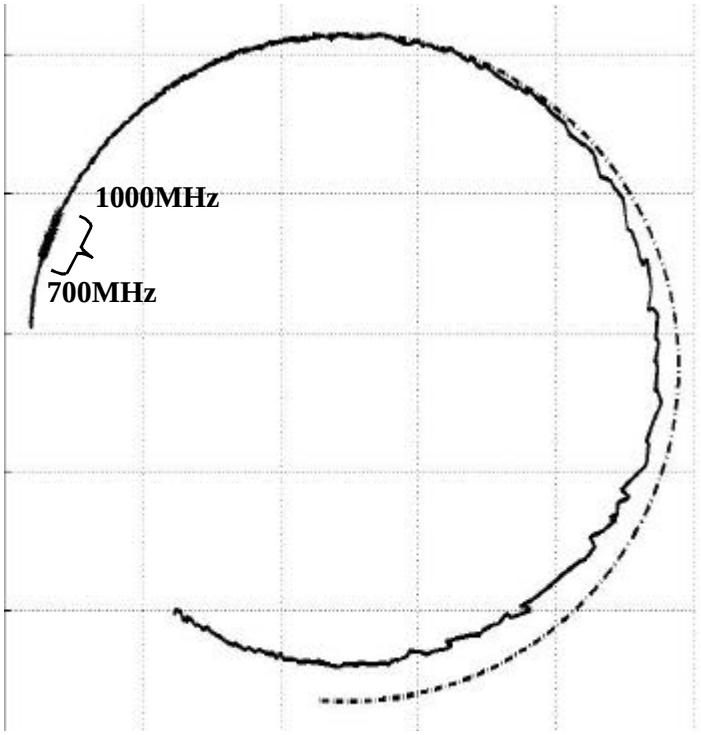

Fig. 107 One-port S-parameter of the inductor and the corresponding fitting curve

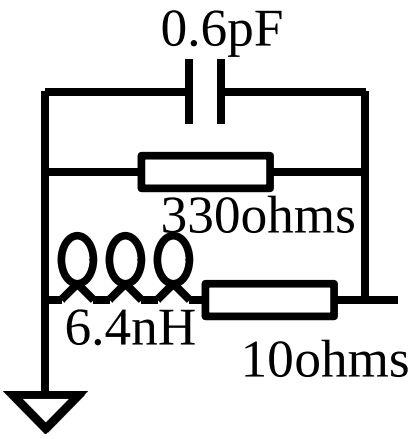

Fig. 108 Narrow band model of the spiral inductor

Table 4 Summary of parameters of inductor

	Calculated	Measured
Inductance	6.6nH	6.4nH
Parasitic capacitance	0.6pF	0.6pF
Quality factor	N.A.	2.1

Varactor

Fig. 109 shows the testing structure of the varactor. The varactor includes the 132 P+ N-well junction diodes and the N-well P-substrate parasitic diodes (186 and 186 unit diodes in the voltage-controlled oscillator). The P+ N-well junction diode is used for the varactor while the parasitic diode adds extra capacitance to the varactor and reduces the available tuning range.

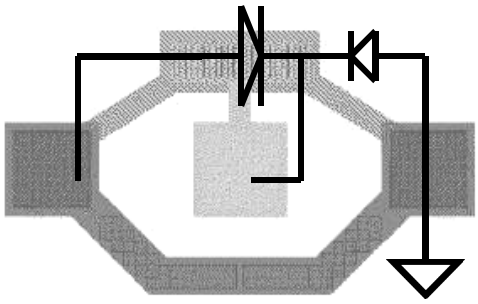

Fig. 109 Testing structure of the varactor

Fig. 110, Fig. 111 and Fig. 112 show the capacitance, the series resistance and the quality factor of the varactor under different bias. Compared to inductor, capacitors are less frequency-dependent. As the reverse bias increases, the capacitance of the varactor is reduced because the depletion width of the diode increases. The increase of the depletion width also reduces the length of the required lossy N-well which the current has to go through. As a result, the quality factor increases. Around the nominal bias condition, 1V reverse bias, the quality factor is around 35 and the capacitance can change about 20% per volt.

When the diode is nearly forward biased. The capacitance increases a lot. The diode also starts to conduct and a lossy parallel resistor is put in parallel to the varactor. Therefore, the quality factor of the varactor is very poor when it is nearly forward biased. Table 5 shows the summary of parameters of the varactor. The measured

capacitance and tuning range is larger than the designed values. It may be due to higher doping on N-well which increases the capacitor P+ N-well diodes.

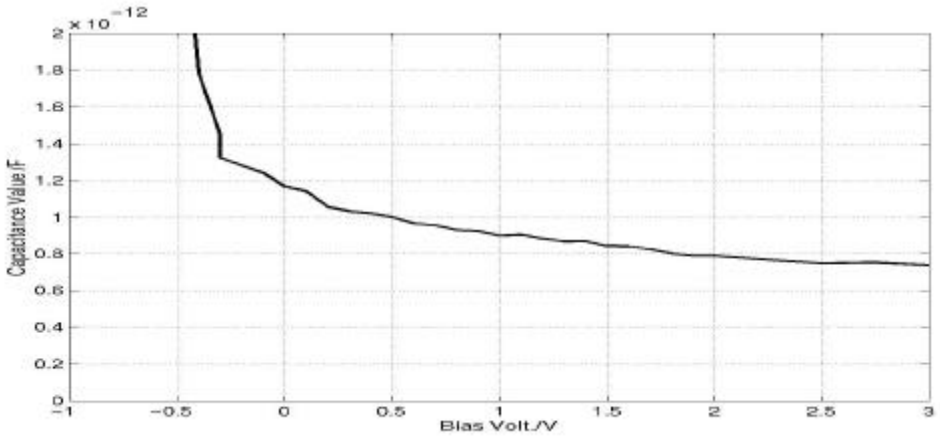

Fig. 110 Capacitance of the varactor vs. bias

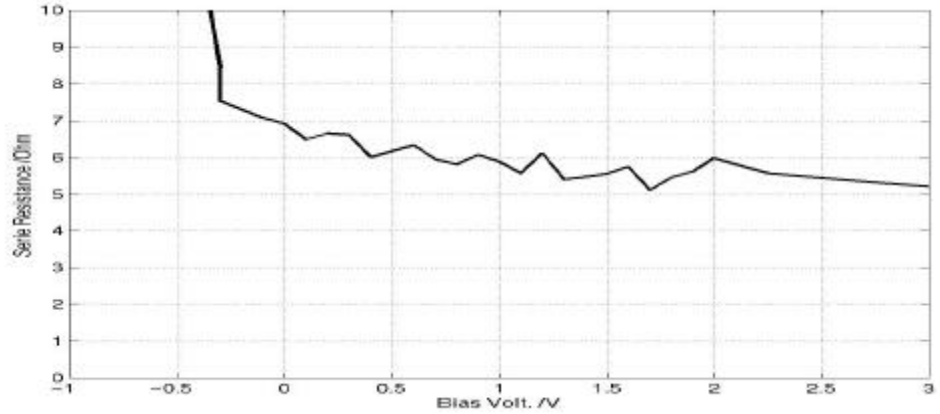

Fig. 111 Series resistance of the varactor vs. bias

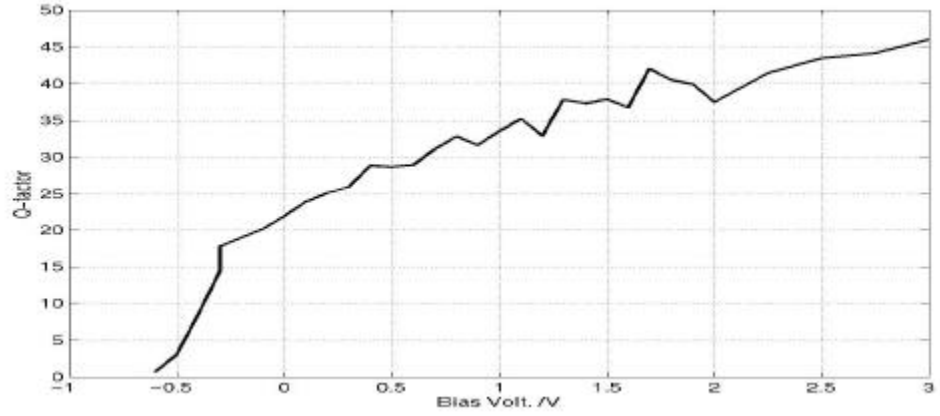

Fig. 112 Quality factor of the varactor vs. bias

Table 5 Summary of parameters of varactor (132 diodes)

	Calculated	Measured
Capacitance at 1.5V reverse bias	0.454pF	0.85pF
Capacitance at 0.5V reverse bias	0.496pF	1pF
Tuning per volt (around 1V reverse bias)	9%	15%
Quality factor	N.A.	35

To find out the net effect of the parasitic N-well substrate diode, the testing structure shown in Fig. 113 is used. The measured capacitance, series resistance and quality factor of this parasitic diode against frequency are shown in Fig. 114, Fig. 115 and Fig. 116With 1.5V supply, this parasitic diode is always 1.5V reverse biased. The capacitance of it contributes to about 30% of the total capacitance of the varactor. The quality factor is around 35 which is similar to the value of the whole varactor. Table 6 shows the summary of the N-well substrate parasitics.

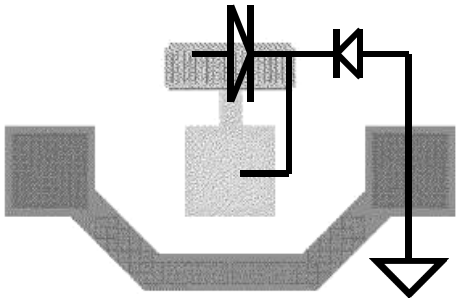

Fig. 113 Testing structure of the N-well substrate parasitic diode

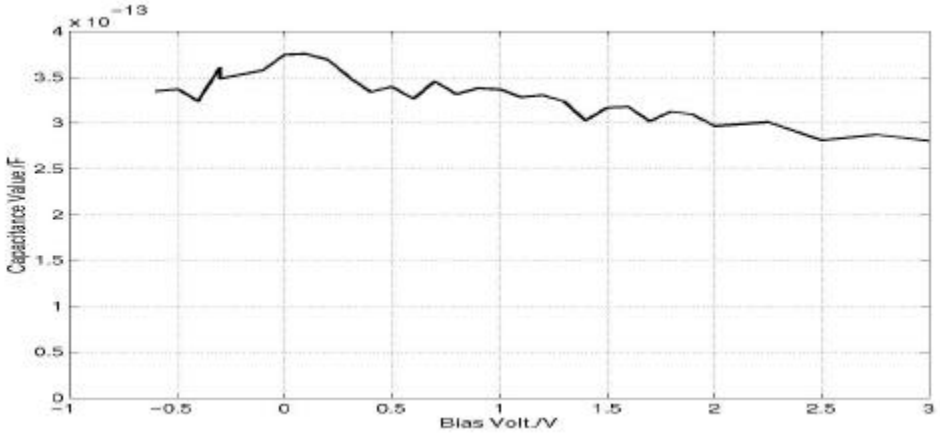

Fig. 114 Capacitance of the N-well substrate parasitic diode vs. bias

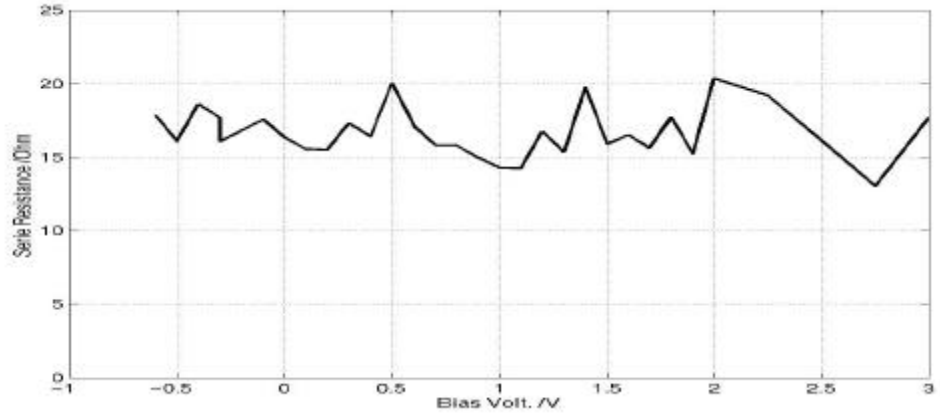

Fig. 115 Series resistance of the N-well substrate parasitic diode vs. bias

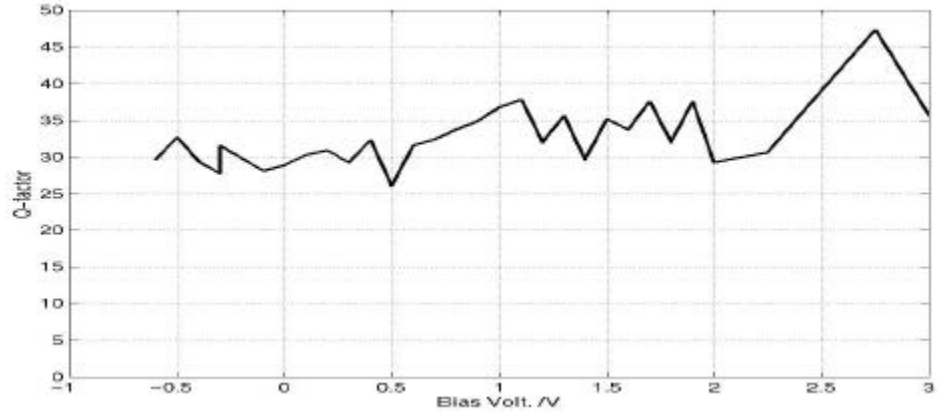

Fig. 116 Quality factor of the N-well substrate parasitic diode vs. bias

Table 6 Summary of N-well substrate parasitcs

	Calculated	Measured
Capacitance at 1.5V reverse bias	0.2pF	0.3pF

Switchable-capacitor array

The testing structure is shown in Fig. 117 while the bias to the NMOS switch is connected to some other peripheral bonding pads. The capacitance, series resistance and quality factor of the switchable-capacitor array against gate voltage on the switches are measured and shown in Fig. 118, Fig. 119 and Fig. 120. Similar to the varactor and other capacitors, the switchable-capacitor array has a very weak frequency-dependency. When the switch is turned off, the capacitance is only 60% of the maximal value (2.4pF) with the on-switch. The quality factor is 11 and 15 when the switch is turned off and turned on with 1.5V respectively. The lower quality of the turned-off array is because the current has to flow in the parasitic capacitors which are in serial with the high-resistive substrate. The turned-on quality factor mainly depends on the turned-on resistance of the NMOS switch. The quality factor can be improved by increasing the bias voltage to the switch, but it can only has little effects on the overall all quality factor of the LC tanks due to the domination by the inductor's quality factor. As expected, when the switch is slightly turned on with 0.65V, the quality factor of the array is the poorest. As the quality factor is larger than 1 (or reactance is smaller than resistance), the value of the capacitance determines where the current goes. Therefore, even the series resistance is very high, the most of the current still prefers to flow in the linear capacitor and the NMOS switches instead of the low-resistive parasitic capacitors. Thus, the quality factor is very low (but still larger than one) when the switch is slightly turned on.

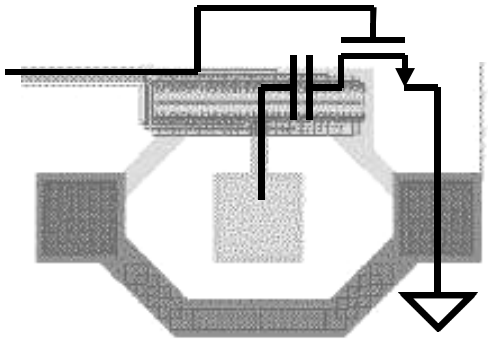

Fig. 117 Testing structure of the switchable-capacitor array

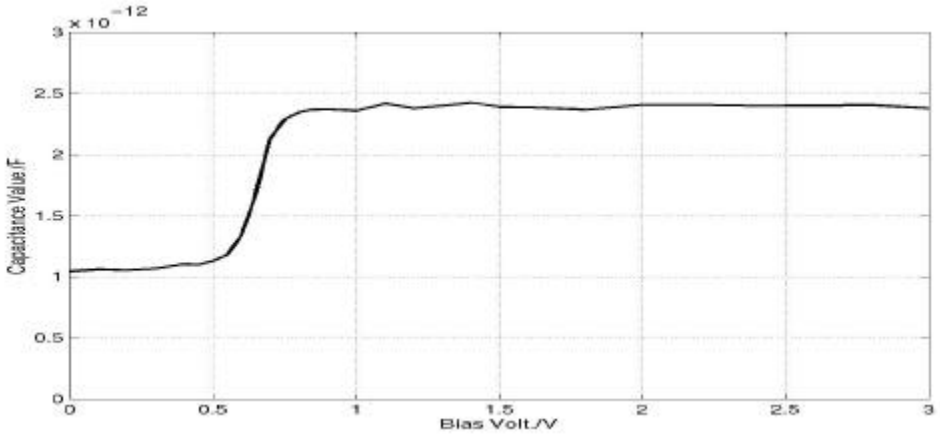

Fig. 118 Capacitance of the switchable-capacitor array vs. bias

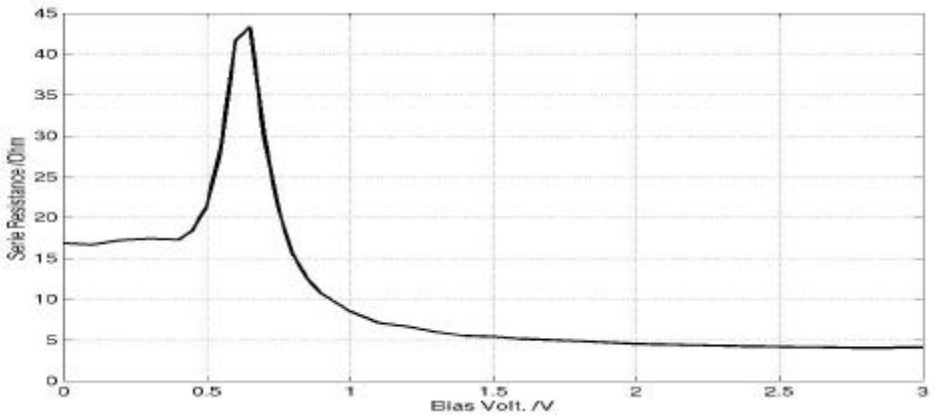

Fig. 119 Series resistance of the switchable-capacitor array vs. bias

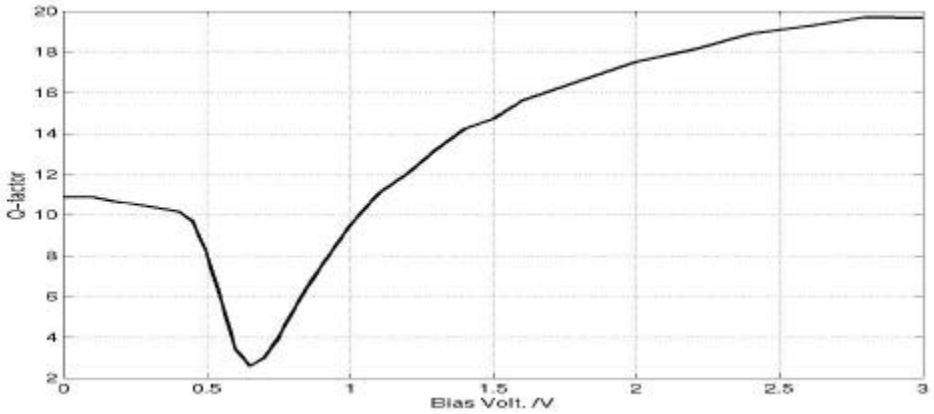

Fig. 120 Quality factor of the switchable-capacitor array vs. bias

Not only the switch has series resistance, the linear capacitor also has some resistance due to the resistance of the two electrodes (poly and N+ active). To measure the net performance of the linear capacitor, the testing structure shown in Fig. 121 is used in which all the NMOS switches are shorted by metal. The measured results are shown in Fig. 122, Fig. 123 and Fig. 124. Similar to other capacitors, the capacitance and resistance are weakly frequency-dependent. The series resistance is 2 ohms which contributes to 1/3 of the total resistance (6 ohms) of the switchable-capacitor array. The quality factor of the linear capacitor is 40 at 900MHz.

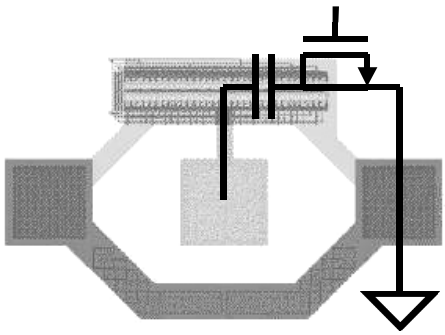

Fig. 121 Testing structure of the linear capacitor of the switchable-capacitor array

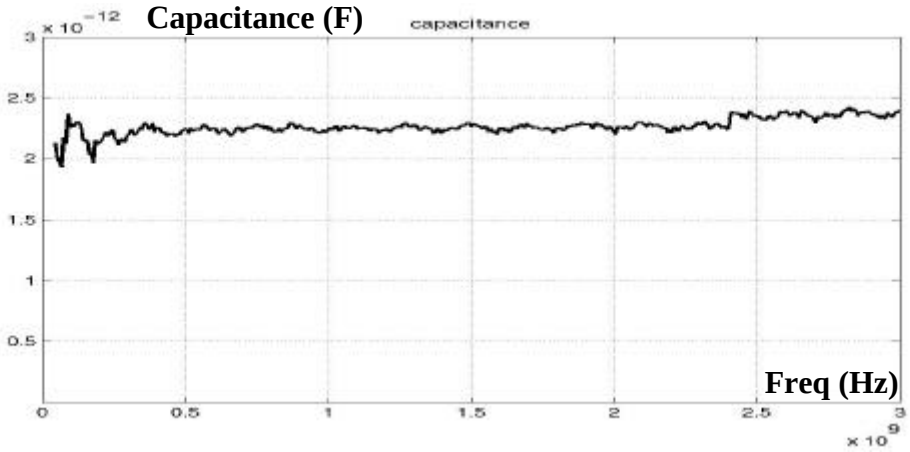

Fig. 122 Capacitance of the linear capacitor vs. frequency

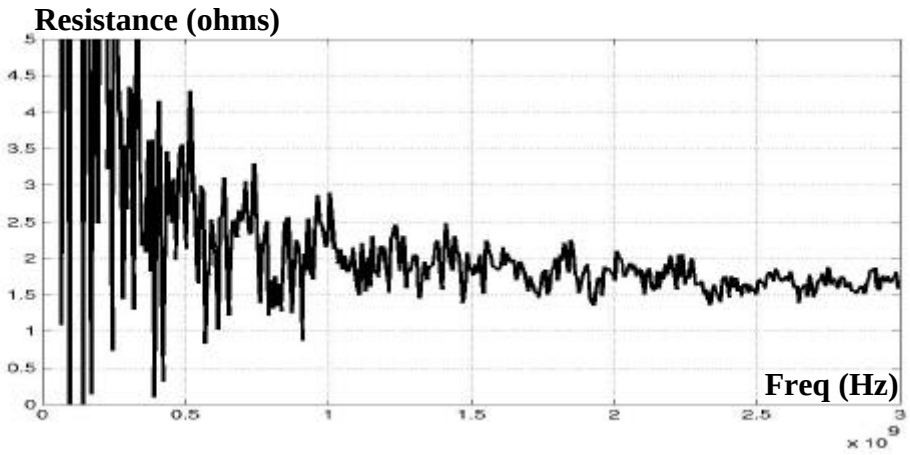

Fig. 123 Series resistance of the linear capacitor vs. frequency

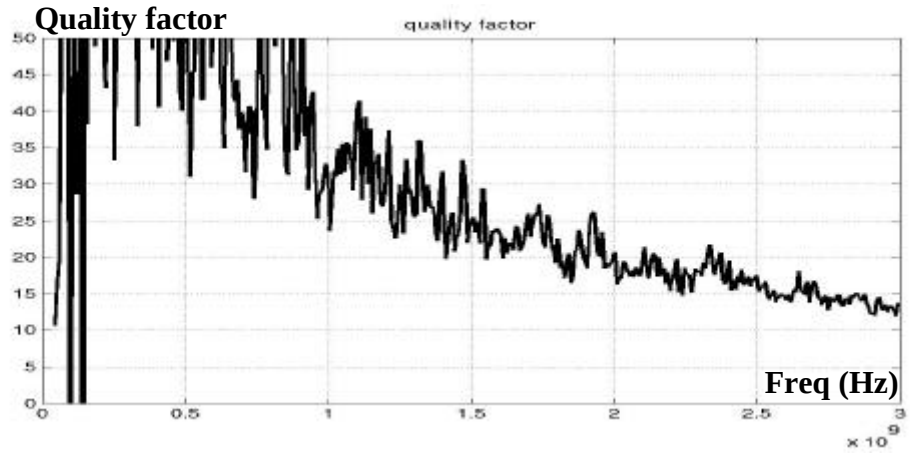

Fig. 124 Quality factor of the linear capacitor vs. frequency

Table 7 shows the summary of parameters. The increase in capacitance is due to the increase in both capacitances of the Nwell substrate parasitics and the linear capacitors.

The decrease in quality factor is due to the ignorance of the quality factor of the linear capacitors.

Table 7 Summary of parameters of switchable-capacitor array

	Calculated	Measured
Capacitance (tuned-on with 1.5V)	1.95pF	2.4pF
Capacitance (tuned-off)	0.61pF	1.05pF
Tuning range	63%	56%
Quality factor (tuned-on with 1.5V)	19	15
Quality factor (tuned-off)	N.A.	11
Capacitance of linear capacitors	1.95pF	2.3pF
Quality factor of linear capacitors	N.A.	40

Voltage-controlled oscillator and frequency synthesizer

Testing setup

The testing setup for VCO and frequency synthesizer measurements is shown in Fig. 125. A signal generator is used to provide the frequency reference source for the synthesizer. A computer program is used to provide the channel selection word to the synthesizer and program the shift register for saving the number of peripheral pads, which stores the coefficients for the gain and offset adjustments. Bond wires and flat cables are used to connect the frequency synthesizer to the parallel port of the computer. A data generator or a pulse generator is used to direct modulate the frequency synthesizer. A high-impedance probe or a DC probe connected to a signal analyzer is used to measure the tuning voltage of the voltage-controlled oscillator. The high-impedance probe is used when the dynamic response of the frequency synthesizer is measured. The DC probe is used when the internal bias condition is measured. The

output of the voltage-controlled oscillator is probed by a high-impedance probe or a DC probe and amplified by a low-noise amplifier. Both the high-impedance probe and the DC probe which have the similar attenuation of 26dB at 900MHz can be used because there are output buffers, as shown in Fig. 126, between the voltage-controlled oscillator and the pads. However, the driving power of the on-chip output buffers is too small and the attenuated signal is too small to be measured by the spectrum analyzer. Therefore, the low-noise amplifier is needed to amplify the signals. The spectrum analyzer is used to measure the phase noise and spur performance of the signal.

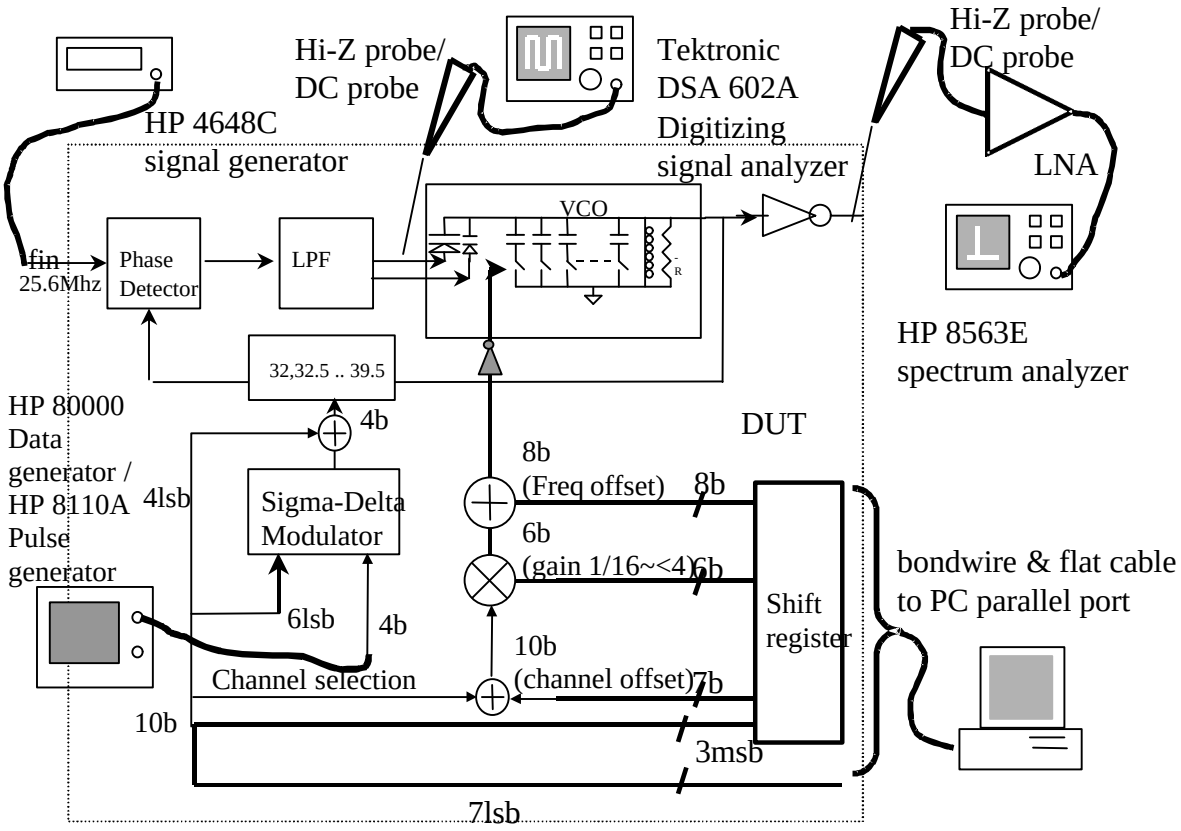

Fig. 125 Testing setup for VCO and synthesizer measurements

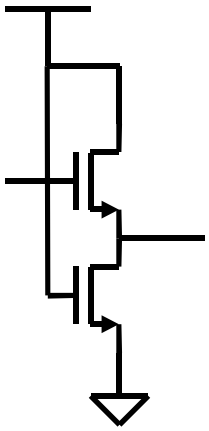

Fig. 126 Schematic diagram of the pad buffer for the VCO outputs

The whole synthesizer is fabricated on a single chip. The chip (a) is glued on a printed circuit board (PCB), as shown in Fig. 127. All the DC biases, low-speed inputs and outputs are connected by bond wires from the die to the PCB. The DC biases (b) are connected to a battery DC supply through flat cables. The frequency reference source from a signal generator is connected through SMA cable to SMA connector (c) on the PCB. The channel selection word (d) and the shift register's inputs and outputs (e) are connected through flat cables the computer. The digital modulation inputs (f) are controlled through the SMA cables from the data generator.

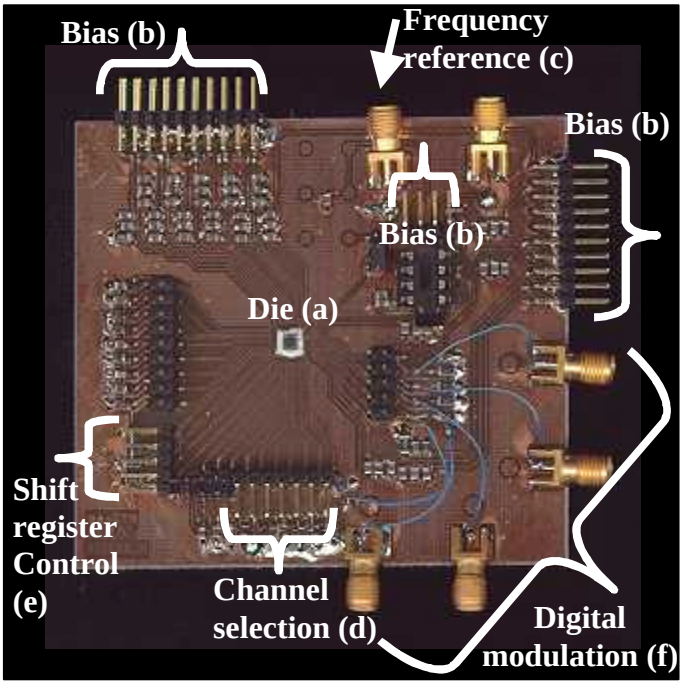

Fig. 127 Printed circuit board for VCO and synthesizer measurements

Frequency tuning by switchable-capacitor array

The switchable-capacitor array inside the voltage-controlled oscillator can provide monotonic frequency tuning from 760-980MHz as shown in Fig. 128. In this 8-bit switchable-capacitor array, each least-significant bit (LSB) corresponds around 0.6MHz frequency change at 760MHz and 1.25MHz frequency change at 980MHz, as shown in Fig. 129. Compared to the designed tuning range (800MHz – 1100MHz), the frequency is shifted down and the tuning range is smaller due to larger capacitance in the switchable-capacitor array. At the 890MHz, each LSB is about 1MHz which is about five channel spacings. The differential-non-linearity (DNL) of the switchable-capacitor array due to the mismatches between the unit switchable capacitors is much less than 0.5 LSB. Thus it is possible to use a switchable-capacitor array of larger number of bits to provide finer frequency step and higher resolution. The only limitations are the minimal feature sizes of capacitors and switches and the extra parasitic capacitance added due to the increase of redundancy and longer peripheral of the smaller devices.

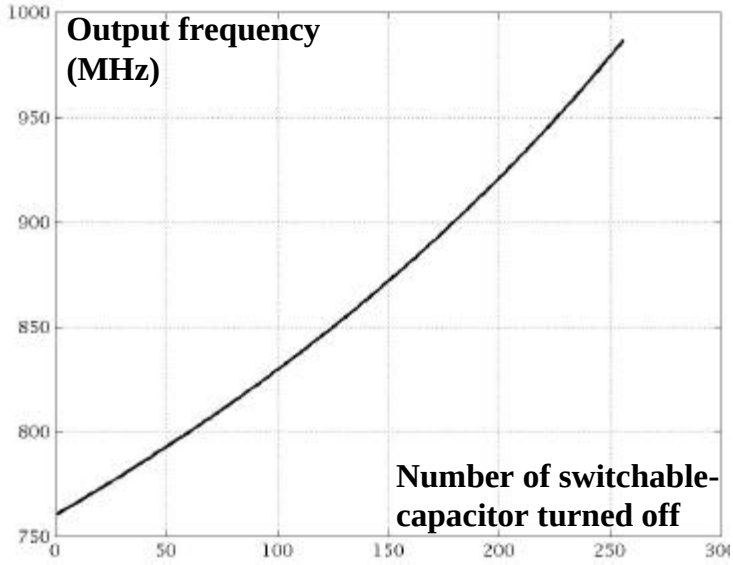

Fig. 128 Fequency tuning by the switchable-capacitor array

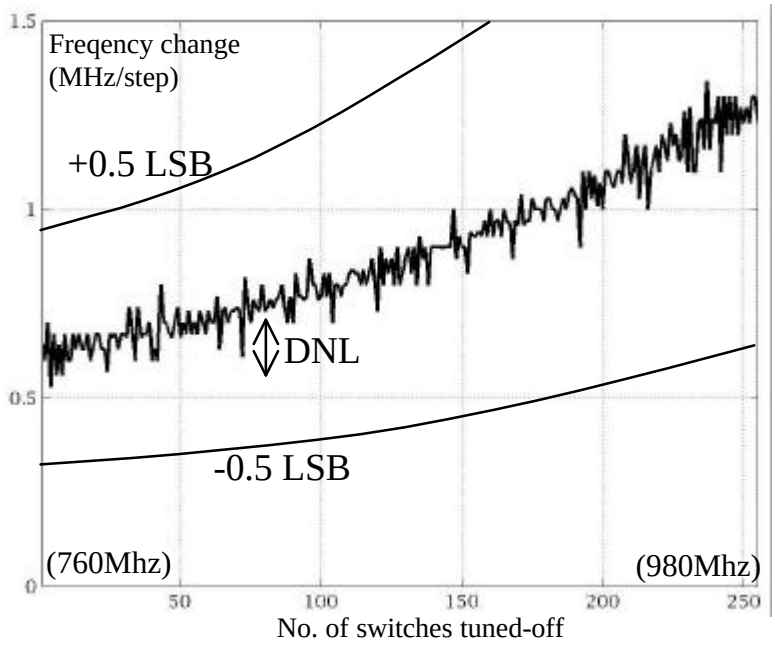

Fig. 129 Frequency change per step

Frequency tuning by varactor

The varactor inside the voltage-controlled capacitor is used to provide the frequency tuning within the minimal frequency step (~1MHz) provided by the switchable-capacitor array. Fig. 130 shows the frequency tuning by the varactor at the lowest frequency (around 750MHz, dashed line), at the highest frequency (around 970MHz,

solid line) and the nominal frequency (around 890MHz, dotted line). With 0-1.5V tuning voltage (or 1.5-0V reverse biased), the corresponding frequency tuning is 756-748MHz, 899-885MHz and 975-957MHz.

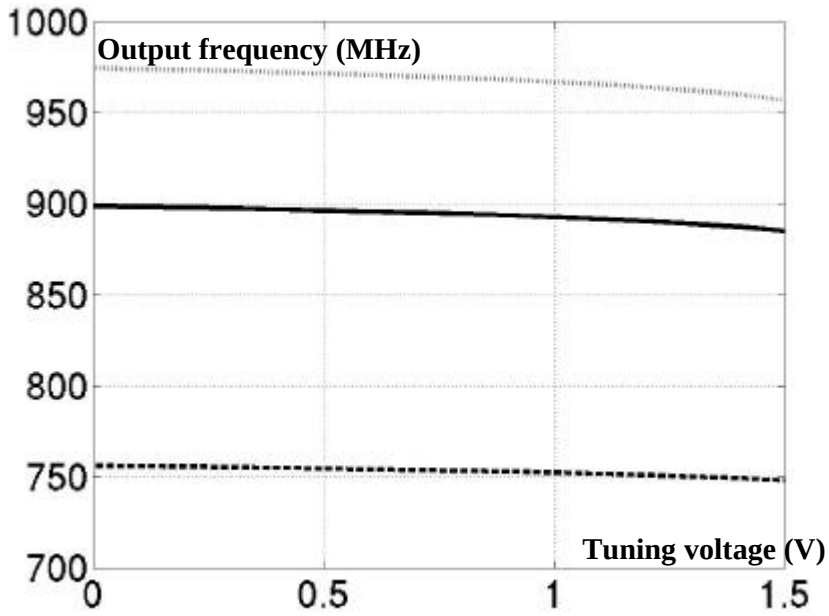

Fig. 130 Frequency vs. tuning voltage of the voltage-controlled oscillator

The gains of the voltage-controlled oscillator at these three frequency ranges are shown in Fig. 131. At nominal bias condition, the gains are 4MHz/V, 6MHz/V and 7MHz/V at 750Mhz (dashed line), 900MHz (solid line) and 970MHz (dotted line). The gains increase when the tuning voltage increases. The maximal values 13MHz/V, 23MHz/V and 33MHz/V are obtained when the tuning voltage is closed to 1.5V. Compared to the designed gain at 900MHz (9MHz/V), the measured gain is smaller due to the larger capacitance in the switchable-capacitor array.

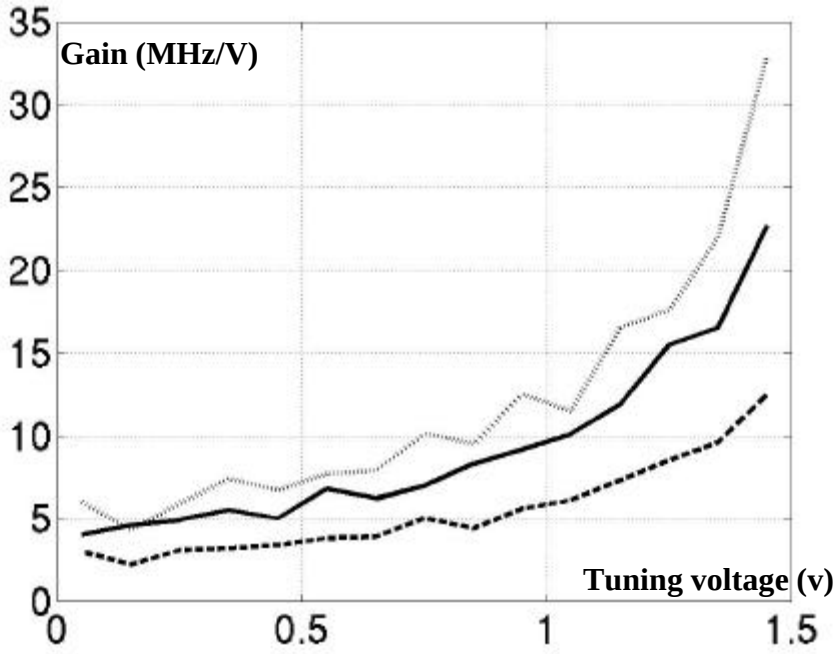

Fig. 131 Gain of voltage-controlled oscillator vs. tuning voltage

Amplitude and phase matchings

This voltage-controlled oscillator can provide quadrature outputs for the image-rejection mixer. The amplitude and phase matchings of the quadrature outputs of the oscillator affect the available image rejection. Since the outputs are at high frequency, it is very difficult to directly measure the phase difference between the quadrature outputs. Instead of directly measuring the phase, a single-sideband mixer as shown in Fig. 132 can be used to measure the amplitude and phase matchings. A low-frequency quadrature signal is applied to the mixer and up-converted by the quadrature output of the voltage-controlled oscillator. The up-converted signal contains the wanted sideband and the unwanted sideband. Assuming the low-frequency quadrature signal has very good amplitude and phase matchings, the amplitude difference between the two sidebands can show the mismatches in the quadrature outputs of the voltage-controlled oscillator. The measured amplitude difference between two sidebands is around 30dB which corresponds to smaller than 1-degree phase mismatch and 0.1-dB amplitude

mismatch. More importance is that the 30-dB amplitude difference shows that the quadrature outputs of the oscillator can provide 30-dB image rejection when it is applied to an image-rejection mixer. Without the shared current source used in the voltage-controlled oscillator, the oscillator can only provide around 10-dB image rejection.

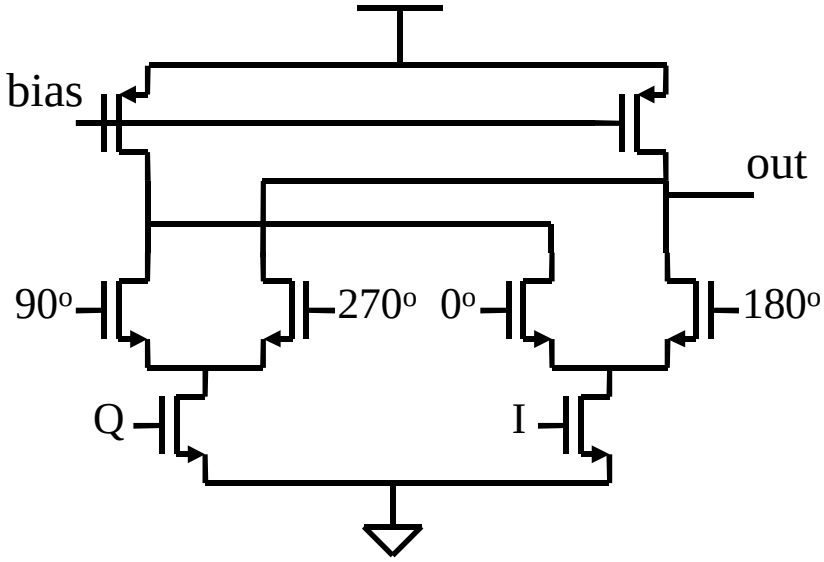

Fig. 132 Schematic diagram of the SSB mixer

Frequency synthesizer calibration and operation

In this frequency synthesizer, the output frequency depends on not only the varactor tuning but also the switchable-capacitor array. The lowest seven bits of the channel selection word, which represents the 125 channels, are used to control the switchable-capacitor array to obtain the correct output frequency. Since these seven bits only represent the channel number but not the exact frequency of the channel, a frequency offset is added to obtain the correct frequency for the channels.

Each least significant bit of the switchable-capacitor array will represent different frequency change at different frequency ranges. The frequency change will also depend

on the process variation. Therefore, a gain adjustment is required to make each LSB of the channel selection word to correspond to 200kHz frequency change.

With the correct offset and gain adjustments, the 125 channel selection words will represent the exact 125 channel frequencies in the receiver band. The criterion to calibrate the offset and gain adjustments is that the phase-locked loop works correctly within these 125 frequencies. The offset adjustment coefficient can be adjusted until the average value of the tuning voltage is the nominal value (0.55). Then the gain adjustment coefficient can be calibrated until the average tuning voltages of the first and second half of the frequency range are both around 0.55V. Fig. 133 shows the tuning voltage against channel number with too large, too small and optimal gain adjustments. Only one calibration at the most beginning is required and the coefficients for the gain and offset adjustments can be always stored and reused.

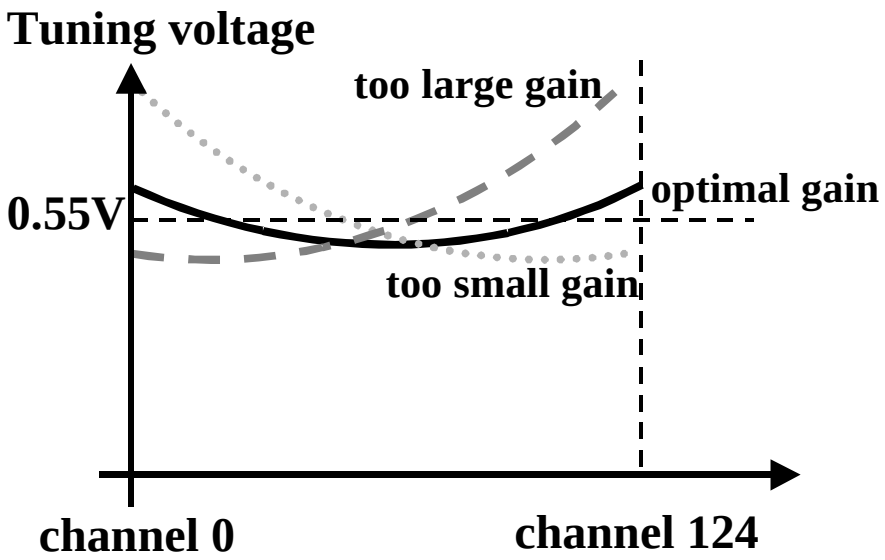

Fig. 133 Tuning voltage vs. channel number with different gain adjustments

The measured tuning voltage of the varactors as a function of the channel number is shown in Fig. 134. The average value is 0.55V. The maximal variation of the tuning voltage is 0.24V for total 1.2-MHz frequency error. It is due to a) the finite frequency

resolution, about 1MHz, provided by the switchable-capacitor array, b) the non-linearity of the relation between the frequency and capacitance, which contributes to 300KHz error, c) 250KHz error by the imperfect gain adjustment provided by the digital multiplier of finite number of bits, and d) the differential-non-linearity of the switchable-capacitor array.

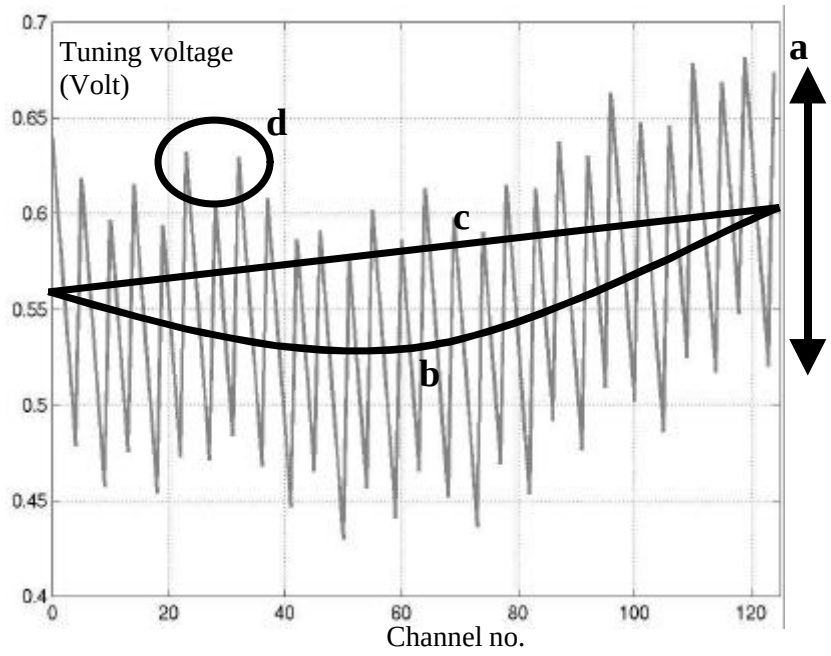

Fig. 134 Tuning voltage of the VCO vs. channel number

Ideally, the two charge pumps used for the dual-path filter are matched. The output current of the large charge pump should be B times of the current of the small charge pump. Unfortunately, there is mismatch between the two charge pumps. When the loop is in locked state, the integrator has a constant output to keep the constant output frequency of the voltage-controlled oscillator. As a result, no net current is provided by the small charge pump. The large matched charge pump should also provide zero net current to the low-pass filter and the output of the low-pass filter is zero. However, as shown in Fig. 135, if there is mismatch between the two charge pumps. Even in the locked state. There is an offset current (Ios) flowed into the low-pass filter and an offset

voltage (Vos = Rp x Ios) appeared. If the offset voltage is large due to the large Rp or an offset current, the output of the large charge pump may be out of the normal operation region. As a result, the low-pass filter path will have smaller gain due to the small output of the large charge pump. Thus, a much smaller loop bandwidth will be obtained. In order to get the designed loop bandwidth, the two charge pumps have to be adjusted to be matched. The adjustment can be done by monitoring the output of the low-pass filter such that the output voltage is the nominal value (0.55V).

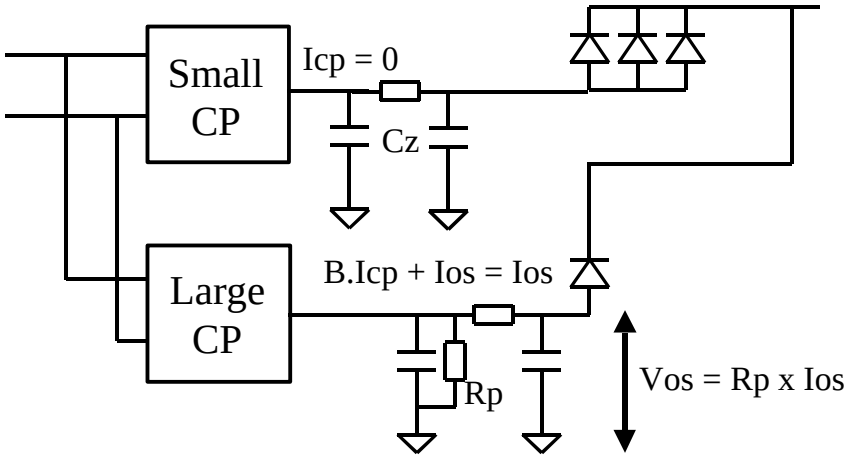

Fig. 135 Schematic of charge pumps and dual-path filter

Phase noise

As shown in Fig. 136, the phase noise of the synthesizer at 400KHz and 600KHz offset is –116dBc/Hz and –118dBc/Hz, respectively. Since the frequencies are out of the loop bandwidth, they are mainly determined by the phase noise of the free-running voltage-controlled oscillator. However, the phase noise of the oscillator is limited by the poor quality of the spiral inductors which is about 2.1. Within 200KHz offset, the phase noise with the slope –30dBc/decade is dominated by the flicker noise of the transistors in the oscillator.

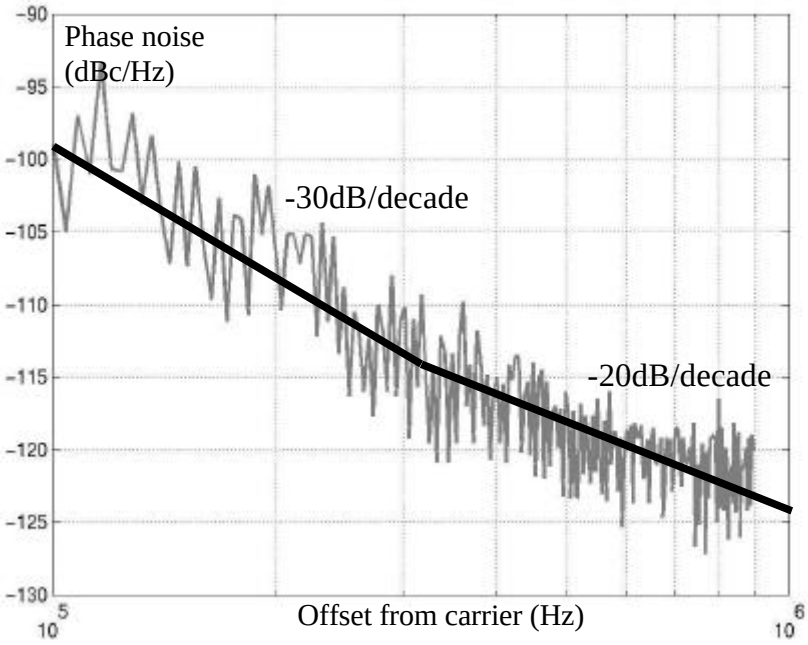

Fig. 136 Phase noise of the frequency synthesizer

Spurs

Despite the high tolerance of substrate noise, the reference frequency of 25.6MHz can still couple to the VCO and spurs of –67dBc at 25.6MHz offset is observed as shown in Fig. 137. It is due to the short separation (~200μm) in this dense layout between the circuits clocked by the reference frequency and the voltage-controlled oscillator.

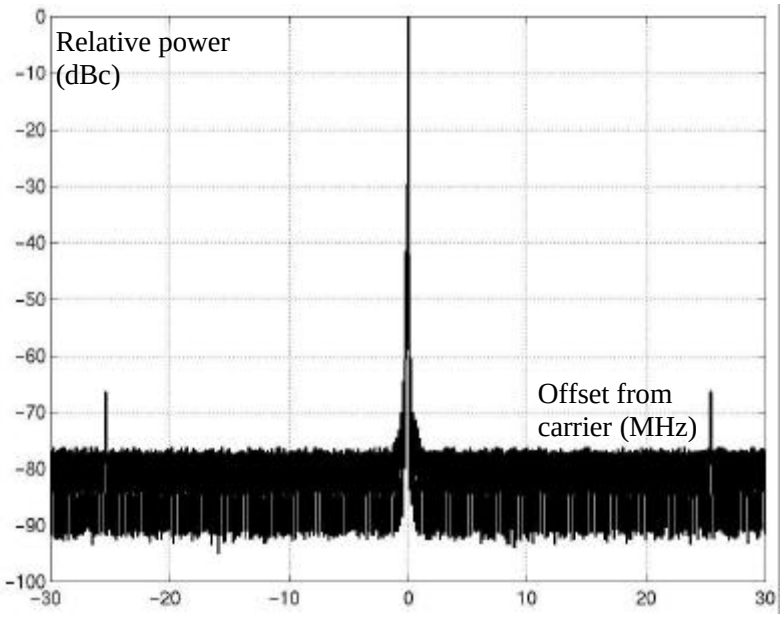

Fig. 137 Output spectrum of the frequency synthesizer

Although the spurs are quite large, they are located at 25.6MHz apart from the center frequency. Only the background noise outside the receiver band, which is already attenuated by RF image-rejection filter, will be down-converted by the spurs to the intermediate frequency.

Frequency switching

The measured loop bandwidth is 80KHz as designed. To measure the settling time of the frequency synthesizer, the tuning voltage of the synthesizer is measured during the frequency transition. The worst case settling occurs when there is a maximal change in the tuning voltage. In this case, the settling time is less than 150μsec for the output frequency within 20KHz of the final value, as shown in Fig. 138. Since the switchable-capacitor array changes the total capacitance in the LC tank of the voltage-controlled oscillator when the channel selection word starts to change, there are glitches in the tuning voltage before the loop starts to settle down.

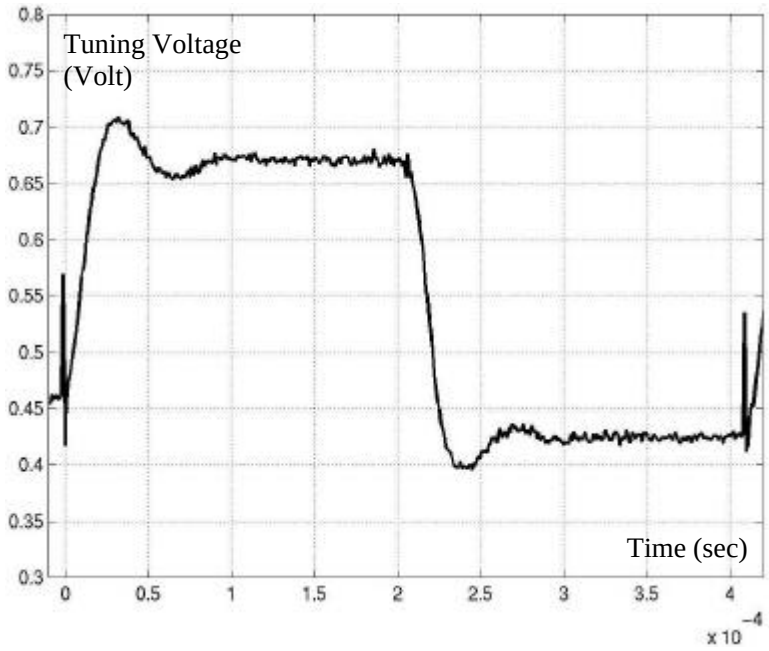

Fig. 138 Tuning voltage of the VCO during frequency switching

Digital modulation

If the division ratio of the prescalar changes rapidly, the output frequency of the synthesizer will be modulated. In this frequency synthesizer, the lowest 4 bits of the sigma-delta modulator can accept the baseband modulation signals. Since the sigma-delta modulator is clocked by the output of the prescalar, the baseband modulation signals have to synchronize to the output of the prescalar. An open-drain buffer shown in Fig. 139 is used to provide the clock signal for the baseband modulation signals. A new set of baseband modulation signals will be applied for every period of this clock signal. The required baseband modulation signals can be generated from a Matlab program in the computer and stored in a pattern generator or a very long shift register. However, due to the incompatibility between the disk formats of the pattern generator and the computer, the generated baseband modulation signals cannot be applied to the pattern generator. A solution is to use Labview to control the GPIB interface of the pattern generator. However, due to the limitation of time, it has not been done.

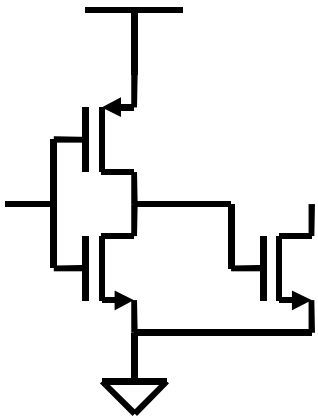

Fig. 139 Schematic diagram of the pad buffer for the prescalar output

For a GMSK modulation, a non-return-to-zero data bit stream is filtered by a Gaussian filter. The filtered bit streams will modulate the frequency of the output of the frequency synthesizer. Fig. 140a and Fig. 141a show the simulated spectrum of a

GMSK signals with 0.3 BT and a bit rate of 270k bits per second. The maximal frequency deviation of a GMSK modulation is +/- 67.5kHz which is a quarter of the bit rate. Originally, the non-return-to-zero data bit stream contains only 1 and 0 which correspond to +67.kHz and –67.5kHz frequency deviations. However, the filtering creates all the levels between 1 and 0 and all the frequency deviations between +67.5kHz and –67.5kHz are needed. Since a digital sigma-delta modulator of 10 bits is used, the smaller frequency resolution of the frequency synthesizer is only 12.5kHz. With a finite frequency resolution, the input frequency deviations will be quantized and the noise floor will rise due to the quantization noise as shown in Fig. 140b and Fig. 141b.

Instead of increasing the bit width of the sigma-delta modulator to reduce the minimal frequency resolution, a sigma-delta representation of the filtered data bit stream is used. The sigma-delta data bit stream uses only 1 and 0 to represent all the quantization levels in between and only high-pass quantization is generated. Due to the low-pass transfer function from the prescalar to the output of the frequency synthesizer, the high-pass quantization is filtered out. With first-order sigma-delta data bit stream clocked at 25.6MHz, the simulated spectrum, as shown in Fig. 140c and Fig. 141c, is very closed to the original GMSK signal (Fig. 140a and Fig. 141a).

Higher-order sigma-delta data bit stream (at most third-order) can be used to further reduce the quantization noise due to more noise shaping. However, the higher-order sigma-delta has the outputs with a larger swing. For example, a second-order sigma-delta modulator has the outputs from –1 to +2 which correspond to –67.5kHz and +135kHz (202.5kHz in total) frequency deviation. However, only the least four bits of this frequency synthesizer can accept the modulation inputs. These four bits can only

provide maximal 100 + 50 + 25 +12.5 = 187.5kHz frequency deviation. Therefore, higher-order sigma-delta bit stream is not accepted in this design. A little modification (just rewiring some inputs of the sigma-delta modulator) of this design in the future is required to accept high-order sigma-delta bit stream. Instead of connected to the lowest four bits of the sigma-delta modulator (bit 0, 1, 2, 3), the modulated inputs are connected to bit 4, 5, and 6 which correspond to the frequency deviations of 200kHz, 400kHz and 800kHz. In this case, the frequency synthesizer can be modulated to any frequency within the 200-kHz channel.

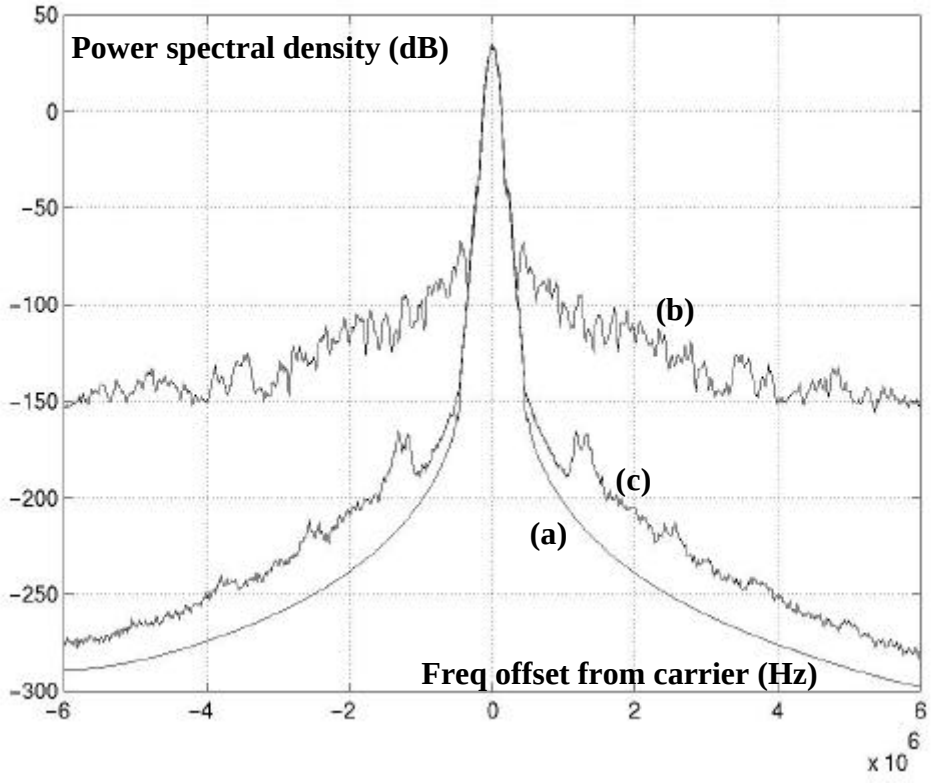

Fig. 140 Simulated spectrum of GMSK signals

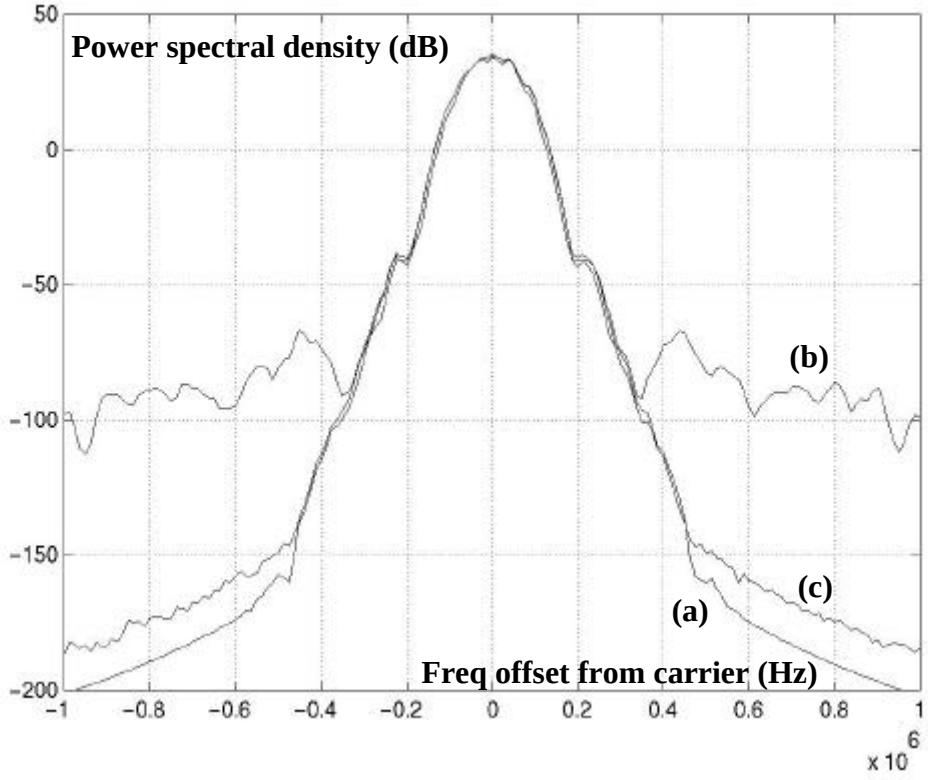

Fig. 141 Zoomed-in simulated spectrum of GMSK signals

Although the GMSK modulation cannot be tested due to problem of the pattern generator, some digital modulation can still be tested. Instead of using the pattern generator, a pseudo-random pattern generator is used. The pseudo-random pattern generator can generate a non-return-to-zero bit stream and the bit stream can be used to modulate the frequency synthesizer. Instead of the GMSK modulation, the FSK modulation is tested since the bit stream is not filtered. Fig. 142 shows the measured spectrums of (a) the baseband bit stream with bit rate 100k bit per second and (b) the corresponding FSK signal with the maximal frequency deviation being half of the bit rate (+/- 50kHz). Compared to the simulated spectrums using a Matlab program, the measured sidelobe power levels are higher. It is due to some non-linearity of the loop.

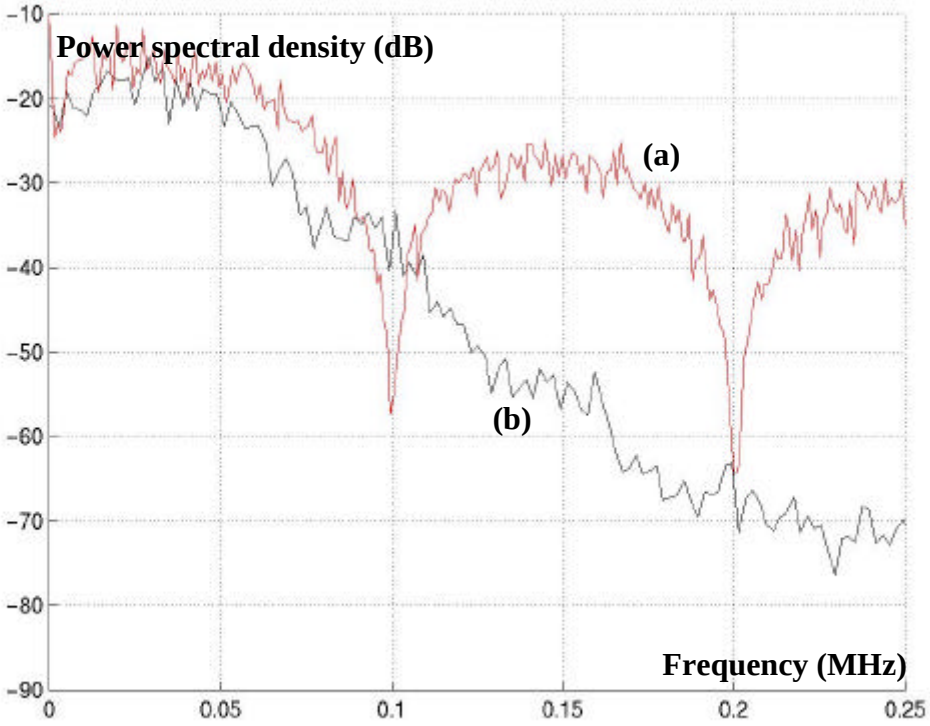

Fig. 142 Measured spectrums of a) the baseband signal and b) the corresponding FSK signal

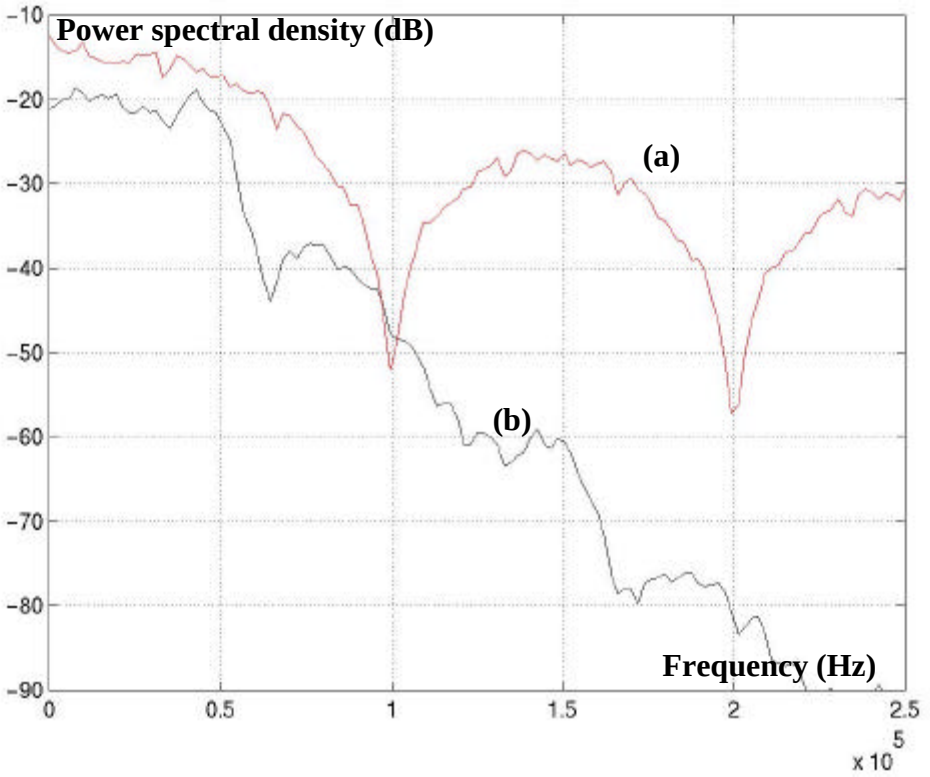

Fig. 143 Simulated spectrums of a) the baseband signal and b) the corresponding FSK signal

Summary of performance

A summary of performance of the voltage-controlled oscillator and the frequency synthesizer is shown in Table 8 and Table 9. Due to the larger capacitance in the switchable-capacitor array, the center frequency and the gain of the voltage-controlled oscillator is smaller while the frequency-tuning step is larger. The phase noise performance is 1dB lower than the design value because the unexpected poor quality factor of the inductor. Most of the measured performances of the frequency synthesizer meet the design specifications including the frequency range, frequency resolution, settling time, loop bandwidth, supply voltage, power consumption and chip area. The spurs, which cannot be predicted, is quite large because of the aggressive layout. However, due to the carefully designed reference frequency 25.6MHz used, the spurs will not be a serious problem in the receiver system. Due to the problem of testing setup, the GMSK modulation cannot be tested. Only the FSK modulation can be tested but it can still demonstrate the ability of digital modulation of the frequency synthesizer.

Table 8 Summary of performances of VCO

	Design specifications	Measured performances
Tuning range by SCA	800 – 1100MHz	760 – 980MHz
Tuning step by SCA at 890MHz	800kHz	1MHz
Gain by varactor	9MHz/V	5MHz/V
Phase noise	-119dBc/Hz @ 600kHz	-118dBc/Hz @ 600kHz
Amplitude matching	N.A.	< 0.1dB
Phase matching	N.A.	< 1 degree

Table 9 Summary of performances of frequency synthesizer

	Design specifications	Measured performances
Frequency range	865-890MHz (70MHz IF receiver) 890-915MHz (digital modulated transmitter)	844.8-972.8MHz
Frequency resolution	200kHz (or finer for digital modulated transmitter)	12.5kHz
Amplitude matching	N.A.	<0.1dB
Phase matching	N.A.	<1 degree
Phase noise	<-119dBc/Hz @ 600kHz	-118dBc/Hz @ 600kHz
Spurs	<-88dBc	-67dBc @ 25.6MHz
Settling time	<865μsec (or smaller for frequency hopping)	150μsec to within 20kHz
Loop bandwidth	80kHz	80kHz
Digital modulation	GMSK	FSK
Supply voltage	<2V	1.5V
Power consumption	<50mW	30mW
Area	<2mm x 2mm	1.1mm x 0.9mm

Comparison of performance

shows the comparison of performance between this frequency synthesizer and some other reported designs. Most of the other designs are based on fractional-N or dual-loop architecture while this design is based on fractional-N and switchable-capacitor array tuning. Compared to other designs, this design has the smallest supply voltage, power consumption and chip area and the highest loop bandwidth. The phase noise and switching time are similar to the others. Only the spurs are poor than some designs due to the dense layout.

Table 10 Comparison of performances

	JSSC 98 Steyaert[2]	JSSC 96 Tham[4]	Yan[21]	Kan[22]	This work
Center frequency	1.8GHz	900MHz	900MHz	1.8GHz	900MHz
Channel spacing	200kHz	600kHz	200kHz	200kHz	200kHz (12.5kHz)
No. of Channel	124	41	124	103	>124
Process	0.4μm CMOS	25GHz BJT	0.5μm CMOS	0.5μm CMOS	0.5μm CMOS
Architecture	FN	FN	Dual loop	Dual loop	FN & SCA
Supply voltage	3V	2.7-5V	2V	2V	1.5V
Power consumption	51mW	50mW	34mW	95mW	30mW
Reference Freq.	26.6MHz	9.6MHz	205MHz 1.6MHz	100MHz 800kHz	25.6MHz
Chip area	3.23mm^2	5.5mm^2	2.64mm^2	2mm^2	0.99mm^2
On chip filter	Yes	No	Yes	Yes	Yes
Loop Bandwidth	45kHz	4kHz	40kHz 27kHz	120kHz 42kHz	80kHz
Phase noise@600kHz	-121dBc/Hz	-117dBc/Hz	-121dBc/Hz	-111dBc/Hz	-118dBc/Hz
Spurs	-75dBc	<-110dBc	--79.5dBc	-45dBc	-67dBc
Switching time	<250μsec	<600μsec	<830μsec	128μsec	150μsec

Chapter 8 Conclusion

In this research, the main objective is to implement a high-performance frequency synthesizer for the monolithic GSM receiver. In order to solve the various problems faced, some techniques on the frequency synthesizer system and the circuits of the building blocks are proposed.

In the frequency synthesizer system, signals in critical paths are proposed to be processed in capacitance domain instead of voltage and current domain. Based on this proposed idea, a binary-weighted switchable-capacitance array is used to replace the digital-to-analog converter while two varactors connected in parallel replace the voltage adder. This approach provides the advantages of simplified and few analog circuitry (e.g. simple charge pump, no voltage adder, digital-to-analog converter and linearization circuitry), low supply voltage, low power consumption, small chip area, fast frequency switching and high immunity of substrate noise.

Another improvement based on the capacitance domain operation is the loop filter. By using the two paths of the dual-path filter to control two varactors in the voltage-controlled oscillators, the dependency of the two paths is broken. The low-pass filter path which cannot provide any tuning range can be designed to optimize for noise. Around half of the capacitors can be reduced by this improvement. Moreover, since no voltage adder is needed, the proposed approach minimizes both noise and power consumption.

As the voltage-controlled oscillator is the most important building block in the frequency synthesizer, some circuit techniques are also proposed to improve its performance. A technique by combining the current sources of the coupled-LC oscillators can provide a unique amplitude matching control and enhance the quadrature phase matching.

Analysis on the design of the LC oscillator for the optimal noise performance is also done. Based on this, the design techniques are discussed and a novel idea to reduce the excess noise factor is proposed. The proposed idea raises the possibility of zero excess noise factor in the LC oscillator design.

Combing on the above system and circuit techniques proposed, a new design of frequency synthesizer is implemented. The frequency synthesizer also employs the sigma-delta fractional architecture to further enhance the performances. The prototype of this frequency synthesizer has been designed and fabricated to demonstrate the proposed techniques and ideas.

Most of the measured parameters meet the design specifications including the frequency range, frequency resolution, settling time, loop bandwidth, supply voltage, power consumption and chip area. Moreover, this frequency synthesizer is the only reported design which can operate with an 1.5-V supply voltage and have 0.9mm x 1.1mm chip area.

The phase noise performance is 1dB lower than the design value because the unexpected poor quality factor of the inductor. The spurs, which cannot be predicted, are quite large because of the aggressive layout. However, due to the careful choice of the reference frequency, the spurs at 25.6MHz will not be a serious problem in the

receiver system. Due to the problem of testing setup, the GMSK modulation cannot be tested. Only the FSK modulation can be tested but it can still demonstrate the ability of digital modulation of the frequency synthesizer.

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