Chapter 1

Introduction

This thesis describes a hybrid analog/digital technique for implementing a Finite-Impulse-Response (FIR) filter (Fig. 1.1). The architecture is designed to utilize the advantages of both analog and digital realizations. Analog circuits are used for speed and efficiency, while digital circuits are used for programmability and as precision delay elements. The FIR filter architecture can achieve the compactness, high-speed and low-power of an all-analog solution, yet is fully programmable and has linear phase as does an all-digital approach. The FIR filter can be used as a programmable-equalizer, or an adaptive-equalizer for application to broadband communication and disk-drive read-write channels.

1.1 Background

Modern consumer electronics and telecommunication systems present several challenges to the integrated-circuit designer. As many end-products are battery-powered portables, such as laptop computers and mobile phones, very low power dissipation and small size is required. On the other hand, as

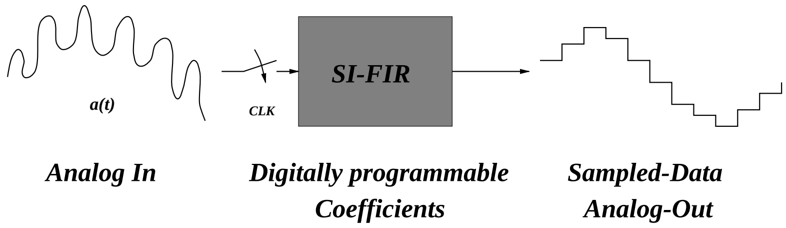


Figure 1.1 Block diagram of sampled-data analog FIR filter.

the number of subscribers to wireless services increases, along with their demand for multi-media networking, much more sophisticated signal processing is needed to compress all user channels into a fixed bandwidth. Therefore, engineers must increase the functionality of their circuits, while at the same time, reducing the power and size.

Improvements in IC Technology Much of the advance that has allowed higher levels of integration and functionality in ICs is due to innovations in processing technology. Current production CMOS processes use 0.5μm minimum geometries with 0.35μm becoming the standard in the coming year. The steady reduction in feature size allows denser and more efficient signal-processing functions. Although the processing technology is rapidly moving forward, there have been relatively few circuit innovations that bring about similar increases in accuracy, or reductions in complexity. The IC designer has basically been getting a free-ride from the process engineers. Circuit designers can keep implementing the same architecture in newer IC processes and still get increased speed with reduced power and area.

Potential for Mixed-Mode Design There is great potential in using mixed-mode (both analog and digital) solutions to problems which previously used either an all-analog, or an all-digital realization. One well-known innovation, which utilizes digital processing to improve analog accuracy, is the $\Delta\Sigma$ (delta-sigma) data converter. The architecture trades speed and complexity for accuracy by taking advantage of digital-processing precision and the high-speed of underlying transistors. Combined with digital filtering, high accuracy is achieved at lower speeds.

As the level of integration continues to increase, much of the analog functions of communication and signal-processing circuits will reside on the same chip as the digital processor. Therefore, significant opportunities arise for hybrid analog-digital solutions to existing problems, which could result in either higher performance, higher speed, or lower power. However, as yet, oversampled converters stand virtually alone as one of the only techniques where analog and digital processing are combined to advantage to produce a single function.

Partitioning of Analog and Digital Functions The fact that few architectures take advantage of the opportunity to combine analog and digital circuits in new ways is primarily due to the way in which analog and digital portions of a system have been partitioned. Designs are generally separated, such that there is a limited interaction between analog and digital components. Each specialization is seen to have well-known advantages and disadvantages as listed in Table 1.1. Analog circuitry can perform complex computations efficiently and at high-speed. For example, summation in the current-domain is realized by simply tying signals to a common node. However, analog solutions lack the flexibility of fully-programmable digital filters and are sensitive to transistor parameters, cross-talk, temperature, etc. Whereas, digital circuits are robust, regular, straightforward to design

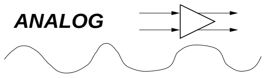
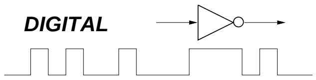
ANALOG 		DIGITAL 	
Disadvantages		*Advantages*	
-	sensitive to many variables	+	insensitive (robust)
-	lack of flexibility	+	flexible / programmable
-	difficult to achieve linear-phase	+	simple linear-phase filters
-	heuristic design approach	+	regular, systematic design
Advantages		*Disadvantages*	
+	computationally efficient	-	computationally inefficient
+	low-power signal processing	-	power-hungry signal processing
+	high-speed signal processing	-	limited-speed real-time processing

Table 1.1 Advantages and disadvantages of analog and digital circuits.

and easy to reconfigure, but require very many transistor to perform simple calculations. Each discipline has its own specializations and methodologies. As a result, boundaries between the two are rarely crossed.

Goal of this Research The goal of this research is to develop an architecture, utilizing both analog and digital techniques, which has most of the advantages of both approaches. Such a circuit was shown conceptually in Fig. 1.1. The input signal is an analog waveform and the output is a sampled-data analog signal. Efficient computations are performed in the analog domain, thus keeping power and area low, yet the design has fully-programmable digital control for maximum flexibility.

The circuit presented herein is a novel hybrid analog/digital low-power programmable implementation of an FIR filter. A block diagram of the circuit is shown in Fig. 1.2. Switched-current memory cells are employed as

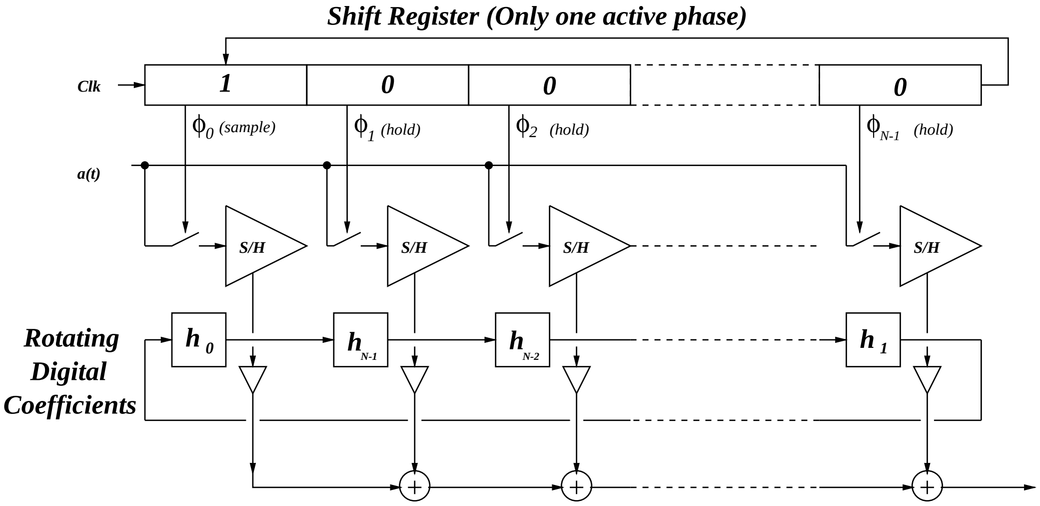


Figure 1.2 Block diagram of hybrid analog/digital FIR filter.

precision track-and-hold elements, while precision delays are implemented digitally as rotating digital coefficients. A key aspect of this design is that the signal is sampled only once; it is not resampled. The digital coefficients, which can easily be resampled without loss of accuracy, are shifted through the filter rather than resampling sensitive analog signals. Multipliers are implemented using an inherently linear current-division technique [1]. This synergy of analog and digital functions allows the realization of a fully-programmable FIR filter with precision delay elements, which has better accuracy than pure analog implementations, because the signal is not resampled, and has lower power, smaller circuit area and operates at high speeds than an all-digital approach.

1.2 Review of FIR Filters Implementations

To substantiate the above claims, that the new filter outperforms existing all-digital and all-analog designs, we must first review the state-of-the-art in digital and analog FIR filters.

1.2.1 Digital FIR Filters

Traditionally, FIR filters have been designed as custom digital circuits or implemented using general-purpose programmable DSP chips (such as the TMS320 series or the Motorola 56000 series). The main disadvantage of these digital FIR filters is the need for multipliers, which limit the overall speed of the filter. Among the processing operations within the digital FIR filter, namely multiplication, addition, and shifting, multiplication is the most time-consuming. For this reason, there has been much research conducted to boost the speed of multipliers and adders. Many different architectures have been developed, such as, carry-save, Wallace-tree, Dadda-tree, etc. [2, Sec. 2.2].

Power-of-Two Coefficients Recently, power-of-two coefficients [3, 4, 5] have been widely used to reduce computational complexity and increase operating speed. The technique aims at minimizing, or eliminating, the number of multipliers in the filter realization process. Filter complexity is a function of the number of multipliers and adders required to implement the filter. One solution to the realization of high-speed filters is to use a set of power-of-two numbers, and to represent the discrete coefficients as the sum or difference of several numbers in the set. Multiplications by power-of-two coefficients can be obtained simply by shifting the data to the left or right by an appropriate number of bits.

Limitation of Digital FIR Filters Despite the recent improvements in digital-filter architectures, using either improved multipliers, or power-of-two coefficients, engineers have not been able to reduce the power consumption for filters greater than 16-taps to a level that is suitable for low-power operation (<100-mW) at high speeds (>20-MHz) [6, 7, 8, 9].

1.2.2 Review of Analog FIR Filters

FIR filters are difficult to implement in the analog domain for one simple reason — they require analog memory. In the digital domain, perfect memory elements are as simple as flip-flops, whereas in the analog domain, high-fidelity memory requires accurate sampled delay lines, which are not readily achievable without introducing errors. These delay lines can be approximated by Charge-Coupled Devices (CCDs) or with switched-capacitor circuits. In both cases the multiple resampling of the signal in a long delay line degrades signal fidelity and limits the number of taps that can practically be implemented. Generally, analog filters for communications requiring linear phase are realized using an Infinite-Impulse Response (IIR) filter with cascaded all-pass functions. However, they can only approximate true linear-phase operation.

Switched-Capacitor Filters In the past, the switched-capacitor technique has been employed in many analog interface portions of mixed-mode designs. However, switched-capacitor circuits require high-quality linear capacitors, which are usually implemented by using two polysilicon layers. Although these double-poly capacitors can be implemented in today's highly tailored digital processes, the extra poly-processing step is generally undesirable as it adds cost to the chip, which is typically 90% digital by area. Metal-metal or metal-poly capacitors can be used in a standard digital process. However, the disadvantage is that the area required to produce the same capacitance is much larger than the poly-poly option. With the newer switched-current technique, mixed analog/digital circuits can be realized in a standard digital process, without the need for linear capacitors. Therefore, in coping with the advances of digital process, switched-current techniques seem to be an attractive alternative.

1.2.3 Switched-Current Circuit Design

Switched-current filters have received much attention recently. The majority of research has been focused on Infinite-Impulse-Response (IIR) filters [10, 11, 12], which have demonstrated the usefulness of the switched-current technique in high-speed filter design. However, there has been little in the literature discussing FIR filter applications. Some of the early FIR filter designs tried to reproduce the delay-line function [13], and realization of coefficients were based on scaled current mirrors [14]. These implementations were limited in that the signal needed to be resampled as many times as there are filter taps, which caused degradation to the signal by clock feedthrough and harmonic distortion. Also the matching accuracy of the current-mirrors used as coefficients limited the accurate control of the impulse response.

1.2.4 Motivation for Improved FIR Filter

Channel equalization is needed in most broadband communication systems and is essential in PRML magnetic storage. A programmable linear-phase filter is needed to realize this function, and low-power area-efficient solutions are desired. In light of the speed and power limitations of FIR filters in the digital domain, and the accuracy limitations of analog filters, it is evident that an improved design would be attractive, Especially for the integration of high-speed data communication systems, where these limitations are important. Overcoming the short-comings of current FIR realizations provided the motivation for this research. The approach taken here, as shown conceptually in Fig. 1.2, is to use a switched-current analog filter with digital coefficients. The advantages of this approach can be better understood in the context of intended applications.

1.3 Applications

Nearly all digital communication channels have bandwidth limitations and multi-path reflections, which cause inter-symbol interference (ISI). FIR filters are used in these systems to implement the inverse transfer function of the channel and thus, *equalize* the frequency response. Use of the proposed FIR filter as such an equalizer circuit will be outlined below for two specific applications.

1.3.1 Adaptive Equalizer

A block diagram of a digital adaptive equalizer is shown in Fig. 1.3. An analog input signal is sampled and quantized by an N-bit ADC. Channel equalization is then performed exclusively in the digital domain. An alternative architecture, taking advantage of the switched-current (SI-FIR) filter, is shown in Fig. 1.4. The SI-FIR filter performs the sampling function and

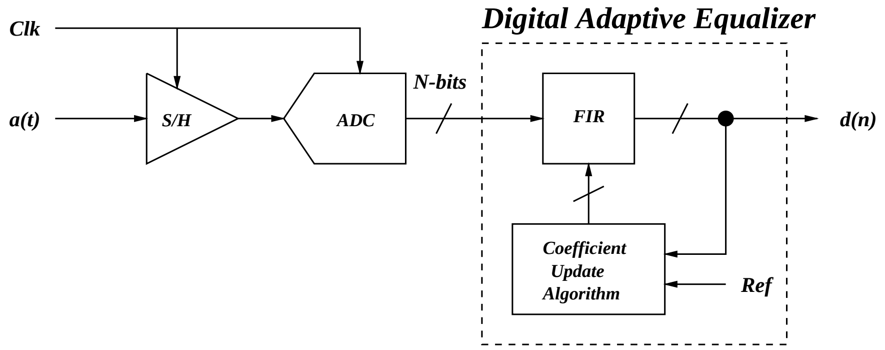


Figure 1.3 Analog front-end ADC with digital adaptive equalizer

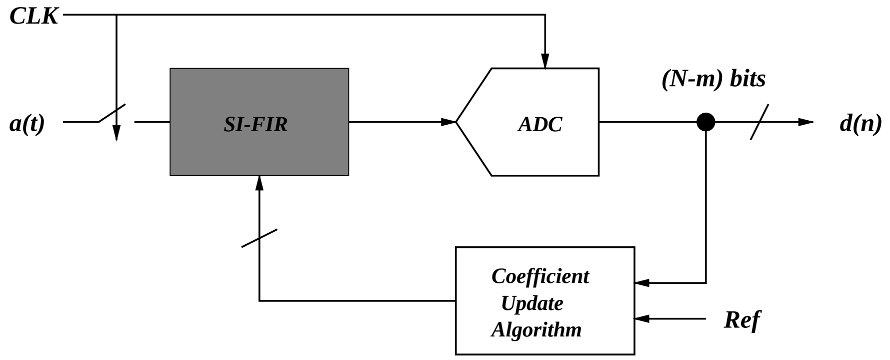


Figure 1.4 Analog adaptive equalizer

equalizes the signal in the analog domain before quantization. Equalization before quantization has the advantage that the ADC resolution can, in many cases, be reduced to $(N\text{–}m)$-bits, where m is 1 to 2. Comparisons of area and power of the digital and analog implementations are given below for a 16-tap equalizer with 9-bit coefficients at 20-MS/s [15].

	Analog SI-FIR	Digital FIR
Area	4.2-mm^2	5.0-mm^2
Power	70-mW	100-mW

This analog equalizer realization is only slightly smaller than an all-digital equalizer, and the power is comparable. However, direct comparisons are misleading, because an all-digital approach requires a sample-and-hold (S/H) and an analog-to-digital converter (ADC). In addition, when considering the differences between Figs. 1.3 and 1.4, significant reductions in area and power of the SI-FIR circuit are due to the following:

i. The all-digital circuits are optimized and take advantage of symmetry in the coefficients, whereas this first-generation SI-FIR filter does not and, therefore, has twice the digital hardware needed.

ii. The SI-FIR includes a sample-and-hold, so a separate S/H preceding the ADC is no longer needed.

iii. The ADC can be reduced in resolution, which can reduce ADC power and area by approximately a factor of 2 per bit.

1.3.2 Programmable Equalizer

The SI-FIR filter is ideal for use as a programmable equalizer, as illustrated in Fig. 1.5. In magnetic disk read channels the current trend is to use a

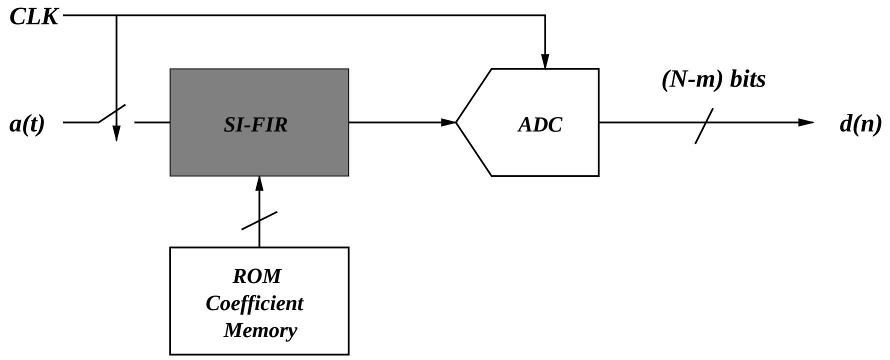


Figure 1.5 Analog programmable equalizer

programmable-, rather than an adaptive-equalizer. The reason is that the channel characteristics for a given magnetic media will not vary significantly over short periods of time. Therefore, the filter coefficients can be programmed for a specific channel and do not need to be continually updated. This differs from mobile wireless communication where the channel characteristics continually change. The SI-FIR filter of Fig. 1.5, therefore, acts as the S/H for preceding the ADC and also performs the channel-equalization filtering.

1.4 Outline of the Thesis

Details of the SI-FIR filter architecture and circuit design issues will be presented in the following chapters. Basic FIR filter theory is reviewed in **Chapter 2**. A brief overview of the the operational principle of the chip is presented, followed by a detailed description of the programmable FIR filter.

The basic circuit building blocks are presented in **Chapter 3**. Small-signal and distortion performance of the transconductor circuit, which acts as the front-end interface is discussed. The fundamental aspects and design considerations of the current-copier cells are given, and the implementation of filter coefficients by the current-division technique is then addressed.

The digital portions of the FIR filter are described in **Chapter 4**; coefficient-storage elements and their associated control circuitry are discussed in detail. Clock-phase generation for the track-and-hold function are also presented.

Chapter 5 discusses the layout generation of the FIR filter using a silicon compiler. **Chapter 6** presents measured results of the FIR filter and summarizes the the architectural advantages and performance gains over existing techniques. Finally, further developments and applications are suggested.