Chapter 3

Analog Signal-Processing Elements

3.1 Voltage-to-Current Conversion

Current is the domain for signal-processing in this SI-FIR filter. Thus a transconductor to convert an input voltage to a current signal is needed as a front-end interface. For the intended applications in this research, several criteria have to be considered in the design of the transconductor, such as bandwidth, linearity, noise and power consumption. Controllability and observability of the transconductance is desirable for testing and prototyping purposes. However, a significant design effort was not applied to the transconductor, as the main objective in this research has been explored a new architecture for the filter itself, not to extend the performance of the transconductor, which essentially serves as interface circuitry. Furthermore, the performance of the complete filter is limited much more by the current-memory cells rather than by the transconductor in terms of harmonic distortion, frequency magnitude-response and phase-linearity. Based on the above factors, the transconductor topology adopted in [20, P. 158][21, P. 163] is suitable for our purposes. This circuit, shown in Fig. 3.1, is a resistively degenerated differential pair, where the single NMOS transistor of a standard differential pair have been replaced by a compound PMOS-NMOS transistor.

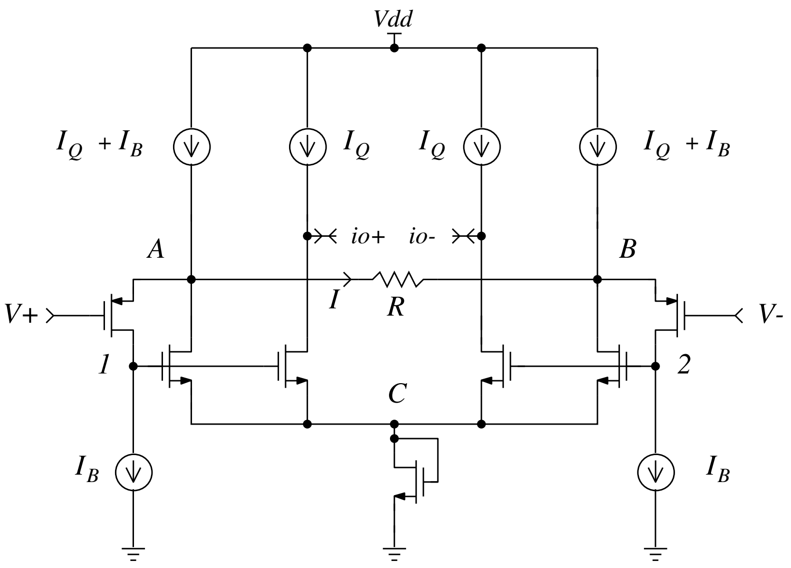


Figure 3.1 Transconductor with its transconductance controlled by an external resistor

Evaluation of the Transconductance Since the circuit will be fabricated in a standard digital CMOS process, to have a consistent layout for both n-well and p-well processes, the body of the PMOS input-transistors are tied to the most negative power supply, instead of to the source of the transistors. To evaluate the transconductance, including the body-effect of the input PMOS transistor, we start by assuming the transistors behave according to the basic square-law MOS equation. For the PMOS input transistors,

$$I_B = \frac{K_p}{2}(|V_+ - V_A| - |V_{tp1}|)^2 \tag{3.1a}$$

$$I_B = \frac{K_p}{2}(|V_- - V_B| - |V_{tp2}|)^2, \tag{3.1b}$$

where

$$\begin{aligned} K_p &= \mu_p C_{ox} \frac{W_p}{L_p} \\ |V_{tp}| &= |V_{to}| + \gamma \left[\sqrt{|2\phi_f| + |V_{SB}|} - \sqrt{|2\phi_f|} \right], \end{aligned}$$

and all other symbols have their usual meaning [22, Ch. 1]. It has been assumed that the bias current sources are ideal, and therefore, have infinite impedance. The output impedances of all the transistors shown in the circuit are also assumed infinite. The above equation relates the voltage across the degeneration resistor $V_A - V_B$ to the input voltage and body-effect parameters. Without the body-effect, the voltage across R, $V_A - V_B$ is equivalent to the input voltage difference $V_+ - V_-$. Combining (3.1a) and (3.1b), we get the following

$$\begin{aligned} |V_+ - V_A| - |V_{tp1}| &= |V_- - V_B| - |V_{tp2}| \\ V_A - V_+ - |V_{tp1}| &= V_B - V_- - |V_{tp2}| \\ V_+ - V_- &= V_A - V_B + |V_{tp2}| - |V_{tp1}| \\ V_+ - V_- &= (V_A - V_B) + \gamma \left[\sqrt{|2\phi_f| + (|V_B - Vdd|)} - \sqrt{2\phi_f} \right] \\ &\quad - \gamma \left[\sqrt{|2\phi_f| + (|V_A - Vdd|)} - \sqrt{2\phi_f} \right] \\ &= (V_A - V_B) + \gamma \left[\sqrt{|2\phi_f| + (Vdd - V_B)} - \right. \\ &\quad \left. \sqrt{|2\phi_f| + (Vdd - V_A)} \right]. \end{aligned} \tag{3.2}$$

The nonlinear terms of (3.2) can be expanding into a Taylor series given as follows, where to make the equation easier to read we define the term

$C \triangleq |2\phi_f| + Vdd$

$$\begin{aligned}
V_+ - V_- &= (V_A - V_B) + \gamma\sqrt{C}\left\{\left[1 - \frac{1}{2}\left(\frac{V_B}{C}\right) - \frac{1}{8}\left(\frac{V_B}{C}\right)^2 + \frac{1}{16}\left(\frac{V_B}{C}\right)^3 + \cdots\right]\right. \\
&\quad \left. - \left[1 - \frac{1}{2}\left(\frac{V_A}{C}\right) - \frac{1}{8}\left(\frac{V_A}{C}\right)^2 + \frac{1}{16}\left(\frac{V_A}{C}\right)^3 + \cdots\right]\right\} \\
&= (V_A - V_B)\left[1 + \frac{\gamma}{2}C^{-\frac{1}{2}} + \frac{\gamma}{8}C^{-\frac{3}{2}}(V_A + V_B)\right. \\
&\quad \left. + \frac{\gamma}{16}C^{-\frac{5}{2}}\left(V_A^2 + V_A V_B + V_B^2\right) + \cdots\right] \qquad (3.3)
\end{aligned}$$

The transconductance is given by the ratio of the output current I to the input voltage $V_+ - V_-$. We assume that the current in the resistor R can be ideally duplicated to produce the differential output current, therefore,

$$G_m = \frac{I}{V_+ - V_-}, \quad \text{and} \quad (V_A - V_B) = IR,$$

We will ignore all but the first three terms of (3.3), which is repeated below.

$$\begin{aligned}
V_+ - V_- &= IR\left[1 + \frac{\gamma}{2}C^{-\frac{1}{2}} + \frac{\gamma}{8}C^{-\frac{3}{2}}(V_A + V_B) + \frac{\gamma}{16}C^{-\frac{5}{2}}\left(V_A^2 + V_A V_B + V_B^2\right)\right] \\
\frac{I}{V_+ - V_-} &= \frac{1}{R\left[1+\frac{\gamma}{2}C^{-\frac{1}{2}}+\frac{\gamma}{8}C^{-\frac{3}{2}}(V_A+V_B)+\frac{\gamma}{16}C^{-\frac{5}{2}}\left(V_A^2+V_AV_B+V_B^2\right)\right]} \\
G_m &= \frac{1}{R\left[1+\frac{\gamma}{2}C^{-\frac{1}{2}}+\frac{\gamma}{8}C^{-\frac{3}{2}}(V_A+V_B)+\frac{\gamma}{16}C^{-\frac{5}{2}}\left(V_A^2+V_AV_B+V_B^2\right)\right]} \qquad (3.4)
\end{aligned}$$

Example G_m Calculation The result of (3.4) shows that the transconductance is smaller than the expected value of $1/R$. To have better insight into how the input voltages affect the transconductance, we can calculate the actual transconductance for a specific case. Since (3.4) gives the transconductance in terms of the variables V_A and V_B instead of the inputs V_+ and V_- we can iterate to find the actual G_m. We first assume that the input voltage maps directly to the voltage across the resistor and rewrite the inputs in terms of differential and common-mode quantities, such that :

$$V_A \approx V_Q + \Delta V/2 \tag{3.5a}$$

$$V_B \approx V_Q - \Delta V/2, \tag{3.5b}$$

where V_Q is the quiescent voltage at nodes A and B, and ΔV is the differential input voltage. The approximation signs in (3.5a) and (3.5b) remind us of the fact that V_{SB} of both input PMOS transistors change with the input voltages (due to body-effect), the above expressions are first-order estimates. Hence the extent of the increased potential at node A is not the same as the potential decreased at node B. Substituting the differential and common-mode values into the appropriate terms of (3.4) results in

$$V_A + V_B = 2V_Q \tag{3.6a}$$

$$V_A^2 + V_A V_B + V_B^2 = 3V_Q^2 - \Delta V^2/4. \tag{3.6b}$$

We will now use (3.6a) and (3.6b) to evaluate G_M, given by (3.4) with typical process values from the past fabrication report of the 0.8μm MOSIS CMOS process. It was reported that γ is 0.4744V$^{\frac{1}{2}}$; $\phi_f = \frac{kT}{q} \ln \frac{Nsub}{n_i} = 0.3746$ volts at 25°C and $C \triangleq |2\phi_f| + Vdd = 5.792$. Substituting the numerical values into (3.4) and letting V_Q equal $3.7V$ and setting ΔV to zero, the transconductance calculated is

$$G_M = \frac{1}{1.1461R} = 0.8725\left(\frac{1}{R}\right). \tag{3.7}$$

Comparison With Simulation The numerical result of (3.7) has been verified by simulation, which is shown in Fig. 3.2 and Fig. 3.3. A 4MHz $1V_{pp}$ differential input voltage was applied in simulation with the transconductance set to $\frac{1}{20k\Omega}$ for Fig. 3.2. For Fig. 3.3, a dc voltage, swept from -1V to 1V was applied and the transconductance plotted for each input voltage. Fig. 3.4

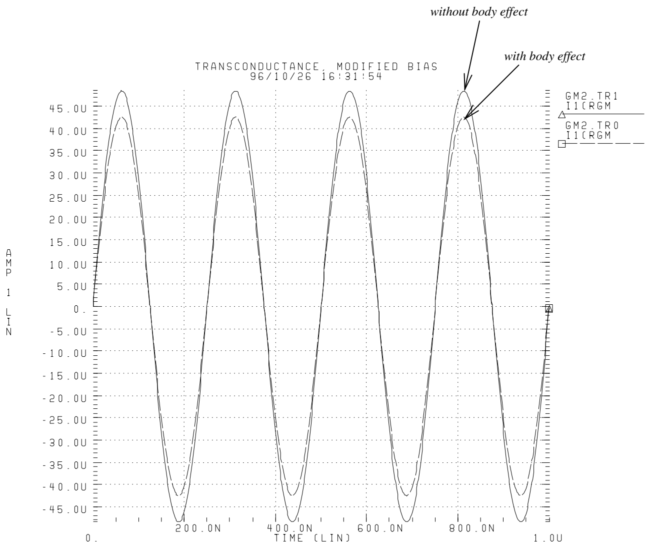


Figure 3.2 Body effect of the input PMOS affects the transconductor output

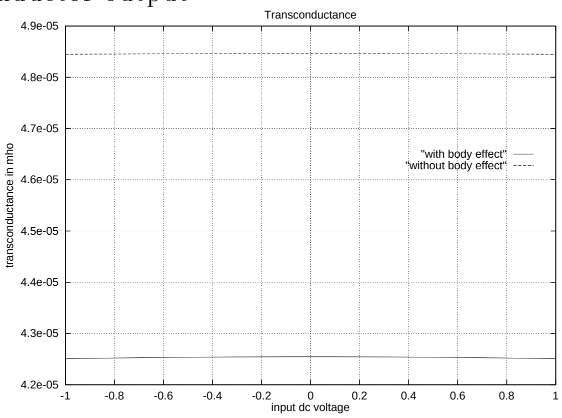


Figure 3.3 Transconductance with and without body effect of PMOS transistor

depicts the transconductor with active current loads and bias transistors.[1]

[1]Transistor sizes are given in the Appendix at the end of the thesis

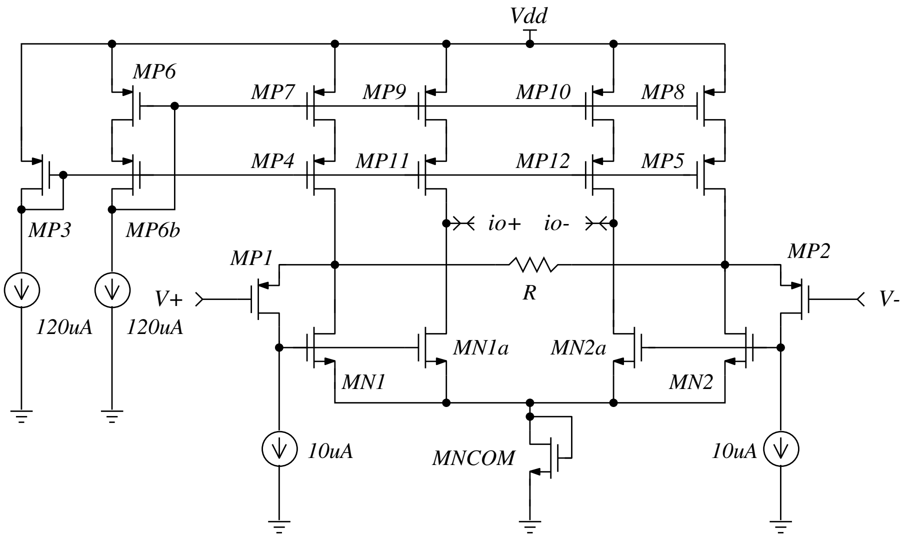


Figure 3.4 Transconductor with active current loads and bias transistors

3.1.1 Harmonic Distortion

What is needed for ideal voltage-to-current conversion is a linear resistor. One method utilizing a linear resistor is a degenerated differential pair. The problem with a simple diffpair is that the effective gate-threshold voltage V_{gt} varies nonlinearly with signal current, and therefore gives rise to distortion. Reducing this effect requires a reduction in ΔV_{gt}, which is the same thing as increasing g_m of the input transistors.

Reduced Distortion Using Negative Feedback The above method of distortion reduction soon becomes unwieldy; one can't increase g_m too far without making the devices huge. Another way to reduce ΔV_{gt} is to use gain within a negative feedback loop. This is why the compound PMOS-NMOS transistor is used at the input; the effective g_m of the input stage is now $g_{mp}[r_{op}g_{mn}]$, so the low-frequency distortion is reduced by the factor $g_{mn}r_{op}$. This keeps the current nearly constant in the input transistors and eliminates nonlinear modulation of the gate-source voltage which is the main cause of distortion at low frequencies. Typically, the loop-gain is high enough at low frequencies to reduce the distortion to insignificantly low levels. As the output impedance r_{op} is increased, the distortion can theoretically be reduced to arbitrarily low levels; for an infinite output impedance, the distortion goes to zero, unless a second-order source of distortion exists. For this transconductor the dominate distortion mechanism for low frequencies is due to the body-effect.

Distortion Due to Body-Effect To estimate the harmonic distortion of the transconductor of Fig. 3.1, we can start with (3.3) which is repeated here with ΔV defined as $\Delta V \triangleq V_+ - V_-$

$$\Delta V = V_A - V_B + \gamma\left[\sqrt{|2\phi_f| + V_{dd} - V_B} - \sqrt{|2\phi_f| + V_{dd} - V_A}\right] \qquad (3.8)$$

We can define differential and common-mode voltages V_d and V_s to simplify the expressions, where the subscript s is for the source voltage at the PMOS transistors.

$$V_A = V_s + V_d/2$$
$$V_B = V_s - V_d/2$$

The input voltage ΔV can, therefore, be rewritten as

$$\Delta V = V_d + \gamma\left[\sqrt{|2\phi_f| + V_{dd} - V_s + V_d/2} - \sqrt{|2\phi_f| + V_{dd} - V_s - V_d/2}\right], \qquad (3.9)$$

defining a voltage V_{ddg}, such that $V_{ddg} \triangleq |2\phi_f| + V_{dd} - V_s$, which is approximately equal to the voltage headroom between the power supply and the input gates, the above result becomes,

$$\Delta V = V_d + \gamma \left[\sqrt{V_{ddg} + V_d/2} - \sqrt{V_{ddg} - V_d/2} \right] \tag{3.10}$$

This equation relates the input differential voltage to the voltage difference across the degeneration resistor, which is in turn directly proportional to the output current. We can obtain the Taylor series expansion of (3.10). Due to symmetry, all the even-order terms vanish. The first and third terms are given below as,

$$\Delta V \approx \left[1 + \frac{\gamma}{2\sqrt{V_{ddg}}} \right] V_d + \left[\frac{\gamma}{64\sqrt{V_{ddg}}} \right] \frac{V_d^3}{V_{ddg}^2} + \cdots \tag{3.11}$$

The third-order preharmonic distortion of the transconductor is found by taking one quarter of the ratio of the first and third-order terms.

$$1/HP_3 = 4 \cdot 64 \left[\frac{1}{2} + \frac{\sqrt{V_{ddg}}}{\gamma} \right] \left(\frac{V_{ddg}}{V_d} \right)^2 \tag{3.12}$$

Numerical Example The predistortion is the amount the input needs to be predistorted in order to produce an undistorted output. Willingham shows that the predistortion is related to the harmonic distortion as

$$HD_3 = -HP_3 \tag{3.13}$$

for $HP_2 = 0$ [20, ch. 4]. Therefore, the third-order harmonic distortion of the transconductor, at low frequencies, resulting from the body-effect, is given by

$$HD_{3\text{dB}} = -20\log(4) - 20\log(64) - 20\log\left[\frac{1}{2} + \frac{\sqrt{V_{ddg}}}{\gamma}\right] - 40\log\left[\frac{V_{ddg}}{V_{d0}}\right], \tag{3.14}$$

where V_{d0} is the amplitude of the sine-wave voltage across the resistor. The first three terms of (3.14) are related to the square-root nonlinearity of the body-effect. The third-term is related to the magnitude of the input voltage with respect to the overhead voltage V_{ddg}. This expression can easily be evaluated for typical bias conditions. The body-effect parameter for the 0.8μm CMOS process chosen is $\gamma = 0.4744\text{V}^{\frac{1}{2}}$, and the flatband voltage is $\phi_f = \frac{kT}{q}\ln\frac{Nsub}{n_i} = 0.3746\text{V}$. For a 5V power supply, assume the input common-mode level is at 2.5V. The input transistors are biased such that the effective gate voltage is approximately $V_{gt} = 800\text{mV}$. If the threshold voltage is approximately 1.15V, then V_s, the voltage at the source of the PMOS input transistors is 2.5V + 0.8V + 1.15V = 4.45V, and the overhead voltage $V_{ddg} = |2\phi_f| + V_{dd} - V_s = 0.75 + 5 - 4.45 = 1.30\text{V}$. For a 1V_{pp} signal, the amplitude of the sine-wave is $V_{d0} = 0.5\text{V}$. For this example, we find that the third-order harmonic distortion is equal to

$$\begin{aligned} HD_3 &= -20\log(4\cdot 64) \quad -20\log\left(0.5 + \tfrac{\sqrt{1.30}}{0.4744}\right) \quad -40\log\left(\tfrac{1.30}{0.5}\right) \\ &= -48.1\text{dB} \quad -9.26\text{dB} \quad -16.6\text{dB} = -74\text{dB} \end{aligned} \tag{3.15}$$

The predicted HD_3 is -74dB with ideal matching and other non-ideal transistor effects ignored completely. The simulated harmonic distortions were tabulated in Table 3.1. Results of third-order distortion, which is the dominant distortion are within 2-dB of the predicted results. Therefore, we conclude that the body-effect is the dominant source of low frequency distortion, and for this bias condition, the distortion is more than adequate to meet our needs.

Frequency	Across the resistor			Across the current conveyor[2]		
	HD_2	HD_3	THD	HD_2	HD_3	THD
2MHz	–81.50dBc	–72.49dBc	–71.93dB	–81.61dBc	–51.44dBc	–51.43dB
4MHz	–81.55dBc	–72.84dBc	–72.23dB	–81.27dBc	–51.17dBc	–51.16dB
8MHz	–97.58dBc	–74.98dBc	–74.88dB	–91.89dBc	–50.19dBc	–50.19dB
10MHz	–81.65dBc	–75.77dBc	–74.65dB	–81.50dBc	–49.60dBc	–49.59dB

Table 3.1 Simulated Harmonic Distortion with full range input ($1V_{pp}$)

3.1.2 AC Response

The ac half-circuit equivalent of the transconductor circuit in Fig. 3.4 is shown in Fig. 3.5. We simply assume the common source node is at virtual ground and the bias current sources are ideal with infinite impedance. Transforming this half-circuit into the small-signal ac equivalent half-circuit gives Fig. 3.6. To further simplify the calculation, C_{gd3} is assumed shunted to ground. We justified this simplification in that v_4 is close to virtual ground as this node is connected to the input of the current conveyor[3], which is a low-impedance node because it is the source terminal of a transistor. Within the operation range of the input current, the voltage at this node is essentially kept constant. Therefore, one of the terminals of C_{gd3} is nearly at virtual ground and the capacitor in parallel with the gate capacitance of M2 and M3.

[2]Two current conveyors are connected to the outputs of the transconductor
[3]It will be discussed in the next section

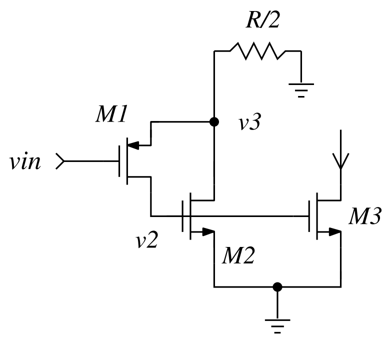


Figure 3.5 Transconductor ac half-circuit

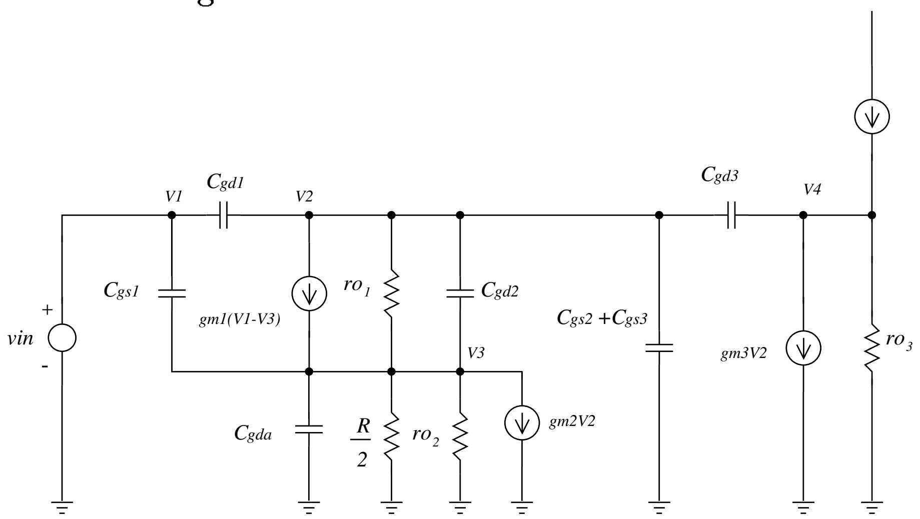


Figure 3.6 Transconductor ac small-signal circuit

Writing nodal equations for this small-signal circuit, we have

$$\begin{bmatrix} go_1+s(c_{gd1}+c_{gd2}+c_{gd3}+c_{gs2}+c_{gs3}) & -(gm_1+go_1+sc_{gd2}) \\ -(-gm_2+go_1+sc_{gd2}) & gm_1+2g+go_1+go_2+s(c_{gs1}+c_{gd2}+c_{gda}) \end{bmatrix} \begin{bmatrix} v2 \\ v3 \end{bmatrix} = \begin{bmatrix} -(gm_1-sc_{gd1}) \\ (gm_1+sc_{gs1}) \end{bmatrix} v_{in} \tag{3.16}$$

Since transconductances of the transistors g_m are much greater than the output admittances $g_0 = 1/r_0$, the above admittance matrix can be approximated as

$$\mathbf{Y} \approx \begin{bmatrix} go_1+s(c_{gd1}+c_{gd2}+c_{gd3}+c_{gs2}+c_{gs3}) & -(gm_1+sc_{gd2}) \\ -(-gm_2+sc_{gd2}) & gm_1+2g+s(c_{gs1}+c_{gd2}+c_{gda}) \end{bmatrix} \tag{3.17}$$

The determinant of the admittance matrix $\mathbf{Y}$ of (3.16) is the denominator of the transfer function of the ac response. The poles are given by the roots of the determinant. From (3.17), we obtain

$$\begin{aligned} \triangle = {} & s^2 \left[(c_{gd1}+c_{gd2}+c_{gd3}+c_{gs2}+c_{gs3})(c_{gs1}+c_{gd2}+c_{gda}) - {c_{gd2}}^2 \right] \\ & +s\left[(gm_1+2g)(c_{gd1}+c_{gd2}+c_{gd3}+c_{gs2}+c_{gs3}) + (gm_2-gm_1)c_{gd2}\right] \\ & +s\left[go_1(c_{gs1}+c_{gd2}+c_{gda})\right] \\ & +gm_1gm_2 \end{aligned} \tag{3.18}$$

Transmission Zeros To compute the zeros, apply Cramer's rule to the system matrix of (3.17), the transfer characteristic from input to v_2 is given by

$$\triangle_2 \approx v_{in} \begin{vmatrix} -(gm_1 - sc_{gd1}) & -(gm_1 + sc_{gd2}) \\ (gm_1 + sc_{gs1}) & gm_1 + 2g + s(c_{gs1} + c_{gd2} + c_{gda}) \end{vmatrix} \tag{3.19a}$$

Evaluating the determinant gives

$$\begin{aligned} -\frac{\triangle_2}{v_{in}} = \; & -s^2\left[c_{gd1}(c_{gs1} + c_{gd2} + c_{gda}) + c_{gs1}c_{gd2}\right] + \\ & s\left[gm_1(c_{gda} - c_{gd1}) - 2gc_{gd1}\right] + \\ & 2g \cdot gm_1 \end{aligned} \tag{3.19b}$$

The symbols used in the foregoing equations have their usual meaning. The typical values are estimated from a recent MOSIS fabrication report for the 0.8μm CMOS process, and presented in Table 3.2. With the above parameter

Parameter	Type	Value	Description
g	R	50.6μA/V	resistor R
gm_1	PMOS	111.7μA/V	transconductance of input PMOS, M1
gm_2	NMOS	920.0μA/V	transconductance of the NMOS, M2
gm_3	NMOS	920.0μA/V	transconductance of the NMOS, M3
go_1	PMOS	4.73μA/V	output conductance of PMOS, M1
c_{gs1}	PMOS	27.4fF	gate-source cap. of PMOS transistor, M1
c_{gs2}	NMOS	72.4fF	gate-source cap. of NMOS transistor, M2
c_{gs3}	NMOS	72.4fF	gate-source cap. of NMOS, M3
c_{gd1}	PMOS	13.7fF	gate-drain cap. of PMOS, M1
c_{gd2}	NMOS	36.2fF	gate-drain cap. of NMOS, M2
c_{gd3}	NMOS	36.4fF	gate-drain cap. of NMOS, M3
c_{gda}	PMOS	493.2fF	the gate-drain cap. of active current load contributed to M2

Table 3.2 Summary of the different parameters

values, the poles were found to be a conjugate pair with values,

$$p_{1,2} = (-50.51 \pm 133.81j)\text{MHz}$$

which corresponds to a resonant frequency of ≈ -143MHz. The computed zeros have the values of

$$z_1 = 996\text{MHz} \qquad \text{z}_2 = -32.9\text{MHz}.$$

The poles and zeros are plotted in the S-plane in Fig. 3.8, where the zero at 996-MHz is ignored; the theoretical transfer function is shown in Fig. 3.7. The calculated response shows a seriously under-damped system, which exhibits 16-dB of peaking in the frequency domain. The simulated response for the complete transconductor is shown in Fig. 3.9. The peaking of the transfer curve with the current conveyor as load follows the calculated curve.

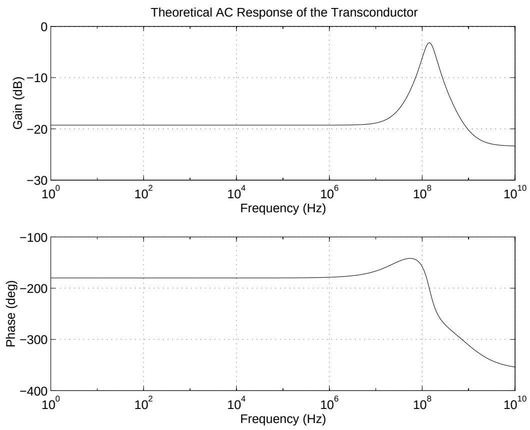


Figure 3.7 Theoretical Bode plot of the transconductance

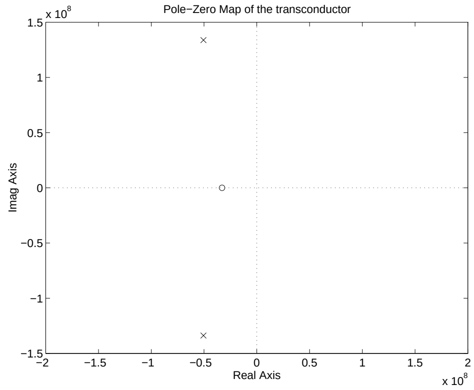
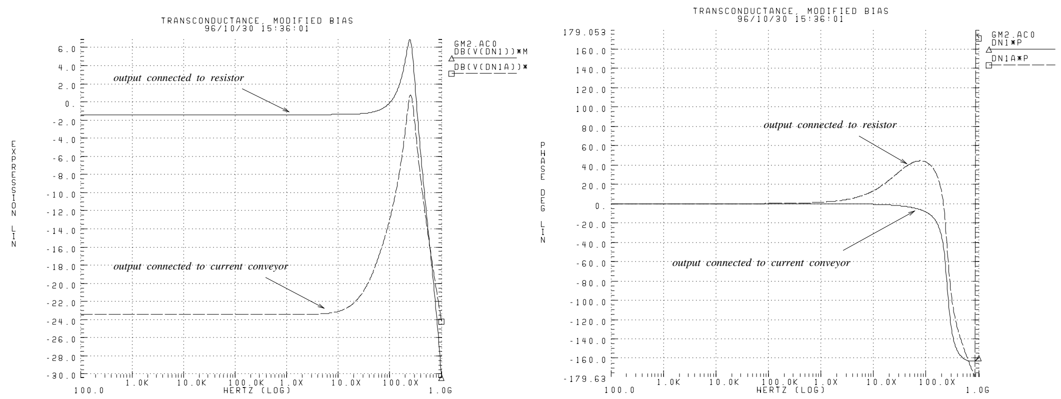


Figure 3.8 Pole-Zero plot

Frequency Compensation The transconductor uses a compound input devices in a negative feedback loop (M_1 and M_2) to improve linearity. This feedback loop, however, can cause instabilities. To increase the stability of the transconductor, compensation can be added. The problem with the circuit, as it stands, is that the capacitance at the degeneration resistor C_{gda}



(a) Simulated frequency responses (b) Simulated phase responses

Figure 3.9 Simulated frequency and phase responses of the transconductor, with the current conveyor bias circuit as the load

places a zero at $\omega = 1/[(R/2)C_{gda}]$, which is at 32-MHz. The signal current that is intended to pass through the resistor, gets diverted to the parasitic capacitance C_{gda}, which requires more current as the frequency increases; therefore the gain increases as the frequency goes up. This is problematic in this particular circuit because the degeneration resistor is *off-chip*, therefore, C_{gda} is an order-of-magnitude larger than the other capacitances in the circuit, and the zero created by this capacitance is at a lower frequency than are other parasitic poles.

To counteract the zero created by C_{gda} and $R/2$, the dominant poles need to be brought to a lower frequency to prevent the frequency response from peaking. If a capacitor is added from the gate of M_2 to ground, this will kill the high-frequency gain at this high-impedance node, thus bringing the poles to a lower frequency and increasing the damping ratio. From (3.18) we can easily find the value of the capacitance needed, in parallel with C_{gs2} and C_{gs3} to obtain the desired damping. For a damping ratio of 0.707, the circuit will behave like a second-order Butterworth filter. The capacitance needed to achieve this damping is approximately 3.25-pF. The calculated transfer function and pole-zero plot for this value of compensation capacitor are shown in Figs. 3.10 and 3.11. The resonant frequency of the transconductor now

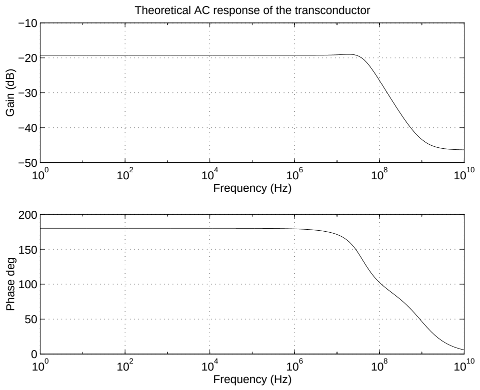


Figure 3.10 Theoretical Bode plot of the transconductance with 3.25-pF compensation capacitor at gate of M_2

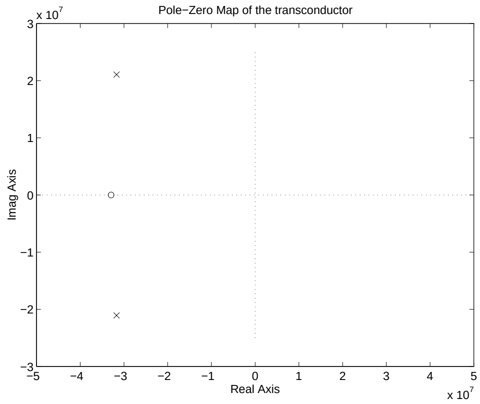


Figure 3.11 Pole-Zero plot

drops from 143-MHz to about 30-MHz after compensation. However, the transfer function no longer shows peaking in the gain response, and is much more stable.

3.2 Current Conveyor

Since the signal, as well as the coefficients, can be either positive or negative, the coefficient multiplications require four-quadrant operation. The SI-FIR filter processes signals in the current domain. Although it is possible to perform all the necessary multiplications using a current signal riding on top of a bias current, power dissipation is reduced, and performance is improved, if the bias current can be removed. Bias removal can be performed at the transconductor by subtracting a bias current from the output signal. However, this requires that the output signal current be dumped to a low-impedance node. The current conveyor circuit of Fig. 3.15 [17, ch. 7],[23, ch. 2] serves two purposes for the SI-FIR filter. First, it provides a low-input-impedance interface between the transconductor and the memory cell. Second, one master conveyor input provides biasing for all the Class-AB current memory cells.

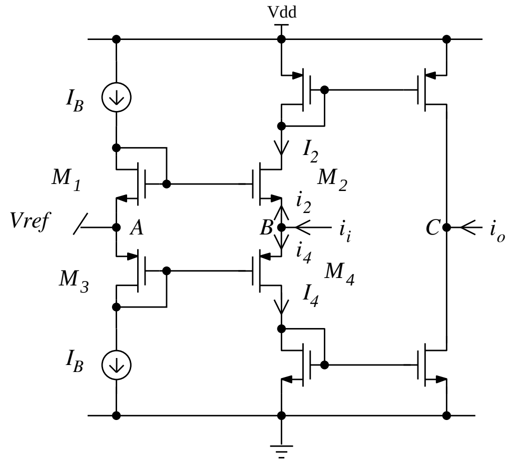


Figure 3.12 Class-AB current conveyor

The conveyor circuit forces the voltage at node B to follow the voltage at node A. Likewise the output current i_o follows the input current i_i. The voltage at node A sets the quiescent voltage at node B to a value of V_{ref} when the input current i_i equals zero. Since both reference transistors carry a current of I_B, the square-law relations imposes the following constraints on the gate-source voltages.

$$I_B = \frac{K_p}{2}(|V_{GS1}| - |V_{tp}|)^2 \tag{3.20a}$$

$$I_B = \frac{K_n}{2}(V_{GS3} - V_{tn})^2 \tag{3.20b}$$

where, $K = \mu C_{ox}\frac{W}{L}$. When an input current i_i is applied, it splits into two parts and is shared between the sources of M_2 and M_4, forcing the current of M_2 and M_4 to be unequal. These currents are then mirrored to the output where the split current recombines at node C to form the output current i_o, with the bias current I_B cancelled from i_o. The corresponding I_2 and I_4 are governed by the following equations,

$$\begin{aligned} I_2 &= I_B - i_2 \\ &= \frac{K_n}{2}(V_{GS2} - V_{tn} + \Delta V_{GS2})^2 \\ &= \frac{K_n}{2}\left[(V_{GS2} - V_{tn})^2 + 2(V_{GS2} - V_{tn})\Delta V_{GS2} + \Delta {V_{GS2}}^2\right] \qquad (3.21a) \\ I_4 &= I_B + i_4 \\ &= \frac{K_p}{2}(V_{SG4} - |V_{tp}| + \Delta V_{SG4})^2 \\ &= \frac{K_p}{2}\left[(V_{SG4} - |V_{tp}|)^2 + 2(V_{SG4} - |V_{tp}|)\Delta V_{SG4} + \Delta {V_{SG4}}^2\right] \qquad (3.21b) \end{aligned}$$

By virtue of the loop created by transistors M_1–M_4, any increase in the absolute value of the source-gate voltage of M_4 must be compensated by a reduction in the gate-source voltage of M_2, such that

$$-\Delta V_{GS2} = \Delta V_{SG4} \qquad (3.22)$$

$$\Delta V_{GS2} = \Delta V_{GS4} \qquad (3.23)$$

To illustrate the ideal operation of the current conveyor, we will assume that the n-channel and p-channel devices have identical characteristics, such that

$$K_n = K_p \qquad (3.24a)$$

$$V_{tn} = |V_{tp}| \tag{3.24b}$$

$$K_n(V_{GS2} - V_{tn}) = K_p(V_{SG4} - |V_{tp}|) \tag{3.24c}$$

The difference current $I_4 - I_2$ will be the current that flows in the output terminal i_o. From (3.21b) and (3.21a) We find that the difference of the total current in each transistor is just the difference of the sum of the incremental signal currents

$$I_4 - I_2 = i_4 + i_2, \tag{3.25}$$

which is related to the input current by

$$\begin{aligned} i_i &= i_4 + i_2 \\ i_i &= -2K_n(V_{GS2} - V_{tn})\Delta V_{GS2} \\ \frac{i_i}{2K_n} &= -(V_{GS2} - V_{tn})\Delta V_{GS2} \end{aligned} \tag{3.26}$$

The ideal conveyor therefore, has the property of being a linear transconductor. If the voltage V_B were driven with an input source, the output current is linearly related to this voltage change. However, this is not a practical linear transconductor, however, as the linearity depends on matching of unlike (p-channel and n-channel) devices.

Operating Range of Current Conveyor We can determine limitations on the operating range of the current conveyor from the above analysis. By Substituting (3.26) into (3.21a) and (3.21b), we can find the maximum input current i_i before either M_2 or M_4 are turned off.

$$I_2 = \frac{16I_B^2 - 8i_iI_B + i_i^2}{16I_B}$$

$$I_2 = \frac{(4I_B - i_i)^2}{16I_B} \tag{3.27a}$$

$$I_4 = \frac{16I_B^2 + 8i_iI_B + i_i^2}{16I_B}$$

$$I_4 = \frac{(4I_B + i_i)^2}{16I_B} \tag{3.27b}$$

By inspecting (3.27a) and (3.27b), it is clear that the currents I_2 and I_4 will remain greater than zero (M_2 and M_4 are on) provided that the input current is bounded by

$$|i_i| \leq 4I_B \tag{3.28}$$

For the input current i_i beyond $4I_B$, the circuit continues to work except one of the transistors turns off.

3.3 Current-Memory Cell as Track-and-Hold

A current conveyor provides a low-impedance interface to the transconductor and allows the signal current to be duplicated in such a way that the signal-current can be sourced or sunk from each supply rail. The SI-FIR filter requires analog memory, the current from the conveyor needs to be sampled and held to produce the memory function.

Class-A Regulated-Cascode Current-Memory Cell

The current-memory cell to be used is shown in Fig. 3.13. This is an improved version of a basic current-memory cell, with modifications based on the regulated-cascode current mirror [24]. The cell operates as follows. On

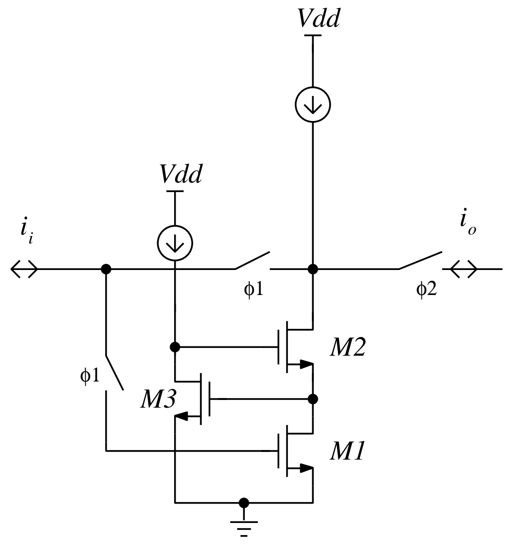


Figure 3.13 Class-A current-memory cell

ϕ_1, M_1 is diode-connected and the input current i_i, along with the bias current, charges the gate capacitance until the gate-source voltage can sustain the drain current. M_3 stabilizes the drain voltage of M_1 because M_3 maintains a constant V_{GS3}, due to the constant current bias of this transistor, which holds the drain-voltage of M_1 constant.

On ϕ_2, the switches connected to the gate of M_1 are opened and the gate-charge is trapped on the parasitic capacitance C_{gs1}. The retained charge holds the gate-source voltage stable, enabling the transistor to continue to deliver the same current to the output.

The regulated-cascode memory cell also significantly increases the output resistance compared to the simple one-transistor memory cell. Using a simple small-signal analysis of the regulated cascode, the output resistance is found to be $ro_1 + ro_2[1 + gm_2 ro_1(1 + gm_3 ro_3)]$, or approximately $ro_1 gm_2 ro_2 gm_3 ro_3$. Using the Extra benefit from the high gain of the loop (M_2 and M_3), the error in current due to changes in output voltage are reduced, and the current-level of M_1 can therefore be reduced to the point where M_1 can work in the non-saturation region.

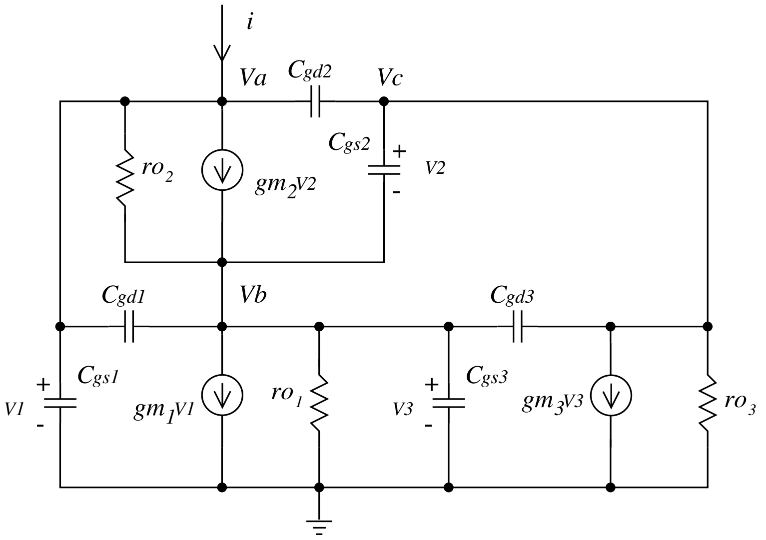


Figure 3.14 Small signal equivalent circuit of Class-A regulated-cascode current-memory cell

Transient Response

Current sampling involves the charging of the gate capacitance of the memory transistor to the gate-source voltage of a diode-connected configuration. The settling behavior is important to achieve a maximum operating frequency and also for accuracy. To a first-order approximation, the impedance seen by the input current is $1/g_{m1}$ in parallel with the parasitic capacitance at the gate of M_1. However, the feedback from the regulated cascode complicates the settling behavior and requires a more detailed analysis. The analysis starts by writing the nodal equations of the small-signal circuit in Fig. 3.14.

We have

$$\begin{bmatrix} s(c_{gd1}+c_{gd2}+c_{gs1})+go_2 & -(gm_2+go_2)-sc_{gd1} & gm_2-sc_{gd2} \\ gm_1-go_2-sc_{gd1} & gm_2+go_1+go_2+s(c_{gd1}+c_{gs3}+c_1) & -gm_2-sc_1 \\ -sc_{gd2} & gm_3-sc_1 & go_3+s(c_1+c_{gd2}) \end{bmatrix} \begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix} = \begin{bmatrix} i \\ 0 \\ 0 \end{bmatrix} \tag{3.29}$$

where

$$c_1 = c_{gd3} + c_{gs2} \tag{3.30}$$

Extracting the dominant terms, the determinant of the admittance matrix of (3.29), simplifies to

$$\triangle_d = \begin{vmatrix} sc_{gs1} & -gm_2 - sc_{gd1} & gm_2 - sc_{gd2} \\ gm_1 - sc_{gd1} & gm_2 + sc_{gs2} + sc_{gs3} & -gm_2 - sc_{gs2} \\ -sc_{gd2} & gm_3 - sc_{gs2} & sc_{gs2} \end{vmatrix} \tag{3.31a}$$

The dc term of the determinant can be found by letting all capacitors go to zero. This can be more clearly seen by rewriting the determinant as

$$\triangle_{d0} = \begin{vmatrix} 0 & -gm_2 & gm_2 \\ gm_1 & gm_2 & -gm_2 \\ 0 & gm_3 & 0 \end{vmatrix} \tag{3.31b}$$

Expanding down the first column, it is clear that the dc term of the determinant is

$$\triangle_{d0} = gm_1 gm_2 gm_3. \tag{3.32}$$

Using Cramer's rule to find the dc value of V_a, we obtain

$$\frac{V_a}{i} = \frac{gm_2 gm_3}{gm_1 gm_2 gm_3} = \frac{1}{gm_1}. \tag{3.33}$$

This shows that the input impedance is approximately $1/gm_1$, as anticipated.

Multi-Time-Constant Analysis The term involving s in the determinant will give the sum of all the time constants of the circuit. We can write this term from (3.31a) by evaluating the determinant down the first column as follows. The first term gives

$$\triangle_{d1a} = sc_{gs1} \begin{vmatrix} gm_2 & -gm_2 \\ gm_3 & 0 \end{vmatrix} = sc_{gs1}[gm_2 gm_3]. \tag{3.34a}$$

The second term gives

$$\begin{aligned} \triangle_{d1b} &= -gm_1 + sc_{gd1} \begin{vmatrix} -gm_2 - sc_{gd1} & gm_2 - sc_{gd2} \\ gm_3 - sc_{gs2} & sc_{gs2} \end{vmatrix} \\ &= -sc_{gd1}[gm_2 gm_3] - sc_{gd2}[gm_1 gm_3]. \end{aligned} \tag{3.34b}$$

The third term results in

$$\triangle_{d1c} = -gm_1 + sc_{gd1} \begin{vmatrix} -gm_2 & gm_2 \\ gm_2 & -gm_2 \end{vmatrix} = 0. \tag{3.34c}$$

From the above results the transfer function from i to V_a can be written as

$$\frac{V_a}{i} = \frac{1}{gm_1}\frac{1}{[1 + s\tau + \cdots]} \quad , \tag{3.35}$$

where the time-constant τ is given by

$$\tau = \frac{\triangle_{d0}}{\triangle_{d1}} = \frac{c_{gs1}[gm_2 gm_3] - c_{gd1}[gm_2 gm_3] - c_{gd2}[gm_1 gm_3]}{gm_1 gm_2 gm_3}. \quad (3.36a)$$

This time constant is approximately equal to

$$\tau \approx \frac{c_{gs1}}{gm_1}, \quad (3.36b)$$

which gives a 3-dB frequency for the tracking state as

$$f_{3dB} \approx \frac{gm_1}{2\pi c_{gs1}}. \quad (3.36c)$$

The above results show that the tracking behavior speed is similar to the speed of charging a simple diode-connected transistor. However, ringing can occur in this circuit, which requires further investigation.

Circuit Optimization in Simulation It is possible to optimize the design based on these equations alone. It is evident that the settling should be governed by third-order behavior, and the small-signal parameters dominant in the settling process are itemized in the equation. Optimization of the circuit from this point-of-view was done in simulation using HSPICE, with the above analysis acting as a very useful guide. Device sizes were modified until the circuit showed the desired second-order settling behavior.

Class-AB Regulated-Cascode Current-Memory Cell

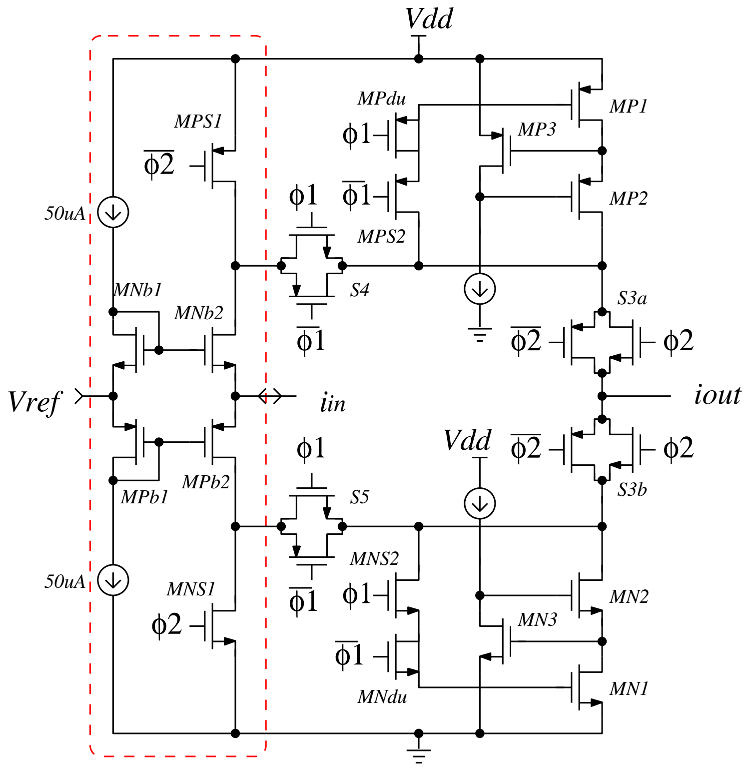


Figure 3.15 Class-AB current-memory cell

The necessity of a bias current that exceeds the signal current makes the Class-A memory cell a non-ideal candidate for application to the SI-FIR filters, where a large number of bias current sources are frequently needed. The wasted power is most pronounced in higher-order FIR filters. To reduce the power consumption, a Class-AB current-memory cell [18, 19][17, ch. 7] offers the advantage that the input signal current can be larger than the bias current.

The Class-AB current-memory cell shown in Fig. 3.15 was developed from the Class-AB conveyor by replacing each of the output current mirrors with the regulated-cascode memory cell of Fig. 3.13. The circuit works in the same way as the current conveyor. The input current splits into the upper and lower parts, these split currents are stored and copied by the NMOS and

PMOS regulated cascode memory cells respectively. The output signal current is reconstructed by combining the upper- and lower-parts of the current signals.

Fig. 3.16 and Fig. 3.18 show the simulated Class-AB regulated-cascode memory cell with a sinusoidal input of 1MHz and 3MHz sampled at 20MHz respectively. The corresponding THD is shown in Fig. 3.17 and Fig. 3.19.

3.4 MOS Current-Division Technique

A technique for dividing currents accurately and linearly was reported in [1], when MOS transistors are used as the current-division elements. Although an MOS transistor exhibits a nonlinear relationship between current and voltage, the current-division function is inherently linear and has the following advantages. It is :

i. insensitive to mobility reduction and body-effect

ii. valid in all operating regions of a MOS transistor, such as, strong inversion, weak inversion, linear- and saturation-region.

The basic working principle of current division is illustrated in Fig 3.20[4]. V_a and V_b are dc voltages that can take any values as long as both of the transistors are turned on. A current I_{in} flowing into or out of the circuit, will be divided into two parts according to the relationship,

$$\frac{\Delta I_1}{\Delta I_2} = -\frac{W_1/L_1}{W_2/L_2} \tag{3.37}$$

[4]The figure is taken from [1]

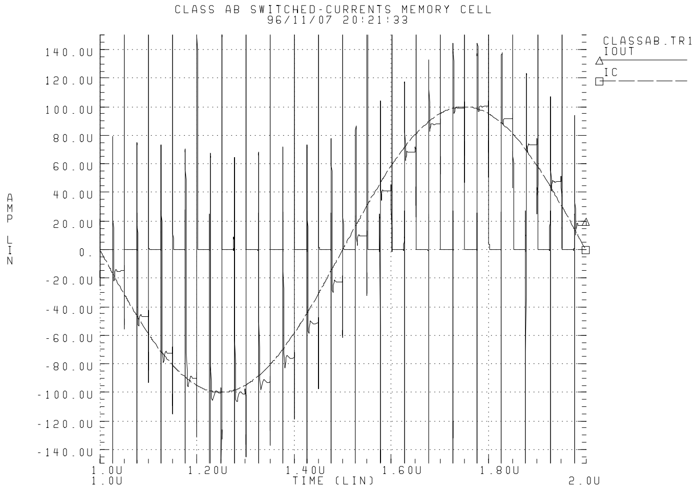


Figure 3.16 Simulated current-memory function of a Class-AB regulated-cascode current-memory cell

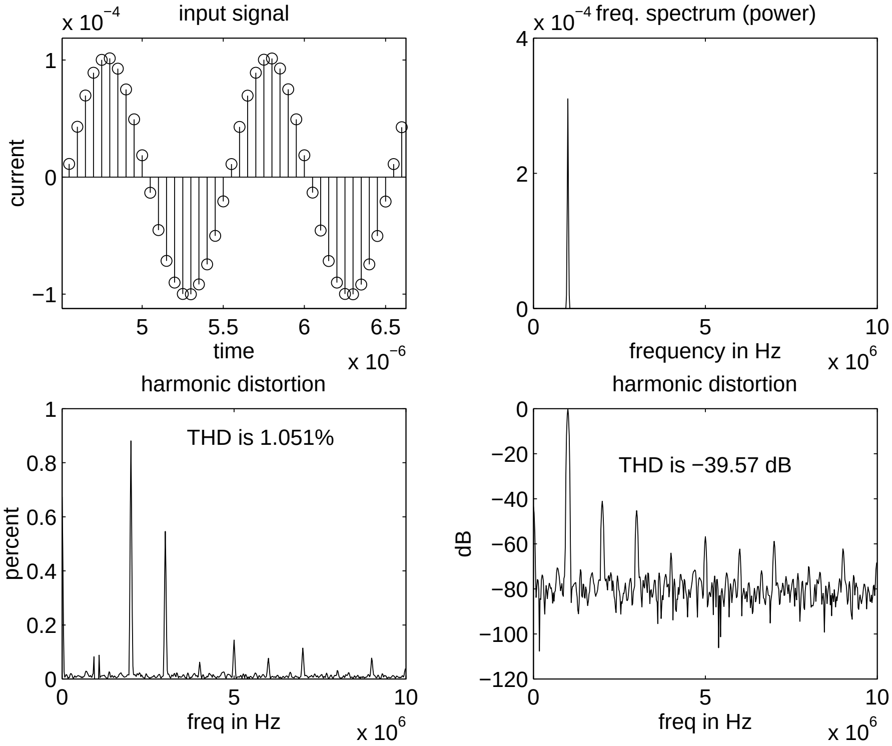


Figure 3.17 Harmonic distortion of the Class-AB memory cell with 1MHz input signal sampled at 20MHz

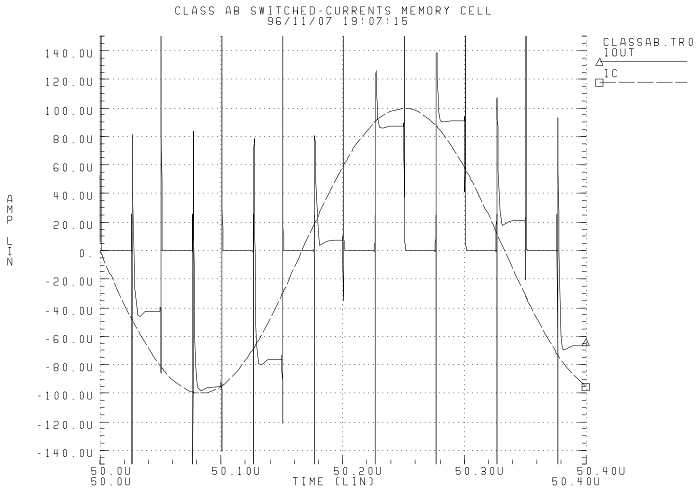


Figure 3.18 Simulated current-memory function of a Class-AB regulated-cascode current-memory cell with 3MHz input sampled at 20MHz

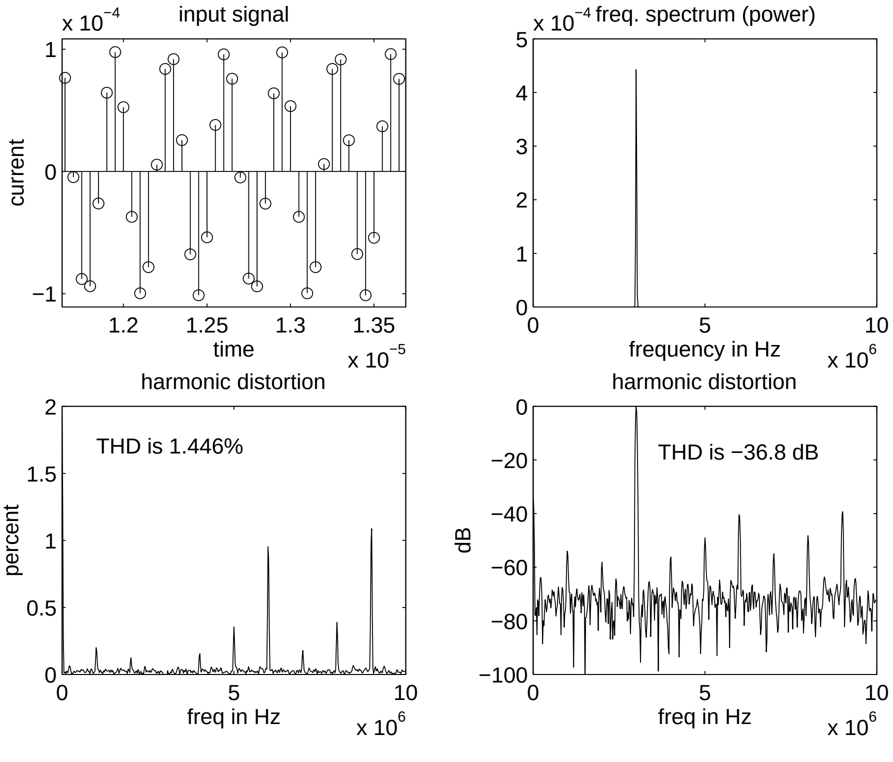


Figure 3.19 Harmonic distortion of the Class-AB memory cell with 3MHz input signal sampled at 20MHz

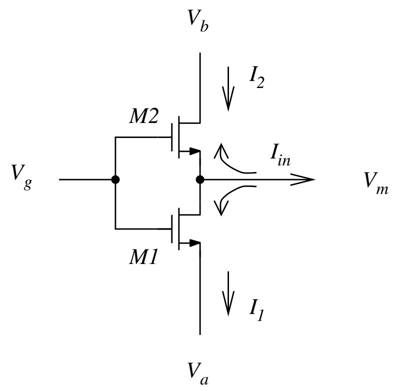


Figure 3.20 The basic principle of current division

and

$$I_{in} = \Delta I_1 - \Delta I_2. \tag{3.38}$$

Equations (3.37) shows that the current split is independent of I_{in} and dependent on the geometry of the devices only. Taking (3.37) together with (3.38) implies that the current division is inherently linear regardless of the square-law relationship of V_{GS} and I_D. For the special case in which $V_a = V_b$, there is no dc current flowing through the transistors and the delta signs are dropped from (3.37) and (3.38), resulting in

$$\frac{I_1}{I_2} = -\frac{W_1/L_1}{W_2/L_2} \tag{3.39}$$

and

$$I_{in} = I_1 - I_2. \tag{3.40}$$

3.5 Filter-Tap Coefficients Using a Current-Division Ladder

Usually, in current-mode analog FIR filters, coefficients are implemented by proper ratioing of the memory transistors [25] or current mirrors [14]. Making use of the MOS current-division property, current-division ladders can be constructed by choosing proper aspect ratios of the transistors. The approach can be envisioned as a resistive network, such as an R-2R ladder for example. Fig. 3.21 depicts one section of such a ladder. All the transistors in

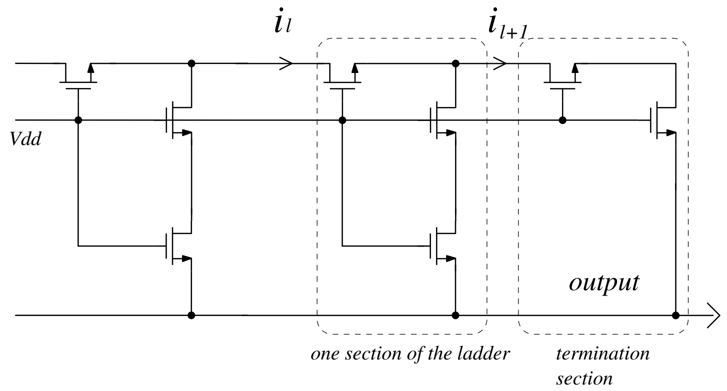


Figure 3.21 Termination section and one section of the ladder

Fig. 3.21 have the same aspect ratio. From (3.37), the input and the output current relationship for any one section within the ladder is governed by:

$$i_{l+1} = \frac{i_l}{2} \quad l = 0, \cdots, M-1. \tag{3.41}$$

where M = number of bits of a quantized coefficient. In other words, the output current of each section is half of its input current and it acts as a divide-by-2 attenuator. To implement the coefficient, the structure of Fig. 3.21 must be modified to divert the unwanted current to another output, namely a dump line. A control signal is required to control the steering of the current. To implement the above changes, the modified structure shown in Fig. 3.22 was used. An extra transistor is placed in parallel with the bottom transistor

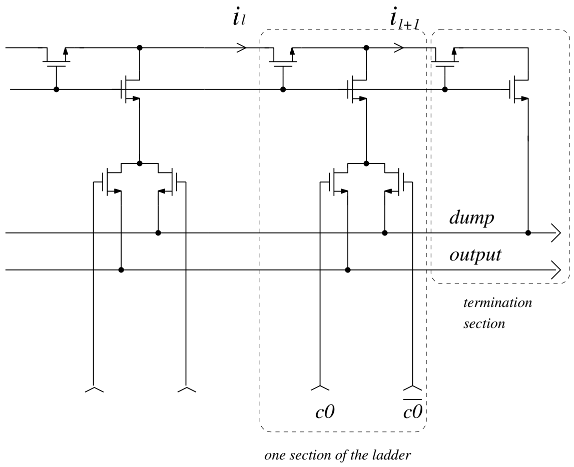


Figure 3.22 Current-division section with current-steering control signal

in each section. It is used to steer the current(corresponding to the unwanted signal) to the dump line. The signals controlling the steering function are the bit values of the coefficients. The flow is controlled by:

$$C_n = \begin{cases} 0 & : \text{ current flows to the dump line} \\ 1 & : \text{ current flows to the output line} \end{cases}$$
$$\text{for} \quad n = 0, \ldots, M-1.$$
$$C_n \quad \text{is the bit value of a coefficient}$$

Subsequently, the current-division ladder is cascaded by many of these divide-by-2 sections. The complete structure works like a multiplier, which implements powers-of-two multiplier coefficients with values less than 1. The output current of a ladder is, therefore, the input current, weighted by the value of the powers-of-two coefficient, which is stored in static flip-flops. The coefficients are cycling synchronously; the first coefficient coinciding with the most-recently-sampled signal. Its bit value controls the flow of the current to either the output(wanted signal) or the dump(unwanted signal) line. Summing all the output currents from individual taps gives the output of this FIR filter. Note that one termination section is added to each ladder in order for the proper functioning of the last stage of current division.

In this prototype filter, the word length is chosen to have 1 sign bit and 8 magnitude bits. The floating-point coefficients from the filter specification have to be quantized to their nearest 8-bit representation. The quantization process is done by first removing the sign of the coefficient and quantizing the magnitude. A sign-bit value of 0 corresponds to a positive coefficient, and 1 to a negative coefficient.

Negative Coefficients In current-mode operation, subtraction means current flowing in the opposite direction from the originally intended path. This inversion is easily achieved in a differential system by adding an extra transistor in parallel with the transistor in the first section of the ladder as shown in figure 3.23. A coefficient is essentially described by:

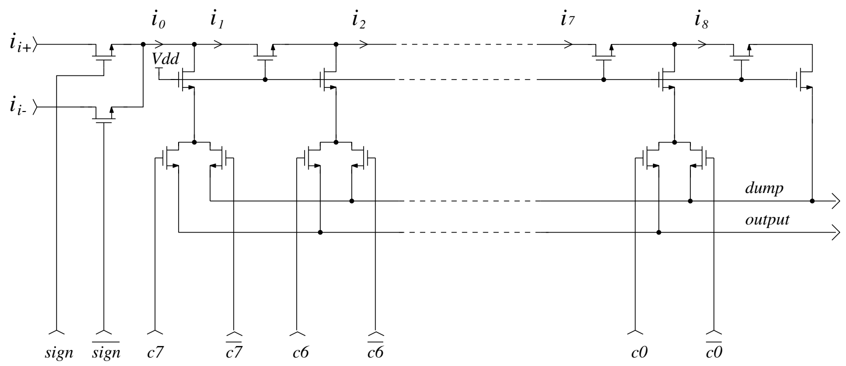


Figure 3.23 Current-division ladder

$$\begin{aligned} b = \pm 1 \times \Big[& C_7\left(\frac{1}{2^1}\right) + C_6\left(\frac{1}{2^2}\right) + C_5\left(\frac{1}{2^3}\right) + C_4\left(\frac{1}{2^4}\right) \\ & + C_3\left(\frac{1}{2^5}\right) + C_2\left(\frac{1}{2^6}\right) + C_1\left(\frac{1}{2^7}\right) + C_0\left(\frac{1}{2^8}\right)\Big] \qquad (3.42) \\ & \text{where} \qquad sign,\ C_n \in [0,1] \end{aligned}$$

This extra transistor is then connected to the opposite output terminal of the transconductor and does not interfere with the current-division structure, as the two transistors in parallel are turned on mutually exclusively. Likewise, for all the transistor pairs in the ladder, only one transistor in each pair will be on at any given time. The function of the pair is to steer the current either to the dump-line or to the output-line. By virtue of the differential design of the transconductor, equal and opposite currents are readily available. No additional circuitry is needed, except the above-mentioned extra transistor, to implement subtraction.

Quantization Effects Undoubtedly, quantization effects do exist and affect the transition-band sharpness and stop-band attenuation of the SI-FIR filter. Extensive analysis has been done by various researchers and the results are reported in various articles and textbooks [26, Sec. 6.8], which discuss the problem thoroughly. We skip the details here and refer the reader to the references.

Common-Mode Offsets Furthermore, the existence of a common-mode DC offset current does not affect a ladder's multiplication functioning. This is shown in the following equations, where an offset current is added to each signal current.

$$
\begin{aligned}
I_{O+}(nT) &= (i_{i+}(nT) + I_{dc})\, b_0 + (i_{i+}((n-1)T) + I_{dc})\, b_1 + \cdots \\
&\quad + (i_{i+}((n-N+1)T) + I_{dc})\, b_{N-1} \\
&= \sum_{k=0}^{N-1} \left[(i_{i+}((n-k)T)) b_k + I_{dc} b_k \right] \qquad (3.43a) \\
I_{O-}(nT) &= (i_{i-}(nT) + I_{dc})\, b_0 + (i_{i-}((n-1)T) + I_{dc})\, b_1 + \cdots \\
&\quad + (i_{i-}((n-N-1)T) + I_{dc})\, b_{N-1} \\
&= \sum_{k=0}^{N-1} \left[(i_{i-}((n-k)T)) b_k + I_{dc} b_k \right] \qquad (3.43b)
\end{aligned}
$$

$\forall n \in \mathcal{Z}^+$ and $i_{i+}(lT), i_{i-}(lT) = 0 \quad \text{for} \quad l < 0$

where

b_x : filter coefficients

N : number of taps

By virtue of differential design, (3.43a)—(3.43b) lead to the following properties,

$$I_{O+}(nT) = -I_{O-}(nT) \qquad (3.44)$$

$$i_{i+}((n-k)T) = -i_{i-}((n-k)T), \qquad (3.45)$$

resulting in

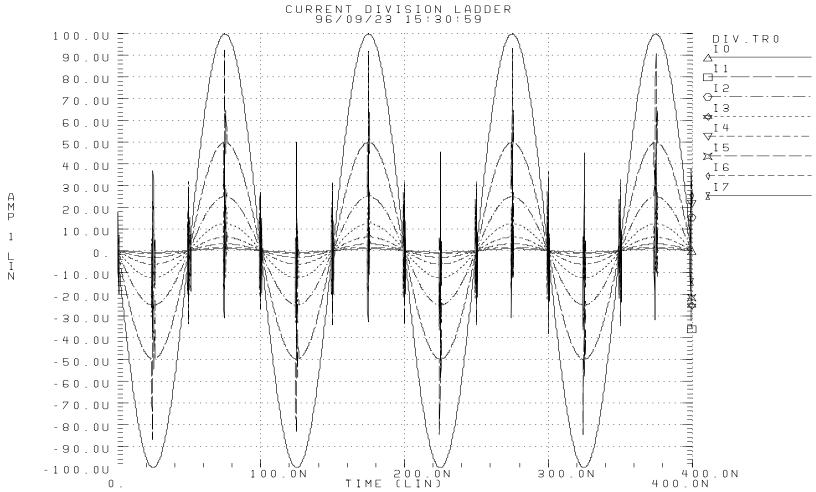
$$
\begin{aligned}
I_{O+}(nT) - I_{O-}(nT) &= \sum_{k=0}^{N-1} \left[i_{i+}((n-k)T) - i_{i-}((n-k)T) \right] b_k \\
2I_{O+}(nT) &= \sum_{k=0}^{N-1} 2 \left[i_{i+}((n-k)T) \right] b_k. \qquad (3.46)
\end{aligned}
$$

where it can be seen that the offset current I_{dc} vanishes in equation (3.46).

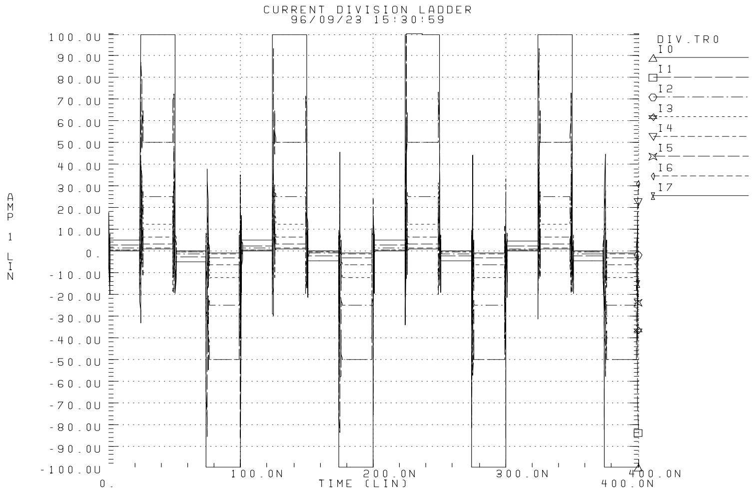
3.6 Transient Response of the Current-Division Ladder

To investigate the transient performance of the current-division ladder, the modified BSIM model (level 28) is used to simulate the circuit. Fig. 3.24a shows the currents going through each section with the coefficients circulating at 20MHz, while Fig. 3.24b shows a sampled-and-held sinusoidal signal. All the transistors in the ladder have the same aspect ratios namely $15\mu m/1.5\mu m$. Fig. 3.25 shows the step responses of the currents in each section across the ladder. The controlling coefficients are rotating at 20MHz. The transients are caused by the changes of the bit values which are controlling the steering of current. The results show 2.5ns settling time under the condition that 1ns rising and falling times are used for the bit-control signal. Shorter settling times are obtained by shortening the rise and fall times of the bit-control signal.

Simulation shows that the current-ladder exhibits very good harmonic distortion. From Fig. 3.26, the total harmonic distortion of the ladder with the non-rotating coefficients remains below 0.02% (-74dB) up to 5MHz. The THD increases linearly with increasing frequency. Larger THD is observed at the middle section of the ladder.



(a) Current passing through sections of a divide-by-2 current ladder.



(b) A Sampled current passing through divide-by-2 current ladder.

Figure 3.24 Current in each section in a current-division ladder.

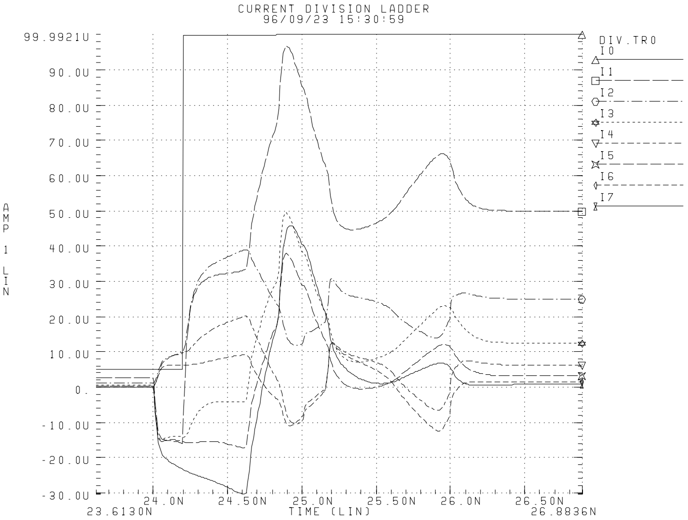


Figure 3.25 Step responses of the current-division ladder in each section

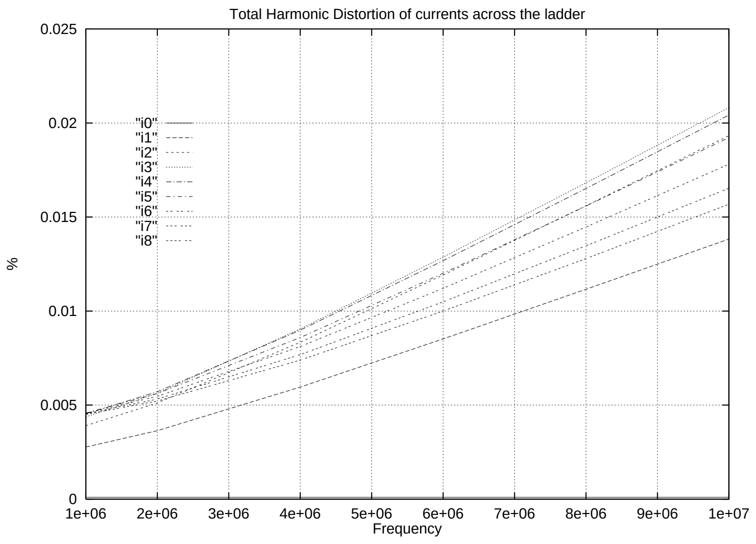
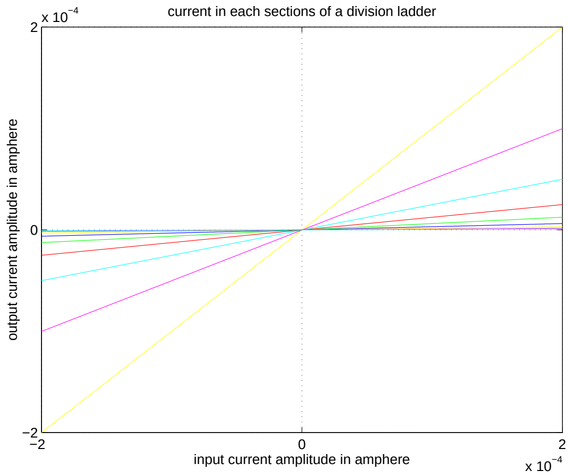
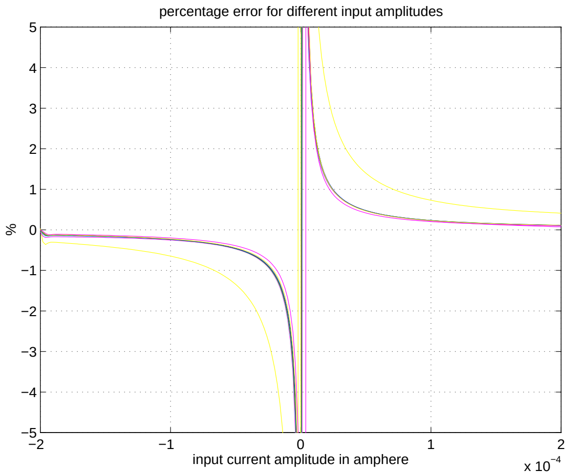


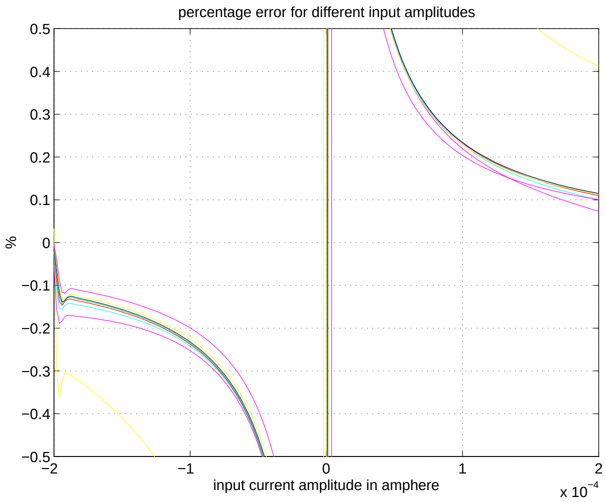
Figure 3.26 Total harmonic distortion of currents in different sections of the ladder.



(a) A linear-ramp current input with slope of $4\mu A$/ns passing through different sections of a current-division ladder



(b) Percentage errors in each section of the ladder with different input amplitudes



(c) Zoom-in portion of (b)

Figure 3.27 Accuracy of current-division.

3.7 Global Bias

A global bias circuit is needed to supply the necessary bias currents for the transconductor and current-memory cells. For a first-generation prototype circuit, external current is used to feed the internal global bias circuit from which different bias currents for various parts of the circuit are generated. Fig. 3.28 is such a circuit; in which cascode current mirrors are employed to minimize the discrepancies in the mirror currents.

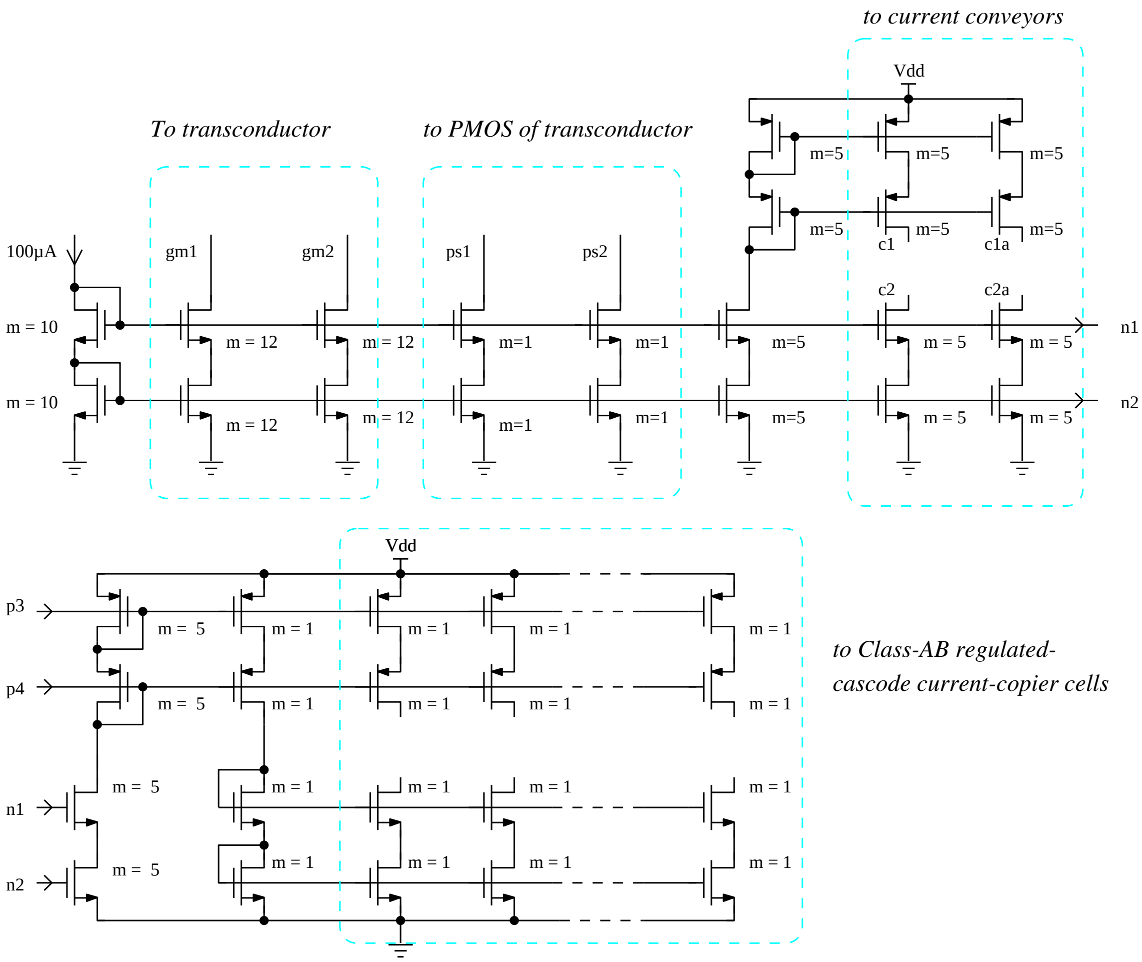


Figure 3.28 Global bias circuit, in which all the PMOS transistors have unit size of $\frac{15\mu m}{3\mu m}$, and all the NMOS transistors have unit size of $\frac{10\mu m}{3\mu m}$.

"Making one's intentions sincere" is not to permit self-deception... As when we do hate a bad odor; or do love that which is beautiful. This is self-fulfilment. For this reason, the superior man is always on guard when alone. The petty man, when he is alone and unobserved, practise evil; but when he catches sight of the superior man, he will immediately try to conceal his evil and display that which is good. But of what use is his disguise, when the other can see his lungs and liver? Hence it is said: what is within will be seen without. Therefore, the superior man must be on guard when alone. As Zeng Zi said: "He whom ten eyes look at and ten hands point to — that man had better keep a serious watch on himself!" As riches will adorn a house, so moral virtue will adorn a man. And it is only when the mind is at ease, that the whole body will be content. Therefore the superior man must make his intentions upright and his thoughts sincere.

Commentary VI — Making one's thoughts and intentions sincere.
The Great Learning, Confucian Classics
Translated by Dr. Mary Ng En Tzu