Chapter 5

Layout

5.1 Floorplan

The SI-FIR filter is a *mixed-signal* design, meaning that both analog and digital elements coexist on the same circuit. It is important to minimize coupling of digital switching-noise into the analog sections of the chip. The most obvious precaution to take in the layout is to provide a clear physical separation between the analog and digital parts to diminish crosstalk. The floorplan of the SI-FIR filter is shown in Fig. 5.1. Analog blocks are placed at the top of the layout and the digital blocks are at the bottom. Several, mixed-analog-digital-layout guidelines [24, ch. 16] were utilized in this design; among the most important are the following:

- Independent power-supply lines for the analog, digital, and I/O pad-cells were used,
- A grounded dummy-line was placed between the analog and digital parts to serve as a horizontal shield, reducing the parasitic capacitances between blocks.

- An N-well guard-ring enclosed the entire analog part to guard against coupling through the substrate.

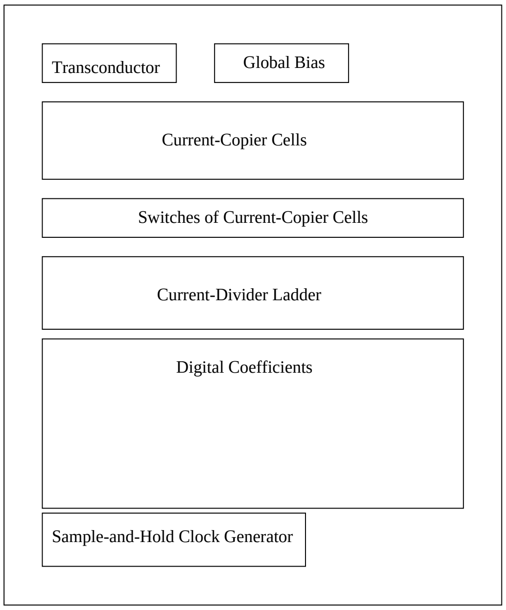

Figure 5.1 Floorplan of the prototype chip

5.2 Automatic Layout Generation

The layout of the SI-FIR filter was not done in a conventional way, by hand-drawing all the devices and interconnects; rather, it was written in software as a generator, or *Silicon Compiler*. In short, a silicon compiler is software that translates the electronic design of a chip into the actual layout of the components. A more thorough definition is as follows:

> "*Silicon compilers are programs that generate layout data from some higher-level description. This higher-level description can be a symbolic layout, a circuit schematic, a set of Boolean expressions, a logic schematic, a behavioral description of a micro-architecture, an instruction set, or just an algorithm for signal*

> *processing. Silicon compilers contain knowledge of how to synthesize higher-level constructs from basic components and how to arrange components and interconnections on silicon. This knowledge is stored in the form of design rules that conform to constraints imposed by the technology used.*[1]"

Silicon compliers are desirable in datapath circuits where a high degree of regularity exists, whereas standard-cell synthesis is the preferred technique for random logic and complex state-machines. The SI-FIR filter is a datapath circuit, therefore, the layout will be highly modular as the complete filter consists of many identical taps. It is also highly desirable to adapt the filter's order and the word-length of the coefficients for different applications. In view of this, the filter lends itself to being layed out as a generator. A simple silicon compiler which takes, as input, the above parameters and generates the corresponding layout was developed.

5.3 Digital Layout Generation Using Standard Cells

The layout generator was written using the Generator Development Tools (*GDT*) from *Mentor Graphics*. The primary layout description languages used by *GDT* are *L* and *Lx* [27, ch. 2]. By virtue of the *L* languages, the *GDT* leaf-cells are highly reusable, because each leaf-cell is actually a generator with many programmable features, which include: transistor sizing, power-bus width, pitch, number of feedthroughs, and the addition of space cells with, or without, wells, for the purpose of pitch matching. For example,

[1] Quotation from reference [27], Chapter 1, Introduction to Silicon Compilation

to generate a series of buffers with different driving capabilities, different pitches, and different bus-widths needs only one generator.

Writing a generator is much more difficult than doing a hand layout. The advantage of a generator is portability across different technologies, and ease of reuse. If written properly, generators in *GDT* require only minor modifications when switching technologies. The generator for this SI-FIR filter was written for a 0.8μm CMOS process. However, a new layout for a 0.5μm process could likely be generated in less than one day. Of course, in addressing the design time, interactive layout design still has the advantage of fast design turnaround time. However, even when a layout generator will not be used a large number of times, the programmability makes it very useful when several iterations of the layout for pitch-matching, perfect cell-abutment, and design optimization are required.

5.3.1 Generation Procedure

Pitch matching is essential for the perfect abutment of the cells. In order to pitch match to a layout that doesn't yet exist, a two-pass procedure was used. First, the program generates all the cells in the layout and the maximum pitch among them is noted. Based on this measurement, all the cells are adjusted to this maximum height accordingly.

Each generator must read a technology file, which describes the design rules for the given process. In addition, this generator takes two configuration files as input; each provides necessary design information. The first file consulted is a list file, which contains all the generators of the required cells in the design, with their configurations and parameters. The second file is the cell-control file, which defines typical- or unit-device sizes and sets default power-bus widths. The generator then produces, as output, cells that are all pitch-matched and have the same power-bus widths. The final core layout for the 16-tap SI-FIR filter is shown in Fig. 5.2.

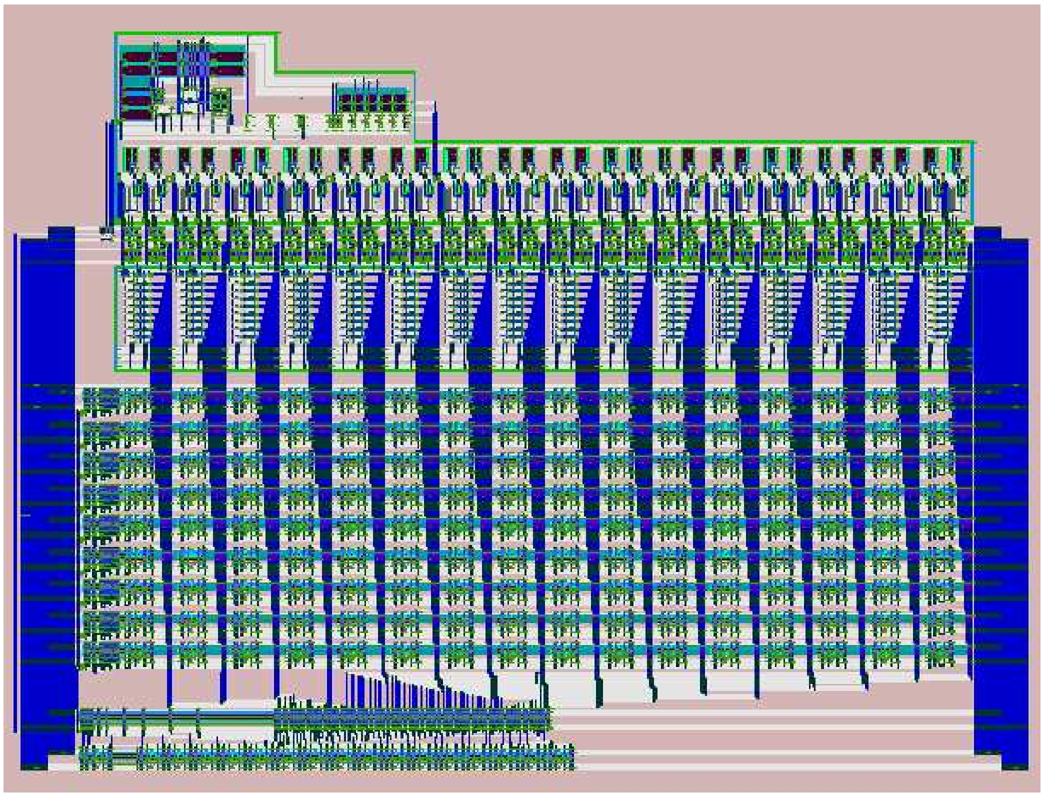

Figure 5.2 Layout of a 16-tap SI-FIR filter.

5.4 Future Layout Improvements

The SI-FIR filter designed for this project is novel. Therefore, a very conservative approach was taken in the layout to ensure functionality and to add a great deal of visibility and controllability in testing. Compactness of the layout was not emphasized in this initial prototype. In some instances a choice was made even to sacrifice some performance to ease circuit measurement and to achieve a certain degree of tunability of the analog blocks. A production version of the filter, for commercial applications, requires that several aspects of the layout be improved. However, nearly all of these can be done with only minor modifications, the most important of which are discussed below.

Use an Internal Resistor for the Transconductor: In the transconductor circuit, parasitic capacitances at the degeneration-resistor terminals is a major source of distortion of the V/I characteristic at high frequencies. Ideally, parasitics at these nodes should be kept low. In this design, however, to provide a simple adjustment of the transconductance, an external resistor is used. Therefore, large capacitances (typically up to a few pF) of the bonding pad is hooked to these terminals. In addition, the series inductance and resistance of the bond wires give rise to another cause of signal distortion. In the current design, this effect could have been reduced by using bond-pads in the center of one of the four sides of the chip for these sensitive signals, where the lead-frame and bond-wires will be the shortest. For a production version of this filter, the degeneration resistor will be internal. This will eliminate the large parasitic capacitance, and thus, improve linearity and bandwidth. This will also reduce the number of I/O pads needed.

Direct Connection from Transconductor to Current-Division Ladder: For this initial prototype filter it is desirable to know how much distortion is introduced by the transconductor. Alternatively, we would like to know how well the switched-current filter can perform with an ideal transconductor. Therefore, instead of making a straightforward internal connection from the outputs of the transconductor, directly to the inputs of the current conveyor, an four additional bond-pads were dedicated for this purpose: Two pads are needed for the transconductor differential outputs; the other two are for the inputs of the current conveyors (current-input to the filter). Although this allowed us to measure the transconductor and the filter independently, it also introduces extra load capacitance to the transconductor, and reduced the bandwidth considerably. In a second-generation circuit, these four pads can be removed and the connection can be made internally.

Remove Redundant Digital Buses: The layout of the SI-FIR filter used redundant digital buses for the coefficient registers. Separate buses are used to simultaneously monitor the input and the output of programmed coefficients. This feature was added for testing purposes to ensure that the digital parts are functioning properly. In a second-generation layout, the dual-bus structure will be eliminated, thus conserving die-area. The output pads connected to the redundant bus will also be removed.

Reduced Charge Injection: To compensate for charge-injection in the current memory cells, a technique using dummy-switches was employed. However, this scheme was not fully optimized in the layout. In a future version of this chip, a layout scheme, such as the one described in [17, p330-4], can be employed to reduce charge-injection even further.