Chapter 6

Test Results

A 16-tap switched-current FIR filter was fabricated in a triple-metal, single-poly (3M1P) 0.8-μm CMOS process (MOSIS-HPCMOS26G). A micrograph of the filter is shown in Fig. 6.1. The entire chip measures 3560μm $\times$ 3560μm, while the core area is 2408μm $\times$ 1762μm. Measured results for this chip are presented in this chapter and are compared to simulations of ideal performance.

6.1 Test Procedures

Two main measurements of interest are the frequency response of the filter and the harmonic- and intermodulation-distortion. Setups for these measurements are illustrated in Figs. 6.2(a) and (b). The frequency response is measured using a *Hewlett-Packard 8752C* network analyzer, which has a bandwidth of 300kHz–6GHz. Spectral measurements are made using a *Hewlett-Packard 8563E* spectrum analyzer with a bandwidth of 30Hz–26.5GHz. Data from the instruments is down-loaded to a PC via an IEEE-488 interface for further analysis and plotting. Frequency responses are plotted in *Matlab*,

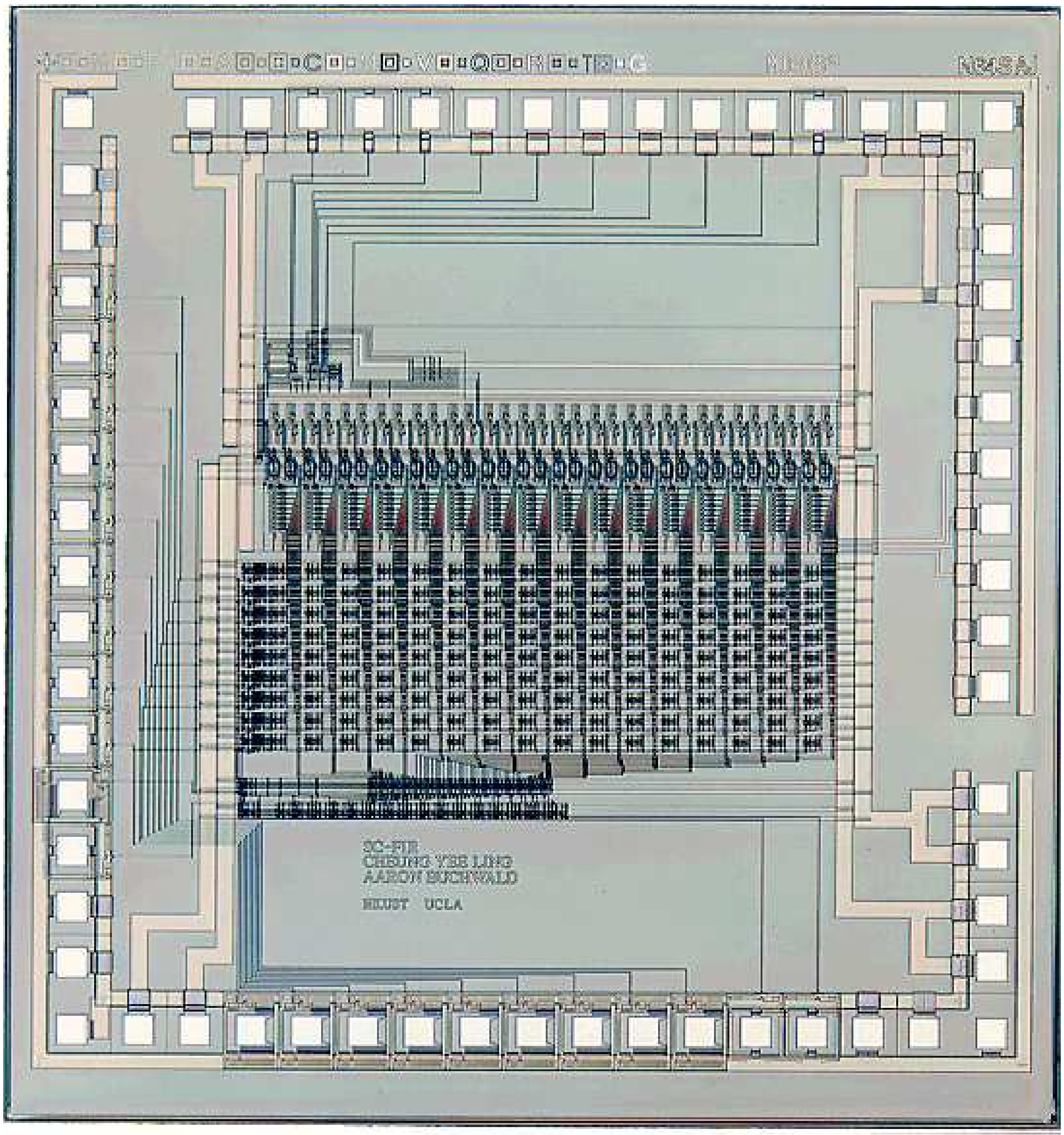
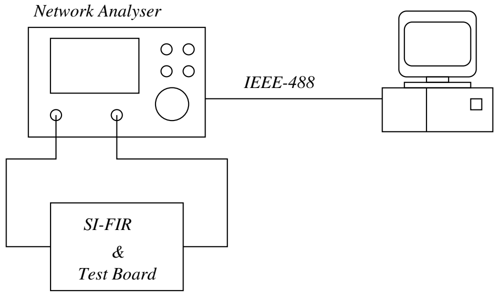
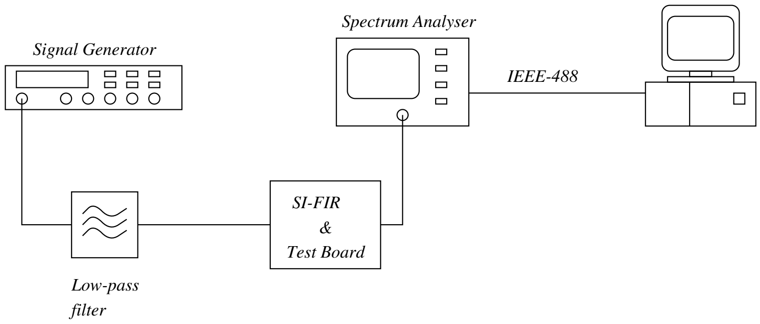


Figure 6.1 Micrograph of SI-FIR filter prototype.

where they are overlayed with the ideal responses for comparison. Distortion measurements are performed using a signal generator in combination with external lowpass filters to further purify the signal-source. A common-mode reference voltage is generated by a variable voltage regulator and buffered by voltage followers. One reference voltage forms an off-chip current source of 100μA which feeds the internal master bias circuit.



(a) Measurement of frequency response



(b) Measurement of distortion performance

Figure 6.2 Test setups for measurements: (a) Frequency response, (b) Distortion performance.

6.1.1 Interface Circuits

The SI-FIR filter is differential, whereas test equipment is almost always single-ended. Therefore, additional circuits are required to interface between the single-ended test instruments and the differential test chip. The input signal is converted to a balanced differential signal using a wide-band RF transformer with a 2.5V DC common-mode voltage applied to the center-tap as shown in Fig 6.3.

The output of the SI-FIR filter is a pair of differential currents, which are the outputs of all the current-division ladders tied together. In order for the current-mode operation of the circuit to function properly, these current-output signals must be terminated to a low impedance. The circuit of Fig. 6.4 is used as a transimpedance differential-to-singled-ended converter to interface to the output. The input impedance remains at virtual-ground for low frequencies and, therefore, provides the required low-impedance current-summing node. A series 50-Ω termination resistor is added to eliminate reflections when connecting to test equipment.

Deimbedding Measurements of Interface Circuit and Cables The performance of input and output interface circuits was measured first. The two circuits were connected in series, via 10kΩ resistors. The frequency response of this cascade was measured, including all the connecting cables, using a network analyzer. It was found that, over the frequency range of interest (0–10MHz), a deviation of approximately 0.5dB in amplitude and a 30° phase shift was observed. This spectral response was stored in the memory of the network analyzer and has been normalized out of the overall

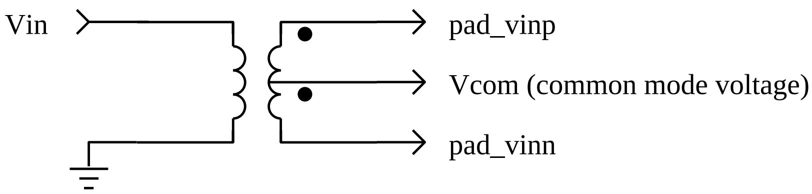


Figure 6.3 Single-ended to the differential-ended input with 2.5V offset applied

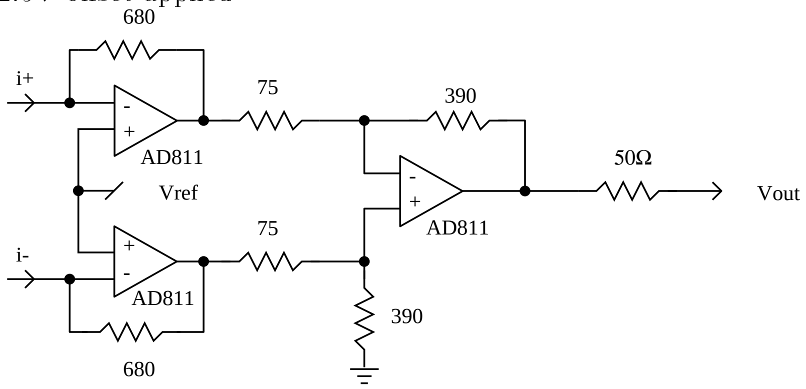


Figure 6.4 Differential to single-ended output interface

SI-FIR measurements. Distortion of the interface circuit was also measured and was found to be negligible for frequencies less than 10MHz.

6.2 Measurements of the Transconductor

Throughout the entire FIR filter, the signal is represented by a current, except at the input, where the signal is a voltage. Therefore, a transconductor is required at the front-end to convert a differential input-voltage to a differential current. This transconductor should not affect the overall performance of the filter and, therefore, should contaminate the input signal as little as possible. The transconductor was designed to provide 8-bits of resolution (>50-dB dynamic-range) for frequencies up to 10-MHz.

6.2.1 Harmonic Distortion of the Transconductor

The transconductor was measured separately and the harmonic distortions found for different frequencies are listed in Table 6.1. As the circuit is fully-differential, we expect the odd harmonics to dominate. However, for low frequencies, (1MHz and 2MHz), it was found that the 2nd-harmonics were the strongest. This was found to be actually due to a limitation of the test setup. The signal-source driving the circuit does not have the spectral purity needed to make measurements at the -50dB level. Therefore, the signal must be filtered to reduce the higher harmonics before they enter the circuit. However, due to the lack of high-quality lowpass filters at 1- and 2-MHz, we were not able to reduce the second harmonic of the signal source to a value low enough to provide accurate measurements. Therefore, the 3rd-harmonic, only, can be used as an indication of the distortion of the circuit itself for measurements below 2MHz.

However, for frequencies greater than 2MHz, better filters were employed which buried the harmonics below -76dB, where the noise floor predominated. Despite the differential nature of the circuit under test, even-harmonics are still present at the higher frequencies. This is due to offsets and imbalances in the interface circuit and the transconductor itself. Fig. 6.5 shows the output harmonic spectrum with an input of 10MHz being driven by a 0.5V_{pp} signal. The transconductor maintains better than 50-dB total-harmonic-distortion THD to 8-MHz. Although the design was intended to maintain this performance level up to 10-MHz, the measured results are more than adequate to maintain a dynamic-range greater than 8-bits for nearly all signals being sampled at the target rate for 20-MHz. Only large-amplitude signals very close to the Nyquist-rate (10-MHz) will experience distortion greater than -50dBc.

frequency	2^{nd} harmonic	3^{rd} harmonic	4^{th} harmonic
1MHz	-52.00dBc	negligible	negligible
2MHz	-59.83dBc	-63.00dBc	negligible
5MHz	-65.83dBc	-66.63dBc	-67.50dBc
8MHz	-57.00dBc	-52.84dBc	-67.84dBc
9MHz	-50.00dBc	-46.66dBc	-62.00dBc
10MHz	-46.33dBc	-42.00dBc	-58.33dBc

Table 6.1 Harmonic distortion of the transconductor with half of the full input voltage (0.5V$_{pp}$) applied to the transconductor.

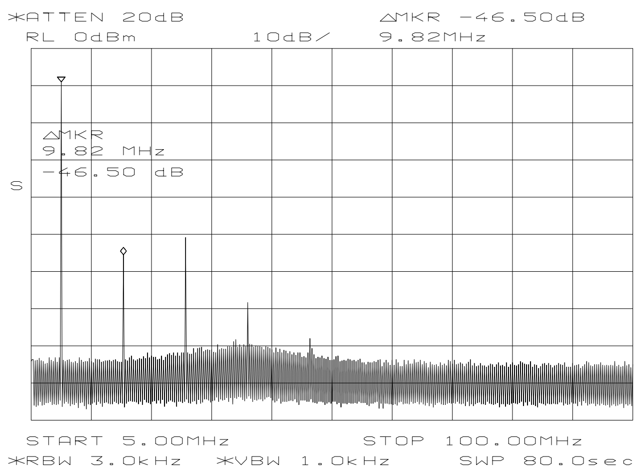


Figure 6.5 Output harmonic distortion with a 10MHz signal input

6.2.2 Frequency Response of the Transconductor

The frequency response of the transconductor was also evaluated and is shown in Fig. 6.6. The response is basically flat up to 3MHz, and maintains a variation within 2dB to 5MHz with little phase shift. The measurement shows peaking in the frequency response that was not noticed in simulation. This is due to the presence of bond-wire inductance and off-chip parasitic capacitances. Simulations of the transconductor in Section 3.1, page 27, showed peaking at 300MHz. When re-simulated with added parasitics, the peaking was moved to approximately 30MHz, which is consistent with the measurement.

The bond-wire parasitics and off-chip capacitances that give rise to this undesirable peaking at 30MHz, will only be encountered in testing, since the transconductor will not drive an external load in normal operation. Therefore, the peaking at lower frequencies will not occur during operation as an FIR filter, and will not effect the frequency response of the overall circuit. The peaking is, however, a concern in one respect; it provides higher gain to noise signals and clock harmonics at higher frequencies. Therefore, care must be taken to provide extra filtering to eliminate high-frequency noise that can couple into the signal through the transconductor.

6.3 SI-FIR Filter: Frequency Response

The SI-FIR filter is a general-purpose 16-tap FIR filter with fully-programmable digital coefficients. It can be configured in a variety of ways. For the measurements that follow, seven different sets of coefficients were chosen to configure the filter for practical lowpass and bandpass applications. The quantized coefficients were stored in an EPROM on the test board. Programming is achieved at a lower clock frequency, and the normal clock rate is restored in the operation mode. The Parks-McClellan optimal equiripple FIR filter design algorithm in *Matlab* was used to compute the coefficients. An eighth

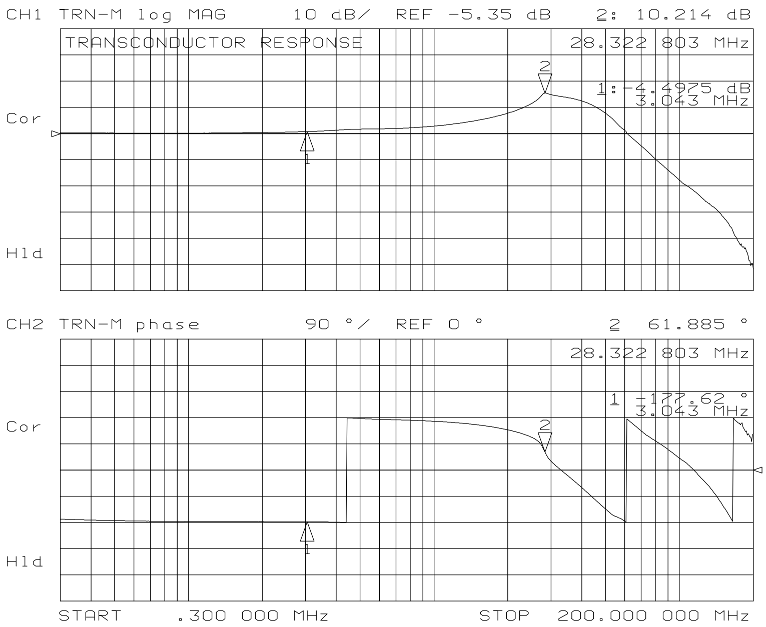


Figure 6.6 Measured frequency response of the transconductor

set of coefficients was also generated, which is essentially an allpass function with the first coefficient h_0 equal to 1 and all others equal to 0. The specifications for the 8 different test configurations are tabulated in Table 6.2.

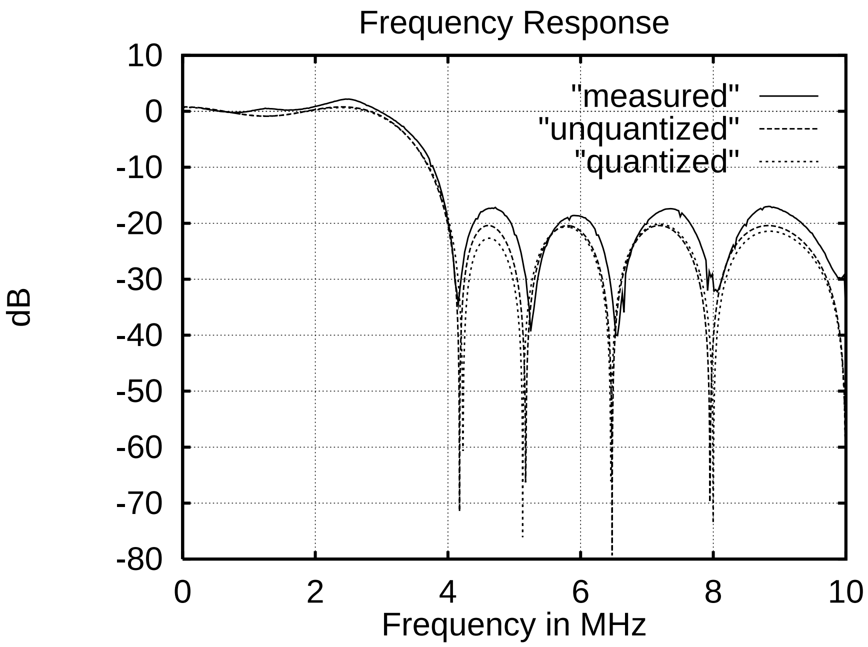
Set	Type	Sampling Frequency	Transition bands
1	lowpass	20MHz	3MHz - 4MHz
2	lowpass	10MHz	3MHz - 4MHz
3	lowpass	20MHz	2.5MHz - 3MHz
4	lowpass	10MHz	2.5MHz - 3MHz
5	lowpass	20MHz	5MHz - 6MHz
6	bandpass	20MHz	1MHz - 2MHz, 3MHz - 4MHz
7	bandpass	20MHz	1.5MHz - 2.5MHz, 5MHz - 6MHz
8	delay	20MHz	not applicable

Table 6.2 Test sets for different sampling rates and different filtering functions

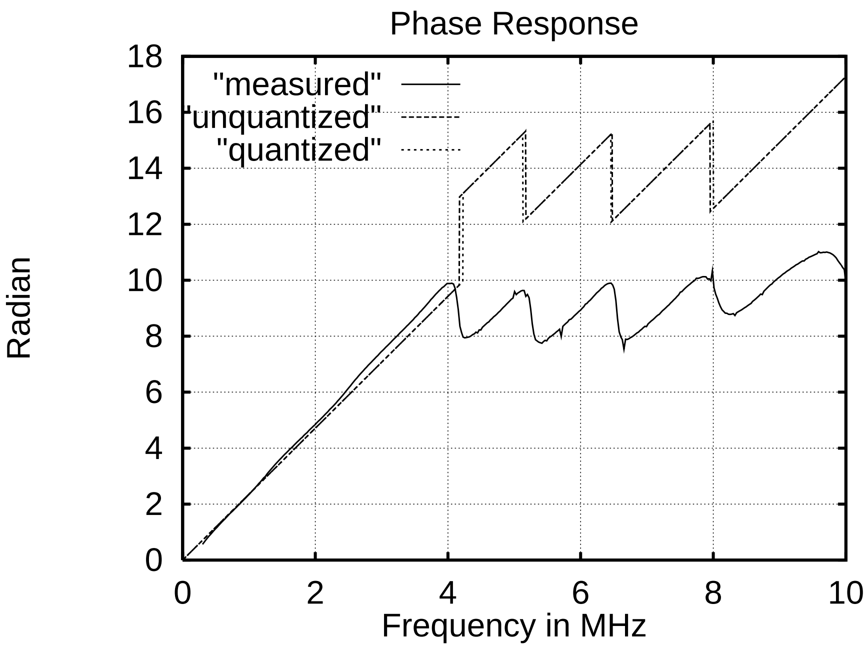
6.3.1 Lowpass Filters

Five different lowpass-filter configurations were tested. The frequency response of the filters in each of these five different lowpass configurations is shown in Figs. 6.7–6.11. In each figure the magnitude response is given in (a) and the phase response is given in (b). Each measured curve is compared to an ideal response shown as a dotted-line.

In all five cases there is excellent correspondence between the ideal and the measured response. This shows that the SI-FIR filter works as designed and can be used in a variety of different lowpass configurations. The measured phase is also clearly linear over the passband.

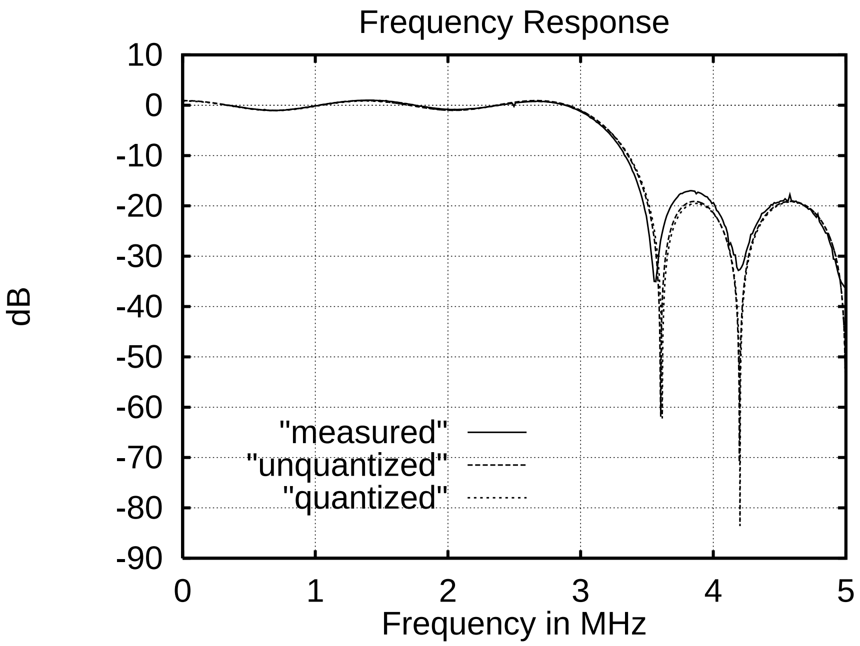


(a) Measured frequency-response plots with the ideal response

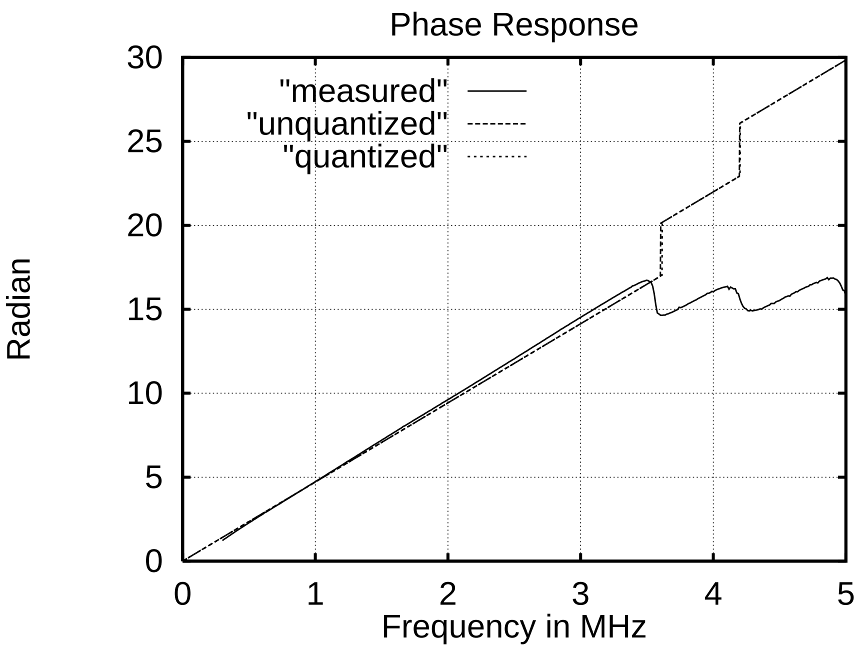


(b) Measured phase-response plots with the ideal response

Figure 6.7 Measurement results of lowpass-filter implementations (Set 1). The solid lines are measured data; dashed lines are ideal responses with (i) ideal coefficients, (ii) 8-bit quantized coefficients.

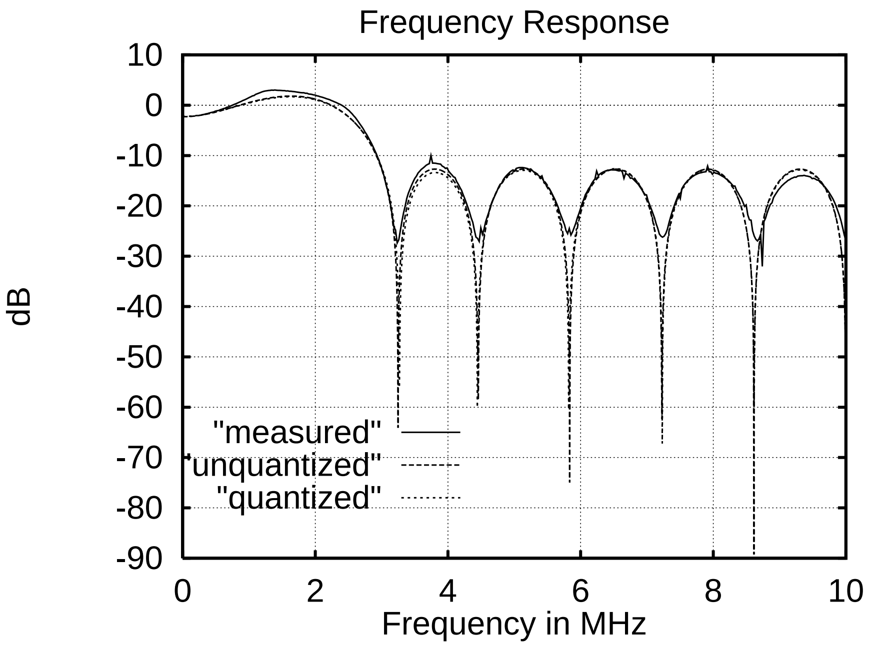


(a) Measured frequency-response plots with the ideal response

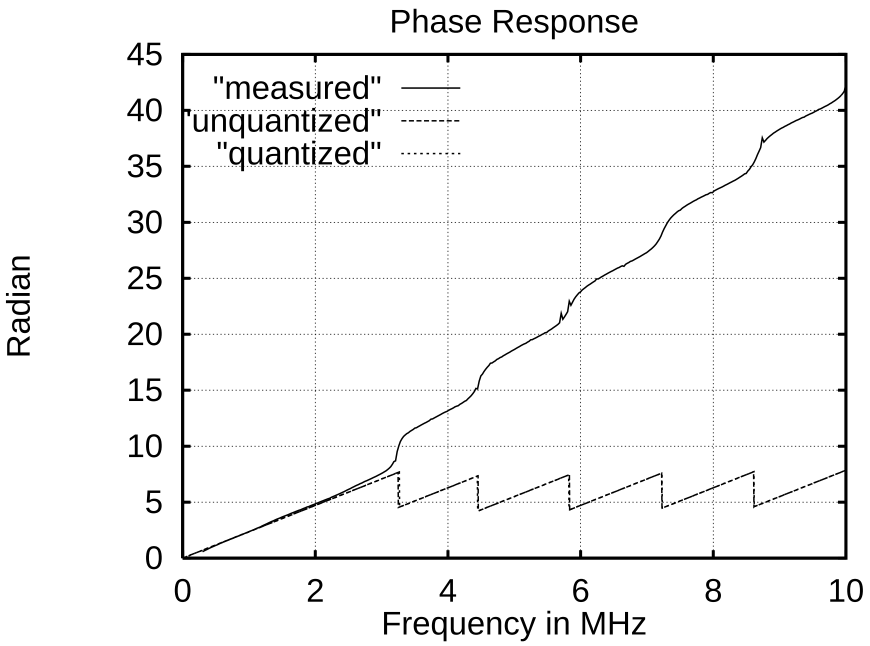


(b) Measured phase-response plots with the ideal response

Figure 6.8 Measurement results of lowpass-filter implementations (Set 2). The solid lines are measured data; dashed lines are ideal responses with (i) ideal coefficients, (ii) 8-bit quantized coefficients.

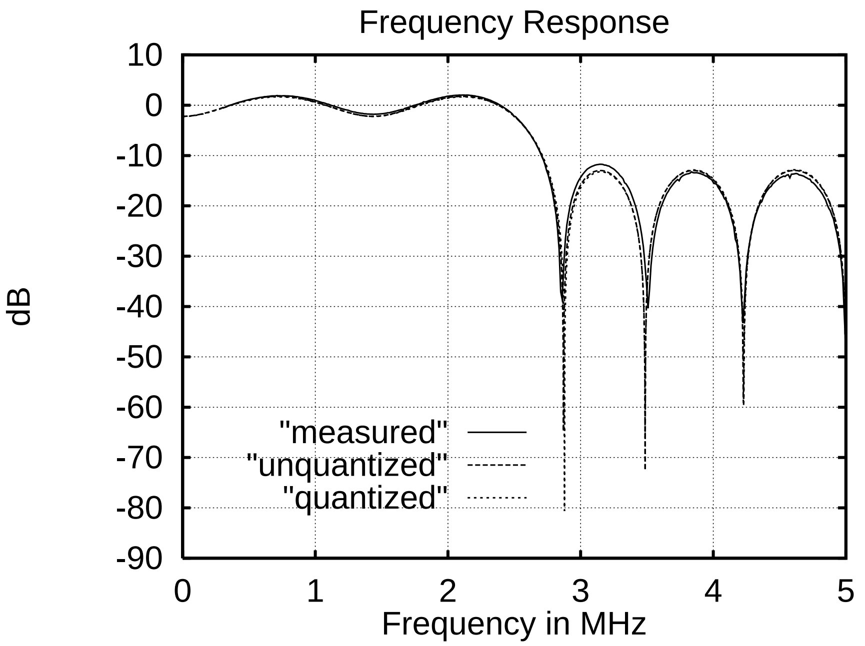


(a) Measured frequency-response plots with the ideal response

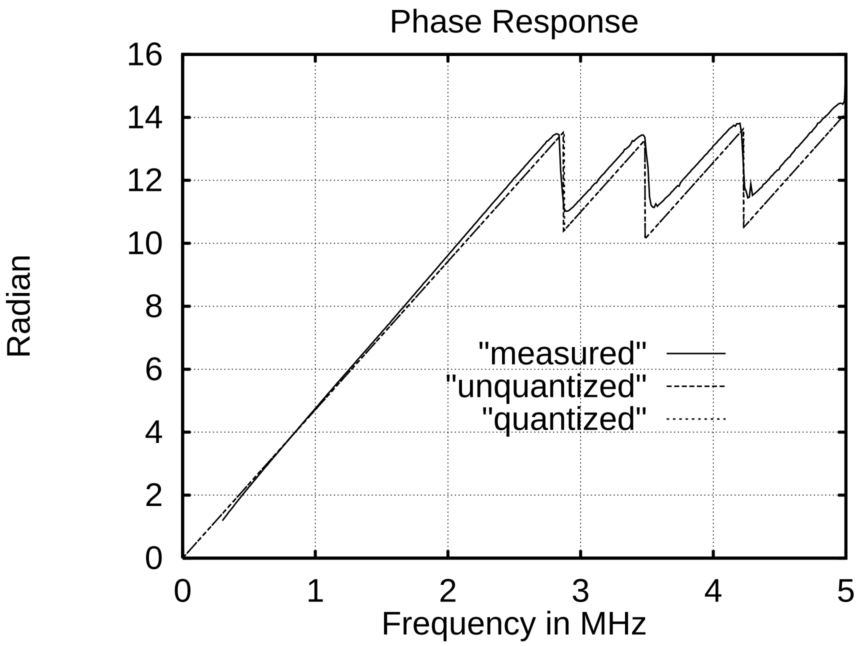


(b) Measured phase-response plots with the ideal response

Figure 6.9 Measurement results of lowpass-filter implementations (Set 3). The solid lines are measured data; dashed lines are ideal responses with (i) ideal coefficients, (ii) 8-bit quantized coefficients.

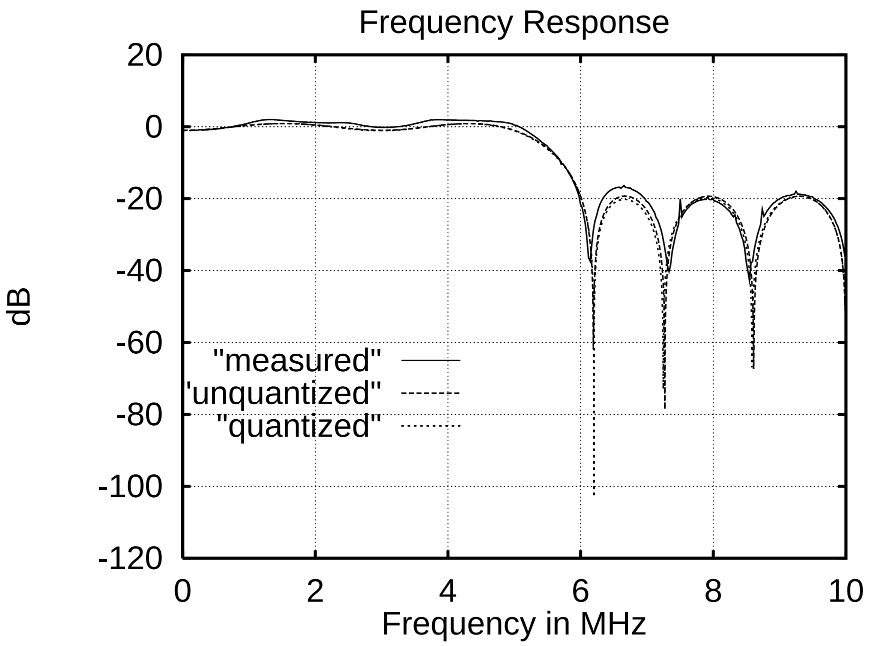


(a) Measured frequency-response plots with the ideal response

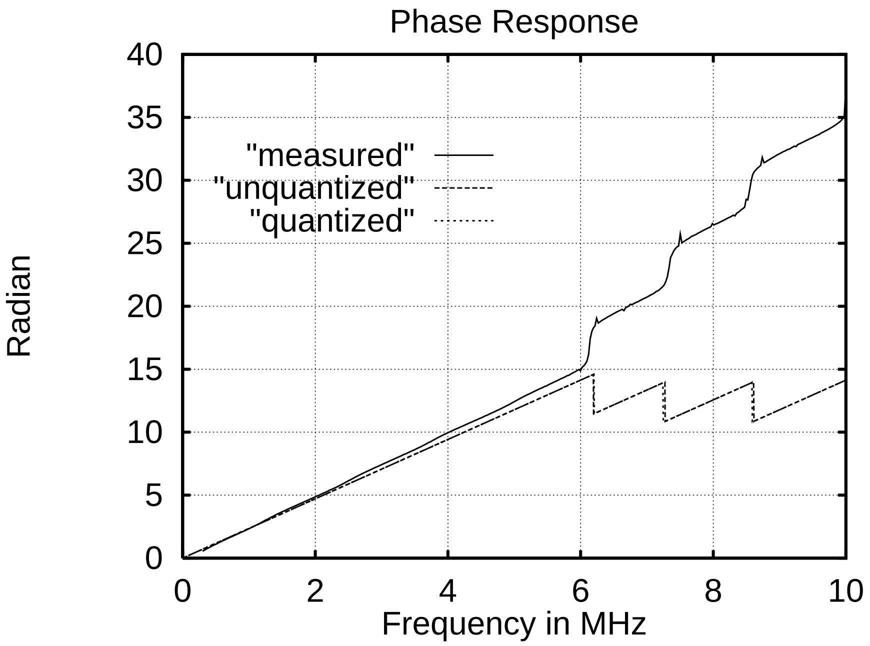


(b) Measured phase-response plots with the ideal response

Figure 6.10 Measurement results of lowpass-filter implementations (Set 4). The solid lines are measured data; dashed lines are ideal responses with (i) ideal coefficients, (ii) 8-bit quantized coefficients.



(a) Measured frequency-response plots with the ideal response

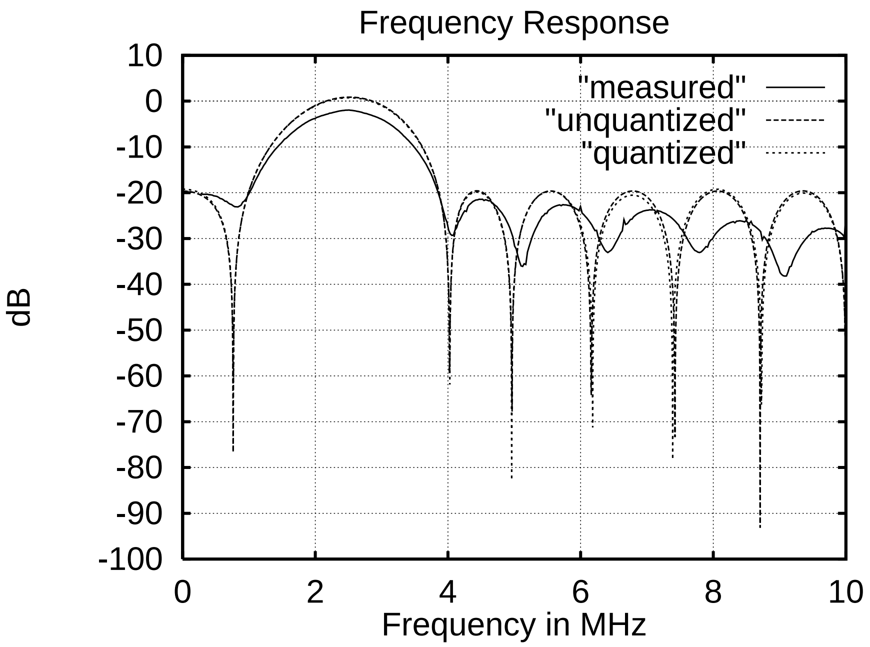


(b) Measured phase-response plots with the ideal response

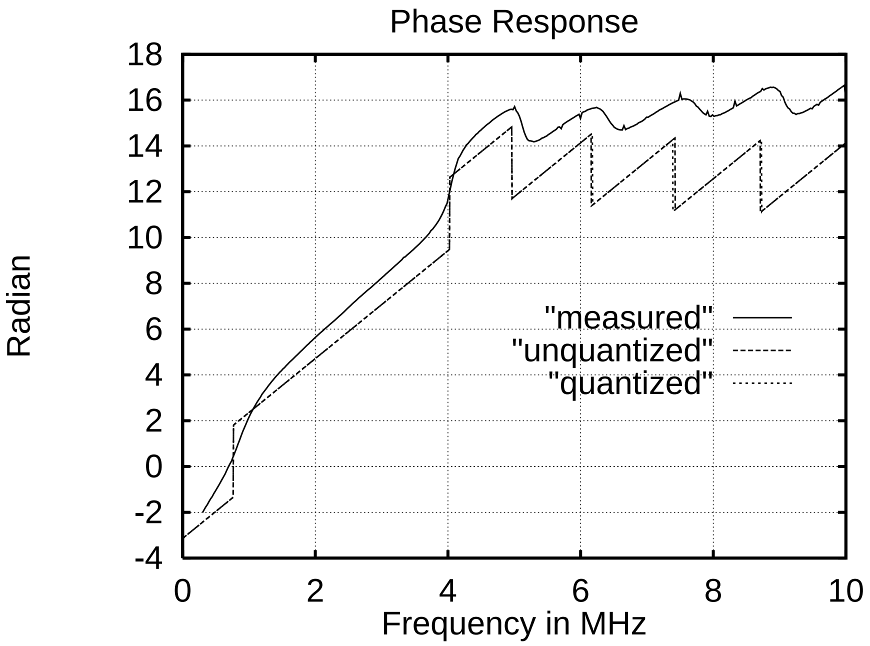
Figure 6.11 Measurement results of lowpass-filter implementations (Set 5). The solid lines are measured data; dashed lines are ideal responses with (i) ideal coefficients, (ii) 8-bit quantized coefficients.

6.3.2 Bandpass Filters

The measured frequency response of two different bandpass-filter configurations are shown in Figs. 6.12 and 6.13. These measurements illustrate that the SI-FIR filter can be configured for various bandpass applications; the center frequency and bandwidth are completely user-programmable. The results of Fig. 6.12 shows a narrowband filter response centered at approximately 2.5MHz with a bandwidth of 2MHz, whereas Fig. 6.13 shows a bandpass spectrum with a bandwidth of 3.5MHz, centered at approximately 3.5MHz. The phase response of each filter also shows linear phase over the passband.

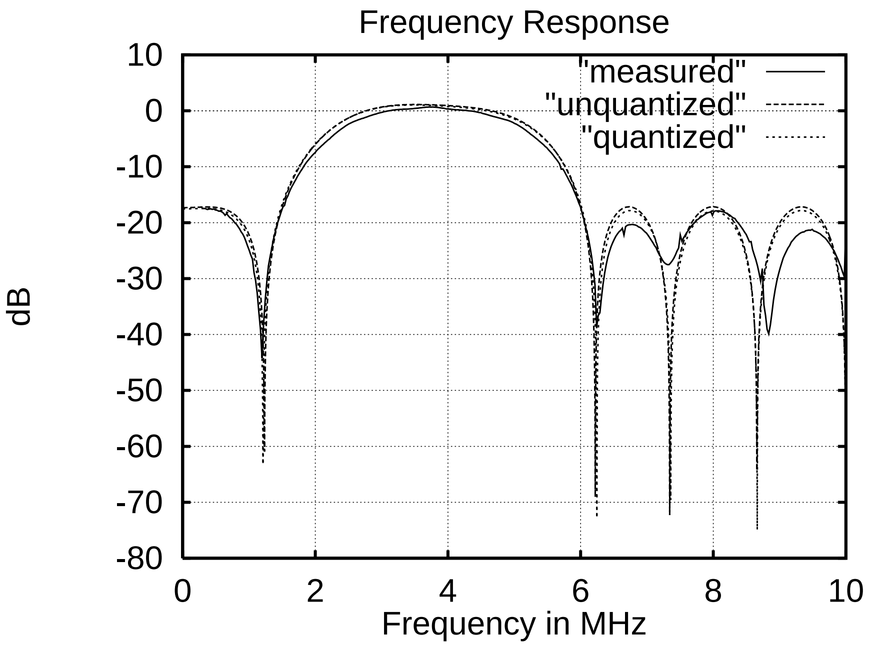


(a) Measured frequency-response plots with the ideal response

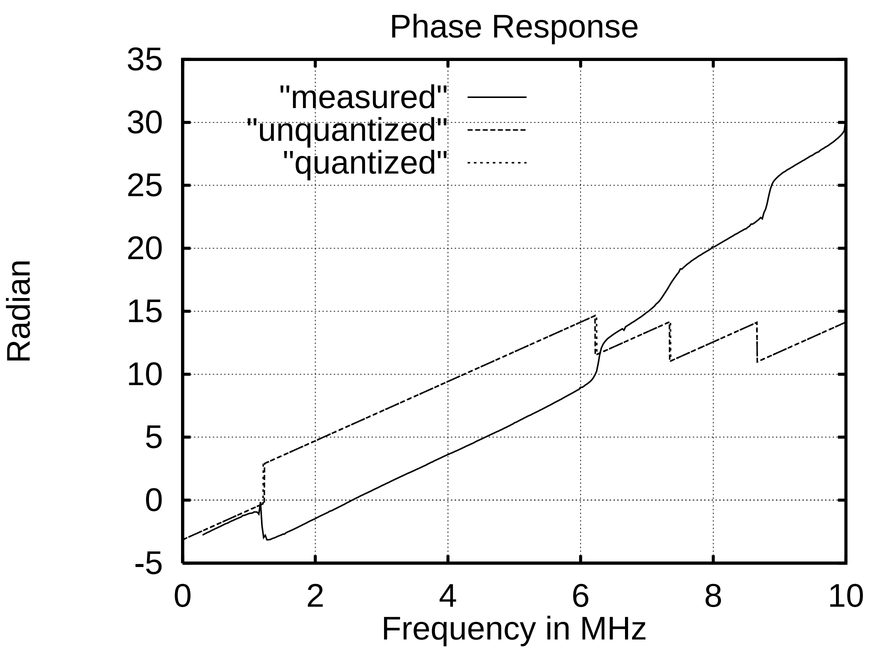


(b) Measured phase-response plots with the ideal response

Figure 6.12 Measurement results of bandpass-filter implementations (Set 6). The solid line are measured data; dashed lines are ideal responses with (i) ideal coefficients, (ii) 8-bit quantized coefficients.



(a) Measured frequency-response plots with the ideal response



(b) Measured phase-response plots with the ideal response

Figure 6.13 Measurement results of bandpass-filter implementations (Set 7). The solid line are measured data; dashed lines are ideal responses with (i) ideal coefficients, (ii) 8-bit quantized coefficients.

6.3.3 Allpass Filter

Response of the SI-FIR filter configured as an allpass function with the center-tap coefficient equal to unity and all other taps equal to zero, is shown in Fig. 6.14. These results show the flat frequency spectrum and linear phase delay as expected. The versatility of the SI-FIR filter makes it useful as a general-purpose analog delay. By setting any one of the 16-taps to 1, a variable delay spanning 16 clock cycles can be generated. This feature may be useful for some communication applications.

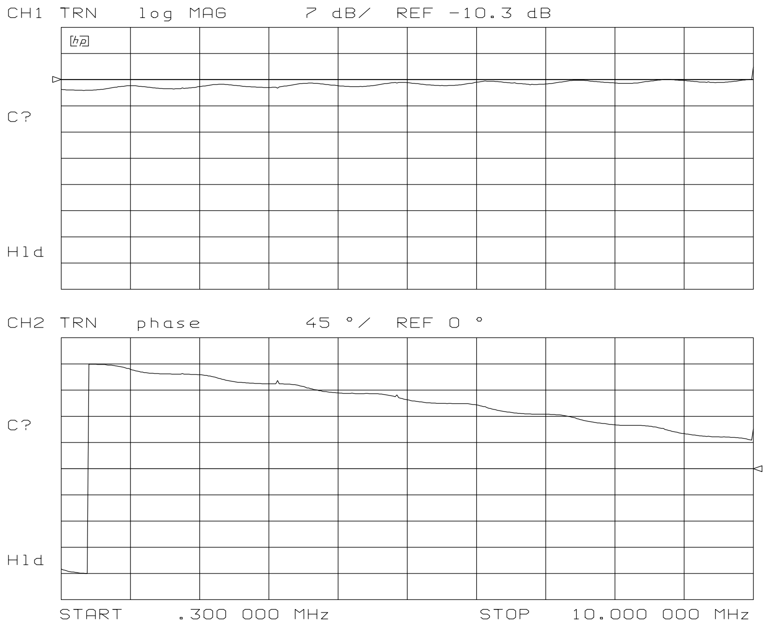
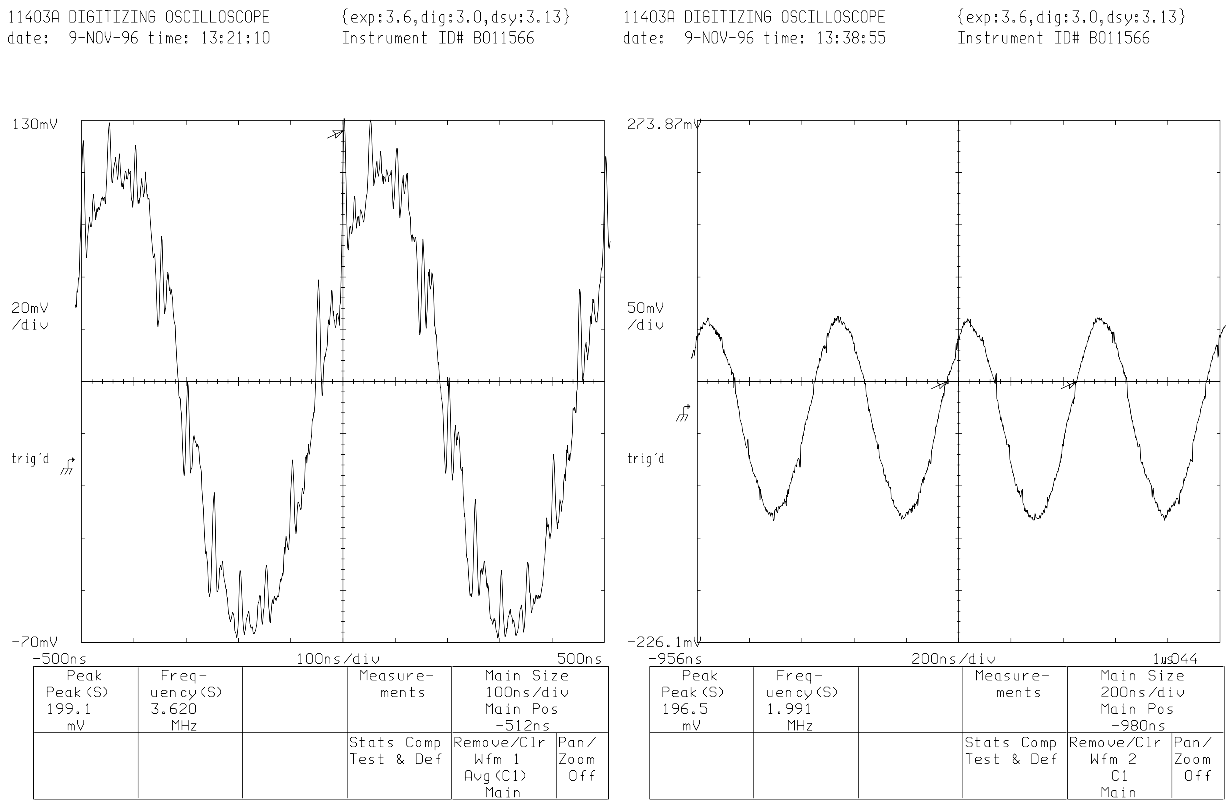


Figure 6.14 Measurement result of a pure delay function (Set 8).

6.4 Time-Domain Measurements

A 2MHz sinusoidal waveform was applied to the filter, and the corresponding output was measured by a sampling oscilloscope as shown in Fig 6.15:

(a) is the direct observation of the output without a post-smoothing filter, (b) shows the output after smoothing by a filter with a cut-off frequency of 10.7MHz. This measurement shows that the time-domain waveform has high-frequency content due to the sampled-data nature of the circuit, and it also contains glitches due to clock-feedthrough, via charge injection from the switches.



(a) Output waveform without a smoothing filter (b) Output waveform with a smoothing filter

Figure 6.15 A 2MHz signal at the output of the filter

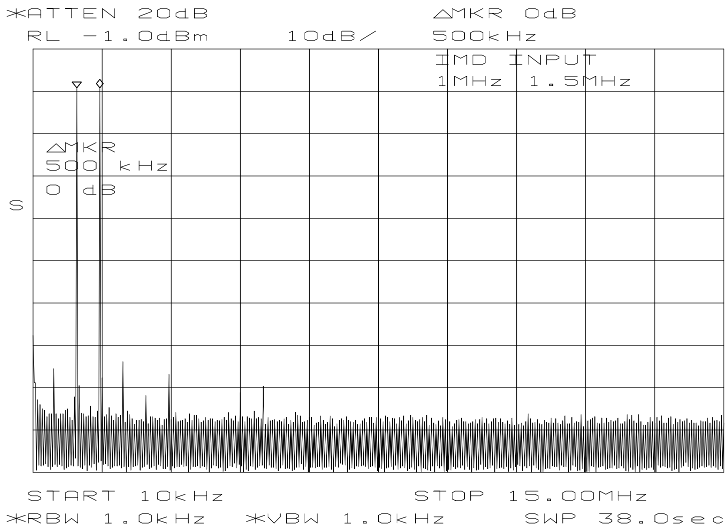
6.5 Distortion of the SI-FIR Filter

The distortion of the filter will limit its applicability to broadband communication systems. For disk-drive read/write channels, 4–6bits of linearity is needed, whereas in 16-QAM and 64-QAM, 5–7bits is desired. The goal of this project was to achieve 7-bits of linearity at 20-MS/s, which is applicable to 64-QAM digital video systems.

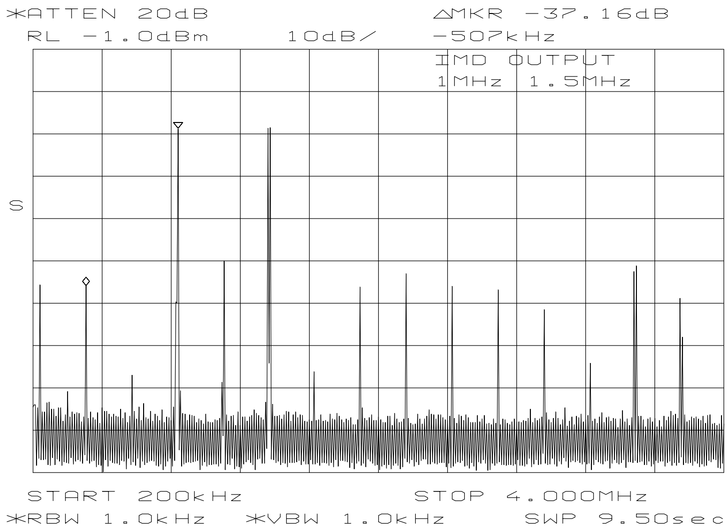
Distortion is often classified using a single tone and measuring the energy of all the harmonics. This ratio of the power in the fundamental, to the total power in all the harmonics, is know as total-harmonic distortion (THD). This is not a very good measurement for determining the distortion of a filter, because the filter will attenuate the higher harmonics it produces.

A much better, and more stringent test, is to perform a two-tone measurement near the passband edge. Nonlinearities will cause intermodulation distortion (IMD) and the IMD products will fall back in band and won't be attenuated by the filter. To perform the two-tone intermodulation distortion test, two equal-magnitude sinusoidal signals with frequencies of 1MHz and 1.5MHz respectively were summed by passing them through an RF power combiner, which is then applied to the input of the filter. The summed amplitude was $0.5V_{pp}$. The input spectrum is shown in Fig. 6.16(a), where 3rd-order intermodulation products are down by approximately -65dB.

The SI-FIR filter was configured as a delay function in this intermodulation distortion measurement. The spurs shown in Fig. 6.16(b) contain the spectrum of the digital noise signals along with the IMD distortion. The presence of a spectral component at 1.25MHz is due to coupling from the digital circuits within the chip. Essentially, this spur arises from the clock frequency divided by the number of taps (20MHz/16 equals 1.25MHz). This can be confirmed by varying the clock frequency, which introduces the expected



(a) IMD input spectrum



(b) IMD output spectrum

Figure 6.16 Input and output spectrum for the intermodulation distortion measurement variation of the output spectrum. Third-order intermodulation-distortion products are expected at 0.5MHz (-37dBc) and 2.0MHz (-40dBc).

Problems with Clock Feedthrough There are two problems with this measurement. The first is that the clock spur at 1.25MHz mixes with the input signals of 1MHz and 1.5MHz to produces sum and difference frequency that lie on top of the 3rd-order intermods. Therefore, it is difficult to determine whether the errors at 0.5MHz and 2MHz are due to distortion or clock feedthrough.

Problems Measuring Distortion of Sampled-Data Systems A much more fundamental problem for finding the actual distortion of the SI-FIR filter arises because this is a sampled-data system, where the output data is only valid for a fraction of the clock cycle. Therefore, any distortion in the sample/track mode due to slewing, or any other nonlinear transient, will show up as distortion, when in fact, it is not. It is only important that the filter have low distortion in the hold-state, after the output settles. What is needed for more accurate measurements is to resample the output for further analysis. Ideally, the data can be resampled and quantized using a 10-bit ADC and the digital samples can be processed to determine a much better estimate of the the distortion of the SI-FIR filter. At the time of this writing no such tests have been performed. From simulations and measurements, the circuit appears to maintain a resolution of greater than 42-dB (7-bits) for frequencies up to 10-MHz. More accurate measurements will be performed in the future to confirm these results.

6.6 Further Research

In this thesis a technique was presented for designing digitally-programmable analog FIR filters. The technique was demonstrated using a 16-tap prototype filter. In the development of the prototype, many features were added to aid in testing and evaluation; these features add parasitics which often degrade circuit performance. By eliminating many of these test features, circuit performance will improve. Other modifications to the prototype, which can be made to improve resolution and speed, are described below.

6.6.1 Switched-Current Memory Cells

In this thesis, a class-AB current-memory cell is used with a dummy-transistor compensation technique to reduce the error caused by clock-induced charge-injection. Alternatively, an enhanced class-AB memory cell can be realized in n-steps (S^nI)[28], which cancels higher-order charge injection errors, and results in a more precise gain. However, there is often a compromise between accuracy, complexity and die-area.

An n-step memory cell needs $2n$ clock phases for sampling and holding the signal; increased complexity of clock phase generation is obvious in this approach. The clock-phase generation circuitry resides in the digital-logic section of the partition, and will grow in size. If we integrate the memory cell with the other analog filter components, the extra clock phases would have to be routed to the memory cells from the digital clock-generation circuit. Noise coupling may get worse as there will be multiple clock signals for each tap. In an FIR filter application, the output is the weighted sum of all taps. Performance improvement due to increased accuracy of each memory cell cannot be easily predicted by intuition. Detailed analysis and simulation have to be used. This is an area where further research is needed.

6.6.2 Fully-Differential Design

Currently, a pseudo-differential design is employed in this prototype chip. A fully-differential design would help to cancel even-order harmonics and common-mode offsets; but such distortion reduction is not guaranteed with a pseudo-differential configuration. Further design work should transform the existing one to a fully-differential architecture to enjoy the benefits cited above.

6.6.3 Optimization of Building Blocks

The primary focus of this work has been to design a first-generation prototype circuit. Correspondingly, we have not focused on optimizing the speed and precision of each circuit block once the architecture was chosen. After this filter has been demonstrated to be fully functional, further optimization will be needed to improve various aspects of performance, such as: sensitivity to temperature, immunity to power-supply variations, the dynamic range of transconductance, and the precision of the current-memory cells.

6.6.4 Layout Improvements

Noise coupling from the digital circuits into the analog output was found to be persistent, as reflected by the measurement results. Thus, there is still room for improvement in the layout. Double guard rings can be used to reduce the noise coupling from the digital part. Careful examination of the layout revealed that crossing of metal clock-lines with signal lines can be eliminated by flipping the current-division-ladders upside-down, which moves the three output current metal lines to the top of the ladders and away from the clock lines.

Chip area can be further reduced using data-path cells rather than standard cells for the digital part. In data-path cells, horizontal routing channel can be eliminated. Adjacent cells can be routed on the top of the cells instead of using dedicated routing channels.

6.6.5 Noise Analysis

This circuit is a sampled-data system. HSPICE has excellent white-noise analysis routines for continuous-time circuit, but is notorious for having no means to add noise for transient simulations. The main noise sources in this circuit are switching noise from both the digital circuits and the analog memory cells. To estimate the noise contributes from the memory cells, equivalent noise sources would have to have been added in parallel with each transistor. Such an addition, not only significantly lengthens the simulation time, but also complicates the design process. Therefore, throughout the design, noise analysis has been omitted due to its complexity and long simulation time. In the future some type of switching noise simulation can be added so that the circuit can be further optimized.

6.6.6 Powers-of-Two Coefficients

In ordinary digital FIR filters, powers-of-two coefficients are widely used. The discrete coefficients are represented as the sum or difference of several numbers in a set of powers-of-two numbers. The proposed architecture is not eligible to implement such a scheme. To represent a powers-of-two number, more than one sampled signal must be provided simultaneously. Further research on the utilization of this feature is strongly encouraged.

6.7 Conclusions

A versatile sampled-data analog FIR filter architecture with fully-programmable digital coefficients was presented. A new architecture was developed which utilized analog circuits for signal-processing operations and digital circuits for precision delays and control. The result is a low-power, small-area circuit, which is extremely flexible and can be used as an adaptive or programmable equalizer in communication and data-storage applications.

A prototype circuit was developed for a 20-MS/s application. The circuit, fabricated in a 0.8μm CMOS 3M1P process, demonstrates that the architecture can provide a variety of transfer functions with a linearity equivalent to a 7-bit digital system. Measured performance is summarized in Table 6.3.

Table 6.3 Summary of the prototype filter

FIR tap numbers	16
Technology	HPCMOS26G 0.8-μm CMOS
Coefficient length	1 sign-bit, 8 magnitude bits
Core area	2408μm x 1762μm
Whole chip with pads	3560μm x 3560μm
Maximum clock rate	20MHz
Power Supply	5V
Power Consumption	70mW @ 20MHz
Packaging	65-pin PGA
Transistor count	9511

A much-higher-speed version (~200-MS/) of the filter can be achieved at the expense of higher power and lower resolution by replacing the transconductor and current-copier cells with simplified versions. By optimizing the architecture for high-speed performance a 150-MHz 5–6bit version can be designed. A pair of such filters can be interleaved for application to a programmable equalizer for Class-IV and PR-IV 300-MS/s magnetic disk read channels.

> *"There is no short cut to success: if you want to reach the promised land, you must go through the wilderness."*