A Wide-Band CMOS Frequency Generation System for Software-Defined Radios

by

Rong Sujiang

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The Hong Kong University of Science and Technology

in Partial Fulfillment of the Requirements for

the Degree of Doctor of Philosophy

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August 2010

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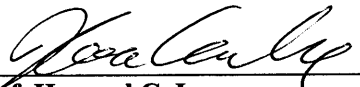
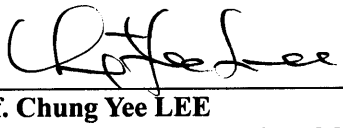


Prof. Howard C. Luong
Thesis Supervisor



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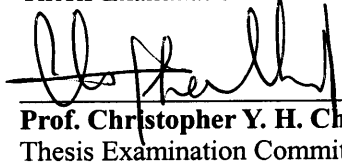
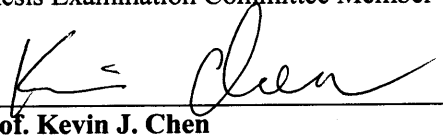


Prof. Christopher Y. H. Chao
Thesis Examination Committee Member

Prof. Philip K. T. Mok
Thesis Examination Committee Member



Prof. Kevin J. Chen
Thesis Examination Committee Member

Prof. Ross D. Murch
Head of Department

Department of Electronic and Computer Engineering
The Hong Kong University of Science and Technology

August 2010

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To little Emma, Zhiyi Rong

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A Wide-Band CMOS Frequency Generation System for Software-Defined Radios

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RONG, Sujiang

Department of Electronic and Computer Engineering

The Hong Kong University of Science and Technology

Abstract

The ever-increasing demand for global mobility and multi-media services has motivated the realizations of multi-mode, multi-band and multi-standard wireless communication systems. Software-defined radio (SDR), in which some or all of the physical layer functions are software defined, encompasses a wide range of design techniques to realize fully reconfigurable transceiver systems. It is an attractive radio platform that covers not only all the existing wireless standards (including cellular, WLAN, WPAN, broadcast, positioning, etc,) but also the future standards. Such a radio requires ultra-wideband (UWB) in-phase and quadrature-phase (IQ) local oscillation (LO) signals with sufficiently high spectrum purity to support diverse specifications. In this thesis, several novel circuit topologies and design techniques are proposed and integrated to realize for the very first time an ultra-wideband frequency generation system (FGS) for SDRs in low-cost CMOS processes.

Firstly, complete analysis is derived and presented for both dual-band one-port and two-port oscillators using transformer-based fourth-order LC tanks. Based on the results, a dual-band quadrature voltage-controlled oscillator (Q-VCO) is systematically designed and implemented in a 0.13-μm CMOS process for SDR applications. The prototype achieves a dual-band operation with IQ output signals

from 2.7GHz to 4.3GHz and from 8.4GHz to 12.4GHz.

Secondly, novel current-bleeding (CB) and current-reusing (CR) techniques are proposed, to efficiently enlarge and maximize the locking ranges of injection-locked frequency dividers (ILFDs) and Miller dividers (MD) without extra inductive components and extra power consumption. Implemented in a 0.13μm CMOS, two CR-ILFD prototypes, operating with 7GHz and 60GHz inputs, achieve around 3x and 2x locking range improvement, respectively. In addition, a 60GHz CB-MD prototype improves the locking range by more than 5x.

Thirdly, new circuit topologies, including a reconfigurable injection locking based frequency multiplier and a tunable 3GHz-to-10GHz transformer-based narrow-band LC-tank for single sideband (SSB) mixers, are proposed to implement the 14-band MB-OFDM UWB carrier generator into the FGS. Experimentally, the generator achieves sideband rejections (SBRs) better than 31dB for all the 14-band carriers from 3GHz to 10GHz.

Fourthly, a novel interpolative-phase-tuning technique is proposed to implement varactor-less multi-phase LC oscillators with a wide tuning range and a low phase noise at millimeter-wave (MMW) frequencies. Two phase-tuning oscillator prototypes, one with 8-phase 50GHz outputs and another with 4-phase 60GHz outputs, achieve state-of-the-art performance in terms of phase noise, figure-of-merit (FOM), and figure-of-merit with tuning range (FOM_T).

Fifthly, an alternative method of using high frequency multipliers to synthesize the MMW LO frequencies is also investigated. Two injection-locked frequency multiplier (ILFM) chains are designed and demonstrated to provide LO signals for both direct-conversion and dual-conversion transceivers operating at 60GHz band. A proposed automatic peak calibration technique is also implemented for the ILFM

chain to effectively improve the output swing and the spur rejection performance with a small area and low power.

Finally, employing these circuit techniques and topologies, a wideband SDR frequency generation system with a reconfigurable phase-locked loop, is proposed and demonstrated. The prototype successfully provides IQ LO signals with sufficiently good phase noise not only from 47MHz to 10GHz but also from 18GHz to 22.5GHz and from 37GHz to 44GHz for all the wireless standards (including GSM900/DCS/PCS, UMTS, WLAN, WiMAX, Bluetooth, DECT, ZigBee, DVB-T/H, GPS, UHF-RFID, MB-OFDM UWB and UWB 802.15.3c).

Chapter 1

Introduction to Software-Defined Radios

1.1 Background

The wireless industry has experienced a phenomenal growth over the past decades. It continues to provide higher data rate, more portable and flexible communications for users. Existing wireless access technologies today have been well developed for specific applications in terms of range, mobility, and data rate. As shown in Fig. 1.1, cellular standards have provided the mobile voice and data services with limited data rate. To improve the speed of communication, the technology has made advances from one generation to the next generation. The standards Wifi and UWB provide high data rate services within a local or personal area network. And access technologies like Bluetooth and Zigbee can provide lower power consumption and longer standard-by period with lower speed wireless communications.

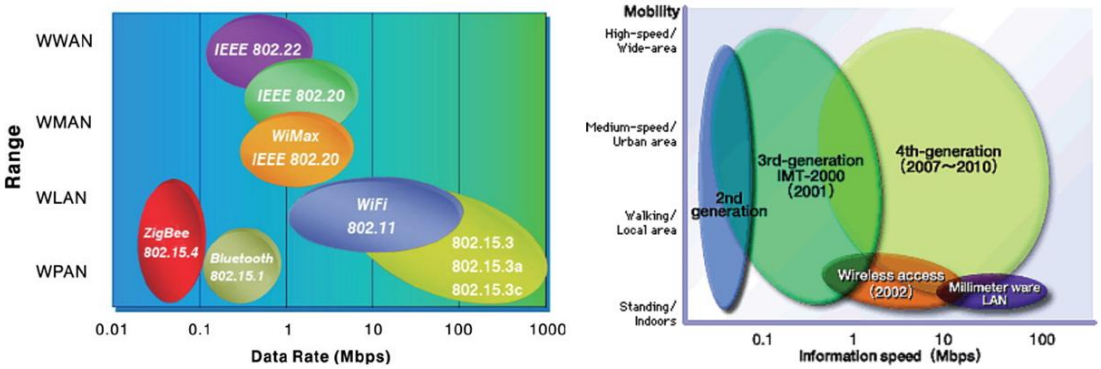


Fig. 1.1 Data rate versus range and mobility for different wireless technologies

In order to fulfill the requirements for diverse applications such as voice, graphic, TV broadcasting, games, positioning, and so on, that can be suitably covered by

different proper access technologies, and also to enable the global roaming within various cellular systems coexisting all over the world, the modern radio is required to support different standards and sub-standards with different carrier frequencies, bandwidth and modulation schemes. A wireless terminal with multiple radios integrated together may provide a short-term solution, but the area and cost would increase proportionally when more and more standards need to be supported. This has driven the wireless industry to look for certain reconfigurable radio whose hardware can be programmed and defined by software to cover diverse standards, namely, a software-defined radio (SDR). The ideal SDR should have the maximal flexibility and cover any existing and future standards with any modulation scheme at any channel frequency. In this sense, the SDR can never be fully implemented [1].

1.2 Definition of SDR

The wireless innovation forum (the former SDR forum) works in collaboration with the IEEE P1900.1 group to provide a simple definition of the technology as "Radio in which some or all of the physical layer functions are software defined" [2].

Compared to traditional hardware-based radios with limited cross functionality and can only be modified through physical intervention, the SDR technology provides an efficient and relatively low-cost solution to allow multi-mode, multi-band and multi-functional wireless devices to be enhanced through software upgrades. The definition points out that the SDR is a group of hardware and software technologies, which are able to carry out the functions of some or all the radios by software or programmable firmware, such as field programmable gate arrays (FPGA), digital signal processors (DSP), general purpose processors (GPP), programmable system on

chip (SOC) and so on. With these technologies, new wireless features and capabilities can be added to the existing radio systems without adding new hardware. Under the scope of the definition, it is not difficult to find that there are numerous SDR adoptions existing in the market, that make use of and benefit from the SDR technology, though, they may not be marked as "SDRs". Combo Cellular and WLAN terminals are now everywhere, which can support multiple standards or sub-standards at various bands by using programmable processing devices. Numerous SDRs have been successfully deployed in defense applications. And satellite "modems" that are commercially available make great use of programmable devices for intermediate frequency (IF) and baseband signal processing [2].

1.3 Motivations for SDR

1.3.1 Benefits

Although there are many technical challenges that need to be solved to enable SDRs to be widely adopted in the market, the advent of this promising technology has already revolutionized the business model of the wireless industry. The potential benefits of SDR can be specifically seen from the perspective of three parties [2][3].

1. For original equipment manufacturers (OEMs): A series of radio products can be implemented based on a common platform architecture, so new standards and new products can be quickly adopted and introduced to the market. The software can be reused across radio products, reducing the cost of development dramatically. Moreover, in terms of the hardware, only a single platform needs to be supported, cutting the time and cost for the "after-sale-service" considerably.
2. For network operators: Firstly, new features and capabilities can be added to the

existing infrastructure, without major new capital expenditures. Secondly, a common radio platform can be reused for multiple markets, saving the cost. Thirdly, by the mean of remote software download, it is easy to upgrade the capabilities for the users.

3. For end users: the cost to access various wireless communications can be much reduced, and the SDR can provide genuine global roaming and full PC-like software upgradability. The maximal hardware sharing of the SDR can also reduce the size and weight of the terminal, making the handset more portable.

1.3.2 Efficient Spectrum Utilization

Spectrum is a precious resource that needs to be efficiently utilized. Fig. 1.2 shows the spectrum allocations of the existing commercial wireless standards [4]. It can be seen that at those frequency bands around 900MHz, 2GHz and 2.4GHz, the applications are already crowded. Even though there is still much spacing remaining in the plot, the rapid growth of the wireless industry will ultimately drain the spectrum resource in the future. However, currently, as the given spectrum is specifically allocated for a fixed wireless service, if time and space dimensions are taken into consideration, the spectrum is under-utilized, for example, even in New York, the usage efficiency is only 13.1 percent for the spectrum from 30MHz to 3GHz, which is quite contradicted with the scarcity of the spectrum resource. This prompts the future radio to dynamically detect the free spectrum and the available radio access technologies, and provide the most appropriate connection based on user needs, in order to efficiently utilize the spectrum resource.

Therefore, more advanced radio concepts are proposed [2], targeting for the future wireless market. These include

1. Adaptive Radio, which can monitor its performance and adaptively modify the

operation parameters to improve the performance.

2. Cognitive Radio, which can be aware of its internal state and environment, like the spectrum environment at any given time and location, and make decisions about its radio operation by mapping that information against predefined objectives.

3. Intelligent Radio, which is a cognitive radio capable of machine learning.

Although SDR is not required to perform any of the above functions, it is a necessary and fundamental platform for all these advanced radios.

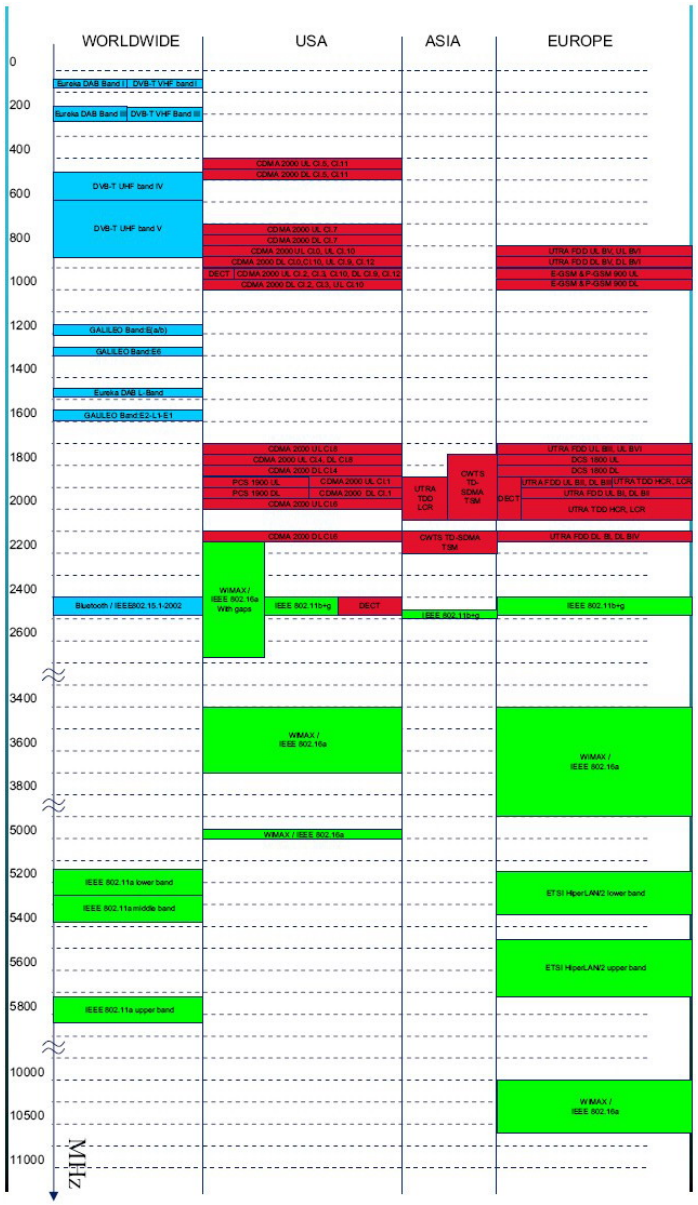


Fig. 1.2 Spectrum allocations of existing wireless standards

Chapter 2

SDR Transceiver Architecture

2.1 Ideal SDR Transceiver Architecture

As shown in Fig. 2.1, the canonical SDR transceiver architecture described by J. Mitola [5] is maximally digitalized. Because digital circuits are more programmable than analog circuits, most of the signal processing is done in the digital domain. As a result, this architecture has the highest reconfigurable ability.

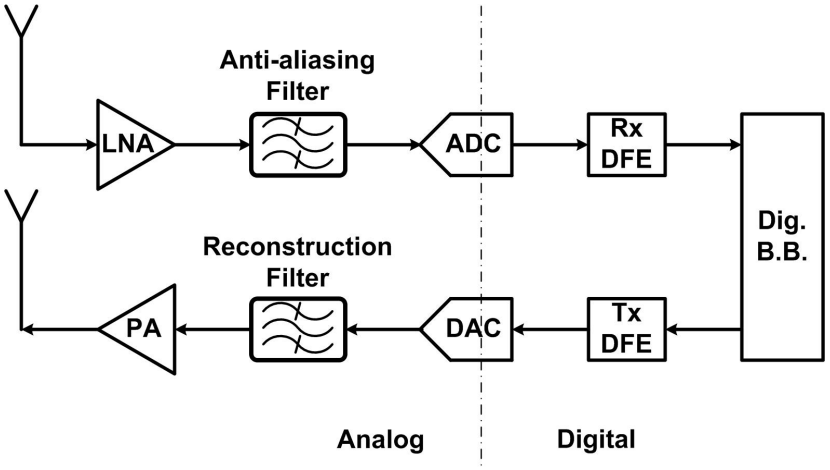


Fig. 2.1 Ideal SDR transceiver architecture

However, in this architecture, the front-end ADC and DAC need to handle the radio frequency signals in a complex environment. For example, to fulfill the blocker specification of the UMTS standard as shown in Fig. 2.2 [4], the ADC needs to provide a dynamic range of more than 100dB at the sampling rate of 4GHz. This requirement is much more than the capability of the realizable ADC as shown in Fig. 2.3 [6]. Considering the rate of improvement of the state-of-the-art ADCs is around 1.5bit per 8 years, such high performance ADC would not be available in the near

future. Besides, the huge power consumption of hundreds of Watts for such high speed high dynamic range ADC makes such an architecture not suitable for portable applications. For these reasons, the classical SDR transceiver architecture is an ideal concept at least in the current stage.

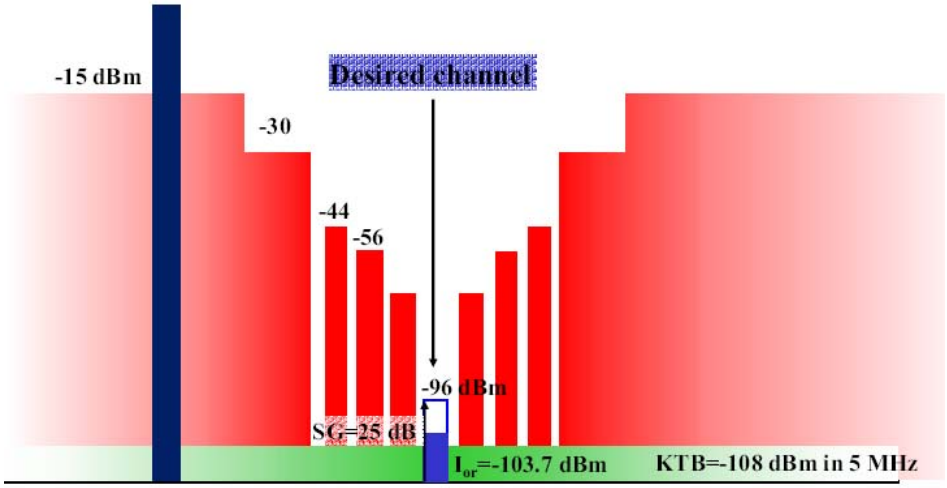


Fig. 2.2 The desired received UMTS channel at block and interference environment

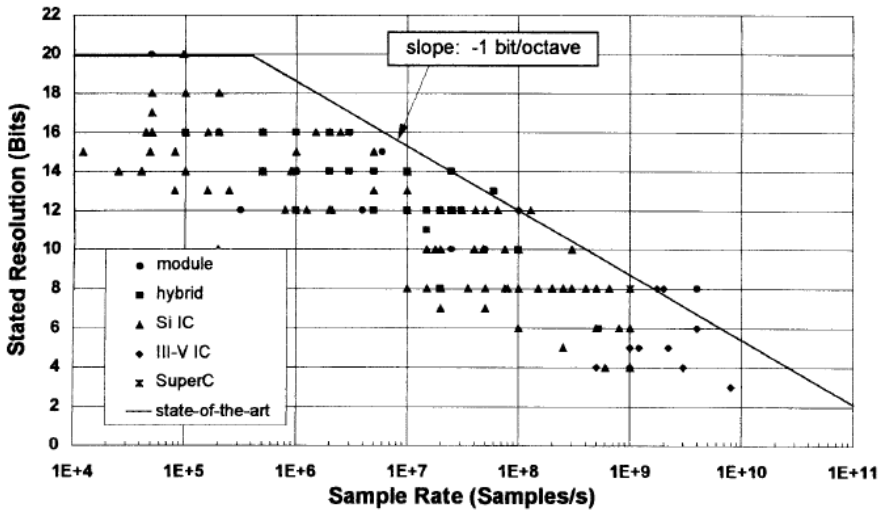


Fig. 2.3 Resolution versus the sampling frequency of the realizable ADC

2.2 Dual-Conversion SDR Transceiver Architecture

Consequently, a RF front-end is required to reduce the operation frequency and dynamic range requirement of the ADC and DAC. Fig. 2.4 shows the dual-conversion

SDR transceiver architecture. Because of the multiple channel selections and filtering provided by the RF/analog front-end, the dual-conversion architecture features a high dynamic range. However, the usage of the off-chip IF filters limits the integration level of the dual-conversion transceiver, and more importantly, the re-configurability of the transceiver's channel bandwidth is restricted by the less adjustable bandwidth of the IF-filters, which makes the dual-conversion architecture inappropriate for the SDR applications.

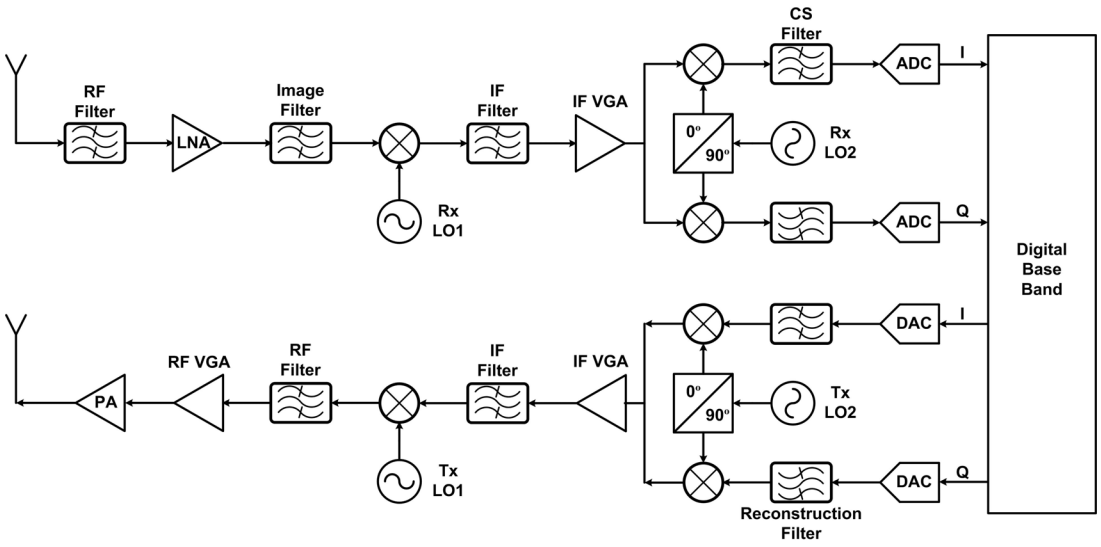


Fig. 2.4 Dual-conversion SDR transceiver architecture

2.3 Direct-Conversion SDR Transceiver Architecture

Fig. 2.5 shows the architecture of the direct-conversion SDR transceiver. The elimination of IF filters allows this transceiver to be highly integrated on chip, and the transmitting and receiving channel bandwidths can be flexibly controlled by adjusting the corner frequency of the low-pass analog baseband filter. In the receiver path, the desired RF signals are directly down-converted to the based-band, therefore the IF frequency is zero. In such a case, the image of the desired signal is itself, thereby, no

image problem exists. The zero-IF receiver allows the ADC to operate at the lowest sampling frequency. However, its performance is limited by the low frequency flicker noise especially in the CMOS technology, and also by the time varying DC-offset at the mixer output due to the self-mixing of the original and leaked LO signals.

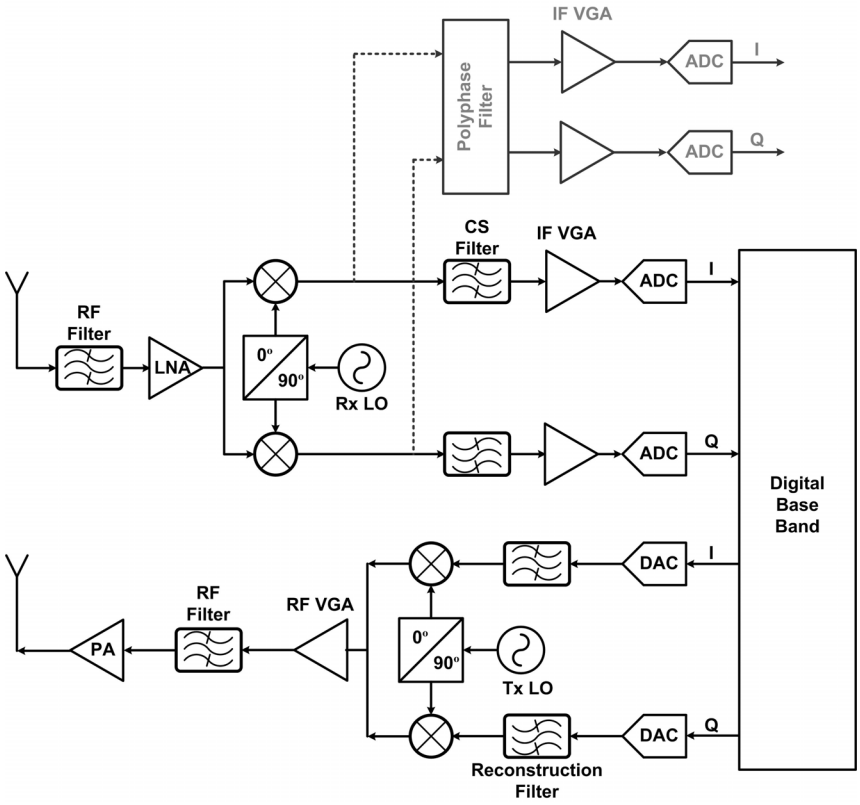


Fig. 2.5 Direct-conversion SDR transceiver architecture

To circumvent the problems, another receiver architecture low-IF receiver can be used, as shown by the gray-line part at the top of Fig. 2.5. The usage of a low frequency IF instead of a DC IF eliminates most of the flicker noise and DC-offset problems. However, the low-IF receiver increases the ADC's sampling frequency and has the image problem. Due to the device mismatch, the image rejection ratio is typically below 40dB. Recently, taking the advantage of the CMOS technology scaling IF signals have been converted and filtered in the digital domain, adding more flexibility and programmability to the SDR transceiver.

The direct-conversion transmitter directly modulates the baseband signals to the RF channels, the issues of the transmitter include the LO-pulling and feed-through, and the biggest issue is the design of the wide-band reconfigurable power amplifier (PA), where sufficient linearization needs to be implemented on the switching mode PA to support modern communications with high power efficiency. More compatible with SDRs, the digital polar [7] and out-phasing [8] transmitters would be more promising than the analog transmitters.

2.4 Proposed SDR Transceiver Architecture

The proposed SDR transceiver architecture is shown in Fig. 2.6. The transceiver targets all the existing wireless standards with channel frequencies from 47MHz to 10GHz as well as 57GHz to 66GHz, including Digital TV, cellular, WLAN, WMAN, WPAN, positioning and passive UHF RFID. The supporting data rate can be up to 3Gb/s provided by the standard 802.15.3c [9] with 2.16GHz channel bandwidth at millimeter-wave (MM-wave) frequency.

The transceiver applies a direct-conversion architecture for standards with channel frequencies below 10GHz, and a dual-conversion architecture to support the MM-wave frequency band. For the dual-conversion transceiver, as the image frequency is 40GHz away from the desired channel frequency, the on-chip building blocks with LC loadings, including the low noise amplifier (LNA), the higher frequency down-conversion and up-conversion mixers, the RF variable gain amplifier (VGA), the power amplifier (PA), can provide sufficient filtering to the image tone, thereby, no IF-filtering is required for the dual-conversion transceiver. As a result, the whole SDR transceiver allows a high level integration.

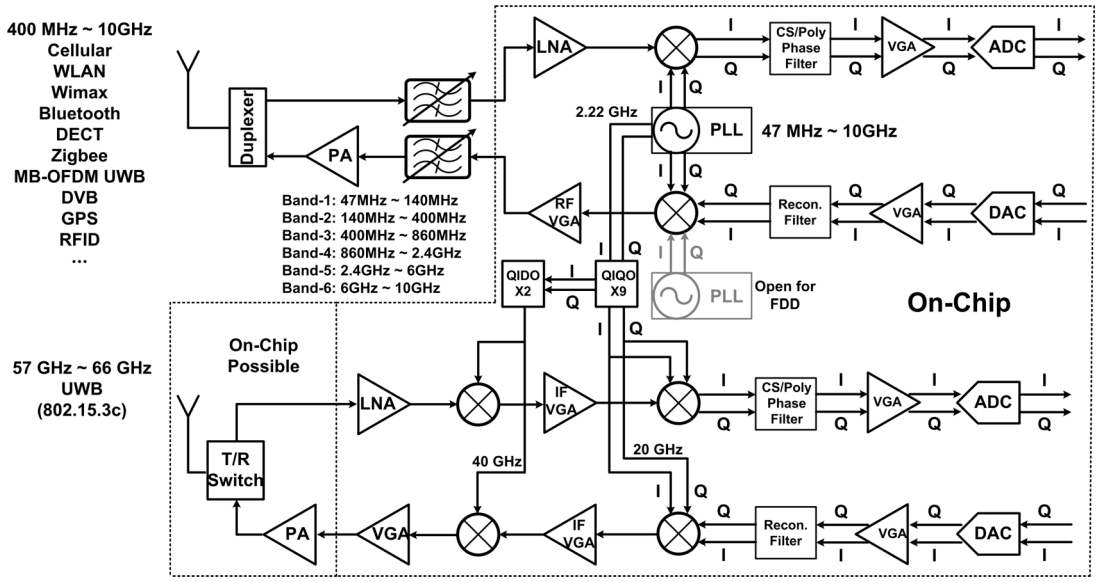


Fig. 2.6 Proposed SDR transceiver architecture

The off-chip components in front of the direct-conversion transceiver, including the RF filter, the PA and the antenna, are selected to operate in 6 bands from band-1 to band-6 instead of a wide band from 47MHz to 10GHz, for the following reasons:

1. The external building blocks, including the tunable filter, the PA and the antenna, can hardly cover the wide bandwidth from 47MHz to 10GHz, which is more than 2 decades. It is more practical to divide the whole frequency range into several sub-bands.
2. Sub-band filtering is required to provide isolations between different categories of standards. Without the sub-band filtering, when the SDR receiver operates at a low-power, short-distance standard mode, such as the Zigbee or Bluetooth mode, the strong interference from the cellular bands can interrupt and saturate the receiver. To deal with the interference, the SDR receiver needs to provide a high dynamic range at the expense of greater power consumption even for the short distance standards. This would make the SDR less competitive compared to a radio dedicated for a single standard.

3. Sub-band filtering is required for the transmitter part to filter out the harmonic tones generated by the up-conversion mixer, and also required for the receiver part to prevent the interference tones at harmonic frequencies of the desired signal being down-converted to the baseband, due to the harmonic-mixing of the receiver mixer.

The Micro-Electro-Mechanical Systems (MEMS) technology can be made use of to select and switch the off-chip components. While the CMOS technology is the most suitable choice for implementing the SDR chip. It can enable the highest integration level for channel selection and signal processing at the lowest cost.

Because the carrier frequency varies from 47MHz to 66GHz, over 3 decades, the channel bandwidth varies from KHz to GHz, and distinguished communication schemes need to be accommodated to support various standards. Most of the building blocks in the SDR system are very challenging. Without numerous novel techniques and extensive efforts, the dream of the SDR can never become a reality.

The following parts of the dissertation address one of the most critical problems – the wide-band carrier generation for SDRs. The organization is as follows. Chapter 3 describes the general issues and specifications of the target FGS. Chapter 4 describes the theory of transformer-based dual-band oscillators and the detailed design aspects of the dual-band Q-VCO for the SDR FGS. Chapter 5 discusses about wide-band frequency dividers including the static dividers used in the FGS, and LC-based high frequency dividers with proposed locking range optimization techniques. The technical details of a novel frequency synthesis scheme for 14-band OFDM UWB are provided in Chapter 6. Chapter 7 describes the issues of the MM-Wave frequency generation, proposing a phase-tuning technique for high frequency oscillators, frequency multiplication circuits based on injection-locking mechanism with a novel

peak frequency calibration method to enhance the circuit performance. Chapter 8 discusses the reconfigurable phase-locked loop for the SDR FGS. The experimental results of the FGS are shown in Chapter 9. Finally, Chapter 10 summarizes the research work and the contributions of the dissertation.

Chapter 3

General View of Wide-Band Frequency Synthesis for SDRs

3.1 Target SDR Frequency Generation System

Fig. 3.1 shows the functional diagram of the target SDR frequency generation system, which fully supports the wide-band carrier signals required by the SDR transceiver shown in Fig. 2.6. It contains 3 parts. The first part includes a dual-band quadrature voltage-controlled-oscillator (Q-VCO) incorporated with frequency dividers to generate the carrier frequency from 47MHz to 6GHz for most of the wireless standards. A phase-locked-loop is applied for the VCO to stabilize the output frequency. The second part is the open loop carrier generator to support the 14-Band MB-OFDM UWB. And the third part is the MM-Wave frequency extension circuits generating the carriers for the dual-conversion transceiver in Fig. 2.6.

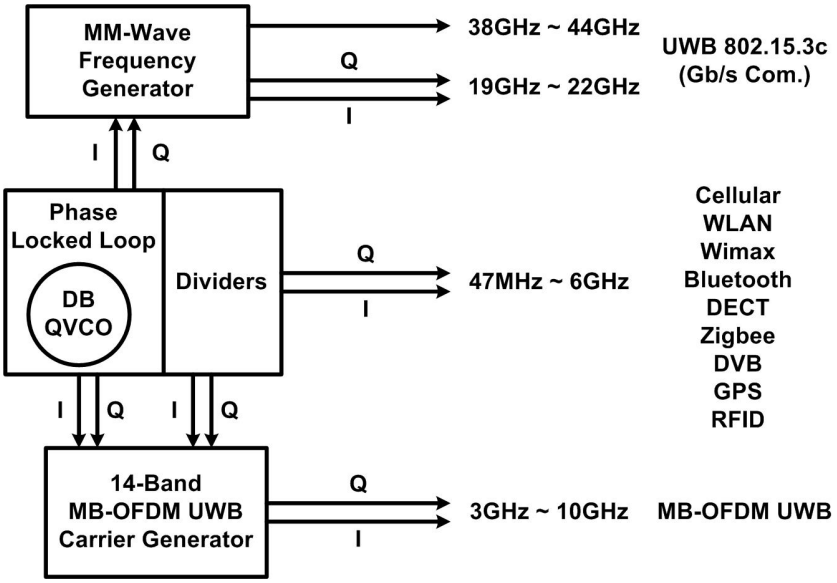


Fig. 3.1 Functional diagram of the target SDR FGS

3.2 General Requirements

The frequency generation system (FGS) is the “heart” of the whole SDR system. It needs to provide high quality local oscillation (LO) signals to the SDR transceiver. The performance of the LO frequency generation system will directly affect the performance of the whole transceiver, and the specifications of the SDR FGS can also be derived from the requirements of the SDR transceiver. In general, the following issues need to be considered in the design of a LO frequency synthesizer (FS).

3.2.1 Frequency Requirement

The frequency synthesizer needs to generate accurate carrier frequency that can be well controlled within a specified range for a given standard. The frequency accuracy required for most communication systems is extremely demanding. For example, the GSM standard requires the transmitting signals to have a frequency accuracy that is better than 0.1 parts per million (PPM). This number is even smaller than the typical value achieved by an off-chip crystal oscillator (tens of PPM). To satisfy the requirement, the cellular phone needs to perform the baseband calibration based on the frequency control burst sent out by the base station, which has a more accurate frequency reference. Besides accuracy, the carrier frequency also needs a given resolution, which is the value of the frequency tuning step, determined by the channel spacing of a certain standard. Another frequency requirement is the tuning range, which is well defined by each wireless standard as the allocated spectrum for transmitting and receiving. For the target SDR application, the FGS needs to provide the LO frequencies tunable from 47MHz to 10.296GHz for the direct-conversion transceiver, and from 19GHz to 22GHz, 38GHz to 44GHz for the dual-conversion transceiver.

3.2.2 Spectrum Purity

Practical oscillators are not able to provide pure sinusoid LO signals due to the device noise and external interference. Therefore, it is important to consider and evaluate the impact of non-ideal carrier signals on communication systems. There are two main sources that degrade the spectrum purity of the LO signals.

3.2.2.1 Phase Noise

Noise would modulate the oscillation signals in both phase and amplitude, resulting in phase noise and amplitude noise, respectively. In the steady state, the phase modulation can circulate along the positive feedback loop of an oscillator, which shapes the phase noise in $1/\omega_{offset}^2$ relationship with the offset frequency [10], and the phase noise is significant at low offset frequencies and rolls off at higher offset frequencies. Comparatively, the amplitude-limiting mechanism of any electrical oscillator prevents the amplitude modulation from propagating regenerative around the feedback loop. Consequently, the amplitude noise is not shaped and contributes negligibly to the output spectrum of the oscillator at frequencies close to the carrier. Nevertheless, at very large offset frequencies, when the noise amplitude modulation is so fast that the amplitude-limiting feedback loop cannot calibrate the amplitude in time, the amplitude noise could become dominant. In general, amplitude noise is not considered in the design of an electrical oscillator, because only the spectrum around the carrier frequency is of interest.

Fig. 3.2 illustrates the phase noise influence on the transmitting signals. In the transmitter, when the IF signal is up-converted to the desired RF channel, due to the existence of phase noise, the transmitting signal is spread out and emits to the

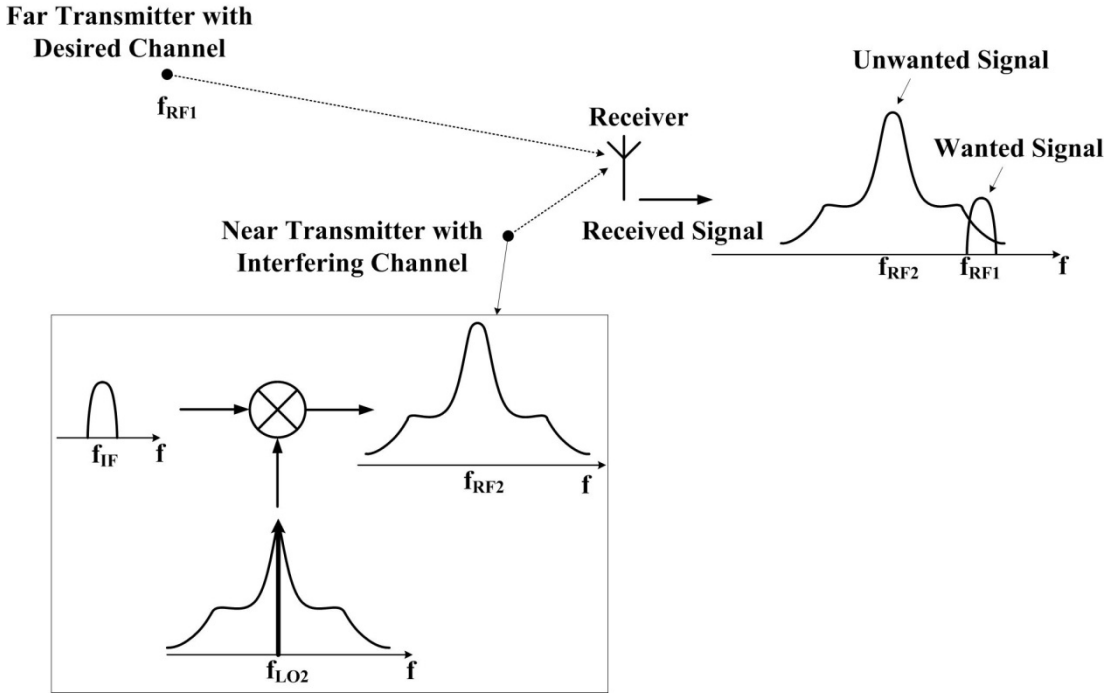


Fig. 3.2 Phase noise influence on the near-far transmitters

neighboring channels. In the scenario described in the plot, the transmitter with the desired channel is far away from the receiver, while another transmitter operating at the neighboring channel is much closer. Consequently, at the receiver, the wanted signal would be seriously compromised by the emission from the neighboring channel.

In order to guarantee proper communications, maximum allowable emission should be clearly specified for each wireless standard. For example, Fig. 3.3 gives the unwanted RF power emission requirement of the digital enhanced cordless telecommunications (DECT) standard [11][12]. Considering the worst case when the transmission signal power is maximal as 24dBm, the phase noise specification at different offset frequencies can be quickly calculated as below

$$PN_{max}(f_{offset}) = P_{emisson}(f_{offset}) - P_{max} - dB(Integration\ BW) \quad (3.1)$$

Here, an assumption is made that the phase noise over the channel bandwidth can be approximated as flat with a uniform phase noise value equal to the one at the center frequency. Numerically, the phase noise at offset frequency 1.728MHz can be easily

calculated as -8dBm-24dBm-10*log(1e6), which is equal to 92 with the unit of dBc/Hz.

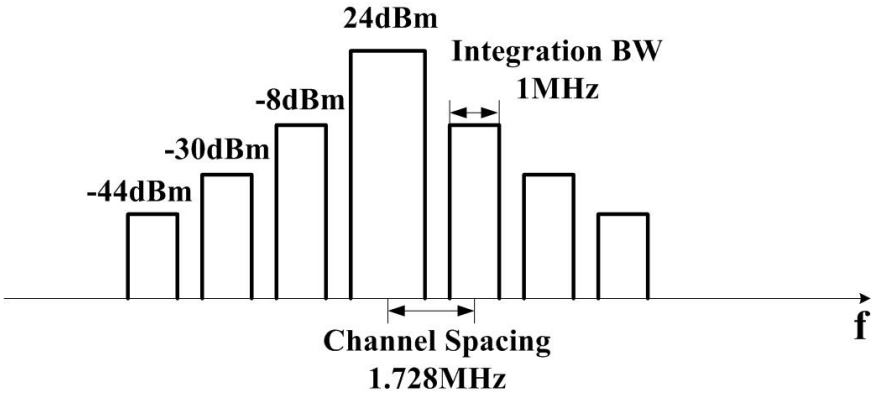


Fig. 3.3 Transmitter emission requirement of DECT standard

Fig. 3.4 illustrates the phase noise influence on the receiver part. Both of the wanted signal and the blocker would be mixed with the LO signal and down-converted to the IF frequency, with the consequence that the wanted signal is corrupted by the phase noise tail of the interferer.

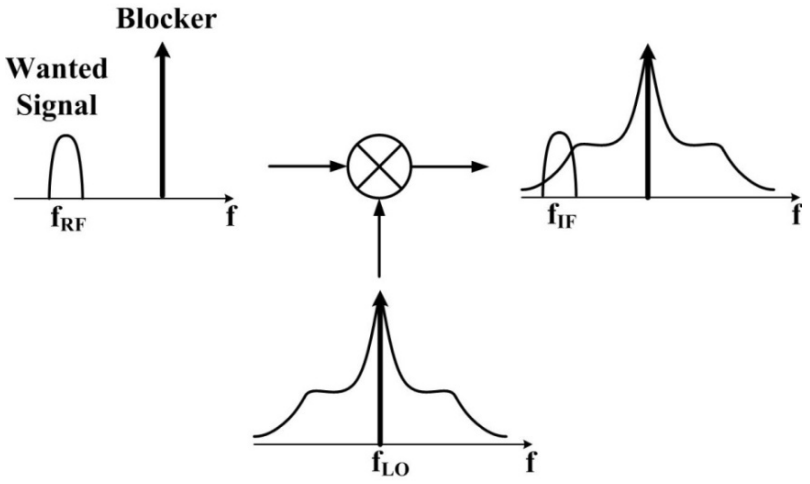


Fig. 3.4 Reciprocal Mixing [13]

Fully taking into account the near-far problem as described in Fig. 3.2, a standard committee specifies the worst blocker scenario for a receiver to ensure it is able to receive the signal properly. For instance, the blocking signal level for the standard GSM 900 is shown in Fig. 3.5 [14][15]. Based on the blocker specification, the

required phase noise can be calculated as

$$PN_{max}(f_{offset}) = P_{min} - P_{blocker}(f_{offset}) - dB(Channel\ BW) - SNR_{min} \quad (3.2)$$

Using the minimum required signal-to-noise ratio SNR_{min} of 9dB for the baseband processing and the channel bandwidth of 200KHz, the phase noise at different offset frequencies can be obtained, as -118dBc/Hz at 600KHz, -128dBc/Hz at 1.6MHz and -138dBc/Hz at 3MHz offset. Notice that the phase noise roll off is 20dB/decade, the most difficult phase noise requirement is the last one, which needs to be as low as -138dBc/Hz at 3MHz offset. Moreover, besides the LO phase noise, other building blocks in the receiver, such as the LNA, the mixer, and so on, also contribute noise and degrade the SNR. As a result, a certain margin needs to be left for the phase noise requirement. A typical realistic value would be -139.5dBc/Hz at 3MHz offset [14].

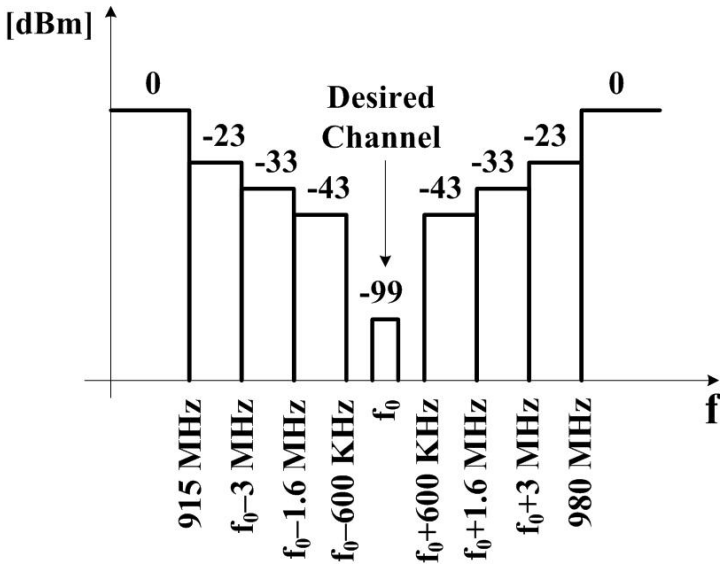


Fig. 3.5 GSM blocking signal environment

3.2.2.2 Spur

Due to the usage of the phase lock loop (PLL), a reference spur would typically appear at the frequency synthesizer's output due to the clock feed-through and mismatch of the charge pump (CP) current. If a fractional-N FS is used for fine

resolution, fractional spur would also appear at the output of the FS. The requirement for the spur rejection is similar to that for the phase noise, which is determined by the transmitter mask and the receiver blocker requirement. The difference is that the phase noise smears the transmitting or blocker signals over the signal bandwidth, while spur does not. With the same power, the influence of spur and that of phase noise would be roughly the same. As a result, the spur specification can be conveniently obtained by converting the spectrum density of phase noise into power, through integrating the channel bandwidth, that is

$$Spur_{max}(f_{offset}) = PN_{max}(f_{offset}) + dB(Channel\ BW) \tag{3.3}$$

As the SDR is wide-band in nature, the transceiver would face channels from multiple standards instead of a single standard. The spur far away from the carrier frequency is also critical, which could down-convert the interference from other standard's channel to baseband or up-convert the baseband signal to other standard's channel.

3.2.3 Channel Switching

In communications, the modulated signals need to be dynamically allocated (or acquired) to (or from) different assigned channels by the transceiver. Consequently, the LO generator should be able to switch the carrier frequency from one channel to the other within a specific time period, also known as the switching time. For most of the wireless standards, the required switching time is in the order of hundreds micro-seconds. This number allows the channel switching to be performed by adjusting the division ratio of the multi-modulus divider in the PLL, as long as the loop bandwidth is sufficiently large (in the order of hundreds KHz). One exception is the multi-band OFDM ultra-wide-band (UWB) standard [16], which uses fast

channel hopping to fully utilize the spectrum and enable low spectrum power density, high data-rate communication compatible with other standards. The required channel hopping time is less than 9.47nS, to accommodate this requirement, the bandwidth of the PLL needs to be more than 1GHz, which is impractical to implement. As a result, extra circuits, such as dividers and mixers, are needed to enable rapid channel switching in an open loop manner. Consequently, the design complexity would be increased. Moreover, in order to support the spectrum scanning for the future cognitive radio, it is also desirable for the SDR FGS to support faster channel switching than the typical standard requirement.

3.2.4 IQ Generation

In-phase and quadrature-phase (IQ) LO signals are the prerequisites for IQ modulation and sideband rejection in modern transceivers. There are a range of methods available to generate the IQ signals.

1. Active all-pass filter: It is able to provide 90 degree phase shift with a broadband unity gain response. However, the operation frequency is limited by the operational amplifier, which limits its application at the frequency of several GHz.
2. Passive poly-phase filter: It is narrow band characteristic in nature, although by increasing the order through cascading, a wideband frequency response is possible, the induced power loss would be too high for the SDR application, and the component mismatch is an important source for the IQ imbalance.
3. Quadrature oscillator: By coupling two VCOs in a ring architecture, IQ output signals can be generated over the tuning range of the Q-VCO. In this method, the trade-off between the phase noise and the IQ accuracy needs to be considered. And in the direct conversion transceiver, since the oscillation frequency of the Q-VCO and the RF signal frequency is close by, the LO pulling or pushing issue

also needs to be taken care of.

4. Frequency dividing technique, frequency divider divides the frequency of the input signal and also the phase of the signal, thereby, IQ phase signals can be obtained by applying differential signals to a divide-by-2 divider. Compared to the Q-VCO, this method separates the procedures of oscillation signal generation and IQ signal generation, thus the design complexity of the VCO is relaxed. The phase noise at the divider's output mainly depends on the one of the input signal, and the output IQ phase error depends on the differential accuracy of the input signal. This technique also has its drawbacks. The VCO needs to operate at a frequency that is double than that for the Q-VCO. And the high frequency wideband frequency divider is difficult to implement when the desired carrier frequency is very high.

3.3 Specifications of SDR Frequency Generation System

3.3.2 Specifications

The detailed specifications of the SDR FGS are summarized in Table 3.1. The phase noise specifications are derived from different standards with some margins referred to the industrial experienced data for more practical communications. The specified values with their outstanding requirements compared to others are highlighted in the table, which are the design challenges of the desired SDR frequency generation system and which will be the focus of this dissertation.

Table 3.1 Specifications of the SDR frequency generation system

Standards		Frequency (min–max)	Channel BW	Resolution Requirement	Phase noise Requirement (dBc/Hz)	Settling time (μs)
EGSM	850-900	824-960MHz	200KHz	**200KHz**	**-139.5@3MHz**	870 228 for HSCSD 310 for GPRS
	DCS	1.71-1.88GHz				
	PCS	1.85-1.99GHz				
UMTS	FDD	1.92-2.17GHz	5MHz	200KHz	-120@3MHz	200
	TDD	1.9-2.025GHz			-145@20MHz	
WLAN 802.11	a	5. 15-5.85GHz	20MHz 10-40MHz	1MHz/5MHz	-102@1MHz	224
	b/g	2.4-2.484GHz				
	n	2.4GHz, 5GHz				
WIMAX 802.16	802.16-2004 TDD/ FDD	2.0-6.0GHz	1.25MHz - 28MHz	1.25MHz/ 1.75MHz/ 5MHz/ **125KHz** (Last two Profiles)	-102@1MHz	**50**
	802.16e-2005					
Bluetooth	802.15.1	2.4-2.479GHz	1MHz	1MHz	-89@500KHz	**62.5**
DECT		1.88-1.9GHz (EU) 1.92-1.93GHz (US)	1.728MHz	**1.728MHz**	-131@4.7MHz	416.67
Zigbee	802.15.4	868-868.6MHz 902-928 MHz 2.4-2.4835GHz	600K/ 1200K/ 2MHz	100KHz	-110@10MHz	192

UWB	802.15.3a MB-OFDM	3.1-10.6GHz	528MHz	528MHz	-100@1MHz	**9.47e-3**
	802.15.3c	**58.32–64.8GHz**	2.16GHz	2.16GHz	-88 @1MHz	100
Broad-casting	DVB-T/H	47-68MHz 174-239MHz 470-598MHz 598-862MHz	6/7/8MHz	1MHz	-87@10KHz -115@1MHz	100
Position	GPS	1.57542GHz	1.023-10.23 MHz	**1.023MHz**	-105@1MHz	200
RFID	UHF	860-960MHz	80K-1MHz	**100KHz**	**-144@3.6MHz**	1000

3.3.3 Challenges

From Table 3.1, it can be seen that the realization of the targeted frequency generation system is quite challenging in the following aspects.

1. Ultra wide frequency range: The required LO frequency varies from 47MHz to 44GHz, for nearly 3 decades. Obviously a single frequency synthesizer is not able to cover this range. A number of extending circuits outside the PLL are required, which makes the FS more like a system.
2. Stringent phase noise requirement: Due to requirement of the cellular standards and the RFID application, the phase noise as low as -139.5dBc/Hz at 3MHz offset for a 2GHz around carrier frequency is required, which is very tough even for a dedicated voltage-controlled oscillator (VCO). And considering the wide tuning range the VCO needs to cover, the phase noise requirement is even more demanding.

3. MM-Wave frequency generation: To support the standard 802.15.3c, wideband carrier frequency at the MM-Wave frequency band is required for synthesis. This is very challenging considering the available process is 0.13μm CMOS, whose f_t is around 110GHz and f_{max} is around 90GHz (275uA/μm, V_G/V_D=0.8V/1.2V). This drives novel MM-Wave circuit techniques to synthesize the required MM-Wave signals with sufficient quality under the process limits, which will be described in chapter 5 and 7. Although simply using more advanced CMOS processes may also relax the design issue for the SDR FGS, these techniques can always lead to superior performance with any given process.
4. Fine resolution: In order to cover all the standards, the resolution of 25-KHz is required. And the resolution requirement of the GPS and the DECT standard are the special number of 1.023MHz and 1.728MHz. Very fine resolutions are desired if a single reference frequency is used. Otherwise, extra crystal oscillators may be required for the FGS.
5. Fast settling: The MB-OFDM UWB standard requires around 9nS settling time. Extra open loop circuits are required to quickly generate all 14-band carrier frequencies for the standard. Consequently, the complexity of the FGS is increased. For other standards, the lowest settling time is required by the Bluetooth and Wimax, at the level of 62.5uS and 50uS.
6. Besides, the FGS needs to provide wide band IQ signals with a high spur rejection ratio. As a result, when designing open loop circuits for frequency extensions, the induced spurious tones need to be minimized.

3.4 Wide-band Frequency Generation Schemes

The stringent phase noise requirement confining the local oscillator has to be the LC-type. The high Q quality factor of the LC-tank helps reduce the phase noise but at the expense of narrow tuning range, in typical less than 30%. The following part will discuss the methods and the corresponding trade-offs to extend the tuning range of the LC-based VCO.

3.4.1 Multiple VCOs

A simple way to get a larger tuning range is using multiple VCOs [17], [18]. By doing so, the performance of the tailor-made VCOs can be optimized. However, it requires multiple inductive coils for multiple VCOs. To minimize the phase noise, the inductor coil used in the LC-VCO typically occupies a large chip area in order to maximize the quality factor (Q). Consequently, the VCO usually dominates the chip area in the whole FS, especially in advanced CMOS processes. As a result, the solution of multiple VCOs would inevitably increase the chip area of the FS, thus increasing the cost considerably.

3.4.2 Single VCO with Divide-By-2 Dividers

Frequency dividers can help generate lower frequency signals than the VCO's output. Current mode logic (CML) divide-by-2 dividers can operate well above 10GHz with a large locking range without using inductors, with the standard 0.13μm CMOS process. Thus, it is an economical and robust solution to use divide-by-2 dividers to extend the VCO's tuning range. To obtain the continuous frequency band from 47MHz to 6GHz, the single VCO's self-tuning range has to be as wide as 66.7%, which is impractical considering the low phase noise requirement.

3.4.3 Single VCO with Divide-By-2 Dividers Plus Mixers

Mixers are able to perform frequency summing and subtraction. The required tuning range of the VCO can be reduced by employing mixers. However, mixing would cause the image and the spurious emission problems. To overcome them, LC filters are required [19]. As a result, this solution also requires extra inductive components and cost will be increased.

3.4.4 Dividers Beyond Divider-By-2

There are also divider circuits beyond divider-by-2, which have the integer division number larger than 2 [20] as well as a fractional division number [21]. These dividers can help reduce the tuning range requirement of the VCO.

Basically, any frequency divider can be considered as one or more mixers with certain feedback. Taking the divider-by-2 for instance, the output signal at frequency f is fed back to mix with the input signal at 2f. At the mixer's output, the signal at f is generated again to form a regenerative loop. Due to the mixing, at a divider's output there also exist other frequency components including the image tones and the harmonic mixing tones. For the integer-N divider, all the parasitic tones locate at the harmonics of the divider's output frequency. As a result, integer-N divider doesn't have non-harmonic spurs. Nevertheless, for division ratio larger than 2, the operation of the divider actually depends on the harmonic mixing of the mixer, which is the high-order effect. Consequently, the larger the division ratio, the smaller the divider's locking range. Taking the process, voltage supply and temperature (PVT) variations into account, the narrow locking range of high division ratio divider [20] limits its applications for SDR. For fractional dividers, the mixing operation can generate rich non-harmonic spurs at the divider's output. A complex calibration algorithm is required to reduce the spurs to an acceptable level, which takes noticeable chip area and power consumption [21].

3.4.5 Multi-Band or Wide-Band VCO

Recently, novel multi-band and wide-band VCOs are implemented for multi-standard applications. By properly dealing with inductors or transformers, these VCOs can achieve multi-mode operations without increasing the number of inductive coils. Although the design of such VCOs becomes more complicated and challenging, it can be a promising solution for SDRs.

Chapter 4

Transformer-Based Dual-Band Oscillator for SDRs

4.1 Introduction

SDR systems require a local oscillator capable of ultra-wide frequency tuning range (TR) while still maintaining a high enough spectrum purity to support diverse specifications. The achievable TR of the commonly-used capacitive-tuning method is traded-off and limited by the capacitive Q, which becomes seriously degraded at high frequencies, and also by the power budget as a large power is required when the resonator is heavily loaded by the tuning capacitors. To alleviate the issues to extend the tuning range, switching inductors or coupled inductors are used to realize dual-band or wide-band VCOs [22]-[26]. However, the size of the switches needs to be very large to prevent the inductor's Q from degrading significantly by their turn-on resistance. Consequently, the switches contribute to large parasitic capacitance, which results in a reduced tuning range and higher power consumption. Multiple frequency bands can also be generated by employing mixers [19][27], but a narrow-band LC filtering is required to overcome the sideband-rejection problem and the spurious emission caused by the mixing. As an alternative to circumvent the spur issues, multiple VCOs are used in [17][18], but these solutions are quite inefficient in terms of chip area and cost.

Recently, multiple frequency peaks of the transformer or multi-tapped inductor based high-order LC tanks are exploited to realize multi-band or wideband VCOs [28]-[33]. [28] and [29] introduce the transformer-based one-port and two-port

oscillators, and demonstrate a dual-mode differential VCO, with employing a small turn ratio and moderately coupled transformer and using one-port oscillator configuration as the lower band mode and two-port oscillator configuration as the higher band mode to cover a wide tuning range from 3.4GHz to 7GHz. In [30], instead of using transformer, multi-tapped inductors are used to build a fourth-order tank, and based on one-port oscillations, a 0.8GHz/1.8GHz dual-band VCO is demonstrated with low enough phase noise applicable for GSM/DCS/PCS standards. Using large turn ratio and tightly coupled transformers, and making use of transformer coupling, [31] demonstrates a 4GHz/10GHz dual-band Q-VCO and shows that one-port oscillators can be stabilized with a proposed notch-peak cancellation technique. With a single multi-tapped inductor and based on two-port oscillations, [32] demonstrates a 3.5GHz/10GHz dual-band differential VCO for area-efficient wideband applications. Employing a three-coil loosely coupled transformer and based on one-port oscillations, [33] exhibits a triple-mode wideband VCO tunable from 1.28GHz to 6.06GHz. As demonstrated in these works, because the inductive components of the high-order LC tank can be integrated as transformer or multi-tapped inductor, the chip area penalty is not much compared to the commonly used second-order LC tank based VCO, and because there is no extra physical resistive loss introduced into the tank in contrast with the switching inductor based VCO, the high-order LC tank based VCO shows its great potential for the wideband or multi-band applications. However, compared to the conventional LC-VCO design, as the order of the resonator increases, the design complexity of the oscillator is also increased, and more design parameters (such as the inductor ratio, the capacitor ratio, and the coupling between the inductors) need to be considered and optimized simultaneously. Moreover, with multiple-port resonant tanks, different oscillator configurations, like one-port and two-port oscillators for a

fourth-order LC-tank, become available and need to be properly selected. As a result, evaluations and comparisons on different circuit topologies and design parameters need to be done to achieve an optimal design for a specific application.

This chapter addresses the detailed design issues of the transformer-based dual-band VCOs, systematically analyzes and compares the properties of transformer-based one-port and two-port oscillators, including the oscillation frequency, the power consumption, the tank Q and the phase noise. It is discovered that, comparatively, one-port oscillator has lower power consumption but needs to be stabilized if the oscillation at the higher peak frequency is desired, while two-port oscillator has no stability issue and has superior phase noise performance at given amount of tank swing, but is less efficient to convert the bias current to tank swing. Incorporating both one-port and two-port configurations and exploiting their respective advantages, a transformer-based dual-band Q-VCO is designed and optimized for the SDR application, which targets to support all the existing wireless standards from DC to 10GHz including the 14-Band OFDM UWB.

4.2 Transformer-Based One-Port Dual-Band Oscillator

Analytical results with the closed form expressions of the oscillation frequencies and the start-up conditions of transformer-based one-port and two-port oscillators can be found in the previous work assuming all capacitors are lossless [29]. To provide a more complete view and facilitate performance evaluations for real applications, in this work, the tank Qs and the phase noise of the two types of oscillators are further investigated and analyzed with the closed form expressions. And the performances of the one-port and two-port oscillators are compared in a systematical way to offer more

design aspects for choosing the circuit topologies. In addition, the effect of the capacitive loss is considered as well, which becomes critical for oscillators operating at high frequencies or with ultra-wide tuning range (TR).

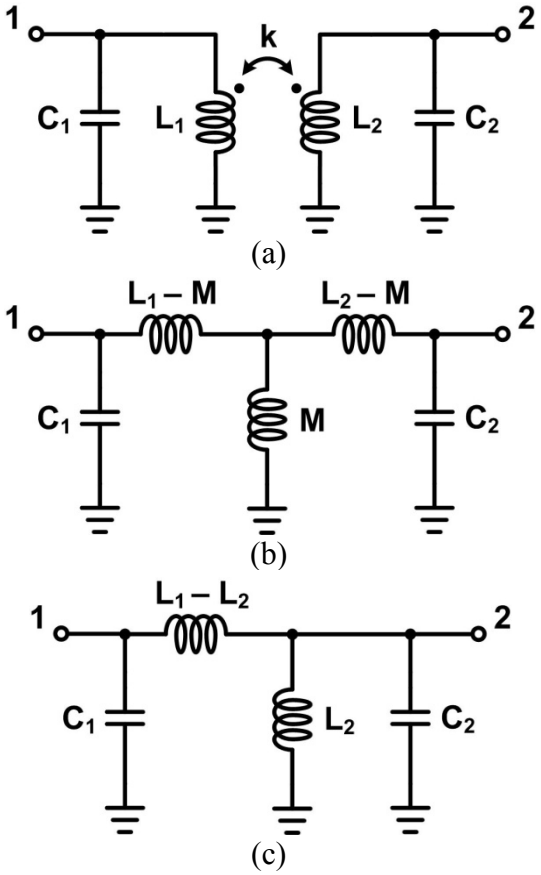


Fig. 4.1 Transformer-based LC tank: (a) original network, (b) equivalent network with T-section ac model, (c) simplified ac network in a special case when M is equal to L_2

It is worthwhile to notice that the multi-tapped inductor based fourth order LC tank can be considered as a special case of the equivalent ac model of the transformer-based LC tank. Fig. 4.1(a) shows the simplified transformed based fourth-order LC tank, with lossless components. By replacing the transformer with the equivalent T-section ac model, the network is redrawn as Fig. 4.1(b), where M is the mutual inductance, equal to $k\sqrt{L_1 L_2}$. Considering a special case when M is equal to L_2 ($k=\sqrt{L_2/L_1}$), the network can be further simplified to the one in Fig. 4.1(c), which is

exactly the fourth-order LC tank based on a tapped inductor, with ignoring the coupling between the inductors. This network is used by many designs [30][32][34], and shows very similar properties to that of the transformer-based LC tank. Nevertheless, it should be noticed that, compared to the transformer, the two inductors of the network in Fig. 4.1(c) have the same dc voltage, consequently, for the associated two-port oscillator configuration, extra ac coupling circuit is required to properly biasing the transistors, which would cause extra loss and noise.

Thereby, most of the conclusions drawn from the transformer-based oscillators are also applicable for multi-tapped inductor based ones.

4.2.1 Oscillation Frequency

Fig. 4.2(a) shows the general model of the one-port dual-band oscillator. Resistive components are added in series with the inductors and capacitors to account for the loss of the network, which can typically be compensated for oscillation by employing a negative transconductance cell at either Port 1 or Port 2. The component Qs are defined as $Q_{L1}=\omega L_1/R_{L1}$, $Q_{C1}=1/\omega C_1 R_{C1}$, $Q_{L2}=\omega L_2/R_{L2}$, and $Q_{C2}=1/\omega C_2 R_{C2}$.

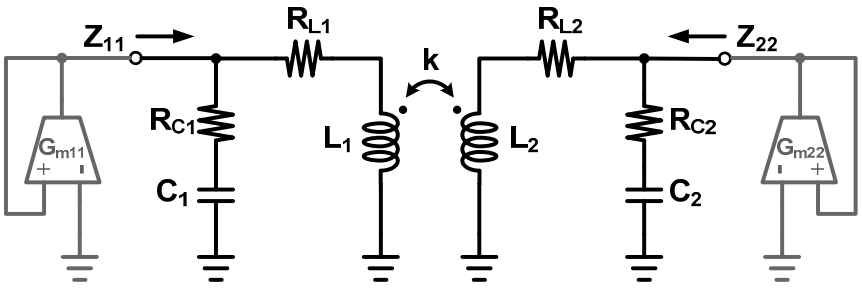
To facilitate the calculation of the tank impedance, the transformer is replaced by an equivalent network as shown in Fig. 4.2(b), and the impedance Z_{L1} can be derived as:

$$Z_{L1} = \Delta R_{L1} + j\omega L_1{}' \tag{4.1a}$$

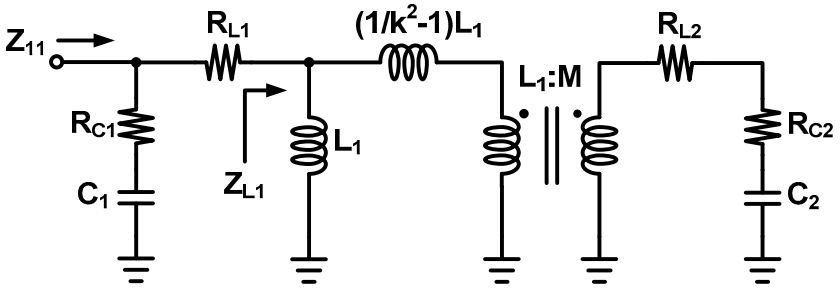
$$\Delta R_{L1} = \frac{\frac{L_1}{k^2 L_2}(R_{L2}+R_{c2})(\omega L_1)^2}{\left[\frac{L_1}{k^2 L_2}(R_{L2}+R_{c2})\right]^2 + \left(\frac{\omega L_1}{k^2}\right)^2\left[1-\left(\frac{\omega_2}{\omega}\right)^2\right]^2} \tag{4.1b}$$

$$L_1{}' = \frac{\left[\frac{L_1}{k^2 L_2}(R_{L2}+R_{c2})\right]^2 + \left(\frac{\omega L_1}{k^2}\right)^2\left[1-\left(\frac{\omega_2}{\omega}\right)^2\right]\left[1-k^2-\left(\frac{\omega_2}{\omega}\right)^2\right]}{\left[\frac{L_1}{k^2 L_2}(R_{L2}+R_{c2})\right]^2 + \left(\frac{\omega L_1}{k^2}\right)^2\left[1-\left(\frac{\omega_2}{\omega}\right)^2\right]^2} L_1 \tag{4.1c}$$

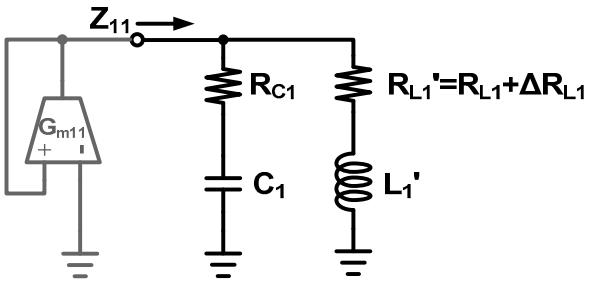
where Z_{L1} contains an equivalent inductor L_1' in series with a resistor ΔR_{L1}, and the angle frequencies $\omega_{1,2}$ are given by $\omega_1 = 1/\sqrt{L_1 C_1}$, $\omega_2 = 1/\sqrt{L_2 C_2}$. Without loss of generality, let's define $L_1 = mL_2 = mL$, $C_1 = nC_2 = nC$, and assume in all the following discussions that $k > 0$ and $mn > 1$ so that $\omega_1 < \omega_2$.



(a)



(b)



(c)

Fig. 4.2 One-port oscillator: (a) general model, (b) equivalent network for Z_{11} calculation, (c) simplified network for Z_{11} calculation

Finally, Z_{11} can be considered as a simplified LC tank as shown in Fig. 4.2(c). The frequency response of Z_{11} can be quickly estimated by assuming a low-loss case (R_{L1},

R_{L2}, R_{C1}, R_{C2} →0), in which case Z_{11} can be derived as:

$$Z_{11} \approx (1/sC_1)||(sL_1{}') = \frac{j\omega_1{}^2 L_1 \omega[(1-k^2)\omega^2-\omega_2{}^2]}{(k^2-1)\omega^4+(\omega_1{}^2+\omega_2{}^2)\omega^2-\omega_1{}^2\omega_2{}^2} \quad (4.2a)$$

Because of the symmetry of the network in Fig. 4.2(a), Z_{22} can be directly rewritten from Z_{11} as:

$$Z_{22} \approx \frac{j\omega_2{}^2 L_2 \omega[(1-k^2)\omega^2-\omega_1{}^2]}{(k^2-1)\omega^4+(\omega_1{}^2+\omega_2{}^2)\omega^2-\omega_1{}^2\omega_2{}^2} \quad (4.2b)$$

From Eqs. (4.2a) and (4.2b), it can be seen that Z_{11} and Z_{22} have exactly the same two peak frequencies located at

$$\omega_{H/L}{}^2 = \frac{\omega_1{}^2+\omega_2{}^2 \pm \sqrt{(\omega_1{}^2-\omega_2{}^2)^2+4k^2\omega_1{}^2\omega_2{}^2}}{2(1-k^2)} \quad (4.3)$$

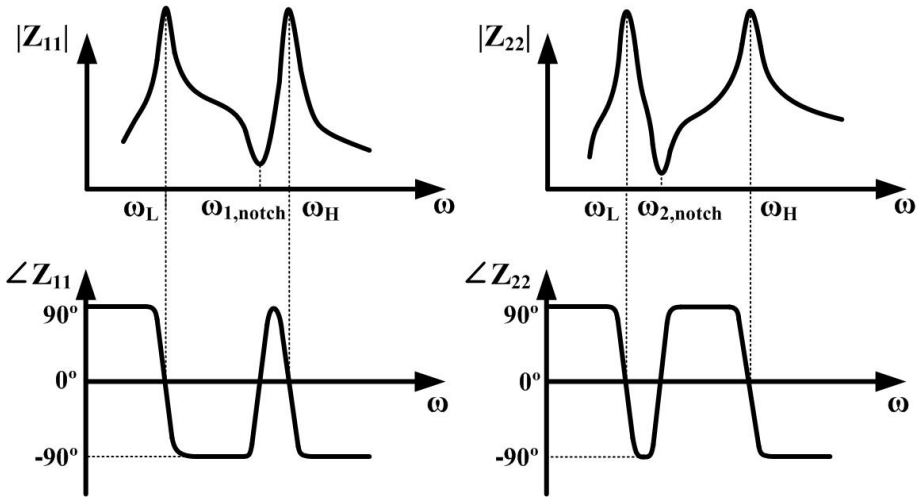
Besides the zero frequency, there is only one notch frequency $\omega_{1,\text{notch}}$ in Z_{11}, and similarly, there exists only one notch frequency $\omega_{2,\text{notch}}$ in Z_{22}, which are given by

$$\omega_{1,notch} = \frac{\omega_2}{\sqrt{1-k^2}} \quad (4.4a)$$

$$\omega_{2,notch} = \frac{\omega_1}{\sqrt{1-k^2}} \quad (4.4b)$$

4.2.2 Start-Up Condition

Fig. 4.3(a) and Fig. 4.3(b) plot the magnitude and phase responses of Z_{11} and Z_{22} with high-Q components. The phase shift begins from 90° at low frequency and crosses 0° at the first peak frequency ω_L. And the phase returns to 90° after the notch frequency either $\omega_{1,\text{notch}}$ in Z_{11} or $\omega_{2,\text{notch}}$ in Z_{22}, and crosses 0° again at the second peak frequency ω_H.



(a) (b)

Fig. 4.3 Frequency response of the fourth-order LC tank: (a) Z_{11}. (b) Z_{22}

The start-up condition of the one-port oscillator shown in Fig. 4.2(a) is given by

$$G_{m11/22} > \frac{1}{real\{Z_{11/22}\}} \tag{4.5a}$$

$$imag\{z_{11/22}\} = 0. \tag{4.5b}$$

If the tank Q is high enough, from Eq. 4.5(a), the minimum G_m for oscillation can be expressed as:

$$G_{m11,min} = \frac{(R_{L1}{}' + R_{C1})C_1}{L_1{}'}. \tag{4.6}$$

Putting Eqs. (4.1b) and (4.1c) into Eq. (4.6), it can be derived that

$$G_{m11,min} = \frac{1}{A_1\omega_{osc}L_1}\left[\frac{1}{A_1}\frac{1}{Q_{L1}} + \frac{1}{Q_{C1}} + \lambda\left(\frac{1}{A_2}\frac{1}{Q_{L2}} + \frac{1}{Q_{C2}}\right)\right] \tag{4.7a}$$

where the high-order terms such as $\frac{1}{Q_{L1}Q_{C1}Q_{C2}}$ are ignored for high Qs, $A_1 = \omega_1{}^2/\omega_{osc}{}^2$, $A_2 = \omega_2{}^2/\omega_{osc}{}^2$, and $\lambda = \frac{A_2(A_1-1)}{A_1(A_2-1)}$.

Symmetrically, $G_{m22,min}$ can be easily rewritten from Eq. (4.7a) as

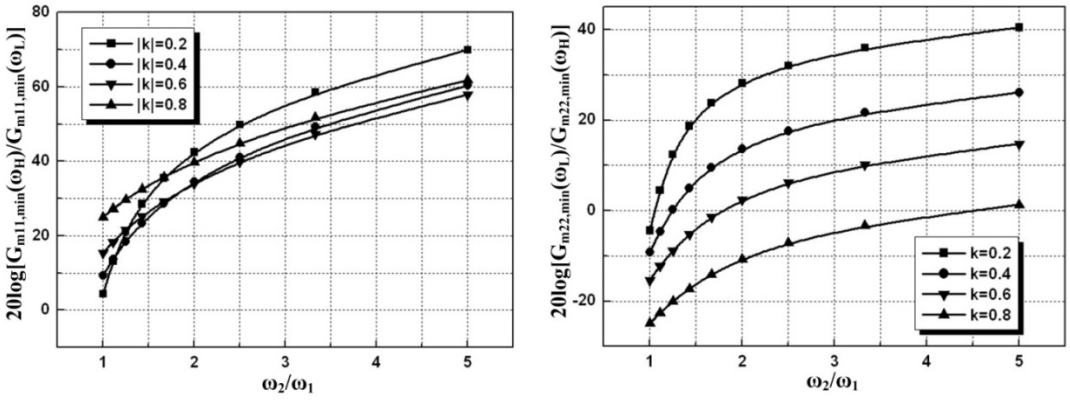
$$G_{m22,min} = \frac{1}{A_2\omega_{osc}L_2}\left[\frac{1}{A_2}\frac{1}{Q_{L2}} + \frac{1}{Q_{C2}} + \lambda^{-1}\left(\frac{1}{A_1}\frac{1}{Q_{L1}} + \frac{1}{Q_{C1}}\right)\right] \tag{4.7b}$$

For the one-port oscillator, at both the potential oscillation frequencies ω_L and ω_H, the phase shift is 0°, and thus Eq. (4.5b) is satisfied, and the necessary and sufficient conditions for start-up oscillation at ω_L or ω_H would become $G_{m11/22} > G_{m11/22,min}(\omega_L)$, or $G_{m11/22} > G_{m11/22,min}(\omega_H)$, respectively. If $G_{m11/22}$ is large enough to satisfy the two conditions, the oscillator can potentially oscillate at either frequency ω_L or ω_H [35] or concurrently oscillate at both frequencies [36][37]. The final steady state oscillations depend on the detailed configuration of the high-order LC tank and the specific form of nonlinearity of the active device [37].

In either case, to avoid the concurrent oscillation and the potential stability problem that the one-port oscillator could jump from one desired equilibrium oscillation frequency to the other (with certain disturbance like an injected interference close to the other peak frequency, or large voltage or temperature variations), it is highly desirable to control the oscillator to operate stably at only the wanted frequency. This can be achieved by introducing the notch-peak cancellation concept [31]. It is not difficult to show that as long as $|k| \to 0$ or $mn \to \infty$, the notch at $\omega_{1,notch}$ in Z_{11} is prone to cancel the higher frequency peak, and the notch at $\omega_{2,notch}$ in Z_{22} is prone to cancel the lower frequency peak. As such, in the Fig. 4.3(a) there would be only one dominant peak at ω_L in the magnitude response of Z_{11}, and with a practical tank Q, the phase shift of Z_{11} would stay around -90° and fail to cross 0° at ω_H as $\omega_{1,notch}$ is close by. Similarly, there is only one dominant peak at ω_H in the magnitude response of Z_{22}, and the phase shift of Z_{22} would stay around 90° and fail to cross 0° at ω_L with $\omega_{2,notch}$ being close by. In both cases, the start-up condition can be satisfied at only one peak frequency, and consequently, there is no stability problem.

In general, $|k| \to 0$ is undesirable in terms of the chip area as the two coils of the

transformer need to be completely decoupled from each other. It would be more desirable to make mn→∞, which is equivalent to $\omega_2 \gg \omega_1$. Consequently, when $\omega_{osc}=\omega_L$, $A_2 \gg A_1 > 1$, and when $\omega_{osc}=\omega_H$, $A_1 \ll A_2 < 1$. From Eq. (4.7a), it can be seen that $G_{m11,min}(\omega_L) \ll G_{m11,min}(\omega_H)$, which is consistent with the discussion above that there is only one dominant peak at ω_L in Z_{11}. Fig. 4.4(a) plots the transconductance ratio $G_{m11,min}(\omega_H)/G_{m11,min}(\omega_L)$ in a log scale, using the component values of $L=1nH$, $C=300fF$, $Q_{L1}=Q_{L2}=7$, $Q_{C1}=Q_{C2}=20$, $m=n=\omega_2/\omega_1$. From the plot it can be seen that with different values of ω_2/ω_1 and k, the transconductance ratio is always larger than 1, which implies that if the cross-coupled G_m cell is placed at Port 1 to compensate the loss of the tank, the VCO always prefers to oscillate at the lower peak frequency ω_L. Moreover, the larger the ratio ω_2/ω_1 is, the more stable the oscillation becomes. In Fig. 4.4(b), the ratio $G_{m22,min}(\omega_L)/G_{m22,min}(\omega_H)$ is plotted in a log scale. In order to enable stable oscillation at ω_H, the oscillator can be designed such that $G_{m22,min}(\omega_H) < G_{m22} < G_{m22,min}(\omega_L)$. In this case, the values of $\sqrt{mn}$ and k need to be properly chosen. For example when k=0.4, $\sqrt{mn}$ needs to be larger than 1.5 to provide at least 6dB margin for designing G_{m22}. On the other hand, when k=0.8, $\sqrt{mn}$ needs to be much larger than 4.5 to prevent the VCO from oscillating at ω_L. Consistent with the notch-peak cancellation concept, large mn and small |k| values are critical for the implementation of dual-band one-port oscillator.



(a) (b)

Fig. 4.4 One-port oscillator: (a) plot of the ratio $G_{m11,min}(\omega_H)$ to $G_{m11,min}(\omega_L)$ in log scale, (b) plot of the ratio $G_{m22,min}(\omega_L)$ to $G_{m22,min}(\omega_H)$ in log scale

4.2.3 Tank Quality Factors – Qs

For one-port oscillators, the tank quality factor Q_{11} at the oscillation frequency is given by

$$Q_{11} = \left|\frac{\omega_{osc}}{2}\frac{d\varphi_{11}}{d\omega}\right| = \frac{\omega_{osc}L_1'}{R_{L_1}'+R_{C1}}\left(1+\frac{\omega_{osc}}{2L_1'}\frac{dL_1'}{d\omega}|_{\omega=\omega_{osc}}\right) \tag{4.8}$$

where φ_{11} denotes the phase of Z_{11} and $\omega_{osc}=1/\sqrt{L_1' C_1}$, which is equal to ω_L or ω_H in the lossless case.

Combining with Eqs. (4.1b) and (4.1c), Eq. (4.8) can be further derived as:

$$\frac{1}{Q_{11}} = \frac{1}{(1+\lambda)A_1}\frac{1}{Q_{L1}} + \frac{1}{1+\lambda}\frac{1}{Q_{C1}} + \frac{1}{(1+\lambda^{-1})A_2}\frac{1}{Q_{L2}} + \frac{1}{1+\lambda^{-1}}\frac{1}{Q_{C2}} \tag{4.9a}$$

by ignoring the high-order terms such as $\frac{1}{Q_{L1}Q_{C1}Q_{C2}}$ for high Qs.

Because of the symmetry of the network in Fig. 4.2(a), Q_{22} can be easily modified from Eq. (4.9a) as

$$\frac{1}{Q_{22}} = \frac{1}{(1+\lambda^{-1})A_2}\frac{1}{Q_{L2}} + \frac{1}{1+\lambda^{-1}}\frac{1}{Q_{C2}} + \frac{1}{(1+\lambda)A_1}\frac{1}{Q_{L1}} + \frac{1}{1+\lambda}\frac{1}{Q_{C1}} \tag{4.9b}$$

Although the expressions of Q_{11} and Q_{22} are exactly the same, because the desired oscillation frequencies are different (A_1, A_2 and λ are functions of ω_{osc}), their values are distinguishable.

4.2.4 Phase Noise

Fig. 4.5(a) shows the schematic of the transformer-based one-port dual-band oscillator, where the negative transconductance cells are implemented with the commonly used cross-coupled differential pairs. The oscillation at either ω_L or ω_H can be selected by controlling the bias current sources. For example, at the low band mode, I_{b1} is enabled while I_{b2} is disabled, and the negative G_m made from M_1 and M_2 are added at Port 1 to compensate the loss of the tank as shown in Fig. 4.5(b), the oscillator operates at the lower peak frequency. At the high band mode as shown in Fig. 4.5(c), the negative Gm made from M_3 and M_4 are added at Port 2 to compensate the tank loss, thereby the oscillator operates at the higher peak frequency. To achieve stable dual-band operation, the LC tank needs to be controlled based on the notch-peak cancellation concept described earlier, as a result, to maximize the capacitor ratio n, in Fig. 4.5(b), C_2 is minimized when varying C_1 to tune ω_L, and in Fig. 4.5(c), C_1 is maximized when varying C_2 to tune ω_H.

Within a narrow bandwidth around ω_{osc}, the characteristic and thus the noise shaping property of a transformer-based LC tank are the same as a second-order LC tank. And with the general definition of tank Q [32][38][39], the high-order tank can be equivalently treated as a single capacitor $C_{1/2}$ in parallel with an effective inductor,

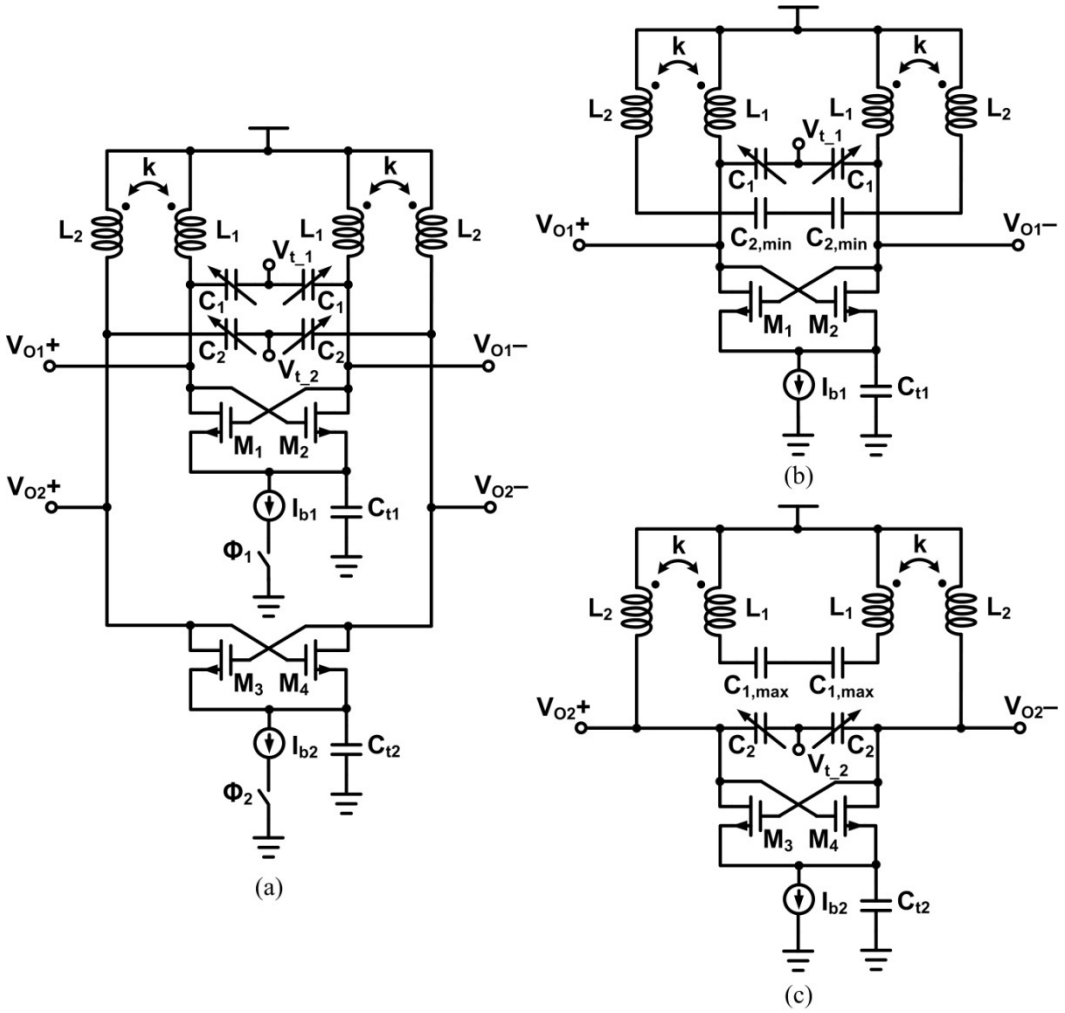


Fig. 4.5 Transformer-based one-port dual-band oscillator:

(a) the complete schematic, (b) simplified schematic for low band mode,

(c) simplified schematic for high band mode

like L_1' in Fig. 4.2(c). Thus, the phase noise of the one-port oscillator can be expressed, directly using the time-variant phase noise analysis result from [40], as

$$\mathcal{L}_{1-\text{port},11/22}(\Delta\omega) = 10\log\left[\frac{k_B T}{C}\frac{\omega_{osc}}{Q_{11/22}\Delta\omega^2 A_{11/22}{}^2}(1+\gamma)\right] \quad (4.10)$$

where C is the differential tank capacitor, equal to $0.5C_{1/2}$, $\Delta\omega$ is the offset frequency from the carrier, γ is close to 2/3 for low-electric-field MOSFETs provided that no large overdrive voltage is required by the differential pair $M_{1\text{-}2/3\text{-}4}$ for completing current switching, which is typically the case [41]. Assuming the current flowing into

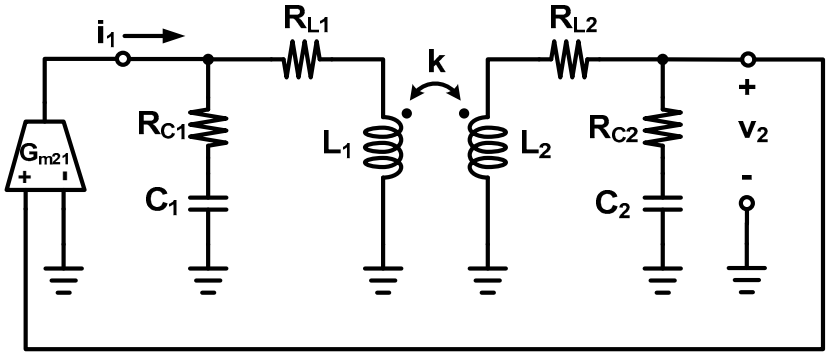
the tank is square wave like, the differential output amplitude $A_{11/22}$ is given by:

$$A_{11/22} = \frac{4}{\pi} \frac{1}{G_{m11/22,\min}(\omega_{L/H})} I_{b1/2} \tag{4.11}$$

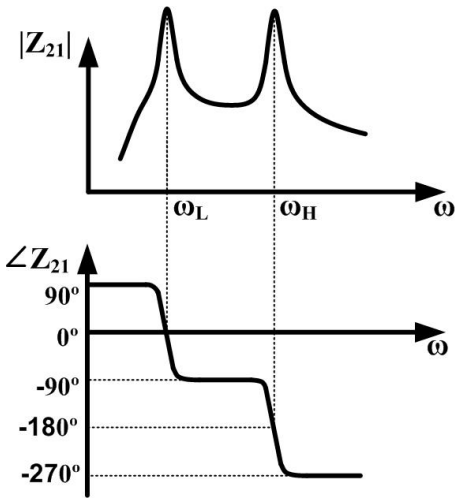
4.3 Transformer-Based Two-Port Dual-Band Oscillators

4.3.1 Oscillation Frequency

Fig. 4.6(a) gives the general model of the transformer-based two-port oscillator.



(a)



(b)

Fig. 4.6 (a) General model of transformer-based two-port oscillator, (b) frequency response of Z_{21}.

The transfer impedance Z_{21} can be derived as

$$Z_{21} = k\frac{\left(R_{C1}+\frac{1}{j\omega C_1}\right)\left(R_{C2}+\frac{1}{j\omega C_2}\right)}{(1-A_1)\sqrt{\frac{L_1}{L_2}}R_2+(1-A_2)\sqrt{\frac{L_2}{L_1}}R_1-j\frac{R_1R_2}{\omega\sqrt{L_1L_2}}+j\omega\sqrt{L_1L_2}[(1-A_1)(1-A_2)-k^2]} \tag{4.12}$$

where $R_1=R_{L1}+R_{C1}$, $R_2=R_{L2}+R_{C2}$, $A_1=\omega_1{}^2/\omega^2$, $A_2=\omega_2{}^2/\omega^2$. It is interesting to note that the result in Eq. (4.12) is perfectly symmetrical with respect to the two ports. That is, Z_{21} is equal to Z_{12}, as expected for such a passive network.

With high-Q assumption (R_{L1}, R_{L2}, R_{C1}, R_{C2} →0), Z_{21} can be simplified as

$$Z_{21} \approx \frac{jk\omega_1{}^2\omega_2{}^2\sqrt{L_1L_2}\omega}{(1-k^2)\omega^4-(\omega_1{}^2+\omega_2{}^2)\omega^2+\omega_1{}^2\omega_2{}^2} \tag{4.13}$$

From Eq. (4.13), the two peak frequencies of Z_{21} can also be expressed as Eq. (4.3), which implies that the potential oscillation frequencies ω_L and ω_H are exactly the same for both one-port or two-port configurations as long as the component Qs are sufficiently high.

4.3.2 Start-Up Condition

For the two-port oscillator as shown in Fig. 4.6(a), the current i_1 provided by the G_{m21} cell flows into the tank and generates a voltage v_2 across the transformer, which is then fed back to the input of the G_{m21} cell to form a feedback loop. The start-up conditions of the two-port oscillator can be expressed as

$$G_{m21} * real\{Z_{21}\} > 1 \tag{4.14a}$$

$$imag\{z_{21}\} = 0 \tag{4.14b}$$

As the sketched frequency response of Z_{21} in Fig. 4.6(b), due to the absence of the non-zero frequency notch, the phase shifts of Z_{21} are distinct as 0° and -180° at the peak frequencies ω_L and ω_H, respectively. As a result, to form a positive

feedback loop to initialize oscillation, G_{m21} needs to be positive at ω_L but negative at ω_H. Consequently, the oscillation frequency of the two-port oscillator can be well determined by controlling G_{m21} to be positive or negative. In other words, there is no stability issue for the two-port VCO as in the one-port counterpart.

From Eq. (4.14a), with high-Q approximation, the minimum G_{m21} to sustain the oscillation can be simplified as:

$$G_{m21,min} = \frac{(A_2-1)\frac{1}{Q_{L1}}+(A_1-1)\frac{1}{Q_{L2}}+A_1(A_2-1)\frac{1}{Q_{C1}}+A_2(A_1-1)\frac{1}{Q_{C2}}}{kA_1A_2\omega_{osc}\sqrt{L_1L_2}} \quad (4.15)$$

Note that when $\omega_{osc}=\omega_L$, $A_2>A_1>1$, and $G_{m21,min}$ is a positive number, and when $\omega_{osc}=\omega_H$, $A_1<A_2<1$, and $G_{m21,min}$ is a negative number. If all the capacitors are assumed to be lossless, $G_{m21,min}$ can be simplified to the result obtained in [29].

4.3.3 Tank Quality Factors – Qs

The tank quality factor Q_{21} for the two-port oscillator at the desired oscillation frequency is expressed as $\left|\frac{\omega_{osc}}{2}\frac{d\varphi_{21}}{d\omega}\right|$, where φ_{21} denotes the phase of Z_{21}. After simplification with high-Q approximation, it can be derived that Q_{21} is exactly the same as Eqs. (4.9a) and (4.9b), which means that both the one-port and the two-port oscillators have approximately the same tank quality factor as long as the tank components have high Qs or low losses.

4.3.4 Phase Noise

Fig. 4.7(a) shows the schematic of transformer-based two-port dual-band oscillator. As discussed above, the low band or high band oscillation can be well determined by controlling G_{m21} in Fig. 4.6(a) to be positive or negative, respectively. When only the current source I_{b1} is enabled, as shown in Fig. 4.7(b), the associated transistors M_1 and M_2 forms an equivalently positive G_{m21}, thereby, the oscillator

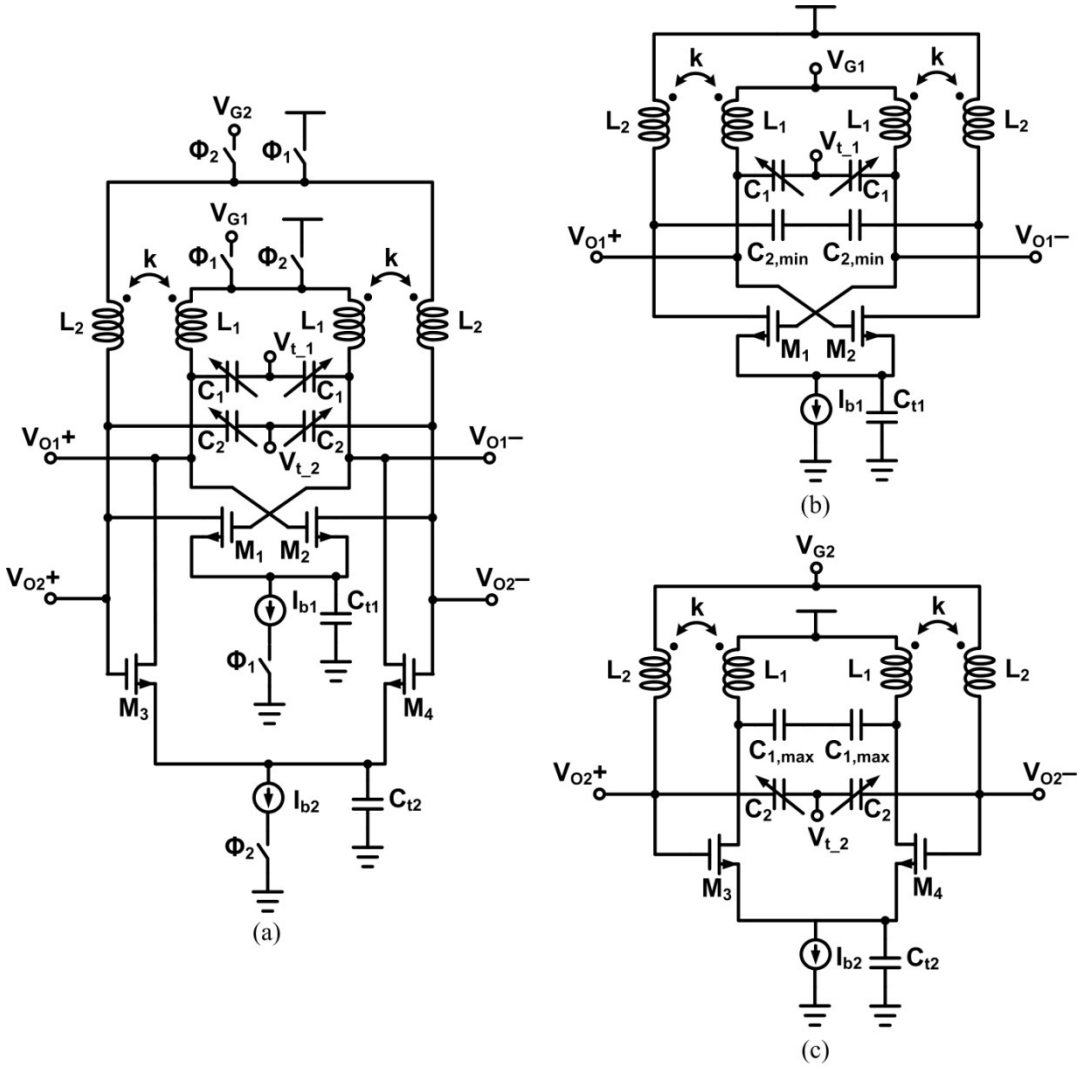


Fig. 4.7 Transformer-based two-port dual-band oscillator:

(a) the complete schematic, (b) simplified schematic for low band mode, (c) simplified schematic for high band mode.

operates at the lower frequency peak as the low band mode. When only the current source I_{b2} is enabled, as shown in Fig. 4.7(c), the associated transistors M_3 and M_4 forms an equivalently negative G_{m21}, consequently, the circuit oscillates at the higher frequency peak as the high band mode. Making use of the transformer, the gate voltages and drain voltages of $M_{1\text{-}4}$ can be independently biased to redistribute the amplitudes and keep the transistors from entering into triode region [42]. Interestingly, the topology of the two-port oscillator is very similar to the Class-C oscillator as

proposed in [43], and the phase noise expression has been derived and can be expressed as:

$$\mathcal{L}_{2-\mathrm{port}}(\Delta\omega) = 10\log\left[\frac{k_B T}{C}\frac{\omega_{osc}}{Q_{21}\Delta\omega^2 {A_{21}}^2}\left(1+\frac{\gamma}{k_{GD}}\right)\right] \quad (4.16)$$

where C is the differential capacitance at the transistor's gate, which is equal $0.5C_1$ for the low band or $0.5C_2$ for the high-band. k_{GD} is the voltage ratio of the gate amplitude to the drain amplitude. To minimize the phase noise, it is desirable to maximize the ratio k_{GD}. Thereby, in the low band mode the drain of $M_{1/2}$ is connected with L_2 as shown in Fig. 4.7(b), in the high band mode the drain of $M_{3/4}$ is connected with L_1 as shown in Fig. 4.7(c). With the above analysis results, k_{GD} can be well determined as equal to $G_{m22,min}(\omega_L)/G_{m21,min}(\omega_L)$ for the low band and $G_{m11,min}(\omega_H)/G_{m21,min}(\omega_H)$ for the high band. From Eqs. (4.7a) (4.7b) and (4.15), k_{GD} is increased with larger frequency ratio of ω_2/ω_1 and smaller coupling coefficient k, which is the same direction as the notch-peak cancellation. Finally, in Eq. (4.16) the differential output amplitude A_{21}, is given by:

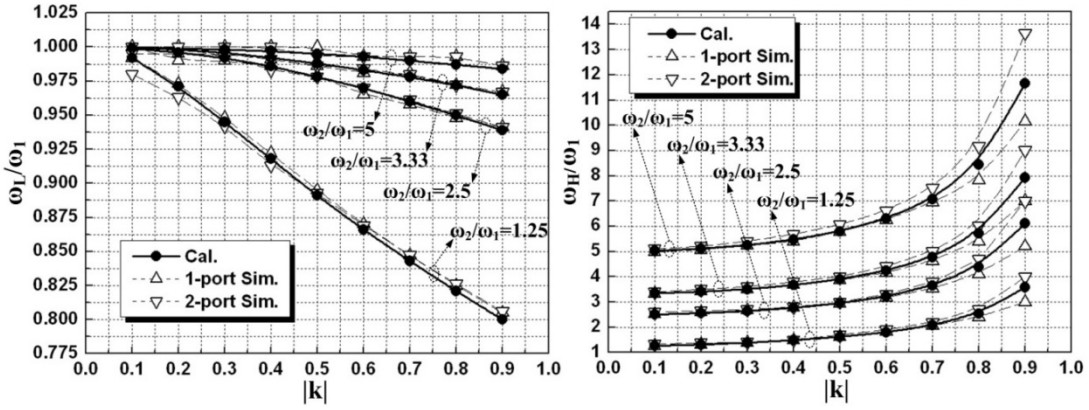
$$A_{21} = \eta\frac{1}{G_{m21,min}(\omega_{L/H})}I_{b1/2} \quad (4.17)$$

where η is equal to $4/\pi$ or around 2 without or with tail current shaping, respectively.

4.4 Comparisons of One-port and Two-Port Oscillators

4.4.1 Oscillation Frequency

Fig. 4.8(a) and Fig. 4.8(b) plot the two peak frequencies ω_H and ω_L given by Eq. (4.3) for different values of coupling coefficient k and ω_2/ω_1, and compare to the peak frequencies of both the one-port and two-port non-ideal oscillators, assuming the same component values as above. From the plots, the calculated result of Eq. (4.3) with



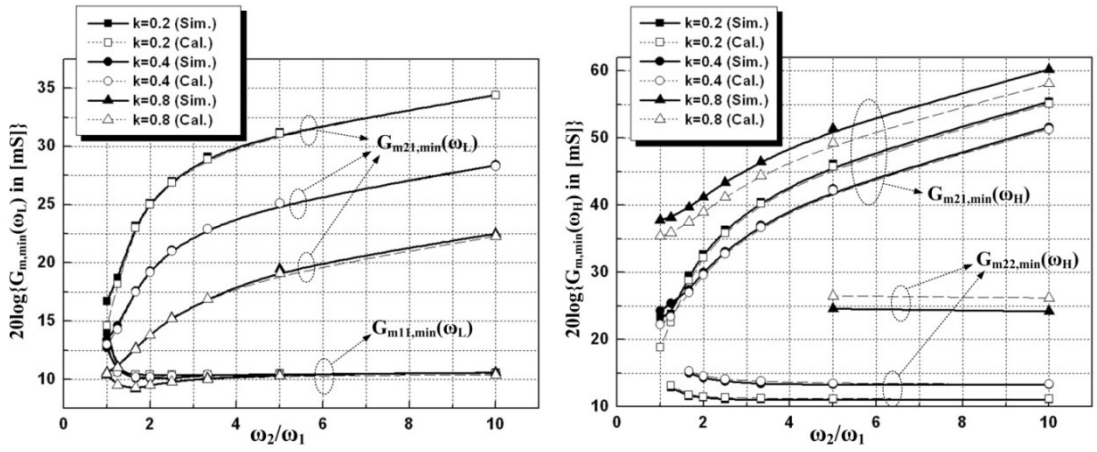
(a) (b)

Fig. 4.8 Plots of the peak frequencies: (a) ω_L in unit of ω_1, (b) ω_H in unit of ω_1.

low-loss assumption is in general a good estimation of the actual peak frequencies of typical one-port and two-port oscillators although special attention needs to be paid for the higher peak frequency when the two coils of the transformer are tightly coupled. Furthermore, the plot also shows that ω_L is always smaller than ω_1 while ω_H is always larger than ω_2. When k is a small number close to 0, the transformer behaves as two independent inductors, and $\omega_{L/H}$ is close to the value of $\omega_{1/2}$. When k increases from 0 to 1, ω_L decreases and eventually reaches a minimum value of $\sqrt{\omega_1^2\omega_2^2/(\omega_1^2+\omega_2^2)}$ when k=1, which is equal to $0.707\omega_1$ if $\omega_2/\omega_1=1$, or ω_1 if $\omega_2/\omega_1\rightarrow\infty$. On the other hand, when k increases from 0 to 1, ω_H also increases and finally approaches to infinity when k is very close to 1. These results are as expected because from Eqs. (4.2a), (4.2b) or (4.13), when |k|=1, there exists only one peak frequency ω_L in Z_{11}, Z_{22} or Z_{21}, and ω_H is pushed to infinity.

4.4.2 Start-Up Condition

Fig. 4.9 plots the calculated and simulated required G_m to oscillate at ω_L and ω_H in both one-port and two-port configurations for comparison. From Fig. 4.9(a) and Fig. 4.9(b), it can be clearly seen that in most situations the two-port oscillator requires



(a) (b)

Fig. 4.9 Start-up condition of both one-port and two-port oscillator: (a) calculated and simulated required G_m in log scale to oscillate at ω_L, (b) calculated and simulated required G_m in log scale to oscillate at ω_H.

much larger G_m to sustain oscillation than the one-port oscillator does. This can be understood by comparing Eq. (4.15) with Eq. (4.7a) or (4.7b) terms by terms. For example, at ω_L, when $\omega_2 \gg \omega_1$, the first term in $G_{m21,min}$, $\frac{1}{k\sqrt{L_1L_2}} \cdot \frac{A_2\text{-}1}{A_2} \cdot \frac{1}{A_1\omega_{osc}} \cdot \frac{1}{Q_{L1}}$, is larger than that in $G_{m11,min}$, $\frac{1}{L_1} \cdot \frac{1}{A_1} \cdot \frac{1}{A_1\omega_{osc}} \cdot \frac{1}{Q_{L1}}$, not only because $\frac{1}{k\sqrt{L_1L_2}} > \frac{1}{L_1}$, but also because $A_2 \gg A_1 > 1$, $\frac{A_2\text{-}1}{A_2} > \frac{1}{A_1}$. Similar comparisons can be also applied to the other terms in the equations. As a result, $G_{m21,min} > G_{m11,min}$ when $\omega_2 \gg \omega_1$. As the frequency ratio ω_2/ω_1 decreases, A_2 also decreases, the term $\frac{A_2\text{-}1}{A_2}$ becomes smaller, and as shown in Fig. 4.9(a), $G_{m21,min}$ is reduced with decreased ω_2/ω_1. Similarly, when $\omega_{osc}=\omega_H$, comparing the coefficient of $\frac{1}{Q_{L2}}$ in $G_{m21,min}$, $\frac{A_1\text{-}1}{kA_1A_2\omega_{osc}\sqrt{L_1L_2}}$, with that in $G_{m22,min}$, $\frac{1}{{A_2}^2\omega_{osc}L_2}$, when the frequency ratio ω_2/ω_1

is large, $A_1 \ll 1$, thus the absolute value of the term $\frac{A_1\text{-}1}{A_1}$ in $G_{m21,min}$ becomes infinitely large. On the other hand, in $G_{m22,min}$, the term $\frac{A_1\text{-}1}{A_1}$ does not exist, and the coefficient of $\frac{1}{\lambda A_1}$ in front of $\frac{1}{Q_{L1}}$ is simply equal to $\frac{A_2\text{-}1}{A_2(A_1\text{-}1)}$. It follows that $G_{m21,min}$ is much larger than $G_{m22,min}$. When the frequency ratio ω_2/ω_1 decreases, A_1 increases, and as shown in Fig. 4.9(b), $G_{m21,min}$ is also reduced with decreased ω_2/ω_1 when $\omega_{osc}=\omega_H$.

For the one-port oscillator, it can be observed from Fig. 4.9(a) that to oscillate at the lower frequency ω_L, $G_{m11,min}$ is relatively constant for different frequency ratios ω_2/ω_1 and k values. On the contrary, Fig. 4.9(b) shows that, to oscillate at the higher frequency ω_H, $G_{m22,min}$ is minimized with large ω_2/ω_1 and small k. Intuitively, in Z_{11}, as the lower frequency peak is always dominant as compared to the higher frequency peak, there is not too much variation for the peak impedance at ω_L. In contrast, in Z_{22}, because the higher frequency peak is not always dominant as compared to the lower frequency peak, the requirements for ω_2/ω_1 and k are the same as stabilizing condition. It is worthwhile to note that $G_{m22,min}$ is not plotted for small ω_2/ω_1 and large k values because the one-port oscillator could hardly oscillate at the lower frequency peak under these conditions.

4.4.3 Tank Quality Factors – Qs

Fig. 4.10 plots the calculated and simulated one-port and two-port tank Qs at the two peak frequencies with the same parameters used previously and with the inductor Q and capacitor Q being set to 7 and 20, respectively. Simulations show that the discrepancy between the calculated and simulated tank Qs for the two oscillators is

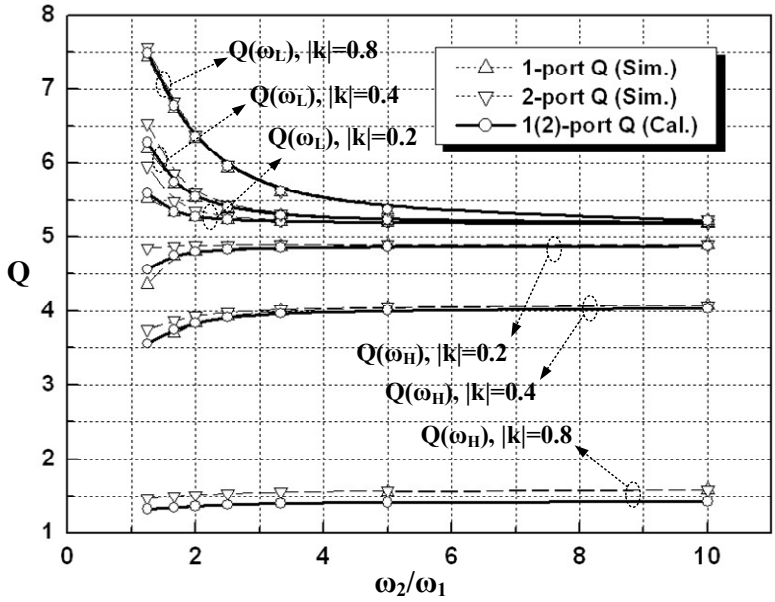


Fig. 4.10 Calculated and simulated tank quality factor $Q_{11/22}$ and Q_{21} at the two peak frequencies ω_L and ω_H.

decreased and finally approaches to zero as component Qs are increased, which validates the derivation. Moreover, Fig. 4.10 shows that, in general, compared to a second-order LC tank with the same component Q, the transformer-based fourth-order LC tank has a better Q at the lower frequency peak but a worse Q at the higher frequency peak. This can be understood from Eq. (4.9a) or (4.9b), from which the terms $\frac{1}{1+\lambda}$ and $\frac{1}{1+\lambda^{-1}}$ reflect the ratio of the contribution from L_1 and L_2 or C_1 and C_2 to the total tank Q (noting that $\frac{1}{1+\lambda} + \frac{1}{1+\lambda^{-1}} = 1$). Assuming that $Q_{L1}=Q_{L2}=Q_L$ and $Q_{C1}=Q_{C2}=Q_C$, where Q_L and Q_C denotes the Q of the L and C in the second-order LC tank, the total contribution from Q_{C1} and Q_{C2} to the fourth-order LC tank's Q will be the same as the contribution from Q_C to the second-order LC tank's Q. As a result, comparatively, whether the Q of the transformer-based LC tank is enhanced or degraded depends on whether the contribution from Q_{L1} and Q_{L2} is reduced or increased, which is determined by the extra coefficient $1/A_1$ and $1/A_2$. At

ω_L, $A_2>A_1>1$, the transformed based LC tank's Q is improved. On the other hand, at ω_H, $A_1<A_2<1$, and the tank Q is degraded.

From Fig. 4.10, the tank Q at the lower frequency ω_L is improved while the tank Q at ω_H is degraded with smaller frequency ratio ω_2/ω_1 and larger coupling coefficient k. This can be also estimated from Eq. (4.9a) or (4.9b). Assuming that $Q_{L1}=Q_{L2}=Q_L$, $Q_{C1}=Q_{C2}=Q_C$ and $m=n=\omega_2/\omega_1$, the equations can be written in the form of Eq. (4.18a) at ω_L and (4.18b) at ω_H, to keep the first term's numerator and denominator positive.

$$\frac{1}{Q_{tank}(\omega_L)} = \frac{(n^2{A_1}^2-1)-k^2}{(n^2{A_1}^2-1)+k^2}\frac{1}{Q_L}+\frac{1}{Q_C} \tag{4.18a}$$

$$\frac{1}{Q_{tank}(\omega_H)} = \frac{(1-{A_2}^2/n^2)+k^2}{(1-{A_2}^2/n^2)-k^2}\frac{1}{Q_L}+\frac{1}{Q_C} \tag{4.18b}$$

As A_1 at ω_L and A_2 at ω_H are weakly dependent on n and k when k is not very close to 1, from Eq. (4.18a) and (4.18b), it can be directly seen that when n is decreased or k is increased, the tank Q at ω_L could be improved while the tank Q at ω_H will be degraded. At the limiting case when $\omega_2/\omega_1=1$ and k=1, ω_L is reduced to $0.707\omega_1$, and A_1 is 2. If the capacitor loss is ignored, the maximum tank Q at ω_L is $2Q_L$. On the other hand under, the same condition, as ω_H is close to infinity, A_2 is close to zero, and the tank Q at ω_H would be infinitely small.

4.4.4 Phase Noise

If comparing the one-port and two-port oscillators' phase noise in an intuitive way with the well-know Leeson equation [44] expressed as

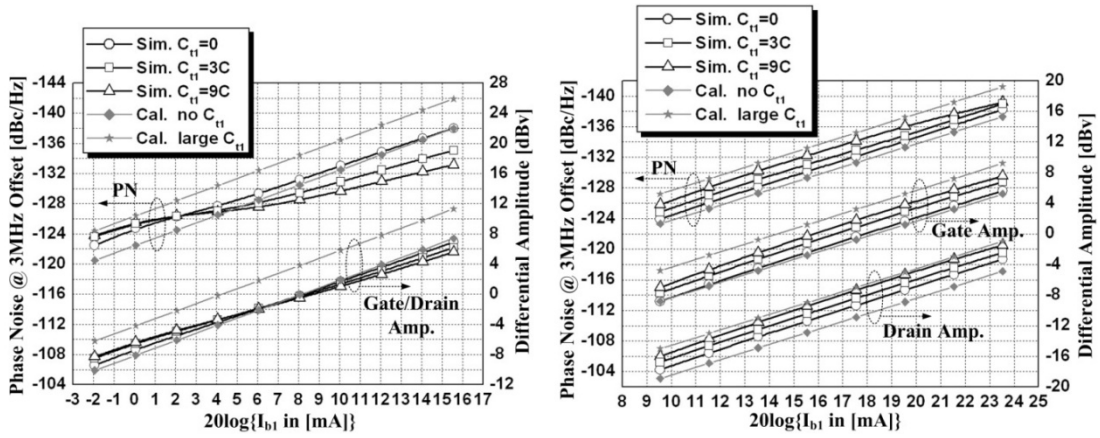
$$\mathcal{L}(\Delta\omega) = 10\log\left[\frac{k_B T}{C}\frac{\omega_{osc}}{Q\Delta\omega^2{A_0}^2}(1+F)\right] \tag{4.19}$$

where F is the excess noise factor accounting for the noise from active devices. The

oscillation frequencies and the tank Qs are approximately the same as long as the tank components are of low loss. On the other hand, in general, the two-port oscillator requires larger G_m than one-port oscillator to sustain the same amount of A_0, which would inject more noise current into the tank. As such, it would be concluded that two-port oscillators have inferior noise performance compared to one-port counterparts. However, this conclusion does not take into account the transistor noise in a time-variant way, and the excess noise factor F would be highly dependent on how the active devices are configured to compensate the tank loss. Eqs. (4.10) and (4.16) clearly show that, the active devices of two-port oscillators actually contribute less phase noise than ones of one-port oscillators.

It should be noticed that both Eq. (4.10) and Eq. (4.16) assume that the switching transistors $M_{1\text{-}4}$ do not leave saturation region when they are on. And Eq. (4.10) assumes that the capacitor at the tail node $C_{t1/2}$ is much smaller than $C_{1/2}$. Using the passive component values in previous discussion and assigning m=n=4, k=0.6, Fig. 4.11(a) shows the simulated (using SpectreRF) output amplitude and phase noise values versus different tail currents and capacitances, when the one-port oscillator operates at ω_L with only I_{b1} enabled. The transistors with size of 50μm/0.12μm in a 0.13μm CMOS process (V_{th} around 0.4V), are used for $M_{1\text{-}2}$ to make the operation close to hard switching. The calculated phase noise and output amplitude based on Eqs. (4.10) and (4.11) are also plotted for comparison with no C_{t1} and very large C_{t1}.

In Fig. 4.11(a), when I_{b1} is small and A_{11} is no larger than V_{th} so that $M_{1\text{-}2}$ do not enter into triode region, both the output amplitude and the phase noise are linearly improved with the increasing bias current, and the simulated results can be well predicted by the calculated ones. Since the tail capacitor can help shaping the current injected into the tank, the output amplitude and thus the phase noise are improved with



(a) (b)

Fig. 4.11 Phase noise and amplitude of transformer-based: (a) one-port, and (b) two-port oscillators.

larger tail capacitance [45]. However, when the I_{b1} is increased further, $M_{1\text{-}2}$ would operate more in triode region with larger output amplitude, and the output amplitude begins to deviate a little from the predicted linear curve because the tank is loaded by the tail capacitor with the finite turn-on resistance of the MOSFETs in triode region [46]. In contrast, with increasing I_{b1}, the phase noise curve deviates further and further away from the predicted linear improvement, and the deviation of the phase noise curve is much more than the one of the output amplitude curve, mainly because the MOSFETs produce much more effective noise when the transistors are operated in the deep triode region [43]. And the larger the tail capacitance, the more the phase noise is degraded from the expected value.

Using the same parameters as above, Fig. 4.11(b) plots the calculated and simulated amplitudes and phase noise with different tail currents and tail capacitance values, when the two-port oscillator operates at ω_L with only I_{b1} enabled. Compared to the one-port oscillator, the I_{b1} of two-port oscillator needs to be around 3 times larger in order to achieve the same output amplitude, as predicted by Eqs. (4.7a) and (4.15).

However, because the drain amplitude is much smaller than the gate amplitude and the gate voltage can be biased to be much lower than the voltage supply, the transistors can be kept away from the triode region even when the differential output amplitude is as large as 2V (VDD is 1.2V). As a result, with the increased bias current, the two-port oscillator shows much better amplitude and especially phase noise "linearity", which is quite close to the ideal calculated results. It follows that, with sufficiently large bias current, two-port oscillator is able to achieve lower phase noise compared to the one-port oscillator.

Moreover, it is worthwhile to notice that all the discussions on the phase noise of one-port and two-port oscillators do not take into account the noise contribution from the current source. In order to minimize this contribution, the tail current MOSFET of one-port oscillators would require larger voltage headroom than that of two-port oscillators, due to the parasitic capacitance from the current source [43]. Consequently, the achievable maximum oscillation swing of two-port oscillators could be larger than that of one-port oscillators.

4.5 Frequency Plan of Dual-band VCO for SDR FGS

Making use of the analytical results, a dual-band transformer-based oscillator is designed for the target SDR FGS. With dual-band operations, the transformer-based VCO can achieve a tuning range larger than 66.7% so that a continuous frequency range from 47MHz to 6GHz can be obtained by simply employing a chain of divide-by-2 frequency dividers. As such, the problem with spurious tones with using mixers or fractional dividers can be totally eliminated. Moreover, to support all the 14 OFDM UWB frequency bands from 3GHz to 10GHz, the VCO is also designed to

provide the fundamental IQ signals at 8.448GHz, and the divider chain in the PLL can be reused in the "UWB" mode to simultaneously generate the required IQ signals at frequencies 4224MHz, 2112MHz, 1056MHz, 528MHz, and 264MHz for single-sideband (SSB) mixings [47].

As discussed in Section 4.4, compared to a second-order LC tank, the Q of a transformer-based LC tank is improved at the lower frequency peak but degraded at the higher frequency peak. It is therefore more desirable to make VCO operate at the lower frequency band when the LO frequencies are generated for those wireless standards with stringent phase noise requirement. Fig. 4.12 shows the frequency planning of the dual-band VCO, in which the frequency of interest can be generated at either of the two frequency bands or at a sub-harmonic of these frequency bands by dividing them down by 2^N. Fortunately, the frequency bands covering all the standards with the most stringent phase noise requirement (such as GSM/DCS/PCS requiring <-139.5dBc/Hz at 3MHz offset and passive UHF RFID requiring -144dBc/Hz at 3.6MHz offset [48]) can be assigned into the lower frequency band while the frequency bands for the other standards with more relaxed phase noise requirement can be assigned in the higher frequency band.

To generate LO signals according to the frequency planning shown in Fig. 4.12, the LO frequency range should be wide enough to cover dual bands from 3GHz to 4.2GHz and from 8.4GHz to 12GHz. For the target system applications, IQ outputs are also required at these LO frequencies. These IQ signals can be obtained by dividing down a differential LO signal operating at twice of the operation frequency, which would require excessively large power consumption for ultra-wideband VCO and frequency dividers at 24GHz. Alternatively, wideband poly-phase filters can be employed at the expense of high loss and large IQ mismatches over the entire

ultra-wideband frequency range. Taking into account all these considerations and trade-offs and considering the limited f_T of the 0.13μm CMOS process used, a dual-band QVCO covering the fundamental frequency bands from 3GHz to 4.2GHz and from 8.4GHz to 12GHz is chosen as the design target.

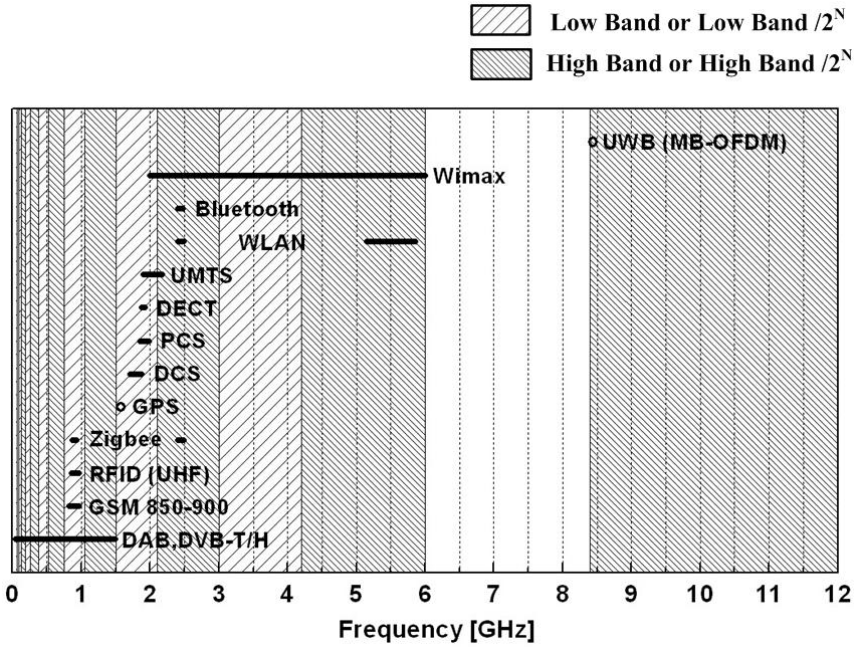


Fig. 4.12 Frequency planning of the dual-band VCO

4.6 Design of Transformer-Based Dual-band Q-VCO

In general, it is complicated to optimize the design of a dual-band VCO because various transformers with different combinations of inductor ratios and coupling coefficients can be used to fulfill the specified frequency bands. According to the frequency plan, around 45% tuning range is required for both of the low band and high band, with some margin for the process variation. Switched-capacitor arrays (SCAs) are employed to achieve the tuning ranges each band. Including all the parasitic capacitance, when all the switching capacitors are on, the total capacitance is around 1.1pF for $C_{1/2}$, and $Q_{C1/C2}$ are around 21 and 7.5 for 3GHz and 8.4GHz, respectively, in

a 0.13μm CMOS process. As pointed out by Eqs. (4.9a) and (4.9b), at ω_L, since $\lambda < 1$, the tank Q is mainly decided by the Q_{L1}, while at ω_H, since $\lambda > 1$, the tank Q is mainly dominated by the Q_{L2}, so Q_{L1} and Q_{L2} should be optimized at the low band frequencies and high band frequencies respectively. Assuming $Q_{L1}=Q_{L2}=14$ at the interested bands, and $Q_{L1}=Q_{L2}=7$ at the other frequency bands, which are the typical values of the achievable inductor Q as simulated by Momentum using the 2μm thick top metal layer of the process, all the profiles, including the required bias currents (to obtain maximum differential output amplitude of 2V), the tank Qs, the phase noise of both one-port and two-port oscillators as well as stability conditions of one-port oscillator, can be fast evaluated as shown in Fig. 4.13 by using the equations in Section 4.2 and Section 4.3.

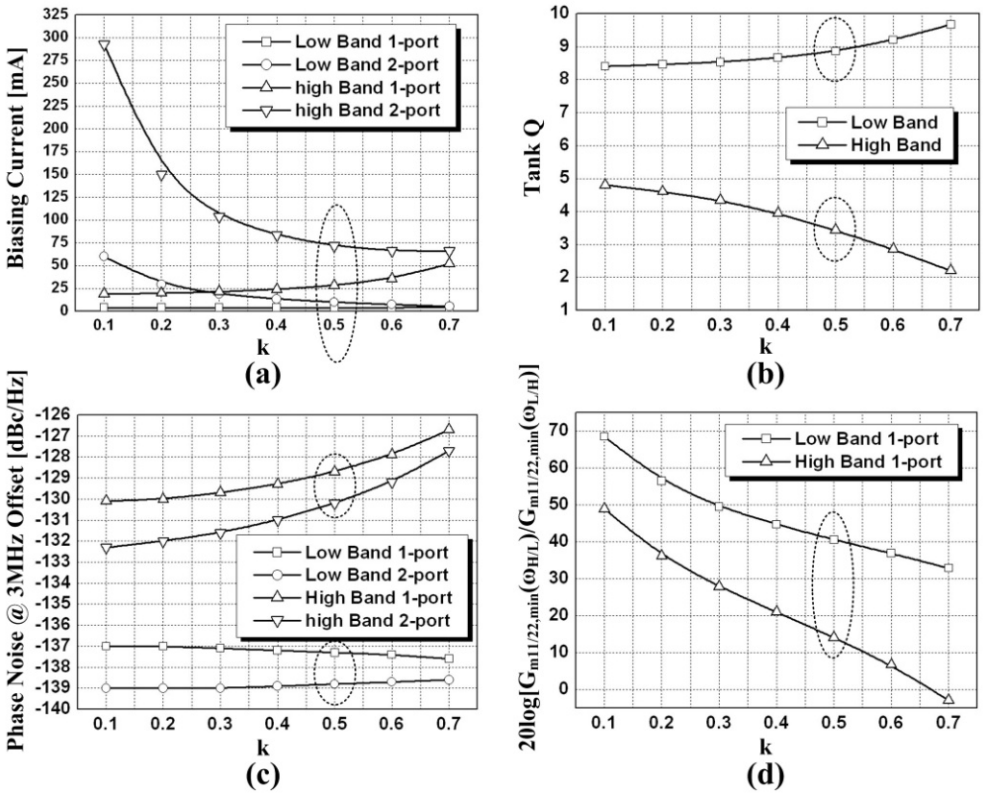


Fig. 4.13 Estimated (a) bias current for maximum output swing, (b) tank Q, (c)phase noise at 3MHz frequency offset, (d)stability margin of one-port oscillator.

Noted that when k is increased from 0, ω_L departs from ω_1 and becomes lower and lower, while ω_H departs from ω_2 and become higher and higher, consequently the desired frequency ratio ω_H/ω_L around 2.8 is not achievable when k becomes larger than 0.77, which can be known from Eq. (4.3) by using $\omega_1=\omega_2$, thus in Fig. 12 the curves are only plotted up to k=0.7.

When plotting Fig. 4.13, L_1 and L_2 are varied to make the dual-band VCO oscillates at 3GHz and 8.4GHz for the worst scenario when all the switching capacitors are turned on, and it is assumed that tail capacitance is zero for the one-port oscillator and is large enough for the two-port oscillator to predict the lowest achievable phase noise at largest output swing. As shown in Fig. 4.13(a), when k is increased, the required bias current is reduced for the two-port oscillator but increased for the one-port oscillator. And when k is increased to around 0.6, the bias current of two-port oscillator can be comparable to the one of one-port oscillator for the low band oscillation. On the other hand, to sustain maximum swing for the high band oscillation, the two-port oscillator requires large current above 60mA and the one-port oscillator required around 25mA when k is less than 0.5. In Fig. 4.13(b), the low band tank Q is improved from 8.4 to 9.7 while the high band tank Q is degraded from 4.8 to 2.2 when k is increased from 0.1 to 0.7. The high band tank Q is mainly dominated by the Q_{C2}, which can be improved by increasing the switch size of the switched capacitor at the expense of smaller tuning range. In Fig. 4.13(c), for one-port oscillator, when k is increased, the low band phase noise is improved because the low band Q is improved, and the high band phase noise is degraded because of the degradation of the high band Q. On the other hand, for the two-port oscillator, when k is increased, because the voltage ratio K_{GD} is decreased for both the low band and high band, the low band phase noise actually degrades slightly although the low band Q is improved, while the high

band phase noise degrades significantly due to the degradations of both K_{GD} and high band Q. Fig. 4.13(d) illustrates that one-port oscillator can operate stably at the low band for any k value but would fail to operate at the high band when k is close to 0.7. Finally, k is selected around 0.5. As a result, the two-port configuration can be used for low band operation to achieve dedicated phase noise performance to meet the cellular standards as well as passive UHF RFID, with less than 10mA bias current for maximum voltage swing. And the higher frequency peak of Z_{22} can be more than 10dB larger than the lower frequency peak, so that one-port configuration can be used for high band operation to greatly save the high band power consumption. In the design, to further reduce the high band power, the high band output swing is reduced from 2V, and the penalty of phase noise is not linearly proportional because for the one-port oscillator the phase noise curve is "compressed" significantly at the large output swing as shown in Fig. 4.11(a), especially a large size tail current transistor is used to minimize the noise contribution from the current source.

Fig. 4.14(a) shows the schematic of the transformer-based dual-band Q-VCO. The operation can be divided into two modes. In the first mode, the current sources I_{core1} and I_{tune1} are turned on and I_{core2} and I_{tune2} are turned off, and the circuit operates as a two-port oscillator as shown in Fig. 4.14(b). As M_1 and M_2 are connected to make the G_{m21} as shown in Fig. 4.6(a) positive, the VCO will oscillate at the lower frequency band. In the second mode, the current sources I_{core1} and I_{tune1} are turned off and I_{core2} and I_{tune2} are turned on, and the VCO operates at the higher frequency band as a one-port oscillator shown in Fig. 4.14(c). In both modes, the fine frequency tuning is realized by varying the coupling current [49] instead of using varactors to reduce AM-to-PM noise conversion and to prevent the tank Q from being further degraded by varactors. A V-to-I converter with tunable transconductance is implemented to convert

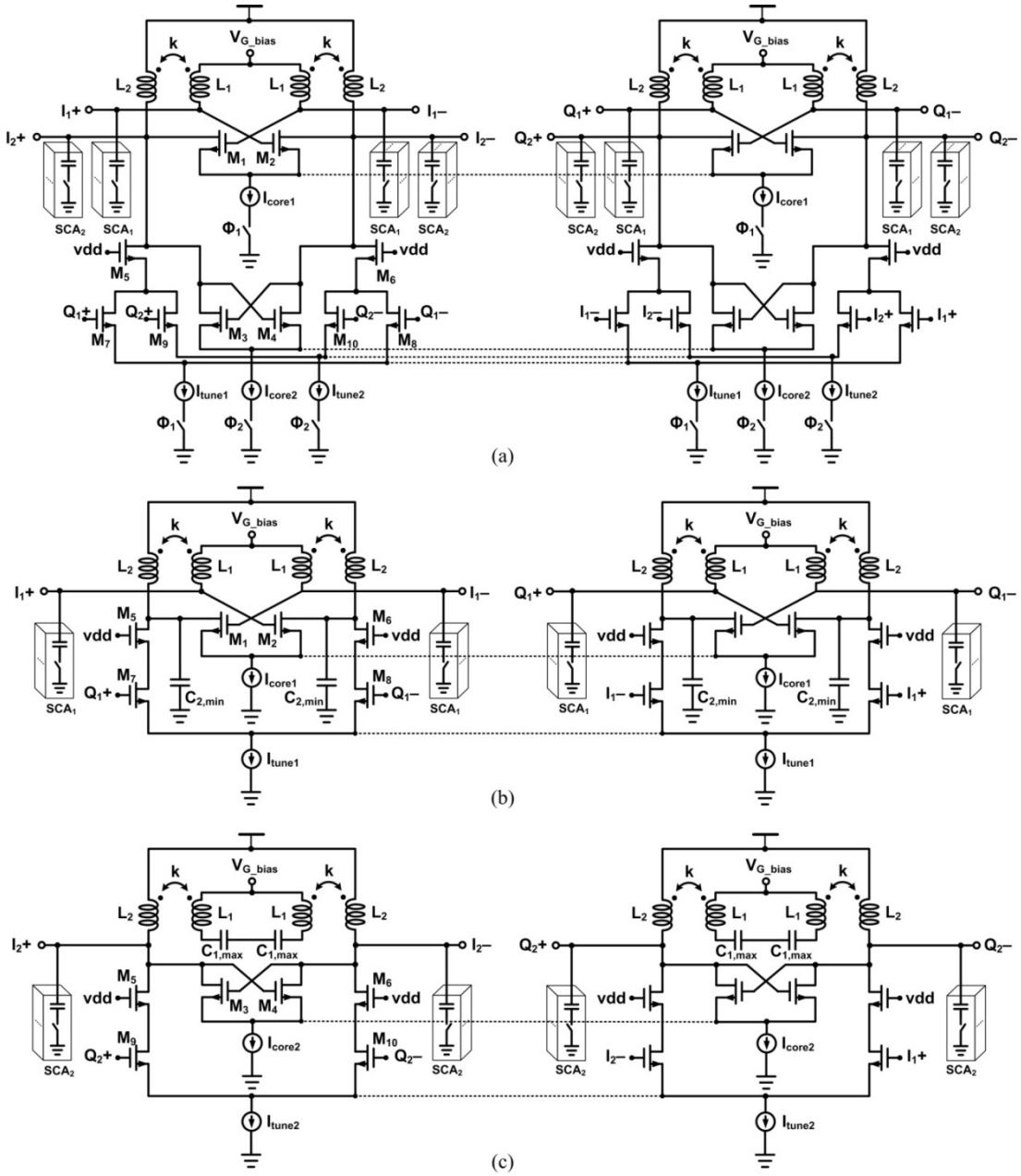
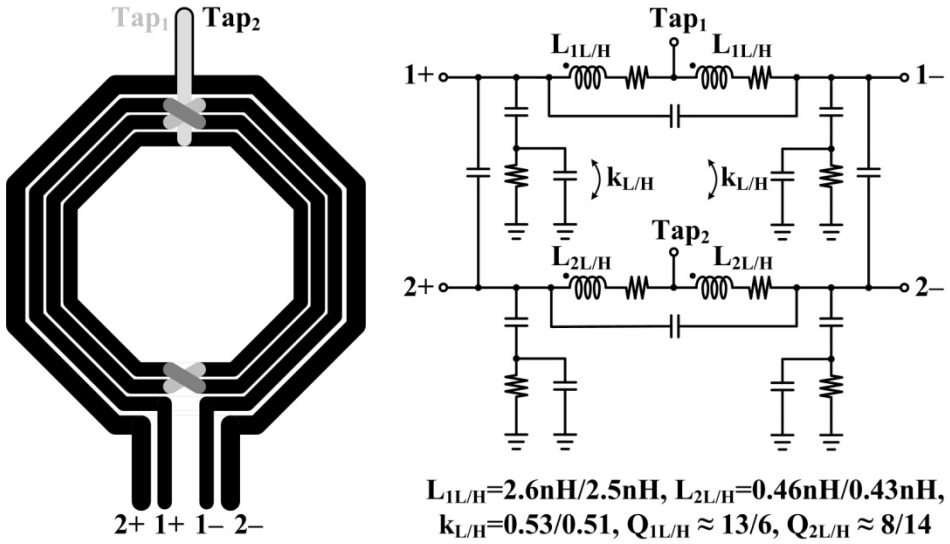


Fig. 4.14 Schematic of the transformer-based dual-band Q-VCO: (a) the complete schematic, (b) simplified schematic for the first mode, (c) simplified schematic for the second mode.

the control voltage from the loop filter to the tuning current to make effective K_{VCO} tunable for dynamic loop bandwidth control. 5-bit binary weighted SCAs are placed at both the first and the second coils of the transformer to realize the coarse tuning and to reduce the required tuning range of $I_{tune1/2}$ and thus the variation in phase noise. A large

frequency ratio ω_2/ω_1 is desirable to minimize the phase noise of the two-port oscillator in the first mode, and to stabilize the one-port oscillator in the second mode, thereby, in the first mode all SCAs at the port-2 are turned off, while in the second mode all SCAs at the port-1 are turned on.



(a) (b)

Fig. 4.15 Transformer's (a) layout, and (b) model.

Fig. 4.15(a) shows the layout of the transformer designed for the dual-band Q-VCO. The 1st coil is laid out as 3-turn octagon inside, and the 2nd coil is laid out as 1-turn octagon outside. The widths of the 1st coil and 2nd coil are optimized as 9μm and 12μm, to make the peak Q_{L1} and peak Q_{L2} located at the low band and high band, respectively. The space between the two coils is set to 3um to achieve the coupling coefficient k around the desired value 0.5. Simulation verifies that at the worst case when all the switched capacitors at the 2nd coil are turned on, the higher-frequency peak impedance $|Z_{22}(\omega_H)|$ is more than 10dB larger than the other peak impedance $|Z_{22}(\omega_L)|$. The transformer model is shown in Fig. 4.15(b). To achieve more accurate results, two sets of model parameters are separately fitted and used in SpectreRF simulations over the two frequency bands. In the dual-band Q-VCO layout, all the

transistors and SCAs for the high-frequency band are placed closer to the transformer than those for the low-frequency band to maximize the ratio C_1/C_2 and to balance the power consumption of the two bands.

For LC-based Q-VCO, bimodal oscillations may occur during the frequency tuning because when all the switched capacitors are off, the inductor Q dominates the tank Q, and the Q-VCO would prefer to oscillate at the frequencies higher than the peak frequency [49]. However, when all the capacitors are switched on, the tank Q would be dominated by the capacitor Q, especially at high oscillation frequency, and consequently the Q-VCO would prefer to oscillate at the frequencies lower than the peak frequency. To eliminate any potential bimodal oscillations, the cascode transistors M_5 and M_6 are added to create enough delay at the coupling path [50].

To improve the IQ matching, the current sources of "I" and "Q" parts are connected correspondingly as shown in the dotted lines in Fig. 4.14[51]. In order to measure the IQ sideband rejection ratio (SBR) directly, the QVCO's IQ outputs are connected to an on-chip single-sideband (SSB) mixer. A low-frequency divider is also embedded to generate the second low-frequency IQ input signals for the SSB mixer from an external low-frequency input signal.

4.7 Experimental Results

The dual-band Q-VCO was fabricated in a 0.13-μm CMOS process. Fig. 4.16 shows the die photo of the Q-VCO together with the on-chip SSB mixer and divider for the SBR measurement, where the Q-VCO occupies an area of 1.2mm*0.7mm.

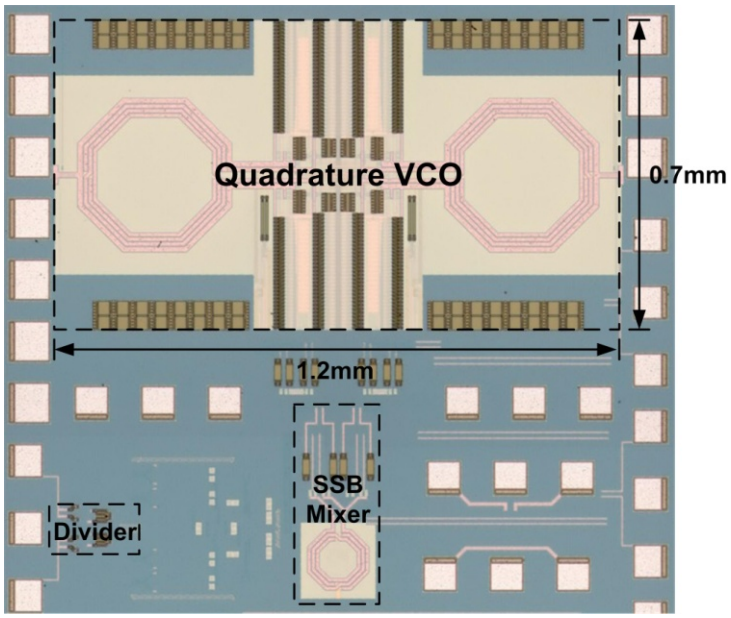
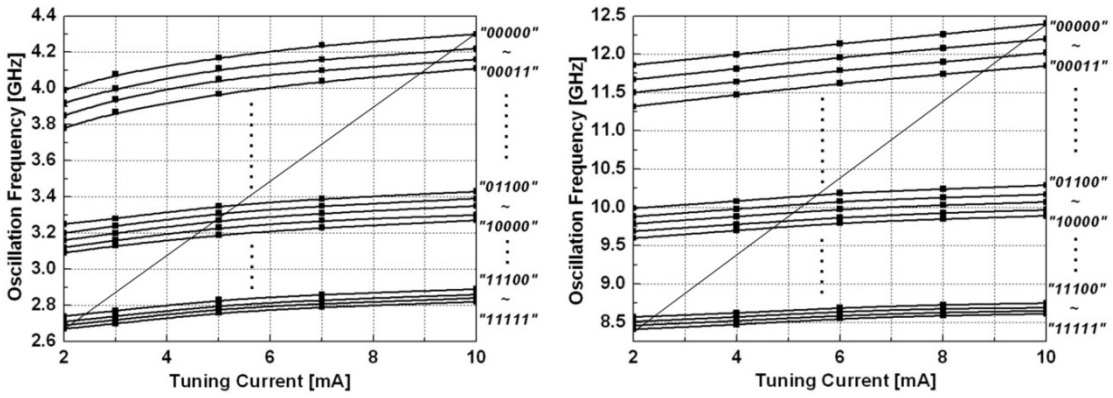


Fig. 4.16 Die photo of the proposed dual-band Q-VCO.

The dual-band Q-VCO draws a current from 12mA to 20mA from a 1.2V voltage supply in both modes. Fig. 4.17 shows the measured frequency curves of the Q-VCO in the two modes as a function of the tuning current. The Q-VCO is continuously tunable from 2.7GHz to 4.3GHz in the first mode and from 8.4GHz to 12.4GHz in the second mode, corresponding to the tuning ranges of 45.7% and 38.5%, respectively.

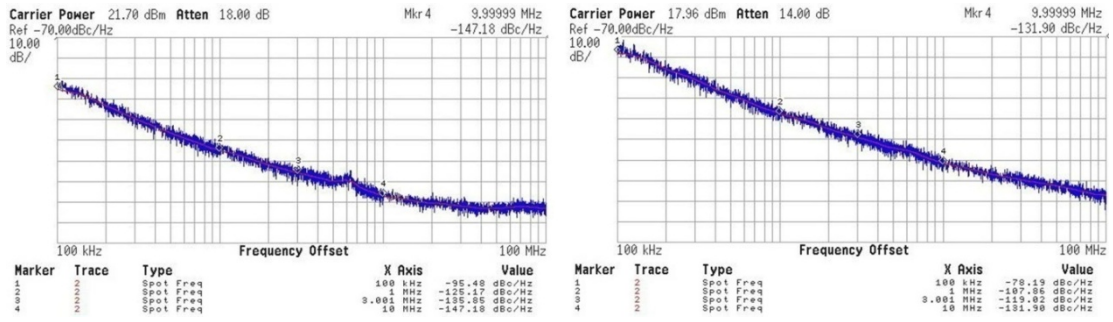


(a) (b)

Fig. 4.17 Measured frequency tuning curves of the dual-band quadrature VCO when the Q-VCO operates at: (a) the first mode. (b) the second mode.

As a result, the experimental dual-band Q-VCO can successfully meet the

frequency requirement for the SDR applications. During the measurement, it is found that in the second mode the Q-VCO could oscillate at the lower frequency peak when the SCAs at the 1st port are all intentionally turned-off while the SCAs at the 2nd port are all on, which shows that keeping a large capacitor ratio C_1/C_2 is important for the stability of the one-port oscillation.



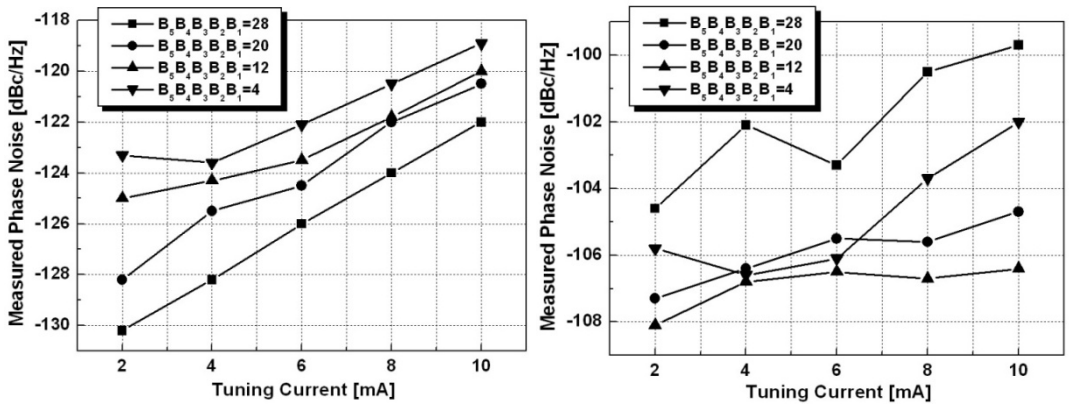
(a) (b)

Fig. 4.18 Measured phase noise curves of the dual-band Q-VCO when it operates at: (a) the lower frequency band 3.6GHz. (b) the higher frequency band 10.4GHz.

To measure the low phase noise at large frequency offset, an external amplifier is used to suppress the noise floor of the testing environment. Fig. 4.18(a) and Fig. 4.18 (b) show the measured phase noise profiles at 3.6GHz and 10.4GHz with the Q-VCO drawing 16mA from the voltage supply, from which the phase noise values of -135.9dBc/Hz and -119dBc/Hz at 3MHz offset are achieved, respectively. In the first mode, the measured phase noise can marginally fulfill the most difficult requirement by DCS/PCS considering a 6dB phase noise improvement after an operation of divide-by-2 and exceeds the requirement of GSM 850-900 considering a 12dB improvement after divide-by-4. In the second mode, the measured phase noise meets all the requirements of the related standards such as WLAN and UWB considering the corresponding frequency division ratio.

Fig. 4.19(a) and Fig. 4.19(b) show the measured phase noise as a function of the

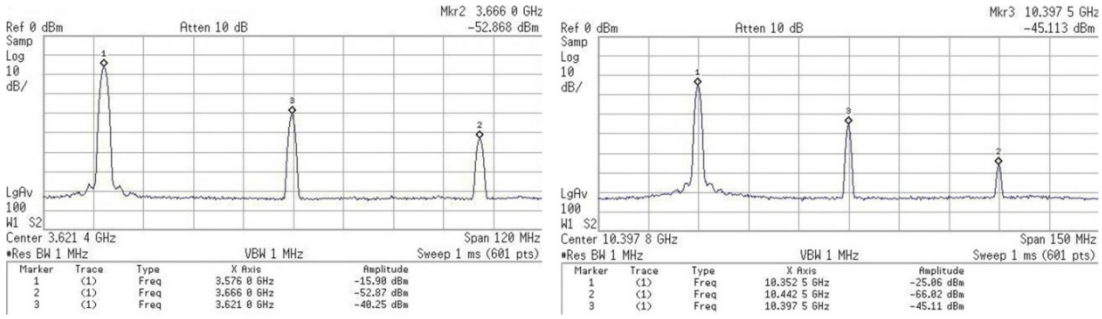
tuning current at different SCA settings. When the tuning current varies from 2mA to 10mA, the phase noise at 1MHz offset is measured between -118.9dBc/Hz and -130.2dBc/Hz for the lower band and between -99.7dBc/Hz and -108.1dBc/Hz for the higher band, respectively. As expected, the phase noise is degraded with increased tuning current. From the frequency tuning curves as plotted in Fig. 4.17, a tuning current from 2mA to 6mA is sufficiently enough for covering the required frequency bands with 5-bit binary-weighted SCAs, thus at 1MHz frequency offset, the low band phase noise variation can be reduced to between 122.1dBc/Hz and 130.2dBc/Hz, and the high band phase noise variation can be reduced to between 102.1dBc/Hz and 108.1dBc/Hz.



(a) (b)

Fig. 4.19 Measured phase noise of the dual-band quadrature VCO at 1MHz offset at different tuning current and SCA settings when the Q-VCO operates at: (a) the first mode. (b) the second mode.

The measured spectrums of SSB mixer's output under the same bias conditions in Fig. 4.18 are shown in Fig. 4.20(a) and Fig. 4.20(b). Assuming that the mismatch of the QVCO is dominant, the SBRs of 37dB and 41dB are achieved for the lower and higher band, corresponding to IQ phase errors of 1.6° and 1°, respectively.



(a) (b)

Fig. 4.20 Measured spectrum at the SSB Mixer's output, when the Q-VCO operates at: (a) the lower frequency band 3.6GHz. (b) the higher frequency band 10.4GHz.

Table 4.1 summarizes the performance of the designed dual-band Q-VCO compared with the other published dual-band VCOs. The figure-of-merit (FOM) and figure-of-merit with TR (FOM_T) are defined as:

$$FOM = 10log\left[\left(\frac{f_0}{\Delta f}\right)^2 \frac{1}{L(\Delta f) \times P_{diss}|mW}\right]$$

$$FOM_T = FOM + 20\log\left(\frac{TR_{total}\,[\%]}{10}\right)$$

Table 4.1 Comparisons of Dual-Band Differential and Quadrature VCOS

Ref.	Tech.	1st Band [GHz]	2nd Band [GHz]	PN [dBc/Hz]	P_{diss} [mW]	Area [mm^2]	Output	FOM	FOM_T
[22]	0.25μm CMOS	0.98 ~1.16 (17%)	1.60 ~2.01 (23%)	-138 /-132 @3MHz	11 /14	0.25	Dif.	178 /177	190 /189
[23]	0.18μm CMOS	0.82 ~0.87 (5%)	1.64 ~1.81 (10%)	-125/-123 @ 0.6MHz	16	0.90	Dif.	176 /181	180 /184
[24]	90nm CMOS	8.1~15.4 (62%)		-106 @1MHz	7.7	-	Dif	179	194

[26]	0.13μm CMOS	3.3~8.4 (87%)		-117 ~-122 @1MHz	7~15	0.1	Dif	181 ~185	200 ~204
[27]	0.18μm Bi-CMOS	6.3~6.6 (5%)	9.45~9.9 (5%)	-106/-104 @1MHz	19.4	1.65[1]	I&Q	177/178	177/178
[28]	0.13μm CMOS	3.4~7 (69%)		-101 ~-119 @1MHz	1~8	0.65[1]	Dif.	167 ~192	184 ~209
[30]	0.5μm Bi-CMOS	0.79 ~0.85 (7%)	1.75 ~1.87 (7%)	-134/-134 @1MHz	15	3.6[1]	Dif.	181 /188	184 /191
[31]	0.18μm CMOS	3.27 ~5.02 (42%)	9.5~11.4 (18%)	-116/-112 @1MHz	6/10	0.88	I&Q	181 /182	197 /198
[32]	90nm CMOS	3.1~3.9 (23%)	8.8~11.2 (24%)	-122/-117 @ 2.5MHz	2.2 ~4.2 /6.7 ~10	0.034	Dif.	181	194
[35]	0.18μm CMOS	2.4 (0%)	4.7 (0%)	-122/-123 @1MHz	3.4	-	Dif.	185 /192	-
This	0.13μm CMOS	2.7~4.3 (46%)	8.4~12.4 (38%)	-136/-119 @3MHz	14~24	0.84	I&Q	185 /177	203 /195

1. The area counted includes pads.

4.8 Summary

In this chapter, dual-band oscillators using transformer-based fourth-order LC tank are analyzed. The closed forms of the oscillation frequencies, start-up conditions,

the tank Qs and the phase noise of both one-port and two-port oscillators are derived and compared. Compared to two-port oscillators, one-port oscillators consume less power but may suffer stability problem, which can be solved by the proposed notch-peak cancellation technique. Analysis also shows that with low-loss tank components, the two configurations have the same tank Qs. And the fourth-order LC tank's Q is better at lower peak frequency but worse at the higher peak frequency than the Q of a second-order LC tank. On the other hand, compared to one-port oscillators, two-port oscillators has better phase noise "linearity" with increased biasing current, which enable them trade off power consumption with phase noise performance more efficiently. Based on the analysis, a dual-band Q-VCO is proposed and designed specifically for the wide-band SDR application. Implemented in a 0.13μm CMOS process, the dual-band Q-VCO prototype achieves IQ output signals continuously from 2.7GHz to 4.3GHz and from 8.4GHz to 12.4GHz, and successfully meets the frequency and phase noise requirement of the target SDR LO generation system for all the wireless standards from 47MHz to 10GHz.

Chapter 5

Wide-Band Frequency Dividers

Frequency dividers are key building blocks in frequency synthesizer to divide down the VCO's output frequency and make it comparable to the reference frequency. Frequency dividers are also widely used to generate IQ carrier signals in the modern transceivers. For the SDR applications, frequency dividing is an important manner to extend the frequency range of the VCO. Comparing different types of frequency dividers, there is a direct trade-off between the operation frequency and the locking range. LC-based injection-locked frequency dividers (ILFDs) feature the highest operation frequency at the lowest power, but their locking range is quite limited due to the high-Q nature of the resonator. LC-based Miller Dividers (MD) [52] have improved locking range than ILFDs, but their operation frequency is lower and the power consumption is typically larger compared to ILFDs. Without employing resonators, static dividers have the largest locking range, while the operation frequency is lowest.

In this chapter, static frequency divider is reviewed and modified for the SDR FGS as described in section 5.1. Section 5.2 presents a proposed current bleeding/reusing technique to improve the locking range of ILFDs. Section 5.3 applies the current bleeding technique on MDs as well to enhance the locking range of MDs. Section 5.4 provides the general theory and method applicable for both of the LC-based frequency dividers, to optimize the operations and the locking ranges of the two divider types. Finally, the experimental results are shown in Section 5.5.

5.1 High Speed Static Frequency Divider

5.1.1 Static Frequency Divider Topologies

Static digital dividers are realized through cascading two latches that are transparent out of phase from each other, as shown in Fig. 5.1, so they are called flip-flop dividers.

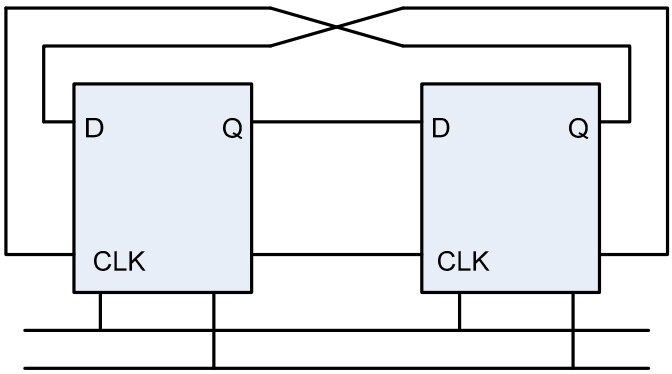
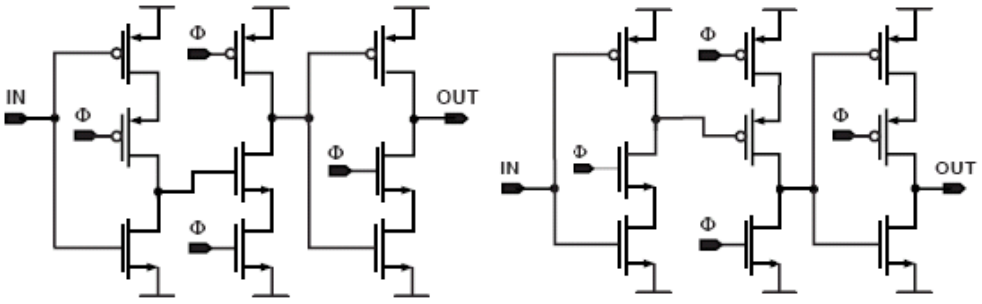


Fig. 5.1 Block diagram of flip-flop based digital divider

For high speed digital circuits, high ratio of the driving current to the loaded capacitance is desired. Increasing transistor width does not help because both the driving current and the load capacitance increase with wider transistors. The voltage supply can be increased, which improves the driving current while keeps the loaded capacitance almost the same. Another more effective solution is to decrease the transistor length, by doing so, the driving current increases and the loaded capacitance decreases. Thereby, static digital dividers directly benefit from the scaling of the CMOS technology, and they can be also used as a manner to evaluate the technology.

There are many kinds of circuit topologies available for implementing the latch. A popular one which is able to operate with single-end input (one phase) clock is called true single phase clocked (TSPC) divider. Fig. 5.2 shows a simplified implementation of TSPC approach with 9 transistors [53]. Feeding back the inverted

output directly to the input either in Fig. 5.2(a) or in Fig. 5.2(b), a divide-by-2 circuit is formed, with the clock signal as the divider's input.

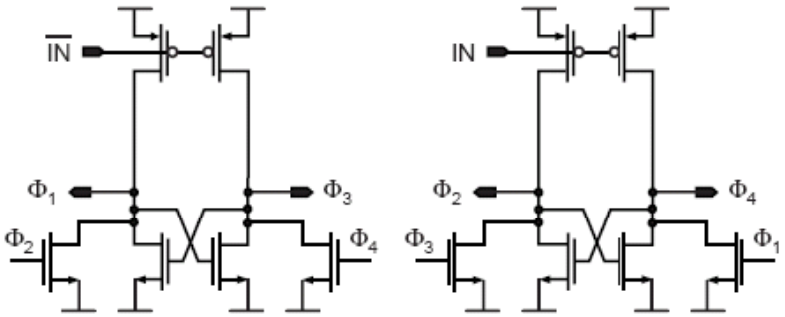


(a) (b)

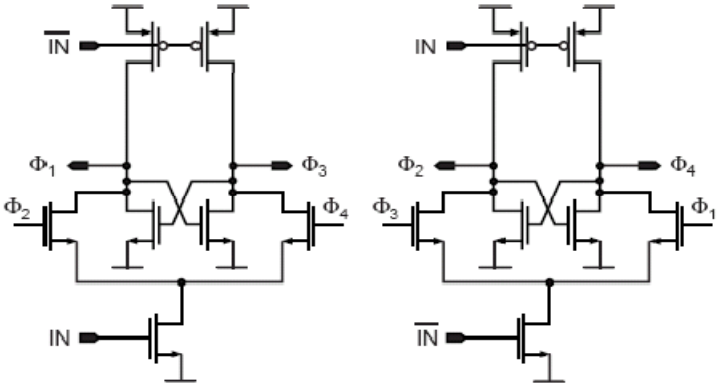
Fig. 5.2 Simplified TSPC registers (a) positive transition triggered (b) negative transition triggered

This kind of divider does not need the differential clock and has no static power consumption, while achieving compact size with a reasonably high speed. However, the divider needs a full swing input clock to properly operate and since the signals have to go through 3 stages per cycle, the speed is still limited.

Faster divider topologies are proposed by Razavi [54] and Wang [55], as shown in Fig. 5.3(a) and Fig. 5.3(b), respectively. For both of the two topologies, speed is improved because the transition signals only have to go through two gates per cycle. But these two dividers require full swing differential input signals and have static power consumptions.



(a)



(b)

Fig. 5.3 (a) Razavi's frequency divider, (b) Wang's frequency divider.

One of the fastest static frequency dividers is the source-coupled logic (SCL) divider, as shown in Fig. 5.4. Since whether the latch is in sensing mode or latching mode is controlled by the current-mode input clock, this kind of divider is also called current-mode logic (CML) divider.

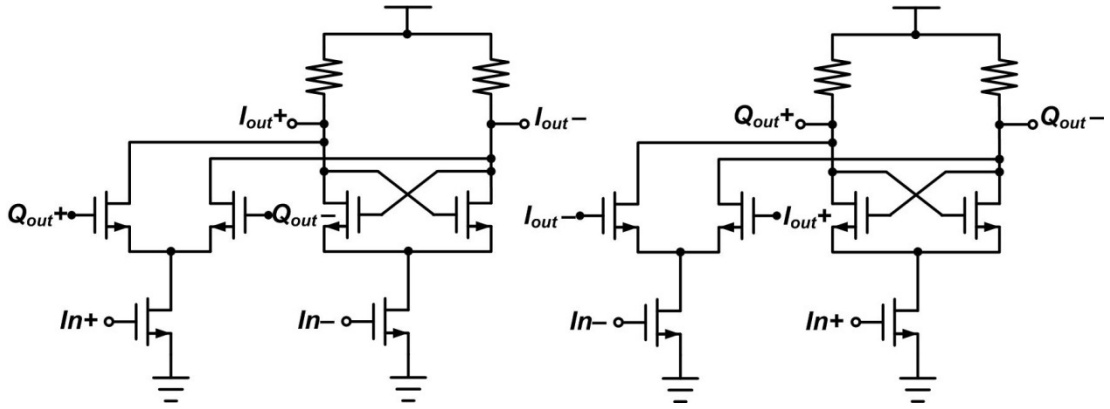


Fig. 5.4 Schematic of SCL frequency divider

The signal goes through only two gates per cycle and the usage of low speed PMOS is avoided. The divider is able to operate with smaller input clock swing than previous approaches, which is very important at high frequencies. However, obviously the SCL divider has static power consumption and needs differential input signals.

In latching mode, the cross-coupled pair needs large load impedance for firm positive feedback. In the sensing mode, the differential pair needs small load

impedance for small RC constants. Therefore, a potential solution to improve the SCL divider's speed is using a dynamic load PMOS instead of the fixed resistive load. However, such solution would be limited by the speed of PMOS, and requires extra biasing for the PMOS, making the circuit more sensitive to PTV variations. Another way to improve the speed of the SCL divider is using inductive shunt peaking to enhance the bandwidth of the divider's load, but at the expense of more chip area.

5.1.2 Quadrature-In-Quadrature-Out (QIQO) SCL Dividers

Fig. 5.5 shows the block diagram of the frequency divider chain in the desired SDR FGS. The dual-band Q-VCO's output frequency range is extended through numbers of QIQO divide-by-2 dividers, as from divider-A to divider-G. As a result, IQ outputs can be supported continuously from 47MHz to 6GHz.

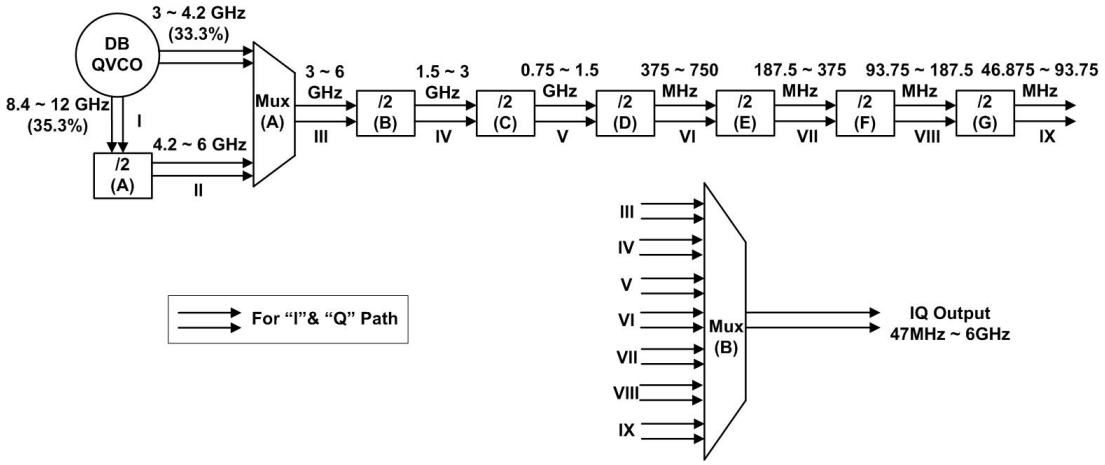


Fig. 5.5 Frequency divider chain for extending DB QVCO's frequency range

In the 0.13μm CMOS, SCL dividers are able to operate with more than 15GHz input frequency, at the expense of 6mA power consumption including the one of IQ divider buffers. Although the power consumption can be much reduced if LC-based ILFD is used instead, static SCL dividers are chosen and applied in the SDR FGS for the following reasons. First, two inductors are required for IQ output LC-based dividers, which consumes much larger chip area, and the much increased size of the

frequency dividers with using inductors can also induce longer running lines among building blocks, which results in reduced output swing at each divider's input, consequently, either divider buffer's power consumption needs to be increased to compensate the loss of running line, or the divider's locking range would be sacrificed. The latter is especially critical for the LC-based ILFD, as its locking range may not be sufficient for the wide-band SDR application.

Because each divider outputs IQ signals while only requires differential input signals, a second dummy divider would be required to balance the IQ loading of the previous divider stage, which consumes extra area and power. To avoid extra dummy dividers, as show in Fig. 5.6, for each divider stage the input IQ signals are combined in current domain, converted into differential signals and then injected into the divider core. Along the divider chain, the dividers' load resistors and bias currents are scaled accordingly, to enable fast design and good matching of the operation frequencies.

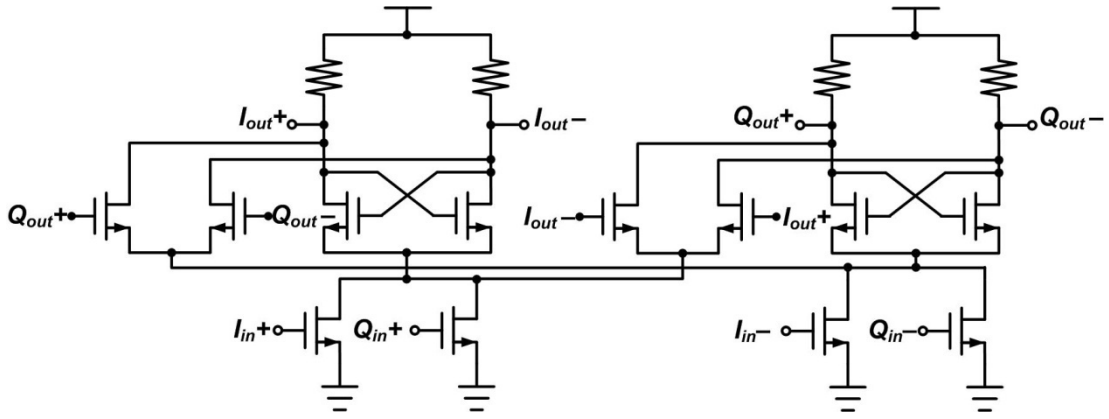


Fig. 5.6 QIQO CML divide-by-2 divider

5.2 Proposed Current-Reusing ILFD (CR-ILFD)

To enable the low power high frequency ILFDs being widely used in wireless communications, intense design techniques have been investigated and reported to

enhance the ILFD's locking range. Injection into two coupled LC-oscillators [56] and sandwiched injection into two identical LC-oscillators [57] were proposed but are only suitable for dividers requiring quadrature outputs. Inductive-peaking and trans-conductance enhancement techniques [58][59][60] were also employed but require extra inductors and thus larger chip area. In this section, a simple but effective technique is presented to significantly enlarge the locking range of ILFDs without extra inductive component while consuming low power.

Fig. 5.7(a) shows the schematic of a conventional ILFD, and its behavioral model is shown in Fig. 5.8(a). The differential pair M_2 and M_3 act as a single-balanced mixer, to mix the fed-back output voltage V_o at frequency ω with both the dc current I_{dc} and the ac current I_{inj} at frequency 2ω provided by the tail transistor M_1, where the current ratio $|I_{inj}|/|I_{dc}|$ is defined as the injection ratio η. I_a and I_b are the mixing products of I_{dc} and V_o, I_{inj} and V_o, with the conversion coefficients k_1 and k_2, respectively. Due to the high selectivity of the LC-tank, only the current components at frequency ω are considered at the mixer's output. Two conditions need to be satisfied for the divider to work properly. The first one is that the loop gain needs to be at least unity, which is easy to satisfy for the ILFD as long as I_{dc} is large enough for self-oscillation. The second condition is that the total phase shift in the loop needs to be zero. Consequently, as shown in Fig. 5.8(a), the phase shift φ needs to compensate the induced phase shift β from the LC-tank at the operation frequency ω. Because of the high-Q of the LC-tank, as ω moves away from ω_0, $|\beta|$ increases rapidly, and $|\varphi|$ needs to be increased accordingly. From the phasor diagrams in Fig. 5.8(b), the maximum $|\varphi|$ is given by $\arcsin(|I_b|/|I_a|)$, which is proportional to $(k_2/ k_1)\cdot\eta$. Due to the mixing property, the conversion coefficient k_2 is always smaller than k_1, which limits maximum achievable $|\varphi|$. As a result, increasing the injection ratio η is critical for the improvement of the

phase condition and thus the locking range.

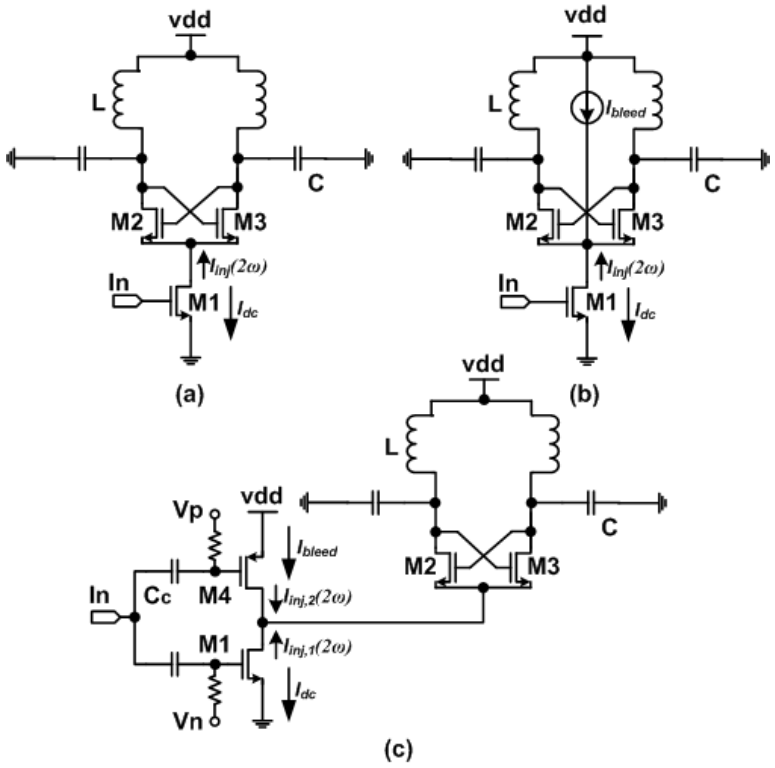


Fig. 5.7 (a) Conventional LC ILFD, (b) current-bleeding LC ILFD, and (c) proposed injection-enhanced frequency divider.

Given a fixed input swing, the injection ratio η can be increased by reducing the bias gate voltage of M_1 to operate it in Class-C mode instead of Class-A mode**.** However, the W/L size of M_1 would need to be increased rapidly to maintain the biasing current, which would result in large parasitic capacitance at the drain node and limit the effective achievable injection ratio [61]. One simple solution to improve the injection ratio is to steer away some of the dc current from M_2 and M_3 by connecting a current source from VDD to the common-source node as shown in Fig. 5.7(b). The current bleeding also reduces the overdrive voltage of M_2 and M_3 and thus improves the switching of the single-balanced mixer. The current source can be simply implemented by a PMOS with a constant gate bias voltage. Moreover, as shown in Fig. 5.7(c), the injection ratio can be improved further by applying the ac input signal to the

gate of the bleeding PMOS M_4 instead of a constant gate voltage. As such, the PMOS transistor acts not only to reduce the dc current but also to inject more ac current to the divider. Since the bleeding current is reused to bias the PMOS transistor, no extra power is required. Fig. 5.8(b) shows the differences on the phasor diagrams between the conventional ILFD and the proposed injection-enhanced ILFD. By increasing $|I_b|$ and reducing $|I_a|$, the phase condition and thus the locking range are significantly improved. Finally, as shown in Fig. 5.7(c), ac coupling is implemented for both M_3 and M_4 to enable the divider to operate at a lower supply voltage.

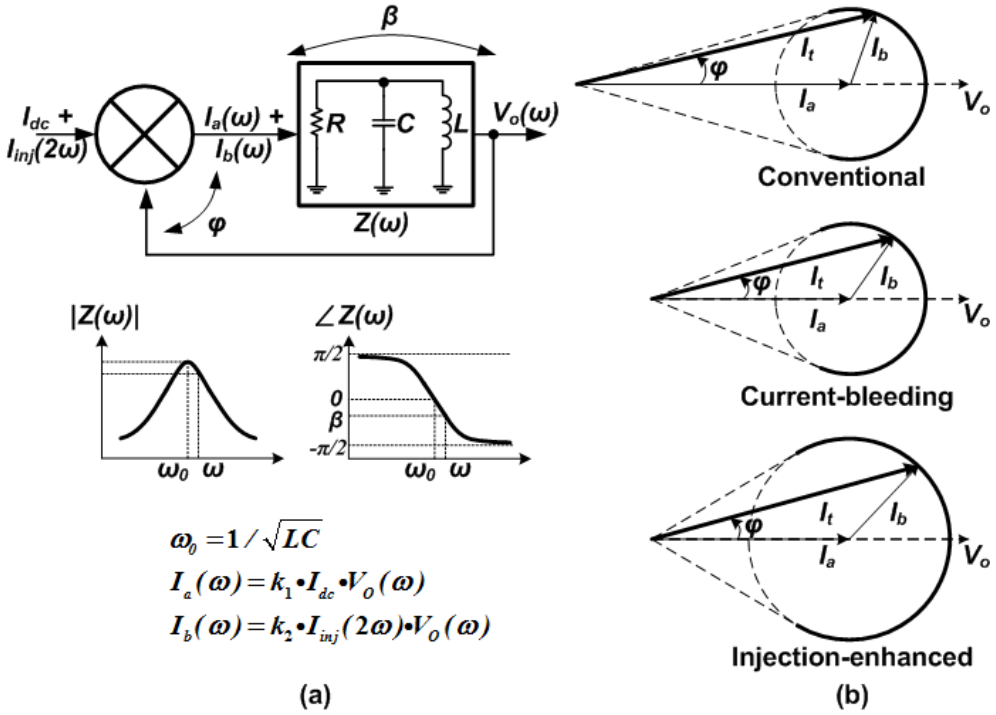


Fig. 5.8 (a) Behavioral model of LC-ILFD, and (b) phasor diagrams of the current injection into the LC-tank.

5.3 Proposed Current-Bleeding MD (CB-MD)

The above ILFDs are operated with only single-ended input signals. When connected to VCOs, which are typically differential to reject common-mode noise and to avoid the grounding issues, especially at millimeter-wave (MMW) frequencies, a

second dummy ILFD is required to balance the loading of the VCO [62]. Such a dummy ILFD would inevitably increase both the chip area and the power consumption. Miller dividers [63][64] can support differential inputs, but they are not as widely used as ILFDs, especially at very high frequencies, mainly due to their inferior gain condition and thereby limited locking range under constrained power consumption. In this section, a simple but effective technique is presented to improve the gain condition and maximize the locking range of Miller dividers at 60GHz without increasing chip area and power consumption.

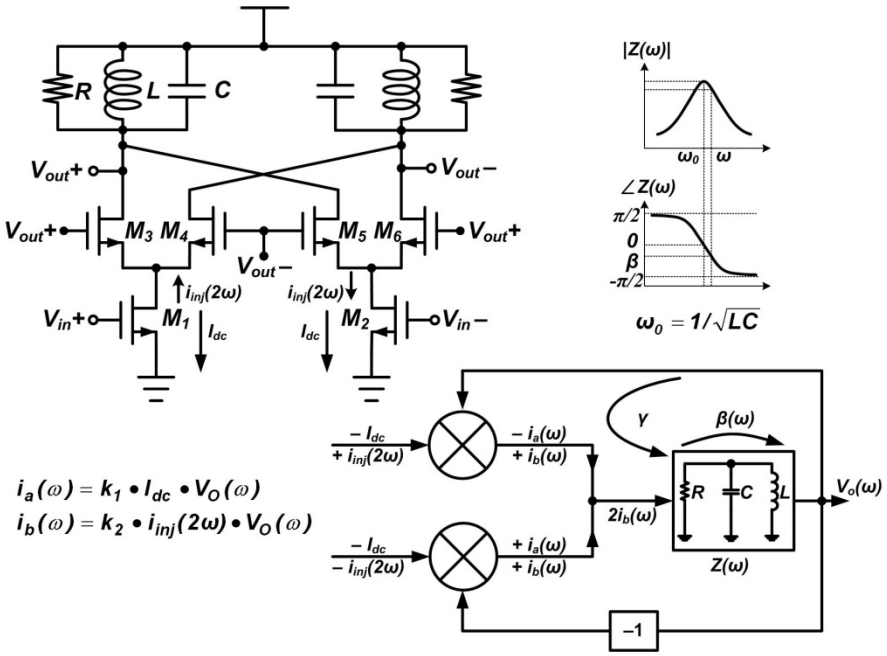


Fig. 5.9 Conventional Miller Divider and its behavioral model

Fig. 5.9 shows the schematic of a conventional MD. The transistors $M_{1\text{-}6}$ function as a double-balanced mixer, whose outputs are fed back to the switching transistors $M_{3\text{-}6}$ to perform divide-by-2 operation. Notice that as described in [63], the output voltages can be also fed back to the gates of the trans-conducting transistors $M_{1\text{-}2}$ and thereby the input signals can be applied to the gates of the $M_{3\text{-}6}$. However, by doing so the typically larger input capacitance of the switching transistors $M_{3\text{-}6}$ needs to be

driven at 2ω rather than ω, which would cause higher power consumption.

The behavioral model of the conventional MD is also shown in Fig. 5.9. The output voltage V_o at frequency ω is fed back to mix with both the input dc current I_{dc} and the input ac current i_{inj} at frequency 2ω provided by $M_{1\text{-}2}$. The output current components i_a and i_b are defined as: $i_a(\omega)=k_1 \cdot I_{dc} \cdot V_o(\omega)$ and $i_b(\omega)=k_2 \cdot i_{inj}(2\omega) \cdot V_o(\omega)$, where k_1 and k_2 are the conversion gains from I_{dc} to i_a and from i_{inj} to i_b, respectively. Two conditions need to be satisfied for the loop to operate properly. The first condition is that the total phase shift in the loop needs to be zero, which means that the phase shift γ from V_o to the current injected to the LC-tank needs to compensate the induced phase shift β from the LC-tank at the operation frequency ω. Due to the double-balance mixing, the injected current only contains the component i_b, and the phase shift γ is determined by the phase difference between the input and the output voltages, which can be any arbitrary value. Consequently, the phase condition is not a problem for MDs.

The second condition is that the loop gain must be at least unity, or equivalently $2k_2|i_{inj}(2\omega)||Z(\omega)| \geq 1$. As the inductance L is small for mm-wave frequencies, $|Z(\omega)|$ is small, and thus $k_2|i_{inj}(2\omega)|$ needs to be large to meet the gain condition. Unfortunately, due to the limited conversion gain k_2, large biasing current and large input swing are typically required, which makes the conventional MDs less attractive as compared to ILFDs. Since the operation of the MD is limited by the gain condition, it is not necessarily beneficial to completely cancel out the current component i_a. In fact, it can be shown that the gain condition and thus the locking range can be significantly improved by intentionally introducing some net current component i_a to the tank. This could be done by sizing or biasing M_1 and M_2 differently, but it would cause significant differential mismatch to the divider's input impedance. Alternatively, $M_{3\text{-}4}$

and $M_{5\text{-}6}$ can be sized differently, which would however make i_a amplitude highly sensitive to the output voltage V_o. For example, when V_o is large enough, both $M_{3\text{-}4}$ and $M_{5\text{-}6}$ operate closely to hard switching, and the net i_a injected into the LC-tank would become very small.

To overcome these problems, current bleeding technique can be applied by adding a PMOS M_7 to steer away a dc current I_{bleed} from M_3 and M_4, as shown in Fig. 5.10. For clarity, transistors $M_{3\text{-}6}$ have been redrawn in Fig. 5.10 but their connections remain exactly the same as in Fig. 5.9. From the behavioral model in Fig. 5.10, the current bleeding introduces a well-controlled extra current component i_c into the LC-tank, which is proportional to the bleeding current I_{bleed}. It will be shown in the following section that I_{bleed} can be well determined so as to optimize the divider's operation and maximize its locking range.

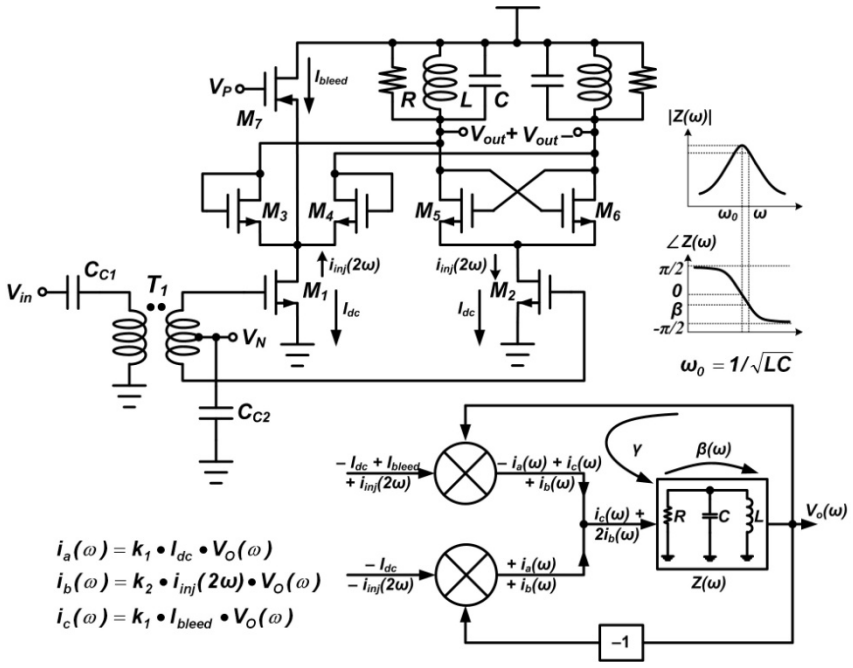


Fig. 5.10 Proposed current-bleeding MD and its behavioral model

5.4 Locking Range Optimizations of LC-Based Frequency Dividers

5.4.1 Analysis of Optimal Condition

The phasor diagram of the total current injected into the LC-tank i_{total} is plotted in Fig. 5.11. When the operation frequency ω is farther away from the peak frequency ω_0 of the LC-tank, as the tank impedance $|Z(\omega)|$ decreases and the induced phase shift from the tank $|\beta|$ increases, both the magnitude $|i_{total}|$ and phase shift $|\gamma|$ from $|i_{total}|$ need to be increased in order to maintain the same output amplitude and satisfy the phase condition.

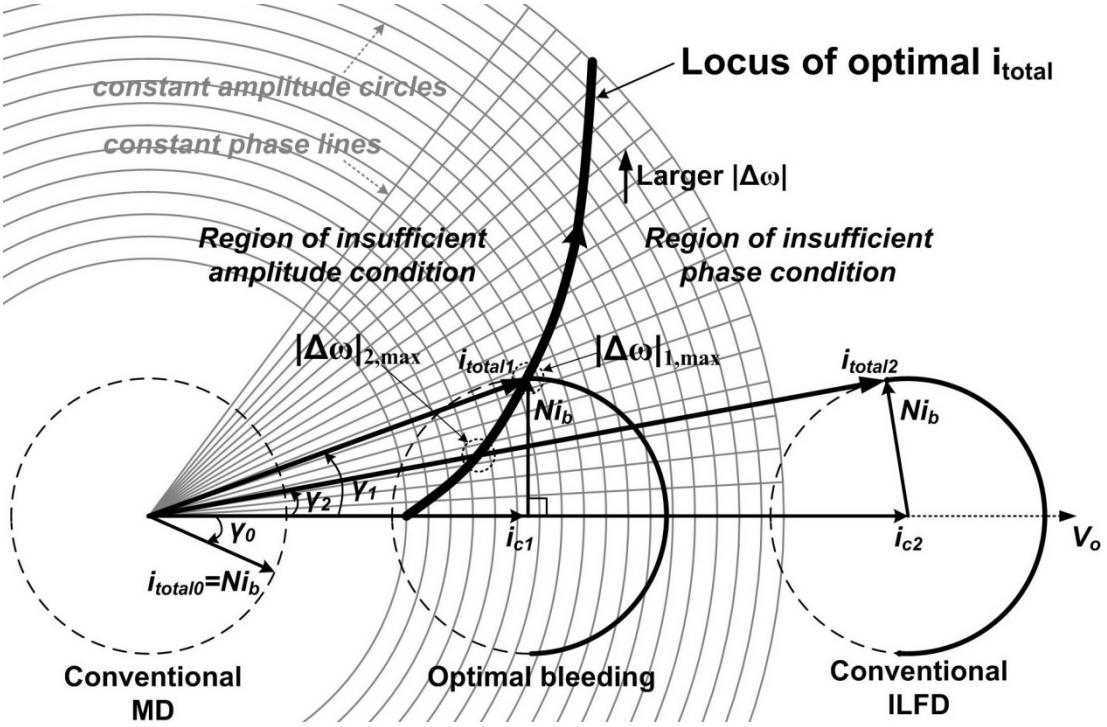


Fig. 5.11 Phasor diagram of the currents injected into the LC-tank

For a given LC-tank and a specified minimum required output amplitude $V_{o,min}$, at the edge of the locking range $\omega_{min/max}$, the minimum required $|i_{total}|$ is $V_{o,min}/|Z(\omega_{min/max})|$, and with such a value as the radius, the constant amplitude circle can be plotted as shown in Fig. 5.11 to specify the minimum required amplitude condition of i_{total}. Similarly, at $\omega_{min/max}$, the minimum required phase shift $|\gamma|$ is equal to

$|\beta(\omega_{min/max})|$, and with such a value as the angle, the constant phase line can be also plotted to specify the minimum required phase condition of i_{total}. As a result, the optimal locus of i_{total} to exactly meet both the amplitude and the phase conditions can be plotted as the bolded curve in Fig. 5.11. At the edge of the locking range, if i_{total} locates in the left region of the optimal locus, the divider has excess phase but insufficient amplitude condition to achieve larger operation range with the required output swing. If i_{total} locates in the right region of the optimal locus, the divider has enough amplitude but insufficient phase condition to achieve larger locking range.

For conventional MDs, the i_{total} locus falls in the insufficient amplitude region in Fig. 5.11. To improve the divider's output amplitude, $|i_b|$ needs to be increased at the expense of larger biasing current or larger input swing. On the other hand, by introducing i_c, the current-bleeding can effectively improve the amplitude condition and optimize the locking range of MD. If the bleeding current is too much, the MD actually would work similarly as conventional ILFD, and the locking range would be limited by the insufficient phase condition. It is interesting to note that for ILFDs, because of the single-end input, the coefficient N in front of $|i_b|$ is equal to 1, while for MDs, the radius of the locus circle is doubled as $2|i_b|$ (N=2) due to the differential input, which indicates ILFD has a smaller achievable locking range compared to the current-bleeding MD.

Without loss of generality, the injected ac current $i_{inj}(2\omega)$ can be expressed as

$$i_{inj}(2\omega) = I_{inj} \cos 2\omega t \tag{5.1}$$

with an initial phase of zero. Similarly, the output voltage $v_o(\omega)$ can be defined as

$$v_o(\omega) = V_o \cos(\omega t + \varphi) \tag{5.2}$$

where φ is the phase of $v_o(\omega)$.

Assuming that the output amplitude V_o is large enough to make the transistors $M_{2\text{-}3}$ in Fig. 5.7 or $M_{3\text{-}6}$ in Fig. 5.10 operate as hard switches, and the offset frequency $|\Delta\omega|$ ($\Delta\omega=\omega-\omega_0$) is small compared to ω_0, the total current injected into the LC-tank $i_{total}(\omega)$ can be derived as

$$i_{total}(\omega) = \mathrm{Re}\left\{\frac{4}{\pi} I_{inj} e^{j(\omega t+\varphi)} \left(\frac{1}{\eta} + \frac{N}{2} e^{-j2\varphi} - \frac{N}{6} e^{j2\varphi}\right)\right\} \tag{5.3}$$

where η is the effective current injection ratio, defined as $I_{inj}/I_{DC,effective}$ ($I_{DC,effective}$ is equal to $I_{DC}-I_{bleed}$ for ILFD, and I_{bleed} for MD). The amplitude and phase conditions as discussed above can be derived and simplified to an inequality and an equation, respectively, as below

$$\frac{4}{\pi} I_{inj} R \left(\frac{1}{\eta} + \frac{N}{3}\cos 2\varphi\right) \geq V_{o,min} \tag{5.4a}$$

$$\Delta\omega = -\frac{\omega_0}{Q} \frac{2\eta \sin 2\varphi}{3 + N\eta\cos 2\varphi} \tag{5.4b}$$

where Q is the tank's quality factor, equal to $R/(\omega L)$.

By solving $\cos 2\varphi$ from Eq. (5.4b) and putting it back into the inequality (5.4a), it can be shown that when $\cos 2\varphi=0$, the maximum lock range (LR_{max}) can be achieved, as

$$LR_{max} = 2|\Delta\omega| = \frac{8N}{3\pi} \frac{\omega_0}{Q} \frac{I_{inj} R}{V_{o,min}} \tag{5.5}$$

Intuitively, the vector "Ni_b" in Fig. 5.11 is composed by two vectors expressed by the terms of "$(N/2)e^{-j2\varphi}$" and "$-(N/6)e^{j2\varphi}$" in Eq. (5.3). With φ changing, the locus of "Ni_b" is more like an ellipse instead of a circle as plotted in Fig. 5.11. When $\cos 2\varphi=0$, $2\varphi=\pm\pi/2$, the two vectors expressed by the terms of "$(N/2)e^{-j2\varphi}$" and "$-(N/3)e^{j2\varphi}$" in Eq. (5.3) are exactly in phase and thereby $N|i_b|$ is maximized. With the vector "Ni_b" in vertical with a proper "i_{c1}", the composed vector "i_{total1}" is able to reach the highest

point of the optimal locus. As a result, the locking range of the divider can be maximized.

The optimal $I_{DC,effective}$ can be derived as

$$I_{DC,opt} = \frac{\pi}{4}\frac{V_{o,min}}{R} \tag{5.6}$$

Interestingly, the expression of $I_{DC,opt}$ is independent of the magnitude of the injected ac current I_{inj}. Moreover, it is exactly the same as the expression for the bias current of a LC-oscillator to obtain a given output amplitude of $V_{o,min}$.

To verify the analysis results, an LC-tank is designed with ω_0 equal to 3.7GHz for an ILFD. Under different values of I_{inj}, the bias current $I_{DC,effective}$ is varied to find out the optimal biasing current $I_{DC,opt}$ such that the divider's locking range is maximized and at the same time the output amplitude is no less than $V_{o,min}$.

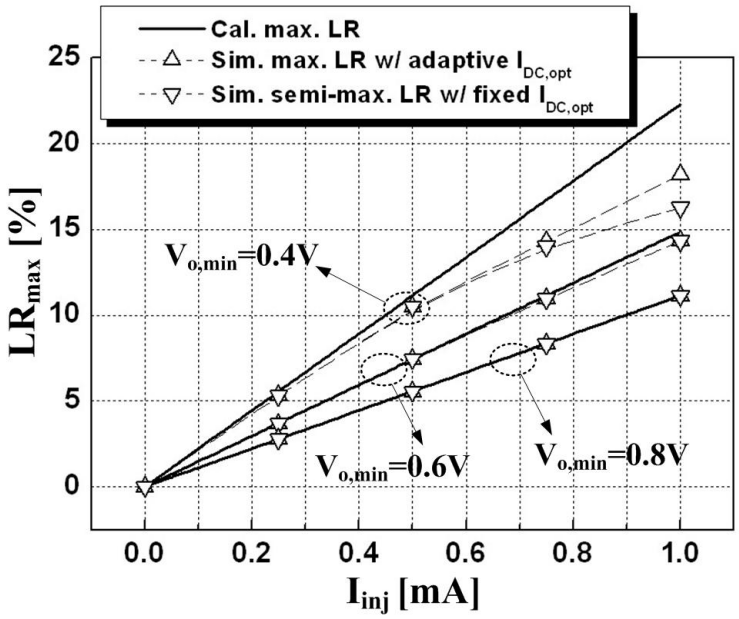


Fig. 5.12 Calculated and simulated LR_{max} of an optimized 7GHz ILFD

Fig. 5.12 shows the calculated, the simulated maximum and the simulated semi-maximum locking ranges using a 0.13μm CMOS process**.** The simulated maximum LR is obtained with adaptively tuning $I_{DC,opt}$, and the simulated

semi-maximum LR is obtained with a fixed $I_{DC,opt}$ wherein the self-oscillation amplitude of the divider is equal to $V_{o,min}$. Fig. 5.12 shows that the calculated LR_{max} using Eq. (5.5) can agree well with the simulated results, especially when the ILFD's output amplitude is large and the switching transistors operate more like hard switches. The locking range obtained with the fixed $I_{DC,opt}$ is very close to the one with adaptive $I_{DC,opt}$.

A current-bleeding MD is also designed and simulated with higher input frequencies around 60GHz. When ideal switches are used as transistors M_{3-6} in Fig. 5.10, the simulated LR_{max} and $I_{bleed,opt}$ (or $I_{DC,opt}$) are accurately predicted by Eqs. (5.5) and (5.6), respectively. However, in transistor-level simulations, the results do not agree as well because the assumption that the transistors M_{3-6} operating as hard switches is not quite valid when the operation frequency is very high and approaching close to transistor's cut-off frequency ω_T. Nevertheless, an extra coefficient Γ can be added into Eq. (5.5) to model how far away the operation of the transistors M_{3-6} is from hard switching. As such, Eq. (5.5) can be rewritten as

$$LR_{max} = \frac{8N}{3\pi}\Gamma\frac{\omega_0}{Q}\frac{I_{inj}R}{V_{o,min}} \tag{5.7}$$

where Γ is close to 1 when the operation frequency is well below ω_T and decreases with increasing operation frequency.

Fig. 5.13 shows the simulated locking range as a function of I_{bleed}. When I_{bleed} is increased from zero to I_{dc}, at the beginning because the amplitude condition is improved, the locking range is increased. When I_{bleed} gets larger than a certain value, the phase condition becomes degraded and eventually limits the operation of the MD. Consequently, the locking range becomes decreased with increasing I_{bleed}. To achieve maximum locking range at different I_{inj}, I_{bleed} can be simply designed to be fixed at

$I_{bleed,opt}$ as plotted in Fig. 5.13, and $I_{bleed,opt}$ can be easily designed so as to make the divider's self-oscillation amplitude equal to $V_{o,min}$.

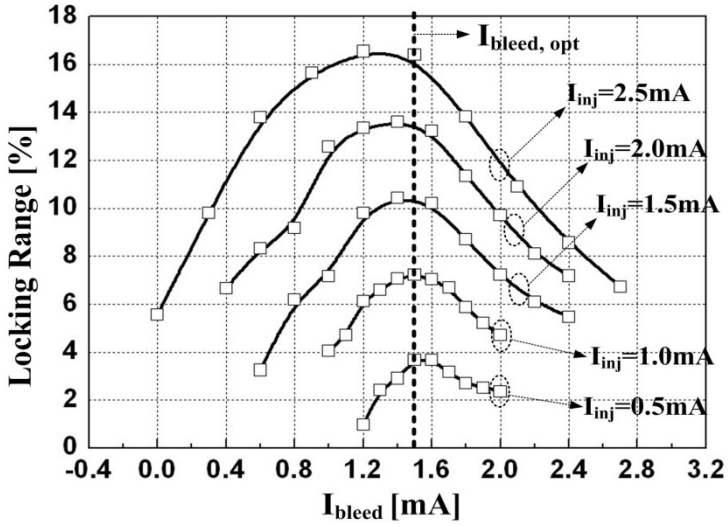


Fig. 5.13 Simulated locking range versus I_{bleed}

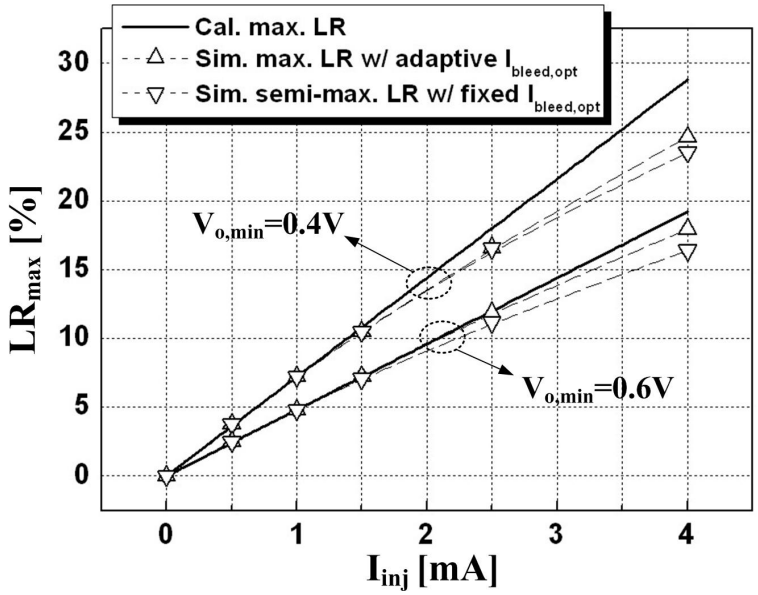


Fig. 5.14 Calculated and simulated LR_{max} of the proposed MD

Fig. 5.14 shows the calculated, the simulated maximum and the simulated semi-maximum locking ranges, where Γ is equal to 0.5 for the used 0.13μm CMOS process when the MD's input frequency is around 60GHz**.** It can be seen that the calculated LR_{max} using Eq. (5.7) can well predict the simulated results especially when

injection ratio η is small, and that the locking range obtained with the fixed $I_{bleed,opt}$ is close to the one with adaptive $I_{bleed,opt}$.

Putting Eq. (5.6) into Eq. (5.5), the LR_{max} of the current-bleeding MD can be rewritten as

$$LR_{max} = \frac{4}{3}\frac{\omega_0}{Q}\eta \tag{5.8}$$

which is double of the ILFD's locking range as derived in [61], showing that with optimal current bleeding, the differential-input MD can indeed achieve much larger locking range compared to the single-ended-input ILFD.

From the amplitude and phase conditions (5.4a) and (5.4b), the locking range of the conventional MD can be also obtained by using $\eta \rightarrow \infty$, as

$$LR_{conv.MD} = 2\frac{\omega_0}{Q}\sqrt{(\frac{8}{3\pi}\frac{I_{inj}R}{V_{o,min}})^2 - 1} \tag{5.9}$$

in which the term $(8I_{inj}R)/(3\pi V_{o,min})$ needs to be larger than unity. Comparing Eq. (5.9) with Eq. (5.5), it can be seen that the bleeding technique can provide significant locking range improvement, especially at high operation frequencies when R is so small that the term $(8I_{inj}R)/(3\pi V_{o,min})$ is comparable to 1 and the locking range of the conventional MD approaches zero.

5.4.2 Design Considerations for Maximum Locking Range

The expression of the maximum locking range, Eq. (5.7), can be rewritten in percentage, as

$$LR_{max}[\%] = \frac{8N}{3\pi}\Gamma\frac{I_{inj}}{V_{o,min}}\sqrt{\frac{L}{C}} \times 100 \tag{5.10}$$

Eq. (5.10) reveals lots of information about the maximum achievable locking range of LC-based frequency dividers, with the optimal current bleeding.

1. LR_{max}[%] is proportional to the number of properly injected (ac) current signals (here "properly" means the induced current i_b by the number of injected (ac) signals needs to be in phase), thereby, differential input MD has 2x LR_{max}[%] than single-end input ILFD.
2. LR_{max}[%] is proportional to the switching coefficient "Γ". At higher operation frequency ω, for devices under given technology, because Γ is lower, achievable LR_{max}[%] is smaller.
3. LR_{max}[%] is proportional to the strength of injected (ac) current signal, so the current-reusing technique helps further improve the locking range of the proposed ILFD.
4. LR_{max}[%] is inversely proportional to the required minimum output amplitude of the divider. This is true because the output amplitude V_o or the amplitude condition can be always traded off for phase condition, thereby, the locking range can be improved. It must be noticed that this conclusion is only true when the open loop gain is larger than 1, which is the gain condition. Also, when V_o is not sufficiently large, as the transistors operate further away from "hard-switching", Γ would decrease.
5. LR_{max}[%] is proportional to sqrt(L/C), so at given ω, it is beneficial to minimize C and maximize L.
6. LR_{max}[%] is not related to tank's Q. This is because at higher tank's Q, although the required phase shift needs to be larger to achieve a given locking range, because the tank impedance is also larger, the effective DC biasing current $I_{DC,effective}$ can be reduced for a given divider's output amplitude, thereby, the injection ratio η can be improved, and thus the provided phase shift is larger, as a result, LR_{max}[%] stays the same with current bleeding technique to optimize the

divider's operation. To verify this conclusion, the maximum locking ranges of the 7GHz input ILFD are simulated at different values of the tank Qs. As shown in Fig. 5.15, at I_{inj} of 0.5mA, 1mA or 1.5mA, the maximum locking range is almost unchanged when the tank Q varies from 3 to 8. And the simulated LR_{max} is consistent with the calculated value especially when the LR is not large so that the "narrow band" assumption made at the beginning of the analysis is true. It can be seen that, the conventional method to improve the locking range of ILFD through decreasing the tank Q, is not wise because by doing so, the output swing of the ILFD is sacrificed. For the output swing constrained locking range optimization, the achievable LR_{max} is actually independent of the tank Q.

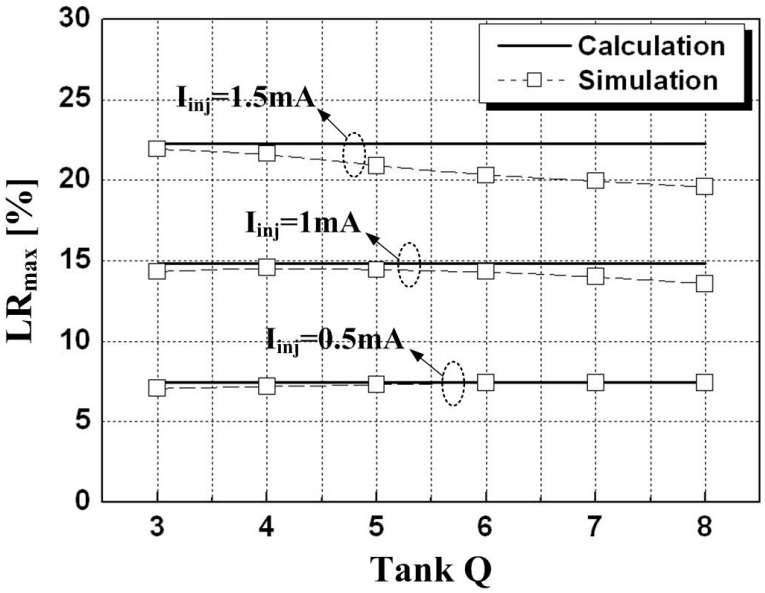


Fig. 5.15 Calculated and simulated LR_{max} of the 7GHz ILFD at different tank's Q.

5.5 Experimental Results

5.5.1 7GHz and 60GHz CR-ILFDs

Two dividers with the same topology shown in Fig. 5.7(c) are designed and fabricated in 0.13μm CMOS process ($V_{th,n} \approx 0.4V$, $|V_{th,p}| \approx 0.3V$). The first divider is

designed to operate around 7GHz, in which the transistors M_3 and M_4 are biased in Class-AB mode to provide the required bias current with small W/L sizes. The shunted dc current through M_4 is designed as large as possible to maximize the trans-conductance of M_4 while leaving enough dc current through M_1 and M_2 for the divider's self-oscillation, which is necessary to guarantee the ILFD to operate with a lower power compared to that of a Miller divider. To further demonstrate the feasibility of the proposed technique for wide range of frequencies and applications, a second divider is designed to operate around 60GHz. Fig. 5.16 shows the die photographs of the two proposed ILFDs, which occupy active area of 0.033mm^2 and 0.0165mm^2, respectively.

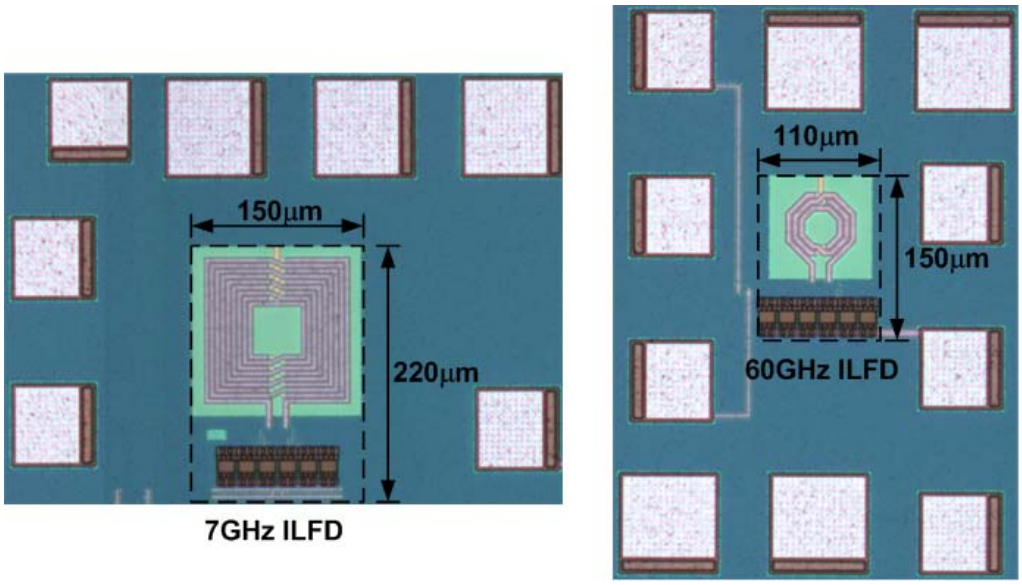


Fig. 5.16 Die photographs of the CR-ILFDs

Fig. 5.17 shows the measured input sensitivity curves of the 7GHz ILFD under different bias conditions. Operated with a 1.1mA current from a 0.8V supply voltage and a 0dBm input signal, the divider measures a locking range of 12.8% from 6.65GHz to 7.56GHz when the PMOS is turned off. A much improved locking range of 33.6% from 6.02GHz to 8.45GHz is measured when the PMOS is turned on. As the

supply voltage is increased to 1.2V, the divider measures locking ranges of 14.6% from 6.52GHz to 7.55GHz and of 45.2% from 5.45GHz to 8.63GHz when the PMOS is disabled and enabled, respectively. When the input power is 6dBm and the supply voltage is 1.2V, the maximum locking range with the PMOS enabled is up to 50%, which is about three times larger than that without the PMOS.

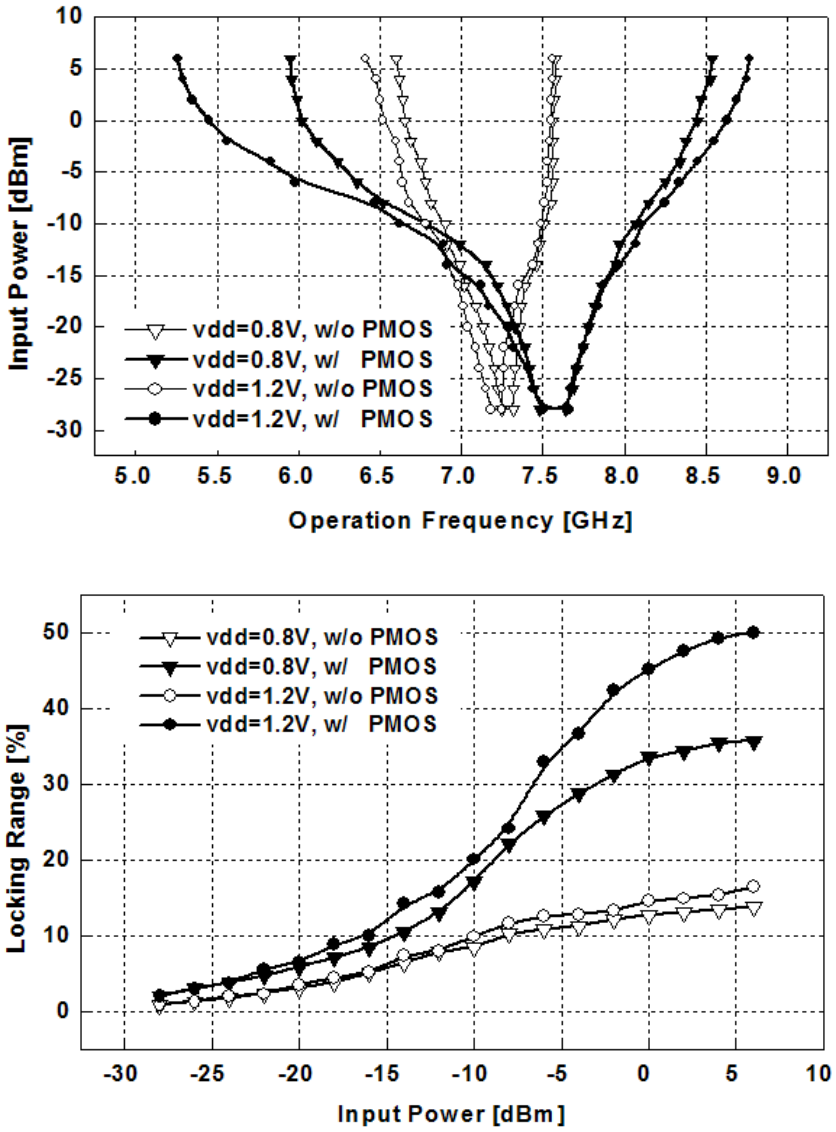


Fig. 5.17 Measured sensitive curves and locking ranges of the 7GHz ILFD under different bias conditions.

Fig. 5.18 shows measured input sensitivity curves of the 60-GHz ILFD. The divider draws only 2mA from a 0.8V supply voltage. With 0dBm input power, the

divider measures a locking range of 6.5% from 59.93GHz to 63.97GHz with the PMOS disabled. When the PMOS is enabled, the divider's locking range is extended to 11.6% from 59.6GHz to 66.96GHz. The improvement in the locking range for the 60-GHz divider is smaller as compared to that of the 7-GHz divider because the parasitic capacitance contributed by the PMOS becomes more significant at higher input frequencies. Inductive peaking could be applied to cancel the parasitic capacitance and improve the locking range further at the expense of larger chip area.

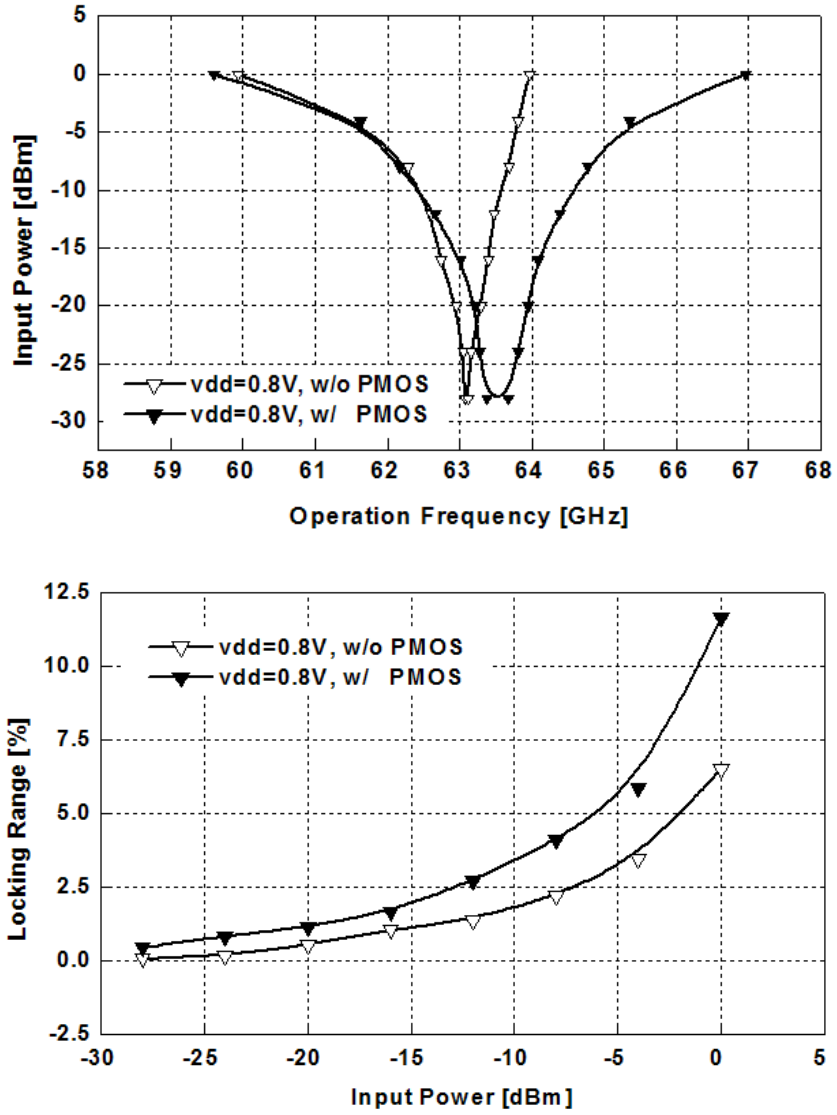


Fig. 5.18 Measured sensitive curves and locking ranges of the 60-GHz ILFD under different bias conditions.

5.5.2 60GHz CB-MD

The current-bleeding MD shown in Fig. 5.10 is also designed and fabricated in the 0.13μm CMOS process. For testing purpose, a transformer T_1 is employed as an on-chip balun to convert single-ended input signal to differential signals for the divider. Fig. 5.19 shows the die-photo of the Miller divider, which occupies an active area of 0.007mm^2.

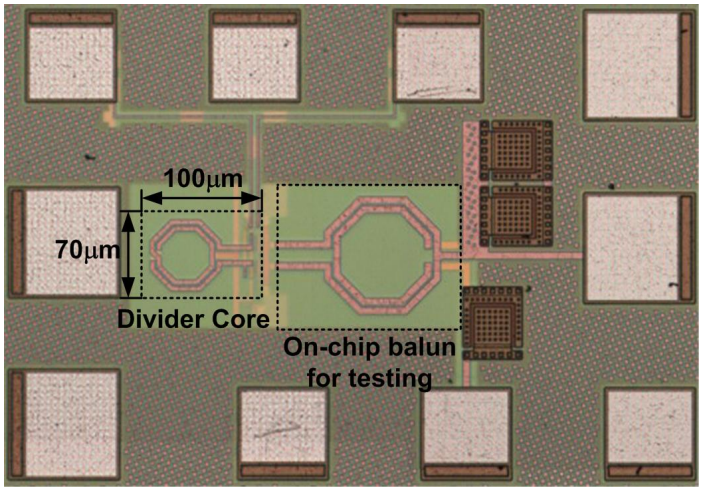


Fig. 5.19 Die photograph of the Miller divider

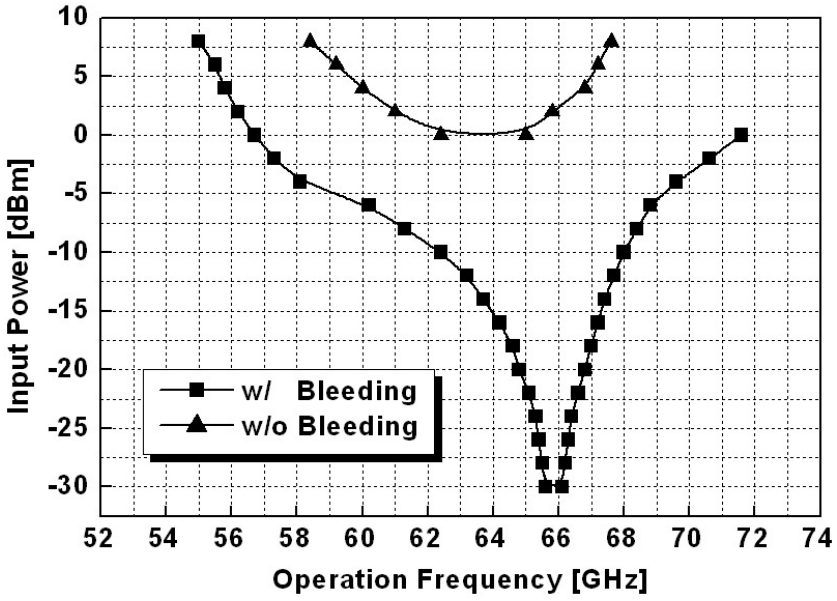


Fig. 5.20 Measured sensitive curves of CB-MD w/ and w/o the current bleeding

Fig. 5.20 shows the measured input sensitivity curves. At a 0.8V supply voltage and with 0dBm input power, the divider measures a locking range of from 56.7GHz to 71.6GHz with the current-bleeding enabled. When the input power is further increased, the minimum operation frequency is measured to be 55GHz while the maximum frequency cannot be measured due to the limitation of testing equipment. For comparison purpose, the current-bleeding is disabled by turning off the transistor M_7, and the divider fails to function for input power less than 0dBm. For 0dBm input power, the divider with the current bleeding disabled can only achieve a narrow locking range from 62.4GHz to 65GHz.

Fig. 5.21 plots the measured locking range and corresponding power consumption of the divider for different input powers. With input power of 0dBm, the divider measures locking ranges of 23.2% and 4.1% with the current-bleeding enabled and disabled, respectively, while consuming the same power of 5mW.

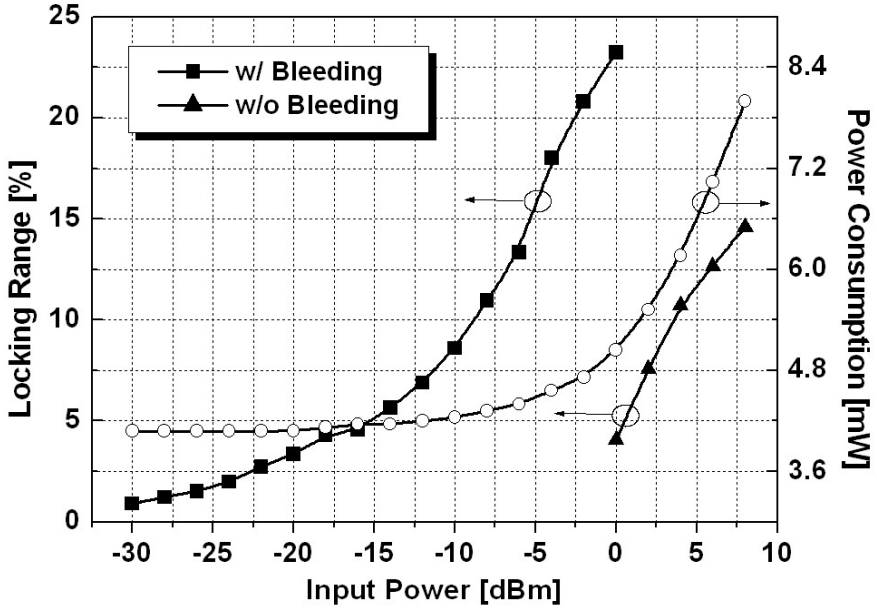


Fig. 5.21 Measured locking range and power consumption of the Miller divider

Table 5.1 summarizes the measured performance of the proposed ILFDs and MD and compares with that of the reported state-of-the-art wide-locking-range dividers.

Table 5.1 Performance summary and comparison of high frequency dividers

Ref.	Technology	Freq. [GHz]	Input Power [dBm]	Locking range [GHz]/[%]	Supply Voltage [V]	Power consumption [mW]	FOM[2]
[65]	65nm SOI CMOS	91	0	10/11.0	2.2	52.4	0.19
[66]	65nm SOI CMOS	85	-5	18.4/21.6	2.4	64.9	0.28
[56]	90nm CMOS	20	4	5.1/25.5	1.2	3.2[1]	1.6
[57]	90nm CMOS	57	0	7.4/13.0	-	2.5[1]	3.0
[59]	0.18μm CMOS	40	0	10.6/26.5	1.0	6	1.8
[60]	90nm CMOS	90	0	11/12.2	1.2	3.5	3.1
1st ILFD	0.13μm CMOS	7	0	2.4/34.3	0.8	0.9	2.7
2nd ILFD	0.13μm CMOS	63	0	7.4/11.7	0.8	1.6	4.6
Miller Divider	0.13μm CMOS	64	0	14.9/23.2	0.8	5	3.0

1. Half of the power reported for the quadrature-output divider

2. FOM=Locking range [GHz] / Power consumption [mW]

Chapter 6

Frequency Synthesis for 14-Band OFDM UWB

6.1 Introduction

FCC defines any radio technology that occupies spectrum more than 20 percentages of the carrier frequency or above a minimum value of 500MHz, to be ultra wideband (UWB). An unlicensed band from 3.1GHz to 10.6GHz is allocated by FCC for different UWB applications. There are two popular approaches that can be made use of to implement a UWB radio. One is called impulse radio technique based on single carrier. It transmits signals by modulating the phase of a very narrow pulse. This approach simplifies the transmitter design but suffers several disadvantages. At first, it is difficult to generate Giga-Hert bandwidth narrow impulse signals that efficiently fit the spectrum mask required by FCC. Secondly, the short time duration makes the receiver's signal processing very sensitive to timing jitter and group delay of the front end circuits. And the spectrum resources are quite wasted for this approach in order to avoid the narrow band interference with other existing narrow band systems [67]. Another UWB approach is the multi-carrier radio technique. It transmits OFDM signals simultaneously over multiple carriers spaced apart at precise frequencies. This approach has better spectrum flexibility and is less sensitive to RF interference and multi-path effects [67]. Moreover, since OFDM modulations are widely used by many other wireless standards, the MB-OFDM UWB approach is more compatible and more suitable to be integrated in SDRs.

Table 6.1 provides physical band allocations of the MB-OFDM UWB standard.

To support the UWB communications, the SDR FGS needs to generate 14 carrier frequencies from 3432MHz to 10296MHz with 528MHz spacing. And to support the time-frequency interleaving coding applied in the standard, the generated carrier frequency needs to hop fast from one to another within 9.47nS.

Table 6.1 Physical band allocations of MB-OFDM UWB standard

Band Group	BAND_ID	Lower frequency	Center frequency	Upper frequency
1	1	3168 MHz	3432 MHz	3696 MHz
	2	3696 MHz	3960 MHz	4224 MHz
	3	4224 MHz	4488 MHz	4752 MHz
2	4	4752 MHz	5016 MHz	5280 MHz
	5	5280 MHz	5544 MHz	5808 MHz
	6	5808 MHz	6072 MHz	6336 MHz
3	7	6336 MHz	6600 MHz	6864 MHz
	8	6864 MHz	7128 MHz	7392 MHz
	9	7392 MHz	7656 MHz	7920 MHz
4	10	7920 MHz	8184 MHz	8448 MHz
	11	8448 MHz	8712 MHz	8976 MHz
	12	8976 MHz	9240 MHz	9504 MHz
5	13	9504 MHz	9768 MHz	10032 MHz
	14	10032 MHz	10296 MHz	10560 MHz

The stringent frequency hopping time requirement limits the 14-band carrier frequencies to be synthesized in an open-loop manner. Intensive research works have been done to optimize the architecture of MB-OFDM UWB frequency synthesizers [68][69][70][71], however, the most efficient synthesizer reported so far still requires 3 groups of IQ single sideband (SSB) mixers with inductive loading for each SSB mixer to filter out the spurious tones due to the mixing [47], the resulted chip area is quite large, which makes it difficult to integrate the UWB part into the SDR synthesizer. In this chapter, new circuit techniques are presented, including a reconfigurable injection-locking based frequency multiplier, and transformer-based single-coil 3GHz-to-10GHz tunable narrow-band LC-tank for SSB mixers. Only 2 extra inductive coils are required to include the 14-band MB-OFDM UWB

functionality in the SDR FGS. Fig. 6.1 shows the architecture of the 14-band UWB synthesizer integrated into the SDR FGS. The 14 carrier frequencies of MB-OFDM UWB are generated by SSB mixing the center frequency 4224/8448MHz with the offset frequency 264/792/1320/1848MHz. An x3/x5/x7 multi-modulus injection locked frequency multiplier (ILFM) is used to generate all the offset frequencies instead of using SSB mixers, to avoid the need of cascading several SSB mixers, which would not only be susceptible to spur and complicated for IQ generation but also consume high power consumption. In such a scheme, the divider chain can be reused in the UWB mode, providing all the required frequencies for the UWB carrier synthesis.

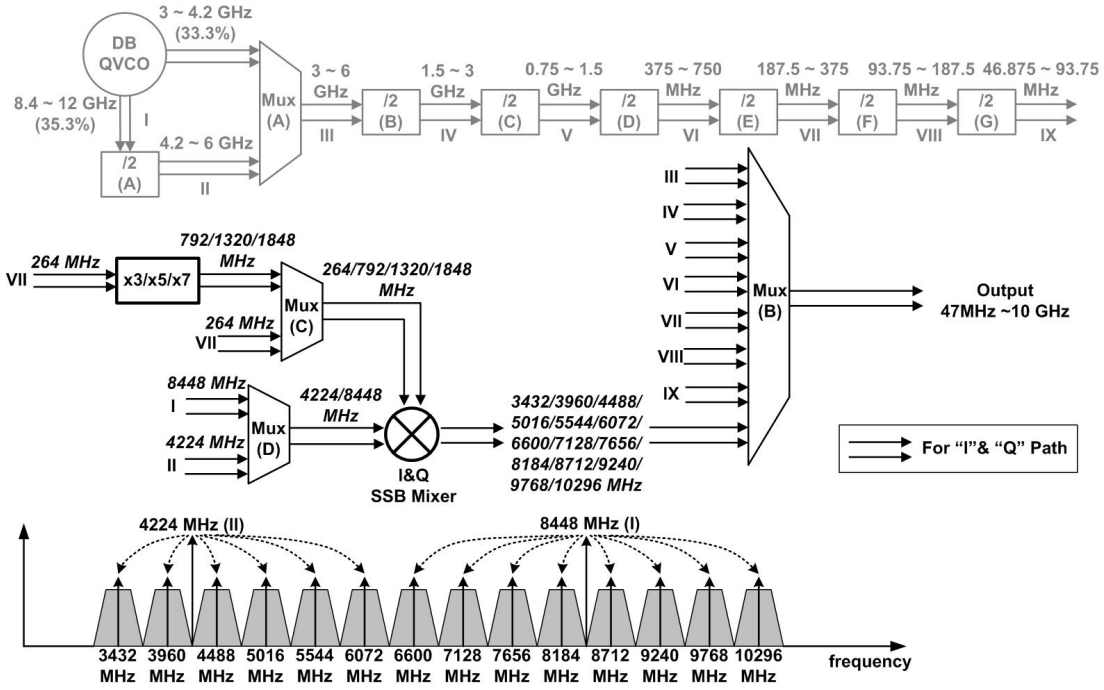


Fig. 6.1 Frequency scheme of 14-band MB-OFDM UWB carrier generation

All the generated IQ signals from Mux-A, divider-B to divider-G and SSB mixers are combined through Mux-B, and the final output signals are selectable from 47MHz to 10GHz. Fig. 6.2 shows the Mux-B circuit, to reduce the cross-talk between building blocks operating at different frequencies, each element of Mux-B

needs to be placed as close as possible to the previous circuit stage, also by doing so, the long lines for signal combining can run in current mode, resulting less power loss compared to the one in voltage mode. As a result, Mux-B is distributed in nature. Cascode circuitry is used to improve the isolation, post-simulations show that the typical isolation value is around 40dB. To achieve better isolation, all the frequency dividers that are not required in a given standard mode can be turned-off completely. For most of the standards, because those dividers operating at lower frequency than the wanted carrier frequency are turned off, the unwanted interfering signals are all at the harmonic frequencies. Except for the "UWB" mode, almost all the dividers have to be turned on. Therefore, special techniques including guard ring and ground shielding are implemented for the associated circuit layout.

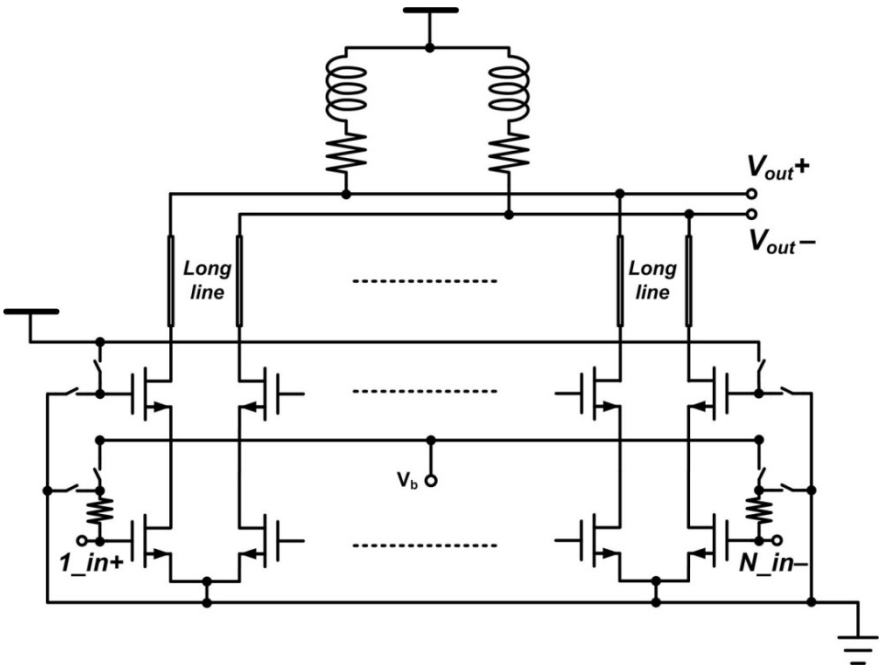


Fig. 6.2 Schematic of Mux-B

6.2 QIQO x3/x5/x7 ILFM

6.2.1 Proposed QIQO x3/x5/x7 ILFM

Fig. 6.3 shows the schematic of the ILFM. The input IQ sinusoidal signals are converted into narrow pulse signals with rich harmonics and then injected into a ring oscillator (RO) to lock its oscillation frequency to the harmonic of the input frequency that is closest to the RO's self-oscillation frequency.

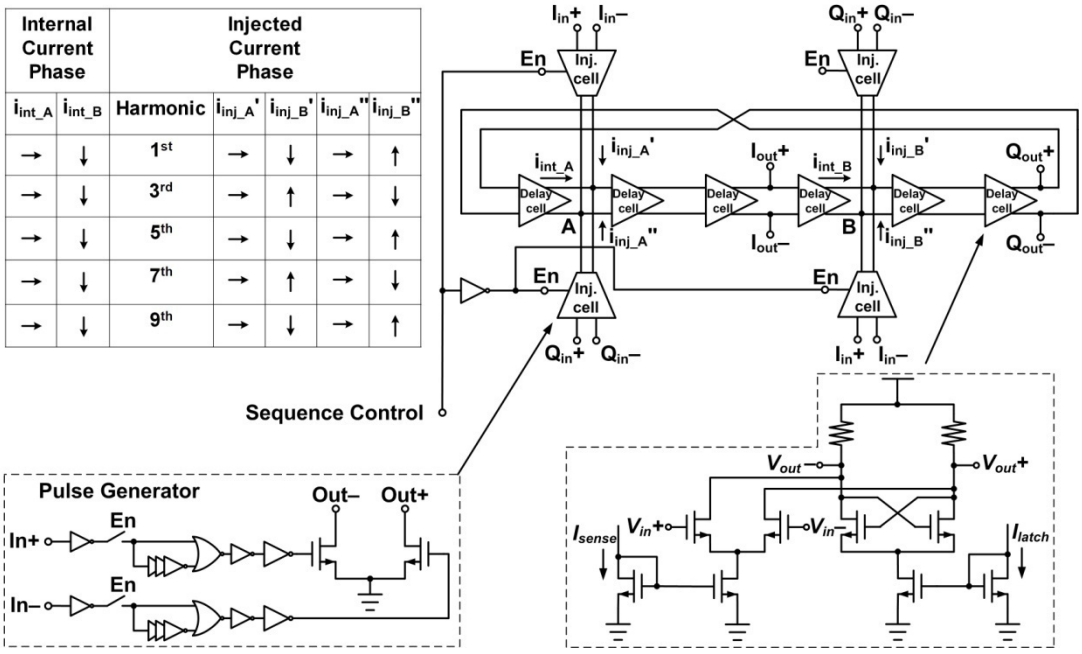


Fig. 6.3 Schematic of x3/x5/x7 QIQO injection-locked frequency multiplier

It can be shown that the RO tends to select the harmonics having consistent phase sequence with its natural phase sequence. For example, when the RO self-oscillates at around 5 times of the input frequency f_{in}, only the two injection cells at the top are enabled, the current i_{inj_A}' and i_{inj_B}' are injected into the RO from Nodes A and B, respectively. For the internal current of the RO, i_{int_A} at Node A leads i_{int_B} at Node B. For the injected current, the 1st, 5th, and 9th harmonics at Node A also lead those at Node B. On the other hand, the 3rd and 7th harmonics at Node A lag those at Node B. As a result, the RO is injection locked to $5f_{in}$, and the injected 3rd and 7th harmonic tones are greatly suppressed by the RO due to the contradicted phase sequence. Moreover, all the even harmonic tones are cancelled out by the differential operation

while all other tones are far enough to be filtered out by the RO. Consequently, only a clean tone at $5f_{in}$ exists at the output of the ILFM. The multiplication ratio 3/5/7 of the ILFM is selected by controlling the biasing current I_{sense} and I_{latch} of the delay cells, as well as enabling and disabling the appropriate injection cells to inject the currents with proper phase sequence.

6.2.2 Experimental Results

The measured spectrums at the ILFM's output with multiplication ratio being 5 are shown in Fig. 6.4, from which the 3rd and 7th harmonics of the input signals are indeed rejected as expected. The largest spurs are the 1st and 9th harmonics, which are more than 30dB lower than the desired tone. For comparison, signals with the reversed phase sequence are intentionally injected, in which case the 3rd and 7th harmonics become much larger with the 3rd harmonic suppression being only 13dBc.

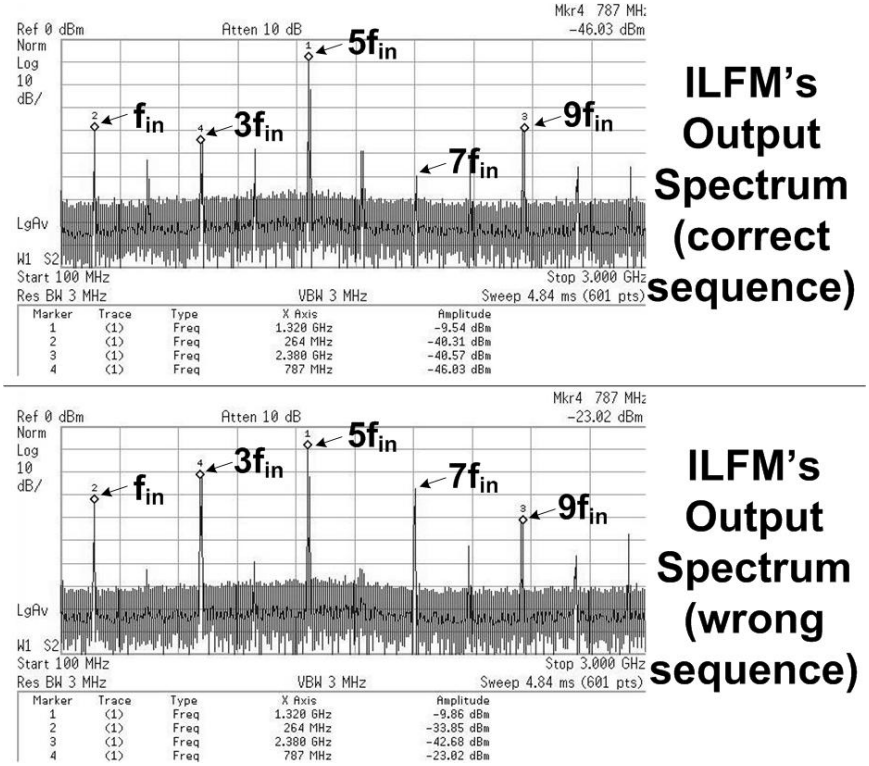


Fig. 6.4 Measured output spectrum of the x3/x5/x7 ILFM

The performance of the QIOQ x3/x5/x7 ILFM is summarized in Table 6.2.

Table 6.2 The performance summary of the QIQO x3/x5/x7 ILFM

Mode	Biasing Current		Locking Range	Power	Spur	Hopping Time
	I_{sense}	I_{latch}				
x3	30uA	50uA	43%	6~8 mW (including Mux-C)	< -30dBc	< 3nS
x5	50uA	40uA	41%			
x7	70uA	20uA	30%			

6.3 3GHz-to-10GHz Single Sideband Mixer

6.3.1 3GHz-to-10GHz Wideband Loading

Fig. 6.5 shows the schematic of the single side-band (SSB) mixer, where the shunt peaking technique is used to enhance the bandwidth of the load impedance. The high frequency input signals are applied at the gates of the bottom transistors as the RF input. While the lower frequency signals are used to switching the upper transistors as the LO input. Fig. 6.6 gives the input phase sequence diagram of two SSB mixers with IQ outputs. It can be seen that the outputs of the IQ SSB mixers can be easily selected to be upper sideband or lower sideband by simply controlling the polarity of quadrature-phase LO signals to be plus or minus.

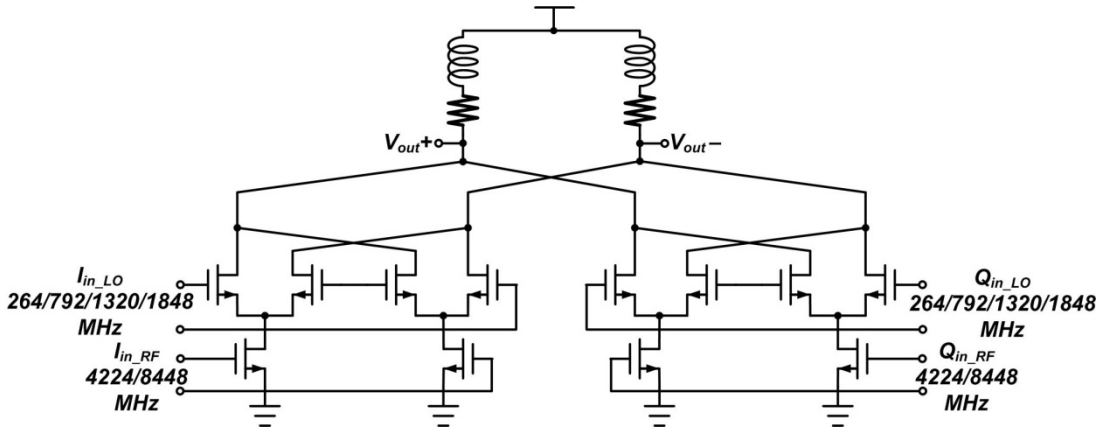


Fig. 6.5 Single sideband mixer with wide-band loading

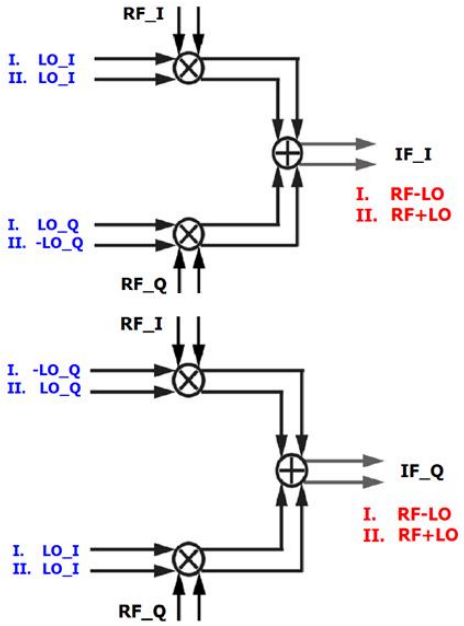


Fig. 6.6 Input phase sequence of IQ SSB Mixers

6.3.2 Proposed 3GHz-to-10GHz Narrow-Band Single-Coil LC-Tank

Although it is convenient to design the shunt peaking wideband load, there is no filtering effect on the spurious tones at the SSB mixer's output. In order to achieve a cleaner spectrum at the mixer's output, a tunable narrow band load can be used instead. This can be done by tuning both of the two peak frequencies in the transformer-based high-order LC tank.

Fig. 6.7 shows the schematic of the SSB mixer with the transformer-based narrow band tunable loading. As discussed in Chapter 4, for the transformer-based LC tank's impedance Z_{22} seen from the secondary coil, the higher frequency peak would dominate when the notch-peak cancellation condition is fulfilled. On the other hand, if the frequency ratio ω_2/ω_1 is not sufficiently large or the coupling coefficient k is high, the lower frequency peak becomes dominant. Based on this property, a transformer with tight coupling is designed, and by controlling the capacitive ratio,

the lower frequency peak or the higher frequency peak can be selected to be dominant and utilized as the loading impedance. To further extend the tuning range, a third capacitor is added inter-between the two inductors, which builds a path to make L_1 in parallel with L_2, if C_3 is increased, the effective L_1 is also increased, as a result, the higher peak frequency is decreased.

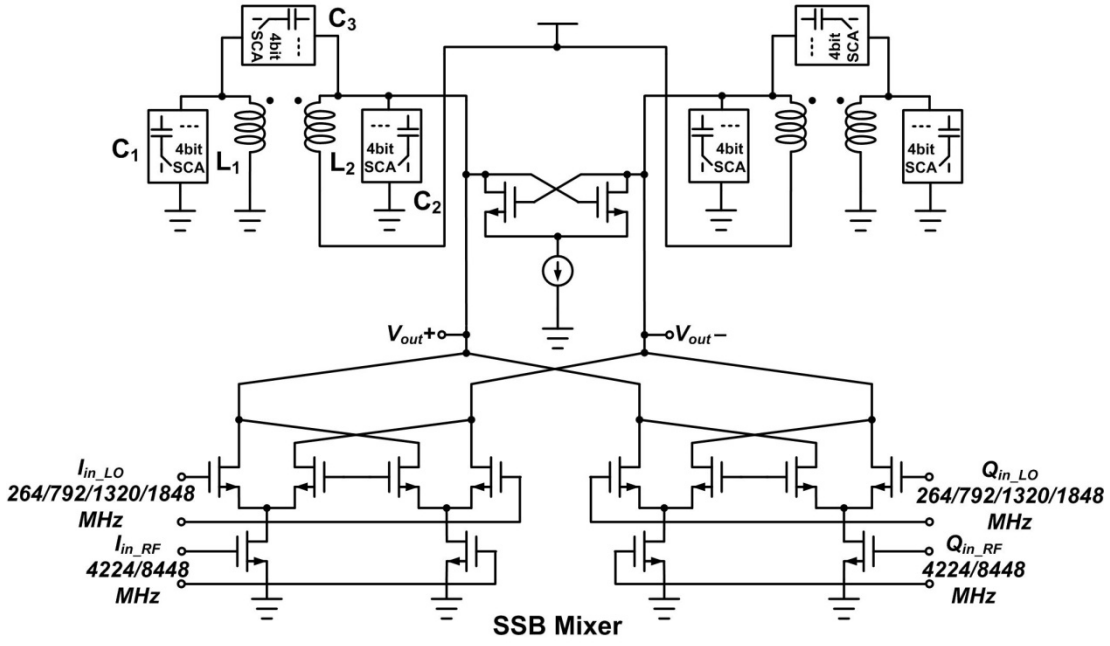


Fig. 6.7 Single sideband mixer with tunable narrow-band loading

Fig. 6.8 shows the frequency tuning response of the transformer-based narrow band LC tank in the post-layout simulations. For clarity, the other unwanted peak is not shown. The desired peak can be tuned from 3.4GHz to 11GHz, fully covering the required range for all 14-band carrier frequency. And by adaptively tuning the current source of the cross-coupling pair in Fig. 6.7, the peak impedance can be compensated to be larger than 300 Ohm.

Since there coexisting two peaks, it is important to properly allocate the unwanted peak such that spurious tone does not fall into the unwanted peak. The image tone due to the IQ mismatch is $2f_{LO}$ away from the desired signal, which is

typically too close-by to be in the unwanted peak. However, the spur due to the harmonic mixing can be $4f_{LO}$ from the desired frequency, and if the mixer operates closely to hard-switching, this spurious tone could be only 9.5dB lower compared to the desired tone, which is significantly large. Therefore in the mixer design, the harmonic mixing spur is reduced by controlling the unwanted peak frequency to not to overlap with the spurious frequency, and also by intentionally operating the switch more softly at the expense of reduced conversion gain.

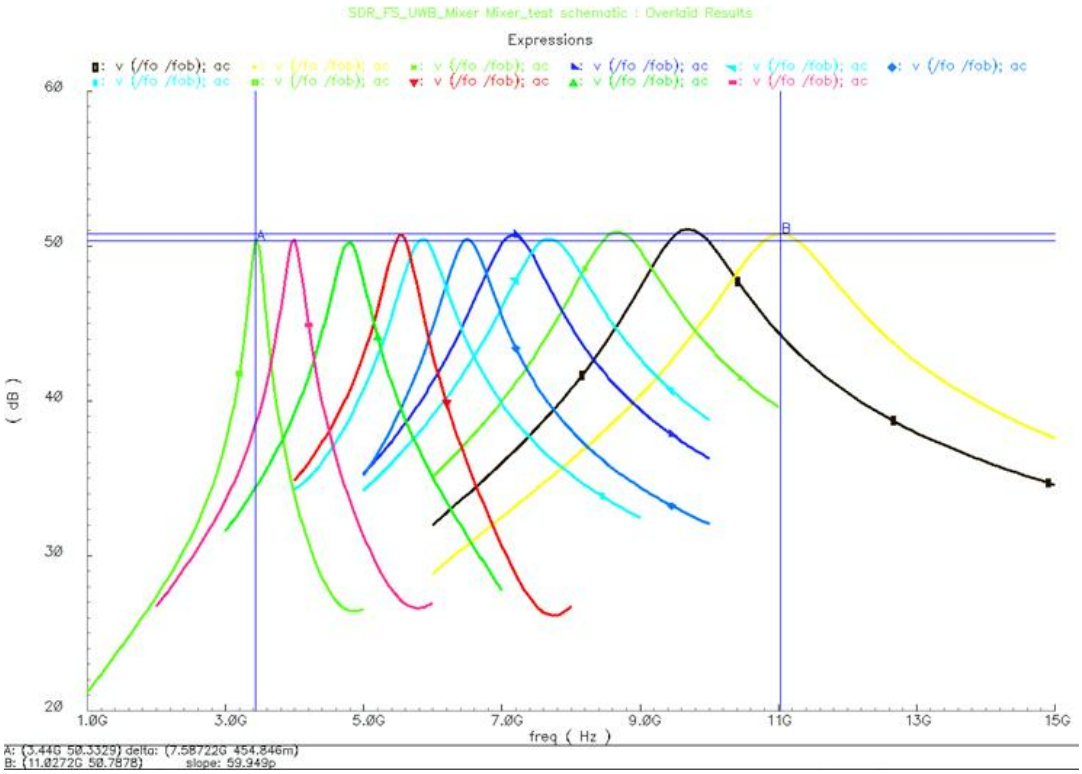


Fig. 6.8 Frequency tuning response of the transformer-based LC-tank

6.3.3 Experimental Results

In the measurement, the desired peak frequency of the proposed tunable narrow-band LC-tank is verified by providing sufficient biasing current for the cross-coupled pair to make the resonator oscillate. The measured tuning range is from 3.3GHz to 10.5GHz, which is very close to the post-simulation results.

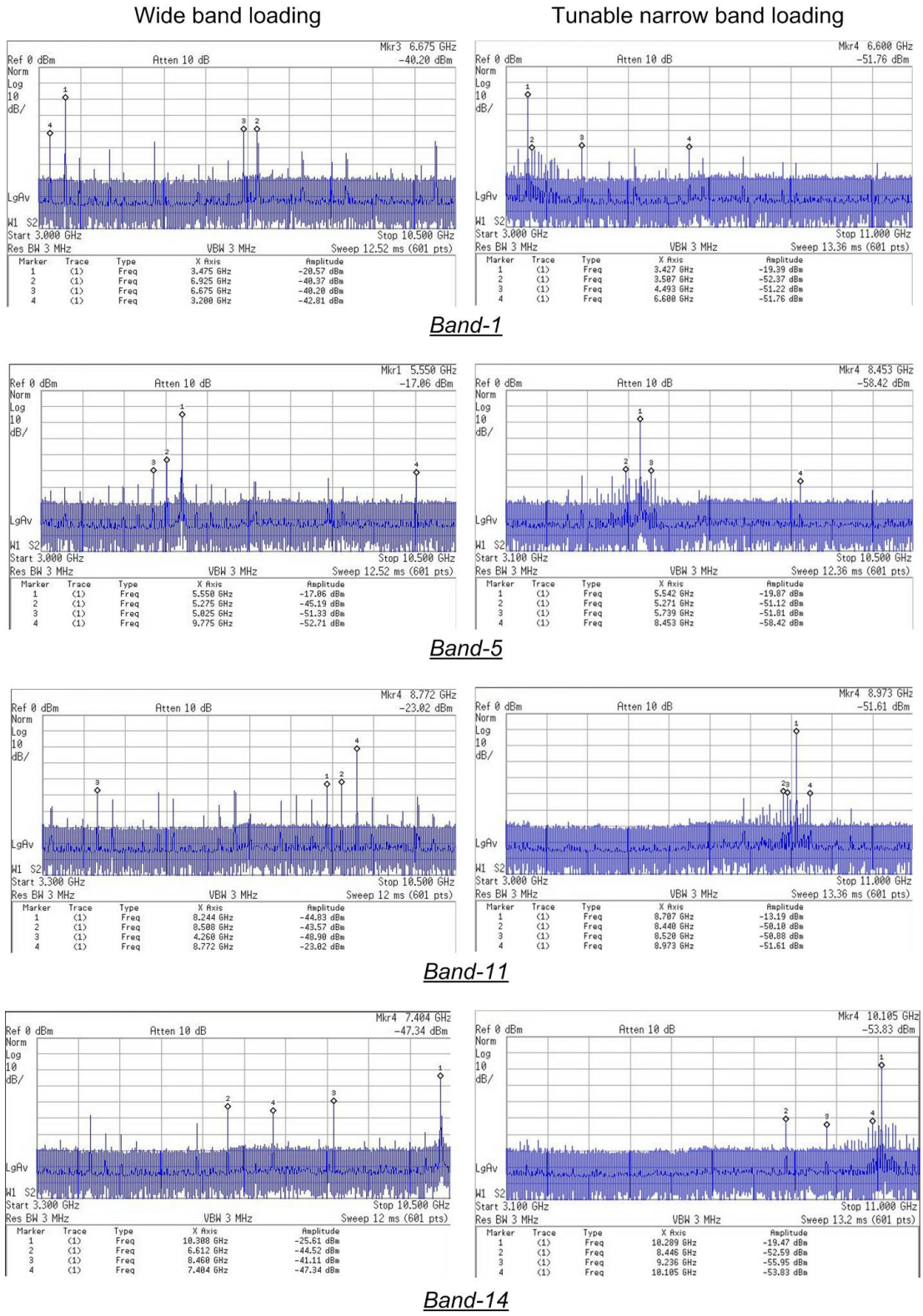


Fig. 6.9 Measured MB-OFDM synthesizer's output spectrum with wide-band loading SSB mixer and tunable narrow-band loading SSB mixer

Fig. 6.9 shows the measured spectrums of the MB-OFDM UWB synthesizer

integrated in the SDR FSG. It can be clearly seen that the proposed narrow band tuning technique improves the spectrum purity significantly. Without narrow band filtering, the spur is mainly contributed by the harmonic mixing tones, while with the narrow-band loading, because the far-away spurs are greatly filtered out, the SFDR is mainly dominated by the near-by tones, which is contributed by the ILFM.

Fig. 6.10 summarizes and compares the spur rejection performance of UWB synthesizers employing the two kinds of SSB mixers. With the wideband loading SSB mixers, the maximum spurious tone varies from -15dBc to -28.1dBc. With the proposed single coil tunable narrow-band LC-tank, the synthesizer achieves spur rejection from 31.3dB to 41.5dB at the 14-band carrier frequencies spanning from 3.432GHz to 10.296GHz.

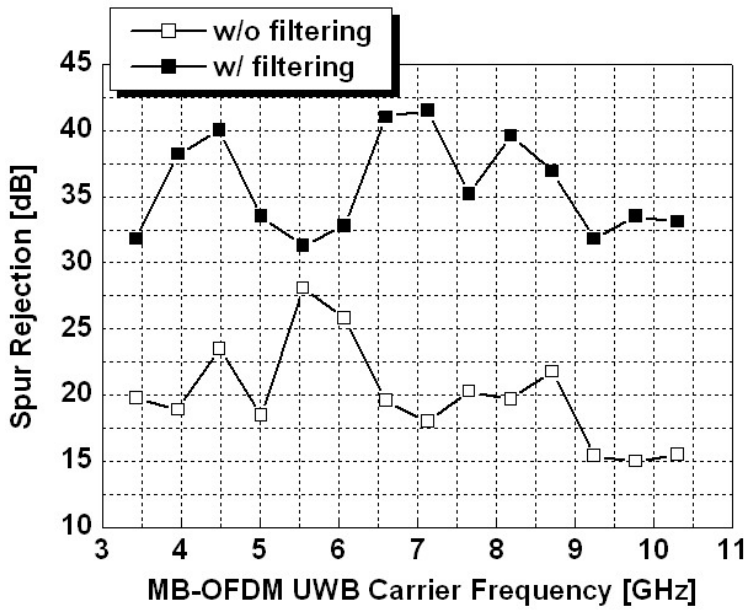


Fig. 6.10 Spur rejections of MB-OFDM UWB synthesizers using wideband SSB mixer and narrow-band SSB mixer

From Fig. 6.10 it is observed that two curves do not follow closely to each other, and the spur rejection improvement by the narrow band filtering varies at different frequencies. The absolute improvement value is determined by two factors. The first

one is the frequency location of the most dominant spur. And the second one is the tank Q or the shaping quality of the transformer based LC tank at the desired peak frequency. For the designed transformer-based LC tank, to make use of the lower frequency peak, all the switched capacitors at the secondary coil needs to be tuned on to suppress the higher frequency peak, and the lower frequency peak is tunable from 3.4GHz to 5GHz with adjusting the SCA at the primary coil. While to make use of the higher frequency peak, all the switched capacitors at the primary coil needs to be tuned on to suppress the lower frequency peak, and the higher frequency peak is tunable from 6GHz to 10.5GHz with adjusting both the SCA at the secondary coil and the SCA between the primary coil and the secondary coil. To cover the frequency band around 5.5GHz, not only the SCA at the primary coil but also the SCA at secondary coil need to be turned off, to increase the lower peak frequency to 5.5GHz. However, the tank Q at this frequency band is degraded compared to that at the other frequency bands. As a result, at the frequency around 5.5GHz, because the most dominant spur is only 264MHz from the desired signal, LC tank cannot filter the spur much. And also because the tank Q is relatively lower as discussed above, the spur rejection is least significantly improved at this frequency as shown in Fig. 6.10.

Chapter 7

Millimeter-Wave Frequency Generation

7.1 Challenges of VCO at Millimeter-Wave Frequency

The scaling of the CMOS technology makes it possible to integrate the VCOs at MM-Wave frequency on chip [72]. But the design of VCOs also becomes much more challenging when the operation frequency is increased from several GHz to tens of GHz.

Firstly, the start-up condition of the MM-Wave oscillator becomes worse. This is because with a given process, as the total parasitic capacitance contributed from the transistors and running lines is typically fixed at certain level. In order to increase the oscillation to tens of GHz, the inductor of the MM-Wave VCO needs to be much scaled compared to the RF VCO. Consequently, the impedance of the LC tank is much reduced. As a result, much larger power and larger transistor size need to be used to make the VCO oscillate. The latter would further increase the parasitic capacitance.

Secondly, as the frequency increases, the Q of the capacitor becomes worse and it is turned out that at 60GHz, the capacitor's Q dominates the total Q of the LC tank. This results the difficulty of the frequency tuning for MM-Wave VCOs. As for the RF VCOs, the fine and coarse frequency tuning are done by tuning varactors and switching capacitors, respectively. However, at MM-Wave frequency, in order to make the Q of the switched capacitor reasonable, the switch needs to be significantly large to minimize the turn-on resistance, consequently, when the switch is turned off, the parasitic capacitance of the switch becomes close to the switch capacitance, which

results the effective capacitance does not change when the switch is turned on or off. Consequently, only varactor-tuning is a feasible method at MM-Wave frequency.

Thirdly, compared to the RF VCOs, the spectrum purity of MMW VCOs are much degraded due to the inferior Q of the varactors at high frequencies and the serious AM-PM noise transformation caused by the large VCO gain on the order of GHz/V [73]. Moreover, the serious trade-off between varactor's tuning ratio and Q [74] and the reduced supply voltage in deep sub-micron CMOS technologies make the varactor-tuning method less effective for MMW VCOs.

Fourthly, at MMW the IQ generation manner through frequency dividing becomes not desirable, because the expense of the doubling the VCO's operation frequency is too much and high frequency dividers are also very challenging to design with sufficient locking range to cover the VCO's tuning range. Thereby, MMW VCOs are preferred to generate multiphase output signals in order to support in-phase and quadrature-phase (IQ) modulation and demodulation in modern wireless transceivers. In addition, phase arrays turn out to be the direction of the MMW radios, for achieving longer communication distance and higher data rate, and more phase LO signals are required for these applications [75]. Besides, multiple phase LO signals are also wanted for the half-rate clock-and-data recovery (CDR) in high speed wire-line systems [76].

Lastly, in general, the device model provided from the foundry doesn't go up to tens of GHz, which makes it difficult to accurately design and predict the circuit.

7.2 Proposed Phase Tuning (PT) Technique

To improve the performance of oscillators at MMW frequencies, in this section

an interpolative-phase-tuning (IPT) technique will be introduced, to tune the frequency of multiphase MMW LC-based ring oscillators without using varactors.

7.2.1 Varactor-Less 8-Phase Output PT CCO

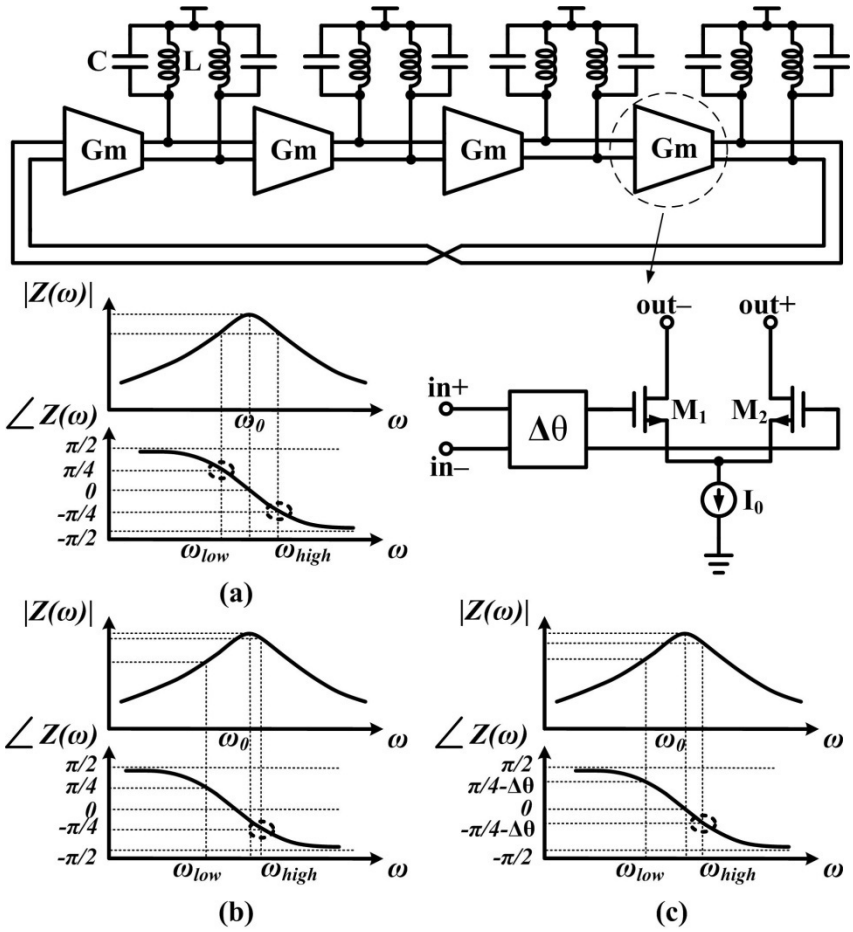


Fig. 7.1 Conventional 4-stage LC ring oscillator and the frequency responses of the LC tank with: (a) ideal parallel LC tank, (b) Q_L dominating tank's Q, and (c) significant phase delay due to the transconductor.

Fig. 7.1(a) shows the schematic of a conventional 4-stage LC-based ring oscillator. To ensure stable oscillation, the voltage gain of each stage needs to be larger than 1, and the phase shift provided by each stage, which is induced by the LC tank, has to be $\pi/4 + (\pi/2)*N$. If a second-order LC tank is used in each stage, N can be either 0 or -1. For an ideal parallel LC tank with symmetrical magnitude and phase responses at frequencies ω_{high} and ω_{low}, as shown in Fig. 7.1(a), where $\omega_{high} > \omega_0 > \omega_{low}$ with ω_0 being

the peak frequency of the LC tank, the tank can provide the required phase shift $-\pi/4$ and $\pi/4$ with the same magnitude. Thus, the oscillator can possibly operate at both frequencies. In practice, the oscillator would preferably operate at one frequency rather than the other, because of two effects. At radio frequencies below 10GHz, the integrated inductor typically limits the tank's Q, and the phase shift of the LC tank at ω_0 is actually none zero as shown in Fig. 7.1(b). Consequently, the oscillator tends to operate at ω_{high} with larger tank impedance [49]. At higher frequencies, in the MMW range, the tank capacitor's Q becomes much smaller, and it is possible that $Q_L > Q_C$. Nevertheless, the non-ideal transconductor devices could introduce significant negative phase shift $\Delta\theta$ when the operation frequency is close to the cut-off frequency ω_T of the transistors. As a result, as shown in Fig. 7.1(c), the required phase shift of the LC tank becomes $\pm\pi/4-\Delta\theta$. It is still typically true that $|Z(\omega_{high})|>|Z(\omega_{low})|$ and the circuit would still prefer to oscillate at ω_{high}.

On the other hand, this interesting phase relationship indicates that extra phase shift $\Delta\theta$ can be placed in the Gm cell to change the required phase shift θ provided by the LC-tank and thus the oscillation frequency. As shown in Fig. 7.2(a), the total phase shift φ including the intrinsic device phase shift $\Delta\theta$ is added in front of the transconductor. Based on the phase condition, each stage needs to provide a total phase shift of $\varphi + \theta = \pi/4 + (\pi/2)*N$. As plotted in the frequency response of the LC tank with assumption of symmetry for simplicity, if φ is a negative value close to zero, θ needs to be close to $-\pi/4$, and the oscillator would operate around the highest frequency ω_{high}. If $\varphi = -\pi/4$, the LC tank doesn't need to provide any phase shift, and the oscillator would oscillate at the peak frequency of the LC tank. When φ is reduced and approaches $-\pi/2$, θ tends to increase to $\pi/4$, and the oscillation occurs at the minimum frequency limit ω_{low}. If φ is further reduced, the oscillator will oscillate again around ω_{high} where the

tank impedance is larger.

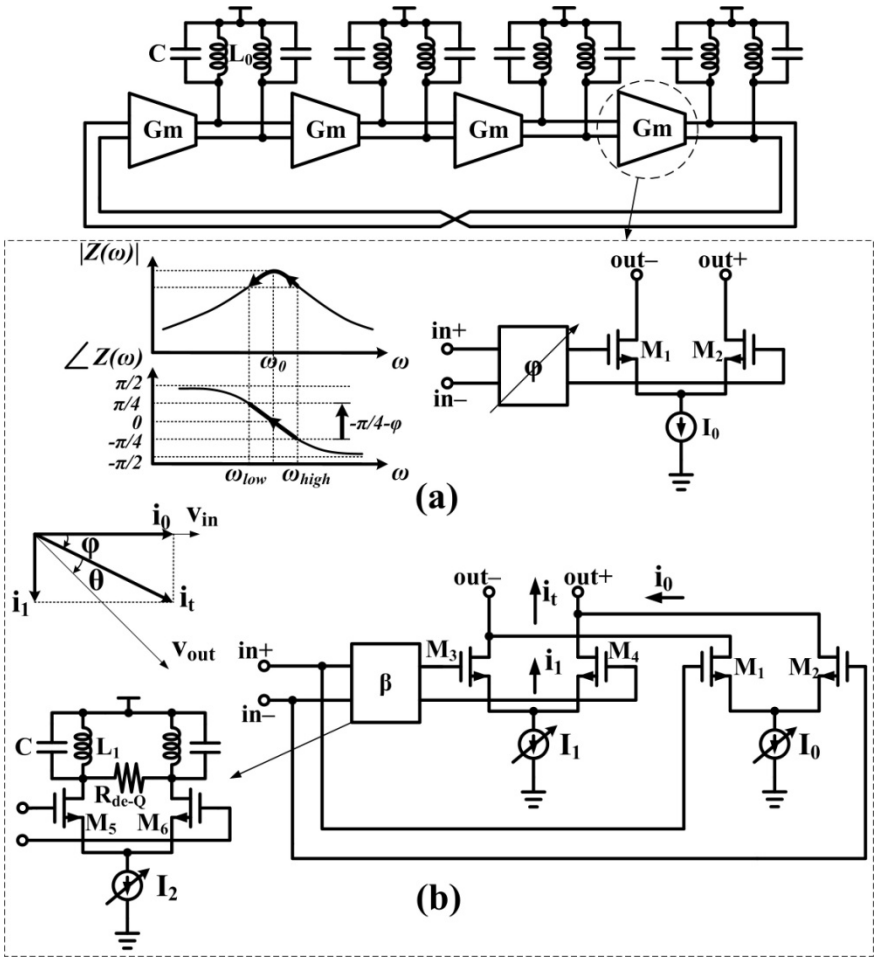


Fig. 7.2 Proposed 4-stage LC ring oscillators with: (a) tunable phase shift, (b) interpolative phase tuning at each stage.

The actual implementation of the proposed interpolative-phase-tuning scheme to tune the phase shift φ and thus the oscillation frequency is shown in Fig. 7.2(b). A fixed phase shift β is used to introduce a delayed current i_1 via M_3 and M_4, which is interpolated with the un-delayed current i_0 provided by M_1 and M_2. By controlling the biasing DC current I_0 and I_1, the delay of the total current i_t can be tuned from 0 to β. Taking into account the intrinsic phase shift of the transistors, β can be designed as $-\pi/2-\Delta\theta_{M3/4}$ to obtain a maximum monotonous frequency tuning range. At high frequencies, the phase shift β can be simply implemented by another LC-based

differential stage, where the inductance L_1 is designed to be much larger than L_0 to make β close to $-\pi/2$. The resistor $R_{de\text{-}Q}$ is added in parallel with the tank to flatten the magnitude response of the differential stage and reduce the variation of β within the tuning range.

7.2.2 Varactor-Less 4-Phase Output PT CCO

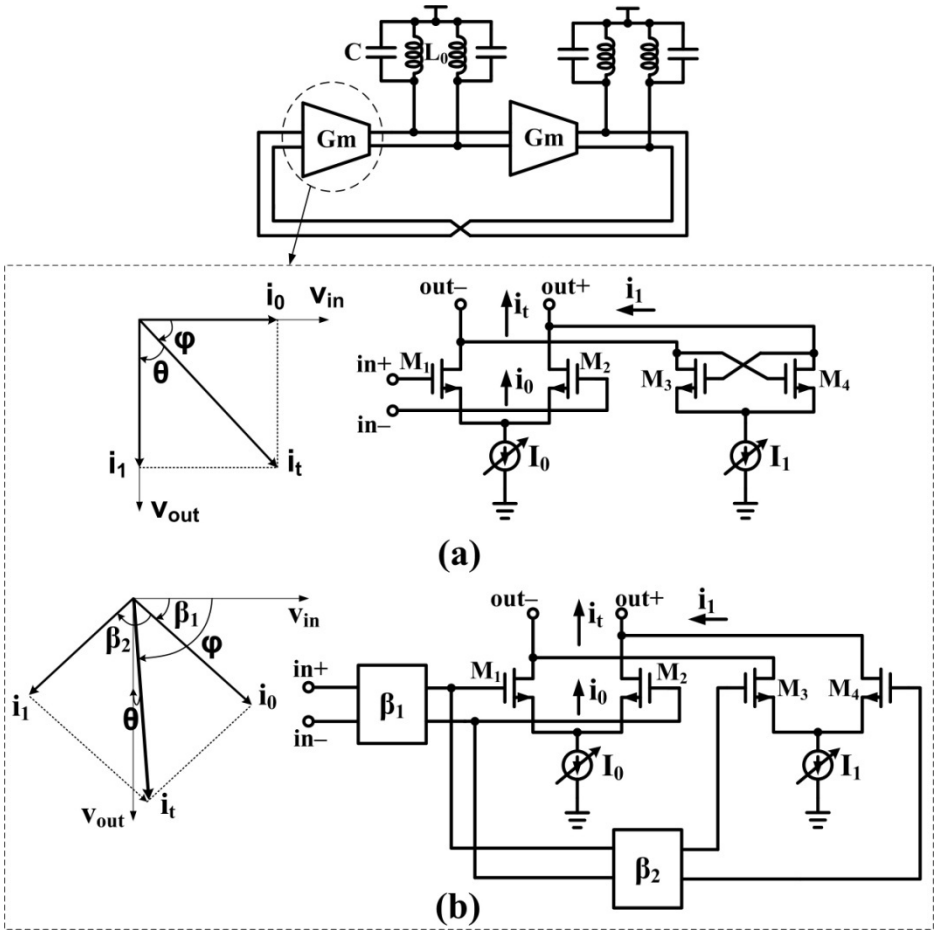


Fig. 7.3 2-stage LC ring oscillators: (a) conventional Q-CCO, (b) IPT Q-CCO.

The IPT technique can be also applied to tune the oscillation frequency of quadrature CCOs (Q-CCOs). Fig. 7.3(a) shows the schematic of the conventional 2-stage ring Q-CCO. As there are only two stages in the ring, each stage needs to provide a phase shift of $+\pi/2$ or $-\pi/2$. As shown in the phasor diagram of the current flowing into the LC tank, the current i_0 provided by M_1 and M_2 is combined with the current i_1 provided by the cross-coupled pair M_3 and M_4 to generate a total current i_t

with a phase shift φ. Since the absolute value of the phase shift φ is smaller than π/2, the LC tank needs to provide an additional phase shift θ to satisfy the phase condition. As a result, the conventional Q-CCO cannot operate at the peak frequency of the LC tank. Because of the asymmetrical frequency response of the LC tank and the phase shift due to the transistors, in general the Q-CCO would prefer to oscillate at the frequencies higher than the peak frequency of the LC tank. Consequently, if i_0 is increased by increasing the biasing current I_0, the phase shift $|\varphi|$ would be reduced, and the LC tank needs to provide more negative phase shift θ, which would increase the oscillation frequency of the Q-CCO. The lower boundary of the frequency tuning is limited by IQ phase error while the upper boundary is limited by the phase noise performance.

Based on the same phase-tuning concept, a novel Q-CCO can be built as shown in Fig. 7.3(b). Two fixed phase shifts β_1 and β_2 are introduced into each Gm cell. From the current phasor diagram, it can be seen that the phase shift φ provided by each Gm cell can be controlled from β_1 to $\beta_1+\beta_2$. To satisfy the phase condition, the phase shift provided by the LC tank needs to vary from $-\pi/2-\beta_1$ to $-\pi/2-(\beta_1+\beta_2)$ assuming β_1 and β_2 are negative, and thus the oscillation frequency would decrease accordingly. Assuming that the LC tank has symmetric frequency response for simplicity, β_1 should be designed as $(-\pi/2-\beta_2/2)$ to achieve a frequency tuning range symmetrically and optimally around the peak frequency of the tank with the maximum tank Q. On the other hand, β_2 determines the actual tuning range and can be ideally designed to be close to $(-\pi/2-\Delta\theta_{M3/4})$ with $\beta_1=0$. Ideally, an infinitely large tuning range could be obtained if the gain condition is not a problem. In practice, $|\beta_2|$ is limited by the power budget as well as the phase noise performance. As $|\beta_2|$ becomes larger and larger, the magnitude of i_t would become smaller and smaller due to the current interpolation, and

it would become difficult to meet the gain condition. Similar to the 4-stage IPT CCO, the phase shift β_1 and β_2 can be simply implemented as differential pairs with low-Q LC tanks. In our design, β_1 and β_2 are designed to be around $-\pi/4$ and $-\pi/2$, respectively. Compared to the conventional Q-CCO, the IPT Q-CCO can oscillate within a much larger frequency range around the peak frequency of the LC tank. Moreover, in the conventional Q-CCOs, only part of the biasing current is used for the coupling pairs. Consequently, at the edge of the tuning range when less current is available to the IQ coupling transistors, the oscillator becomes more sensitive to the mismatches. In contrast, in the proposed IPT Q-CCOs, because all the biasing currents are used for the coupling pairs, over the whole frequency tuning range no matter how the current is distributed, the coupling strength around the loop does not change much, and the loop can self-calibrate for the mismatches among the stages. As a result, the IPT CCO is much less sensitive to mismatches.

Assuming that the LC tank is symmetrical and that β of the 8-phase CCO and β_2 of the 4-phase CCO are around $-\pi/2$, the oscillation frequency of the two IPT CCOs can be estimated based on the phase condition as:

$$\omega_{osc} = \frac{\omega_0}{1 - \frac{1}{2Q_{peak}} \frac{1-a}{1+a}}$$

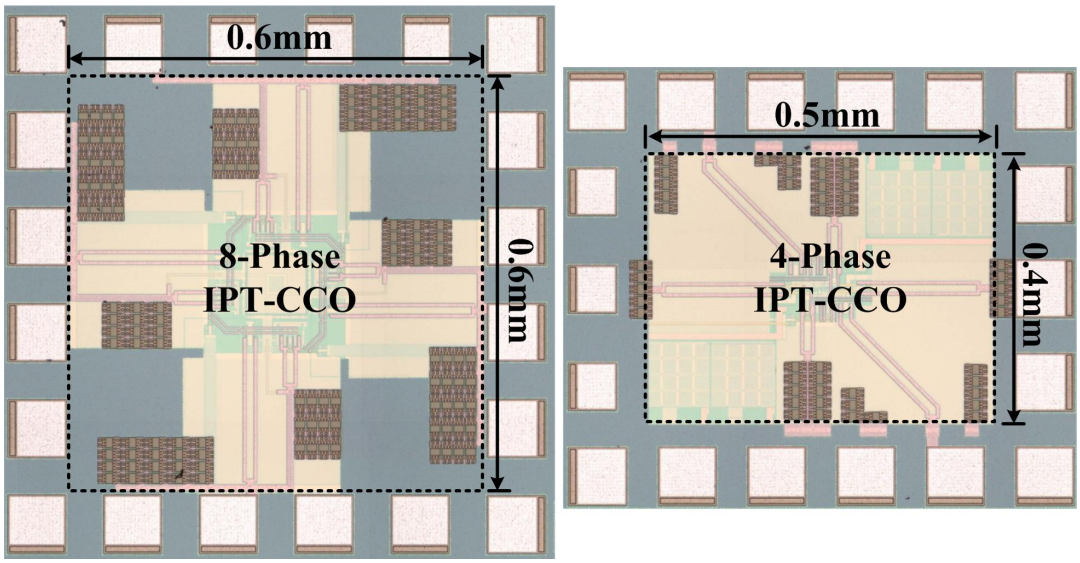
where $a=|i_1|/|i_0|$ is defined as the ac current ratio, ω_0 is the peak frequency of the LC tank, and Q_{peak} is the tank Q at the peak frequency. Numerically, Table 7.1 lists the achievable tuning range of the IPT VCOs with different tank Qs. When Q_{peak} is reduced from 20 to 3, the tuning range can be enlarged from 5% to 33.3%. For the proposed IPT CCOs, there is also a trade-off between Q and tuning range. However, different from the capacitive tuning VCOs, this trade-off is independent of the

operation frequency. As such, when the desired oscillation frequency becomes so high that capacitive-tuning method is no longer effective, the proposed phase-tuning technique would provide a good solution.

Table 7.1 Achievable phase tuning range (TR) at different Q_{peak}

Q_{peak}	ω_{min} (a=∞)	ω_{max} (a=0)	TR
20	$0.976\omega_0$	$1.026\omega_0$	5.0%
15	$0.968\omega_0$	$1.034\omega_0$	6.6%
10	$0.952\omega_0$	$1.053\omega_0$	10.1%
7	$0.933\omega_0$	$1.077\omega_0$	14.3%
5	$0.909\omega_0$	$1.111\omega_0$	20.0%
3	$0.857\omega_0$	$1.200\omega_0$	33.3%

7.2.3 Experimental Results



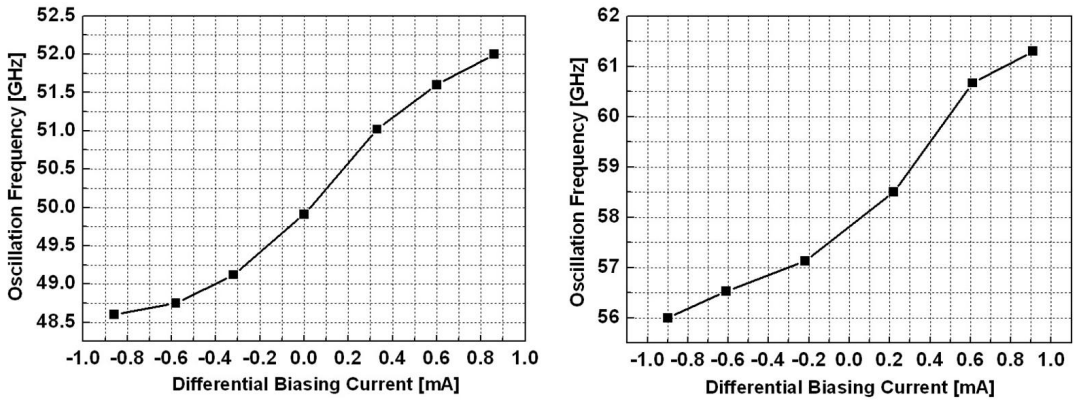
(a) (b)

Fig. 7.4 Die photos of: (a) 8-phase CCO, and (b) 4-phase CCO.

The two IPT CCOs are designed and fabricated in a 0.13-μm CMOS process. Fig. 7.4(a) and Fig. 7.4(b) show the die photos of the 8-phase CCO and 4-phase CCO, which occupy chip area of $0.36mm^2$ and $0.20mm^2$, respectively. Transmission lines are

used to implement all the inductors to reduce the undesired mutual magnetic coupling.

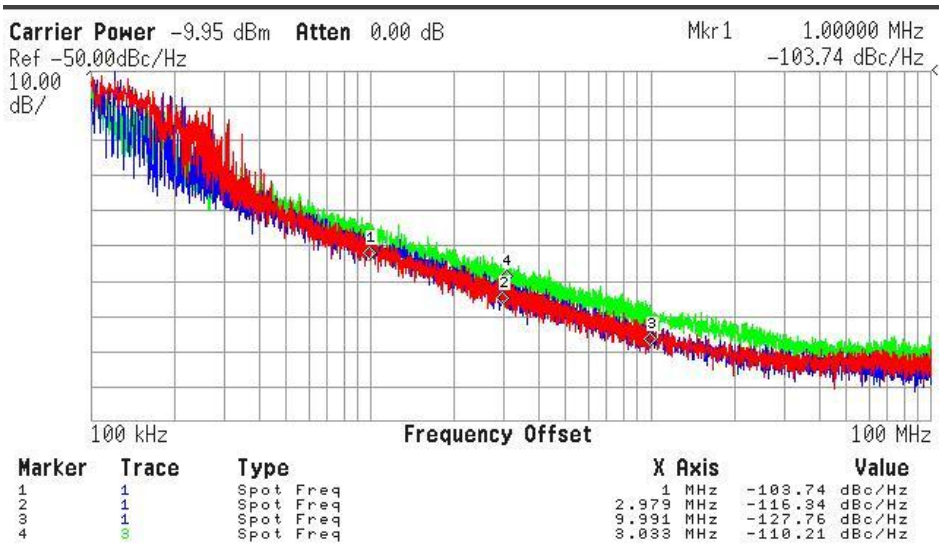
Fig. 7.5(a) and Fig. 7.5(b) show the measured frequency tuning curves of the two oscillators. When the differentially-controlled biasing current is tuned from -0.9mA to 0.9mA, the 8-phase CCO can be tuned continuously from 48.6GHz to 52GHz while consuming 32mW to 48mW from a 0.8V supply. The 4-phase CCO can be tuned continuously from 56GHz to 61.3GHz, with a total power of 30mW to 37mW from a 0.8V supply.



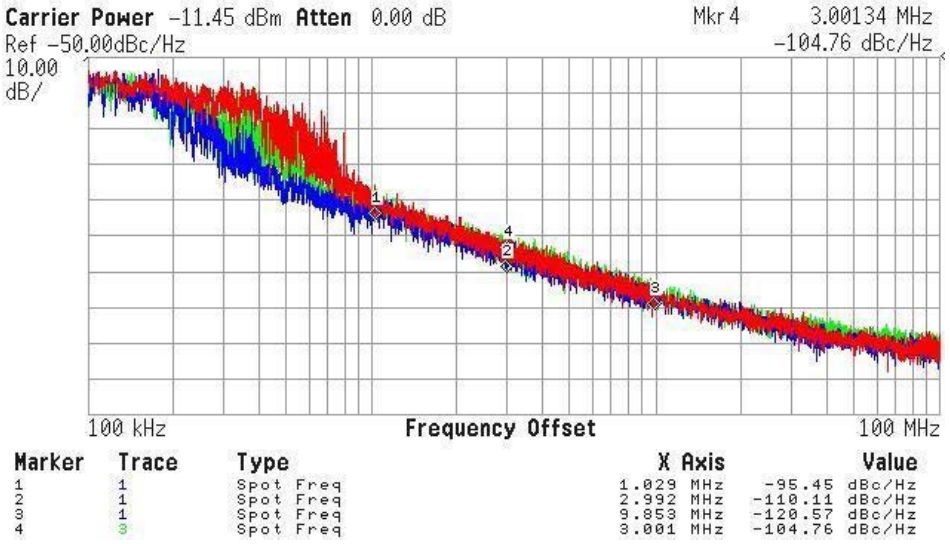
(a) (b)

Fig. 7.5 Measured tuning curves of: (a) 8-phase CCO, (b) 4-phase CCO.

To measure the phase noise, the output signals of the oscillators are down-converted by an external V-Band mixer with LO signal around 50GHz generated by a signal generator. Assuming the phase noise contributed by the mixer and the signal generator is negligibly small, Fig. 7.6(a) and Fig. 7.6(b) plots the phase noise curves of the two IPT oscillators. The red, blue, and green curves are measured when the CCOs oscillate at the lowest, middle, and highest frequencies, respectively. The measured phase noise at 3MHz offset vary from -110.2 to -116.3dBc/Hz for the 8-phase CCO and from -104.8 to -110.1dBc/Hz for the 4-phase CCO. For both of the oscillators, as expected, the lowest phase noise is measured when they oscillate at the middle frequency, at which the tank Q is maximized.



(a)



(b)

Fig. 7.6 Measured phase noise: (a) 8-phase CCO, (b) 4-phase CCO

Table 7.2 summarizes the performance of the proposed IPT oscillators and compares with that of the recently reported MMW oscillators. For n-stage LC oscillators, the phase noise contributed by each stage can be reduced by a factor n^2 while the number of stages is increased by n. As such, theoretically the phase noise can be improved by n. On the other hand, as the power consumption is also increased by n, the FOM as defined below becomes independent of the number of output phases [77].

From Table 7.2, as compared to other MMW oscillators with varactor tuning, the proposed IPT oscillators achieve much lower phase noise and better FOM and FOM_T while providing multiple output phases over comparable tuning range even in a less advanced process.

$$FOM = 10\log\left[\left(\frac{f_0}{\Delta f}\right)^2 \frac{1}{L(\Delta f)\times P_{diss}\,|_{mW}}\right]$$

$$FOM_T = FOM + 20\log[TR/10]$$

Table 7.2 Summary and comparison of MMW oscillators

Ref.	Phase No.	Freq. [GHz]	TR [%]	PN [dBc/Hz]	Power [mW]	FOM	FOM_T	Process
[72]	2	70.2	9.6	-106.1 @10MHz	5.4	175.8	175.4	65nm SOI
[73]	2	58.4	9.3	-91 @1MHz	8.1	177.2	176.6	90nm CMOS
[74]	2	59	9.8	-89 @1MHz	9.8	174.5	174.4	0.13μm CMOS
[74]	2	98.5	2.5	-102.7 @10MHz	7	174.1	162.2	0.13μm CMOS
[74]	2	105.2	0.2	-97.5 @10MHz	7.2	169.4	135.0	0.13μm CMOS
This work	8	50.3	6.8	-127.8 @10MHz	35	186.4	183.0	0.13μm CMOS
	4	58.5	9	-120.6 @10MHz	34	180.6	179.7	0.13μm CMOS

7.3 Frequency Multiplications Based-on Injection-Locking

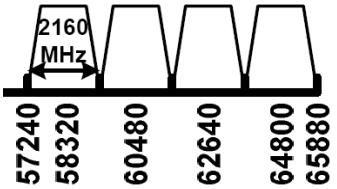


Fig. 7.7 Channel profiles of standard 802.15.3c

Fig. 7.7 gives the channel profiles of the MMW UWB standard 802.15.3c. Based on the SDR FGS, there are several realizable schemes for synthesizing the required carrier frequencies of the standard, as shown in Fig. 7.8. For the conventional direct frequency synthesis scheme, the most challenging building blocks are the high frequency VCO and the following divider, which can be realized by the IPT-CCO as described above and the CR-ILFD or CB-MD as presented in Chapter 5, respectively. After dividing down the output frequency, the phase locked loop used for other standards of the FGS can be shared for the synthesizer.

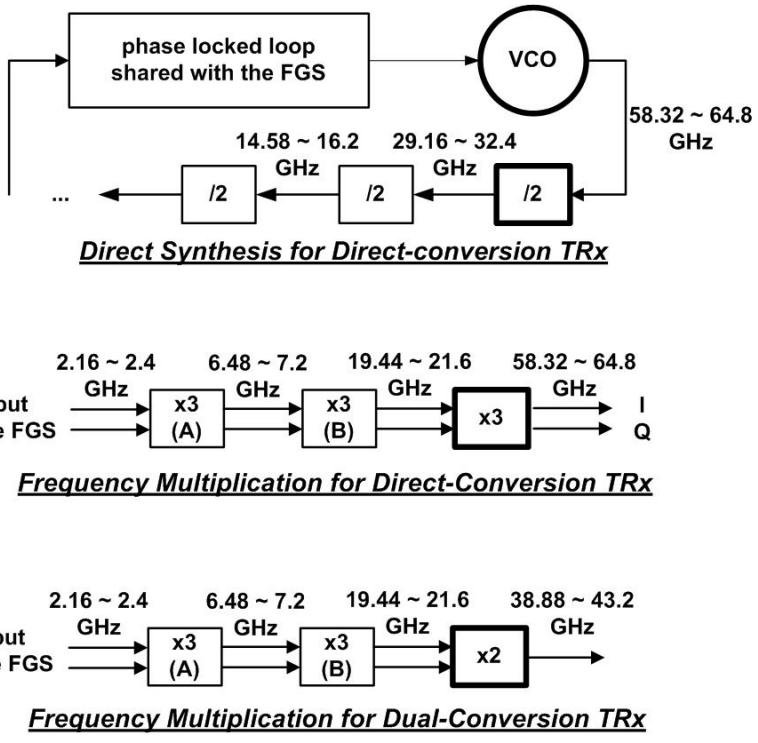


Fig. 7.8 MMW carrier frequency generation schemes for the SDR FGS

Instead of using a VCO with PLL to directly synthesize the LO signals around 60GHz, frequency multipliers can be made use to multiply the frequency of several Giga-Hertz, which is available from the FGS, to the frequency of tens of Giga-Hert as required by the MM-Wave applications. There are several advantages to do so. As first, with the frequency multiplying, the operation frequency of frequency synthesizer can be much relaxed, thus better performance like phase noise, tuning range and power consumption can be achieved. Secondly, as the output phase noise of the injection-locked frequency multiplier is mainly decided by the phase noise of the input signal, the limited available Q at the MM-Wave frequencies would not affect the phase noise of the 60GHz LO signal much, as a result, low phase noise can be achieved as it is easier for the RF frequency synthesizer to obtain the associated good phase noise.

As shown in Fig. 7.8, the carrier frequencies of the direct-conversion MMW transceivers can be realized by three successive multiply-by-3 operations, and the required carrier frequencies of the dual-conversion transceiver can be generated by two multiply-by-3 operations and one multiply-by-2 operation, with the 1st higher frequency differential LO signals generated at the multiplier-by-2's output and the 2nd lower frequency IQ LO signals generated at the second multiplier-by-3's output.

In the following part, different injection-locked frequency multiplier (ILFM) topologies will be discussed, to find the most suitable architecture for the SDR FGS.

7.3.1 Differential-input-different-output (DIDO) x3 ILFM

Fig. 7.9 shows the DIDO ILFM. Transistor M_5 and M_6 compensate the loss of the LC tank, and the circuit would self-oscillate when there is no input signal. By applying the input voltage at frequency ω to the gates of M_1 and M_2, the AC current at frequency 3ω can be generated and injected into the LC tank, making use of the nonlinearity of the transistors. The locking range of the ILFM depends on the current

amplitude ratio between the injected current at 3ω and the current provided by the $M_{5/6}$ at 3ω. The larger the ratio the wider the locking range is. Given certain DC bias current and output amplitude, the current provided by the $M_{5/6}$ is nearly fixed, so maximizing the injected current at 3ω is the key to maximize the locking range. However, as the $i_{in}(3\omega)$ totally depends on the nonlinearity of the transistor, which is the 3rd order effect, consequently, the locking range of the ILFM is quite limited, especially when the operation frequency is high, large input swing is not available.

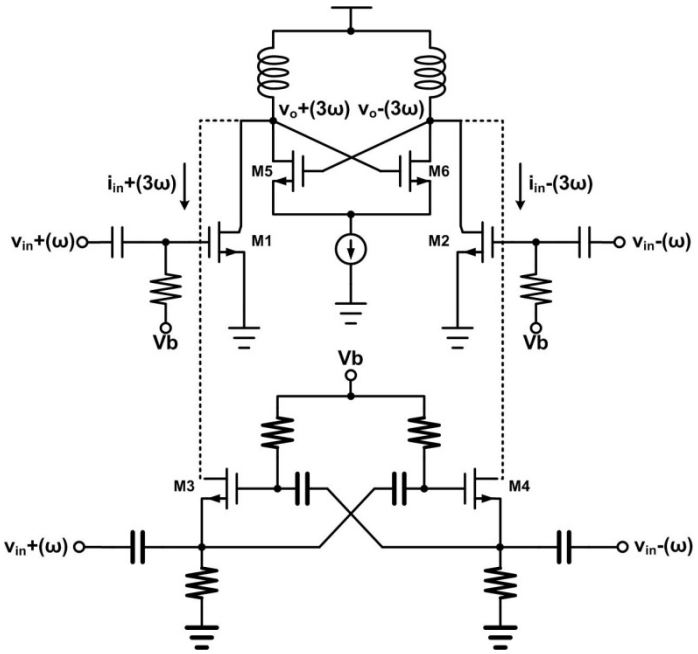


Fig. 7.9 DIDO ILFM with different injection manners

To improve the locking range of the ILFM, injection manner can be changed, as cross injecting the signal from both the source and gate of M_3 and M_4. By doing so, it is not difficult to prove that $i_{in}(3\omega)$ can be improved to 8 times larger given the fixed input swing. The trade-off of the cross-injection is that the input capacitor is large due to the miller effect, and also input resistance can heavily load the previous stage when the input swing is large. As a result, considering a fixed previous driving stage, at the moderate frequency below 10GHz, since the large input swing is still

achievable, the conventional injection manner at the top is better. While at the frequency of tens of Giga-Hertz, the input swing is not sufficient, the cross-injection manner can provide larger locking range.

7.3.2 Quadrature-input-quadrature-output (QIQO) x3 ILFM

The x3 ILFM can be also modified as QIQO, by simply injecting the IQ signals into a Q-VCO, as shown in Fig. 7.10. Noting that as injected current is the third harmonic of the input signal, the IQ sequence is reversed, thereby, the output IQ sequence is different from the input IQ sequence.

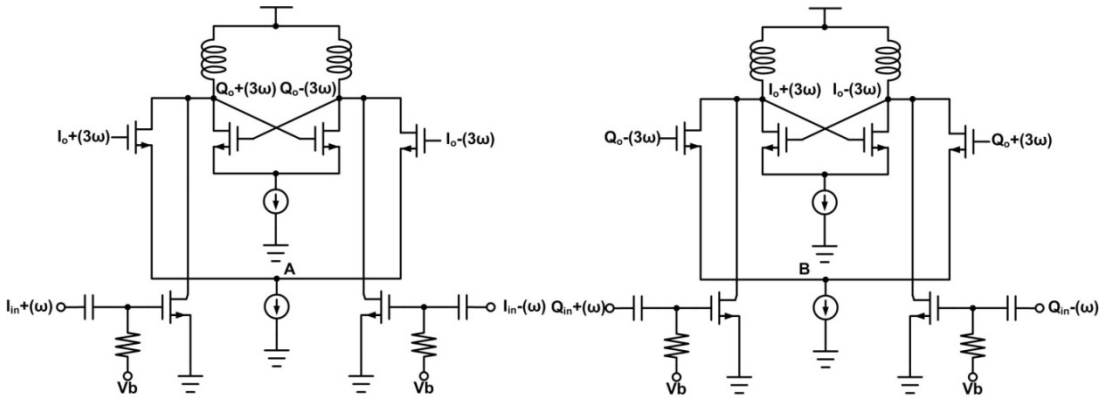


Fig. 7.10 QIQO x3 ILFM

7.3.3 Quadrature-input-differential-output (QIDO) x2 ILFM

For the x3 ILFM circuit, because the injected current is the 3rd order effect signal, the locking range of x3 is quite limited. So a natural choice would be using x2 ILFM to do the frequency doubling. However, for the differential architecture, as the 2nd harmonic current is common mode signal, which is rejected by the oscillator, the same injection manner used by the x3 ILFM cannot be used in x2 ILFM.

Fig. 7.11 shows a QIDO x2 ILFM. The differential signals are applied to a push-push transistor pair to generate the AC current at 2ω. Quadrature input signals are used for to inject current differentially into the VCO core. Although the phase information is lost from the input to the output, this x2 ILFM has no sub-harmonic

tones being with the output signals because the input current at ω is cancelled out, which is an advantage compared to the previous x3 ILFM.

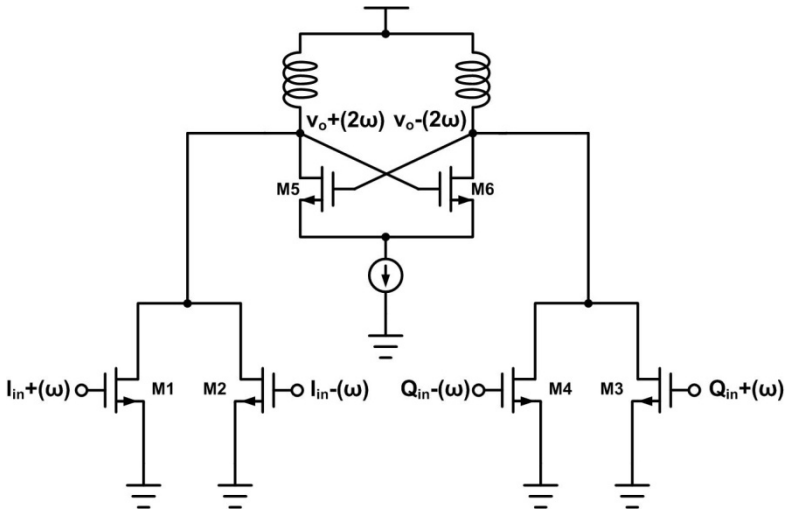


Fig. 7.11 QIDO x2 ILFM

7.3.4 Automatic peak control (APC)

For any LC-based circuit, the accuracy of the peak frequency is important for the circuit performance. For amplifiers, the discrepancy between the input frequency and the peak frequency causes the degradation of gain. For the injection locked circuit, the mismatch between the input frequency and peak frequency causes the degradation of the output swing, worse phase noise, worse filtering on the spurious tones, and even the malfunction of the circuit.

In convention, calibration of the peak frequency needs the circuit to self-oscillate and uses an extra phase-locked loop to calibrate the frequency, which requires much extra chip area [78][79]. Alternative, an APC technique is proposed which applies the peak calibration in digital domain with negligible power and chip area.

The purpose of the APC is to dynamically tune the peak frequency by tuning varactors or switched capacitors, in order to maximize the output amplitude. In general, when the output amplitude is maximized the peak frequency would be

consistent with the input frequency. Considering the automatic amplitude control (AAC) for the VCO [80]. At first the output amplitude is detected though a squaring circuit, and then the detected DC signal is compared with a reference voltage. The error is fed back, amplified and used to control the biasing current of the VCO. For the VCO, because the relationship between the output amplitude and biasing current is monotonous, so negative feedback is enough to control the output amplitude. However, for the peak frequency tuning, the relationship between the loaded capacitance and output amplitude may not be monotonous. Thus, a simple negative feedback loop can't realize the APC.

Fig. 7.12 shows the proposed APC method. The information of the output amplitude is detected through a squaring circuit (for simplicity, the output amplitude can be detected by directly sensing the common mode node A or B of the differential coupling pair in Fig. 7.10, where due to the second harmonic nonlinearity, the DC voltage is proportional to the output amplitude of the ILFM). At the time slot when the clock 1 is high level, the DC voltage at node A is sampled and restored to the capacitor C_S. When the rising-edge of the clock 2 is coming, the counter starts to up- or down-count once to change the capacitance of the LC tank, and the voltage at A will be sampled again when the clock 2 is high level. Till the falling-edge of the clock 2, the comparator delivers the compared result between the two sampled voltages to the shift registers. If the voltage increases, the counter will keep counting towards the correct direction during the next period, if not, the toggling register will change the counting direction to make the counter count correctly. The states restored on the shift register would control the logic (the "Count/Hold" control of the counter is equal to "$Q_2Q_0+Q_2Q_1+Q_1Q_0$"), to let the counter stop when the peak voltage at node A is found. Two cycle delays are placed on the count/hold control signal to guarantee the output

swing is maximal when the counter holds its state. The output of the counter is used to directly control the switched capacitor arrays or switched varactor arrays (at MMW frequencies) in the LC tank.

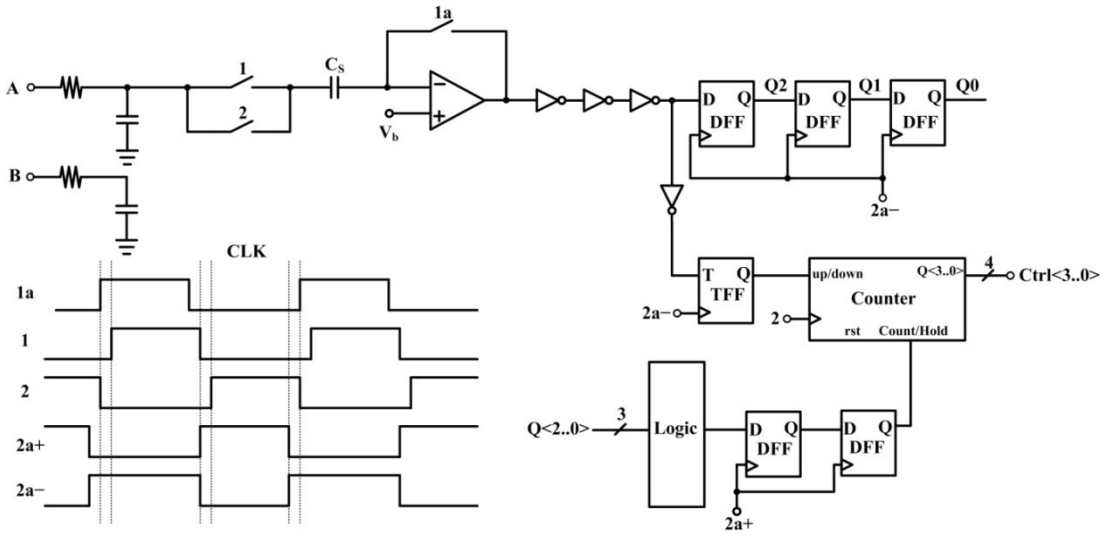


Fig. 7.12 Automatic peak frequency calibration circuit

7.3.5 Experimental Results

7.3.5.1 Measurement of 60GHz Output x27 ILFM Chain

The 60GHz output ILFM chain is fabricated in the 0.13μm CMOS. The die photograph is shown in Fig. 7.13, which occupies an area of 0.8mm by 0.55mm.

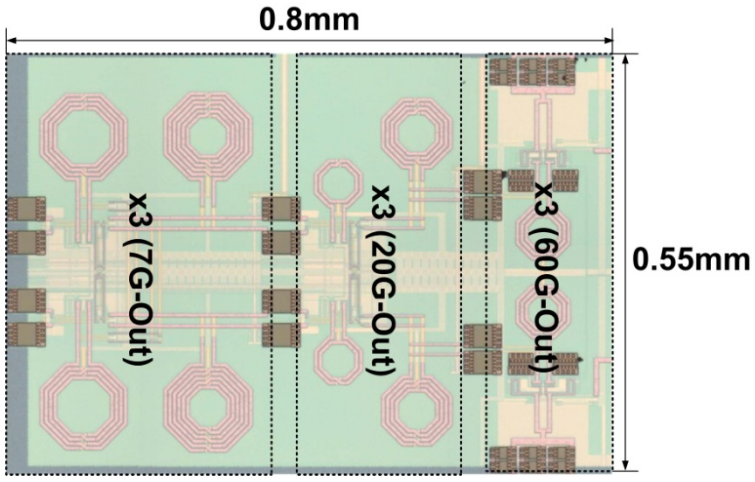


Fig. 7.13 Die photo of 60GHz output x27 ILFM chain

As the ILFM with the highest output frequency is the most critical one in the ILFM chain, an individual testing structure was also fabricated to verify the performance. Fig. 7.14 shows the measured sensitivity of the 60GHz x3 ILFM. With the varactor turned off, as the Q of the LC tank is relatively high, the locking range is quite limited, measured from 59.1GHz to 60.6 GHz when the incident power of the 20GHz input is 6dBm. When the varactor is turn off, as the Q of the LC tank is much degraded, the phase condition and thus the locking range of ILFM is much improved, measured from 53.6GHz to 66.4GHz with input power of 6dBm.

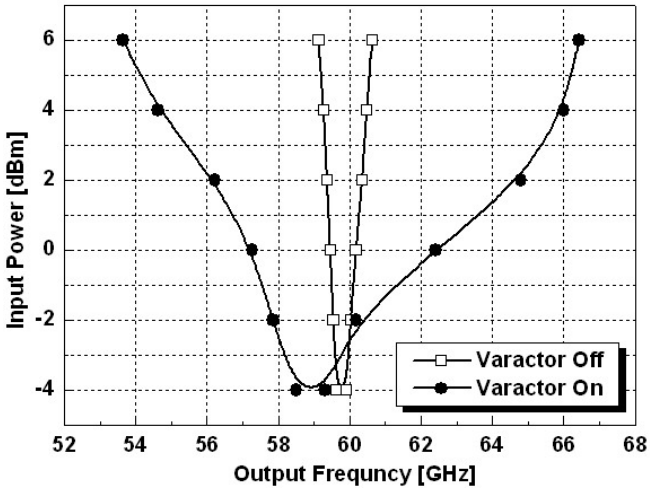


Fig. 7.14 Measured sensitivity curves of the 60GHz x3 ILFM

Fig. 7.15 gives the measured output power and swing of the ILFM, where the output power is measured at the open-drain buffer's output with the loaded 50 Ohm from equipment, and the swing is the calibrated value at the ILFM's output. It can be seen that with the varactor on, the power and swing are reduced significantly due to the degradation of the tank's Q.

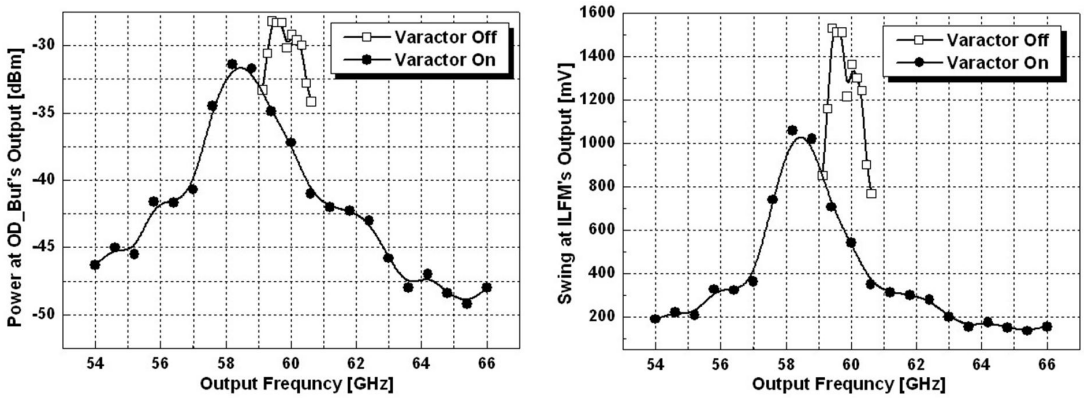


Fig. 7.15 Measured output power and swing of the 60GHz x3 ILFM

The whole x27 ILFM chain is measured with the IQ input signals around 2GHz generated on chip from the divider-B's output in the FGS, or from an on-chip divider-by-2 driven by an external signal generator.

Fig. 7.16 shows the final output power and the swing of the ILFM chain. The whole ILFM chain can only operate from 60.5GHz to 66.7GHz, and the operating range is limited by the last stage the 60GHz output x3 ILFM.

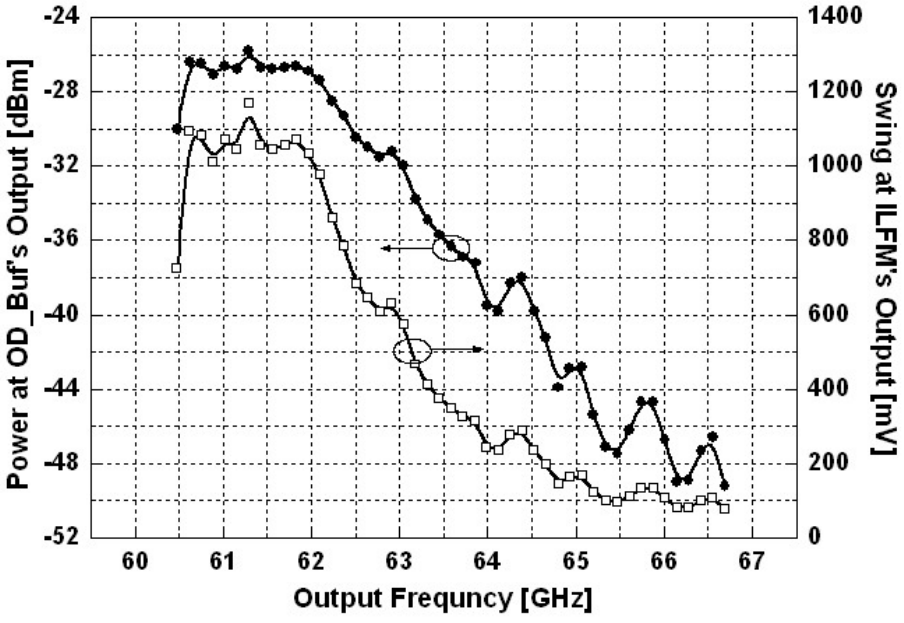


Fig. 7.16 Measured power and swing of the ILFM chain at 60GHz output

7.3.5.2 Measurement of 20GHz and 40GHz Outputs x18 ILFM Chain

The 20GHz and 40GHz outputs ILFM chain with the automatically peak calibration circuits have been fabricated in the 0.13μm CMOS. Fig. 7.17 shows the die photograph. The occupied chip area is 1mm by 0.5mm.

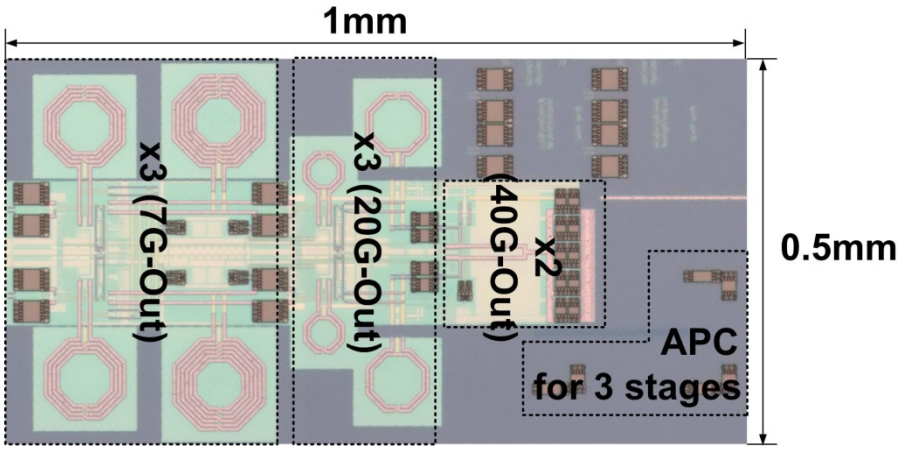
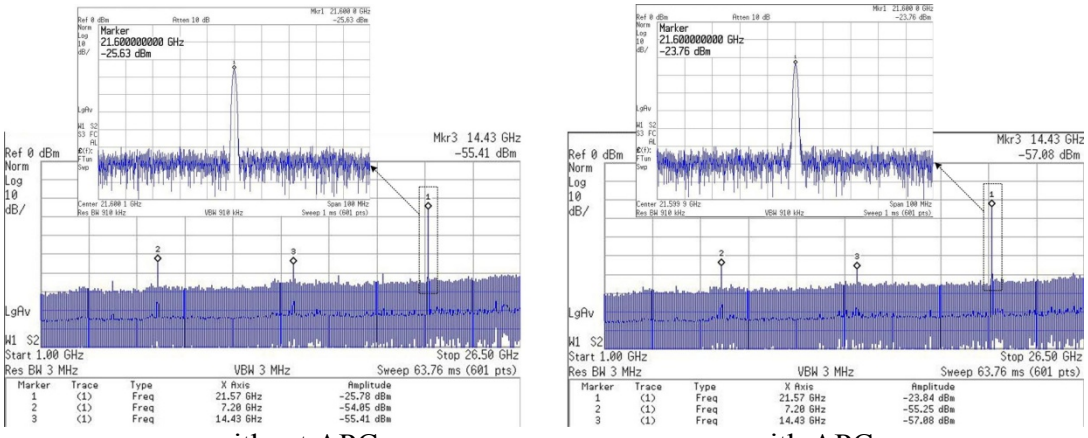


Fig. 7.17 Die photo of 20GHz and 40GHz output x18 ILFM chain

Fig. 7.18 compares the measured spectrums without and with enabling the on-chip automatically peak calibration circuit, at the ILFM chain's 20GHz output. It can be observed that with APC, the power of the desired signal is increased and the filtering of spurious tones at the sub-harmonic frequencies is also improved.

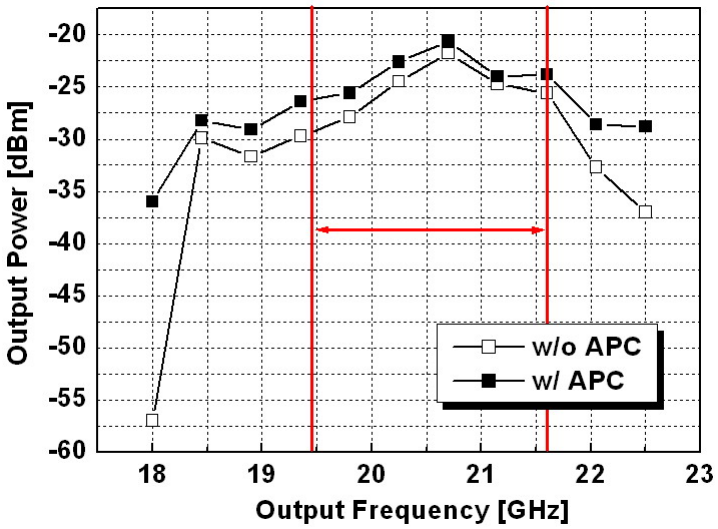


without APC with APC

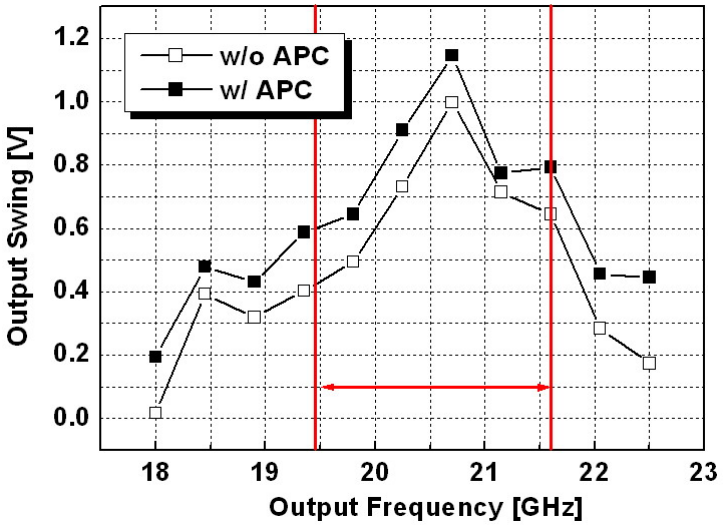
Fig. 7.18 Measured spectrums at ILFM chain's 20GHz output without and with APC

Fig. 7.19(a) summarizes the measured output power of the ILFM at 20GHz output,

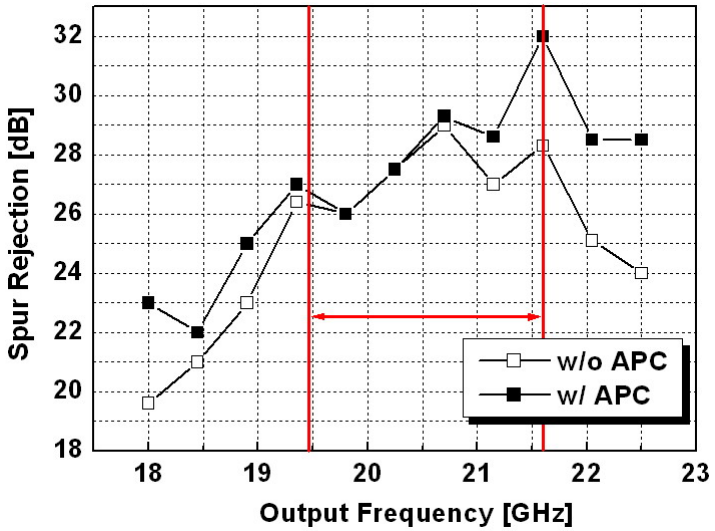
with and without APC. In both the case, the ILFM chain can achieve a continuous locking range from 18GHz to 22.5GHz, well covering the required frequency band from 19.44GHz to 21.6GHz. When the APC is disabled, the SCA is set to be "011" to make the peak frequency locating at the middle of the required frequency band. Within the required frequency band, the measured output power varies from -29dBm to -21.8dBm. When the APC is enabled, the output power varies from -26dBm to -20.6dBm. Fig. 7.19(b) shows the calibrated output swing at the ILFM's 20GHz output. Without the APC, the output swing is above 400mV within the required frequency range. With the APC enabled, the minimum output swing is improved to 600mV, sufficiently enough for driving the up/down-conversion mixers. Fig. 7.19(c) summarizes the spur rejection performance. Within the required frequency range, when the APC is disabled, the measured spur is from -26dBc to -29dBc. When the APC is enabled, the measured spur is suppressed from -26dBc to -32dBc.



(a)



(b)

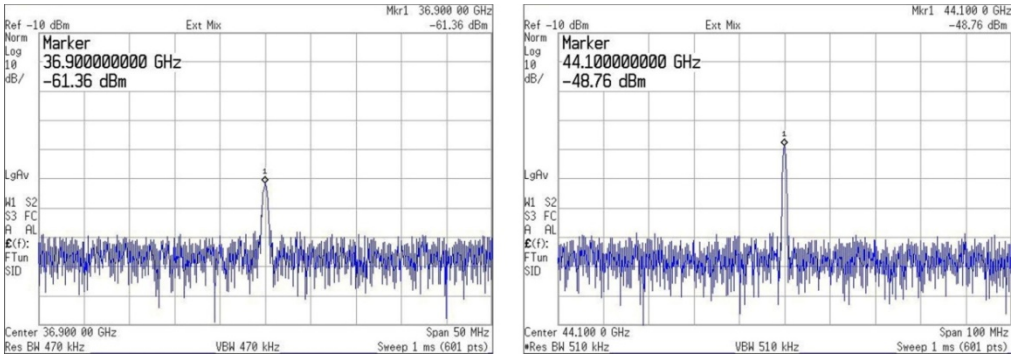


(c)

Fig. 7.19 Measured performance of the ILFM chain at 20GHz output with and without APC: (a) output power, (b) output swing, (c) spur rejection

The 40GHz output signals of the x18 ILFM chain are measured through a Q-Band harmonic mixer cooperating with Agilent's spectrum analyzer E4440A. The whole ILFM chain draws 31.8mA in total including all the buffers from a 1.2V supply voltage. Fig. 7.20 shows the measured output spectrum at the boundary of the ILFM chain's locking range, with APC enabled. The ILFM chain is able to continuously cover a frequency band from 36.9GHz to 44.1GHz, successfully

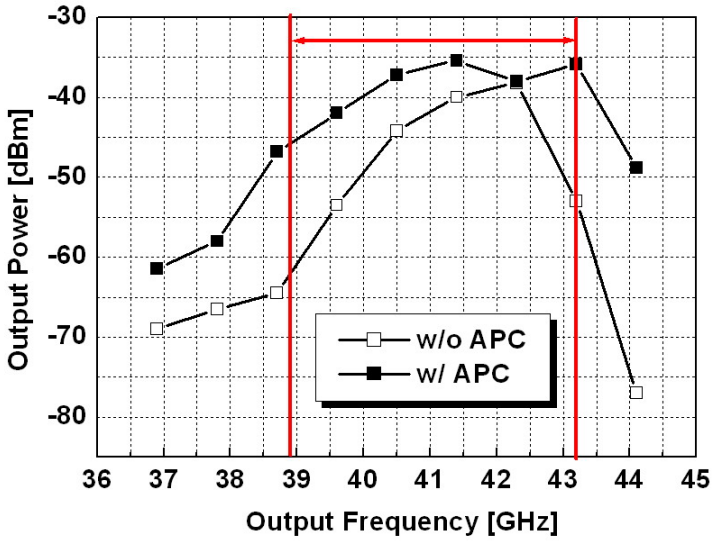
meeting the frequency requirements of the SDR FGS.



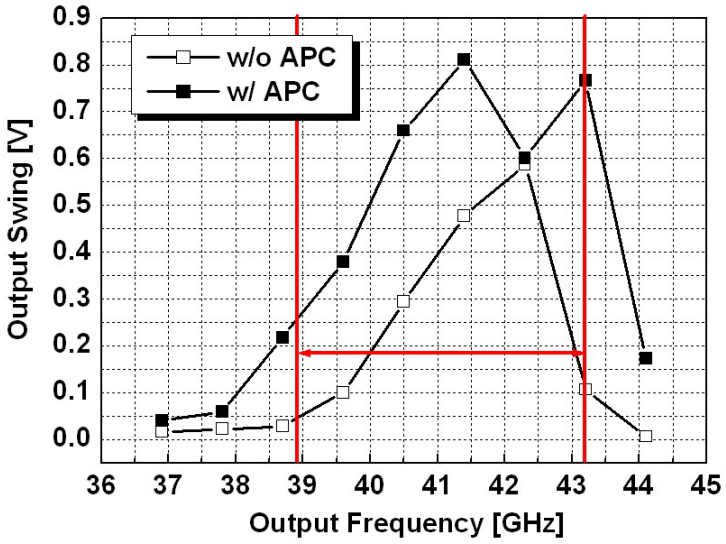
Lower frequency boundary High frequency boundary

Fig. 7.20 Measured spectrums at ILFM chain's 40GHz output

Fig. 7.21(a) shows the measured power of at 40GHz output. When the APC is disabled, the measured output power varies from -62dBm to -38.2dBm within the required frequency band. When the APC is enabled, the output power varies from -46dBm to -35.4dBm. Fig. 7.21(b) shows the calibrated output swing at the ILFM's 40GHz output. Without the APC, the output swing varies from 50mV to 590mV within the required frequency range. With the APC enabled, the output swing can be improved to from 250mV to 810mV. Extra power may need to be consumed in order to improve the swing at the lower frequency boundary. Mainly limited by the set-up, sub-harmonic spurs are not observed from the spectrum analyzer.



(a)



(b)

Fig. 7.21 Measured performance of the ILFM chain at 40GHz output with and without APC: (a) output power, (b) output swing.

Chapter 8

Design of Reconfigurable Phase-Locked Loop

8.1 Phase-Locked Loop (PLL) Architecture

The phase-locking technique can be traced up to as early as 1919 [81][82]. With decades of intensive research efforts, the phase-locked loop theory has been well developed, and detailed design guidelines can be found in numerous literatures [83]-[87]. Depending on the operation domains of each building block, PLLs can be categorized into analog PLL, digital PLL and mixed signal PLL. Analog PLL performs the phase detection in analog domain typically by mixers, the phase detector restricts the loop being able to be locked within a small frequency range, even though, it can be made use of to provide very "quiet" linear phase examining with low reference spur [88]. All digital PLL performs phase/frequency detector, filtering all in digital domain, which has good programmability and re-configurability, but its performance directly depends on the process, requiring stringent intrinsic gating delay to depress the quantization noise, and special design considerations need to be paid in order to reduce the digital spurs to an acceptable level [89][90]. Moreover, the digital controlled oscillator (DCO) [91] is more difficult to design and implement, unavoidably sacrificing the performance. The mixed signal PLL employs digital phase/frequency detector (PFD) together with current charge pump (CP), the control signal is converted back to the analog domain through charging or discharging the loop filter, and then adjusts the oscillation frequency of VCO. It is so far the most commonly and successfully adopted

architecture in the wireless communication systems. With the 0.13μm CMOS technology, the mixed signal type PLL is chosen to stabilize the output frequency of SDR FGS.

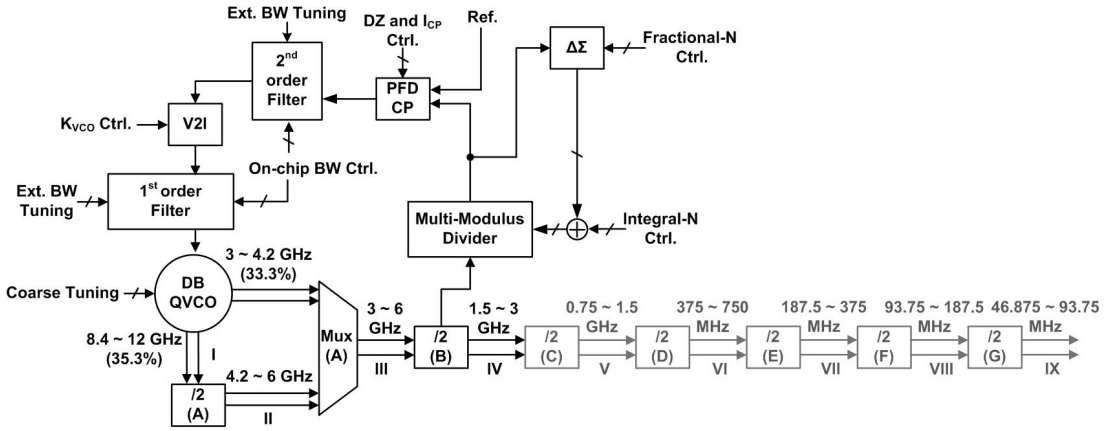


Fig. 8.1 Reconfigurable PLL architecture used in the SDR FGS

Fig. 8.1 shows the PLL architecture used in the SDR FGS. The output signal of the divider-B, from 1.5GHz to 3GHz, is divided down by a multi-modulus divider, which is used to adjust the generated carrier frequency of the FGS. The lower frequency signal at the multi-modulus divider's output is fed to the PFD, and compares with the external reference signal. The dead zone period of the PFD and the CP current are designed to be tunable for adjusting the loop dynamics. The output current signal of the CP flows into a 2^{nd} order low pass filter and is converted into a voltage signal. Through a voltage-to-current (V2I) converter, the voltage signal is converted back to current signal, to control the oscillation frequency of the dual-band Q-VCO. A 1^{st} order low pass filter is added in between the V2I and DB Q-VCO, to perform band-pass filtering on the V2I's noise. Thereby, the total loop filter is equivalent to a 3^{rd} order low pass filter as used in the typical PFD/CP PLL. The VCO gain K_{VCO} can be conveniently adjusted by tuning the trans-conductance of the V2I convertor. And pole, zero locations of the loop filters are controlled both internally

and externally from the chip. The design of each building block will be introduced in the following part of this chapter.

8.2 Frequency Division

The fine frequency resolution requirement, like 200KHz for GSM, necessitates the frequency divider to be able to support fractional-N division number. This can be done by periodically changing the division number of multi-modulus divider. For example, in a 100 periods, if the divider operates as divide-by-2 for 33 periods, and operates as divide-by-3 for the other 67 periods, averagely for the whole 100 periods, the effective division ratio is equal to a fractional number of 2.67. However, any periodicity in the division ratio control pattern causes fractional spurs at the VCO's output. Thereby, certain algorithm needs to be done to control the pattern and depress the fractional spur. One of the most effective methods is to use delta-sigma modulator [92] to randomize the instantaneous division number and shape the quantization noise into higher frequency. As the noise transfer function of the divider is low pass in the PLL, the high frequency quantization noise can be filtered out by the loop filter. The main considerations of choosing delta-sigma for a frequency synthesizer, includes the modulator's architecture, order, sampling frequency, stability, input bit width and output level. Among different architectures, multistage noise shaping (MASH) delta-sigma modulator is most popular for its simplicity, superior noise shaping and unconditional stable properties. It is mathematically proved that to sufficiently randomize the quantization error samples, the order of MASH delta-sigma modulator needs to be no less than 3 [93]. For MASH 1-1-1 modulator, 8 output level needs to be accommodated by the multi-modulus divider,

and within such a range, the PFD/CP has to be linear enough to avoid the high frequency quantization noise folded back into the loop bandwidth. To reduce the output level, MASH 1-2 can be used instead, however it only allows around 75 percent of the whole input range, not applicable for the SDR FGS [94]. Alternatively, single stage modulator with multiple feedback or feed-forward paths can be used, but needs to be carefully designed to avoid stability problem [95]. Finally, MASH 1-1-1 architecture is chosen for the SDR FGS to eliminate the stability issue.

The decisions of the delta-sigma modulator's input bit width, the divider's division ratio and the reference frequencies need to be made together, based on specific requirement. One design consideration is to avoid changing the reference frequency, such that one common crystal oscillator can be used for all the modes for different standards. Table 8.1 shows one potential solution.

Table 8.1 Resolution and division ratio summary with single reference frequency

Standards	Synthesized Frequency	Required Resolution	Ref. Frequency	Prescaler Division No.	Equivalent Resolution at Pres. Input	Required SDM Input Bit Width	Realized Resolution
GSM 850-900	824 ~ 960 MHz	200KHz	32.768MHz	50.2 ~ 58.6	400KHz	15	0.5KHz
DCS	1.71 ~ 1.88GHz	200KHz	32.768MHz	52.1 ~ 57.4	200KHz	15	1KHz
PCS	1.85 ~ 1.99GHz	200KHz	32.768MHz	56.4 ~ 60.7	200KHz	15	1KHz
UMTS	1.90 ~ 2.17GHz	200KHz	32.768MHz	57.9 ~ 66.2	200KHz	15	1KHz
WLAN 802.11a	5.15 ~ 5.85GHz	5MHz	32.768MHz	75.5 ~ 89.3	2500KHz	15	2KHz
WLAN 802.11b/g	2.412 ~ 2.484 GHz	1MHz	32.768MHz	73.6 ~ 75.8	1000KHz	15	1KHz

Wimax-1	2.15 ~ 2.69GHz	25KHz	32.768MHz	65.6 ~ 82.1	25KHz	15	1KHz
Wimax-2	3.4 ~ 4.99GHz	250KHz	32.768MHz	51.8 ~ 76.1	125KHz	15	2KHz
Wimax-3	5.15 ~ 5.85GHz	5MHz	32.768MHz	78.5 ~ 89.3	2.5MHz	15	2KHz
Bluetooth	2.4 ~ 2.48GHz	1MHz	32.768MHz	73.2 ~ 75.7	1MHz	15	1KHz
DECT	1.881792 ~ 1.930176GHz	1.728MHz	32.768MHz	57.4 ~ 58.9	1.728MHz	15	1KHz
Zigbee (LB)	868 ~ 928 MHz	100KHz	32.768MHz	52.9 ~ 56.6	200KHz	15	0.5KHz
Zigbee (HB)	2.4 ~ 2.4385 GHz	100KHz	32.768MHz	73.2 ~ 74.4	100KHz	15	1KHz
RFID (UHF)	860 ~ 960MHz	100KHz	32.768MHz	52.4 ~ 58.6	200KHz	15	0.5KHz
UWB 802.15.3c	58.32 ~ 64.8GHz	2.16GHz	32.768MHz	65.9 ~ 73.2	80MHz	15	27KHz
DTV-1	47 ~ 68MHz	1MHz	32.768MHz	58.75 ~ 85	32MHz	15	1/32 KHz
DTV-2	174 ~ 187MHz	1MHz	32.768MHz	84.9 ~ 91.3	16MHz	15	1/16 KHz
DTV-3	188 ~ 239MHz	1MHz	32.768MHz	45.8 ~ 58.3	8MHz	15	1/8 KHz
DTV-4	470 ~ 750MHz	1MHz	32.768MHz	57.3 ~ 91.5	4MHz	15	1/4 KHz
DTV-5	751 ~ 862MHz	1MHz	32.768MHz	45.8 ~ 52.6	2MHz	15	1/2 KHz
GPS	1.57542GHz	10.23MHz*	32.768MHz	48.07	-	15	1KHz
UWB MB-OFDM	8.448GHz	-	32.768MHz	64.45	-	15	4KHz

The reference frequency is designed to be 32.768MHz, which is 2^{15} times of 1 KHz. The required resolution for each standard can be transferred to the equivalent

one at the prescaler's (multi-modulus divider's) input, with multiplying a coefficient corresponding to the carrier frequency. For example, the GSM900's carrier frequency is half of the prescaler's input frequency. Thereby the equivalent resolution is relaxed and multiplied by 2. With 15-bit input width for the delta-sigma modulator, fine enough resolution can be achieved for every standard. And the prescaler needs to provide a division ratio from at 45 to 92.

One important drawback of such solution is that the frequency synthesizer needs to operate in fractional-N mode for all the standards, even for those ones have relax resolution requirement, such as WLAN and UWB. Consequently, compared to a dedicated single standard integer-N frequency synthesizer, the SDR synthesizer would have lower performance due to the quantization noise generated by the delta-sigma divider. One solution is to reduce the loop bandwidth to filter out the quantization noise, but the in-band noise would be affected more by the VCO's low offset frequency noise. Alternatively, since the quantization noise is deterministic, noise cancellation CP DAC circuit can be implemented to cancel out the quantization noise [96][97][98], but at the expense of more chip area and power consumption. It is therefore desirable to adjust the reference frequency and enable both integer-N and fractional-N mode in accordance with different standards. This can be done by adding an extra low frequency synthesizer or implementing direct digital synthesis (DDS) for the reference frequency.

Fig. 8.2 shows the schematic of the designed multi-modulus divider. The true-modular programmable divider architecture [99] is used. Compared to the more conventional dual-modulus prescaler [100][101], this architecture has better flexibility and reusability, which is beneficial for the SDR applications.

In each stage of the divider, if P_i is enabled, equal to "1", the divider swallows

one period of the input signal when mod_{in} is also equal to high level. The "mod" signal transverses oppositely as the clocking signal does, so that it can be re-synchronized by each stage along the way. When the most significant bit (MSB) P_7 is "0", the last stage is bypassed and has no controlling on the "mod" signal. Thereby the total division ratio is equal to $32+16P_5+8P_4+4P_3+2P_2+P_1$. When P_7 is "1", the circuit functions as a typical swallowing ripple divider, and the division ratio is equal to $64+32P_6+16P_5+8P_4+4P_3+2P_2+P_1$. As a result, the total division ratio can be adjusted from 32 to 127.

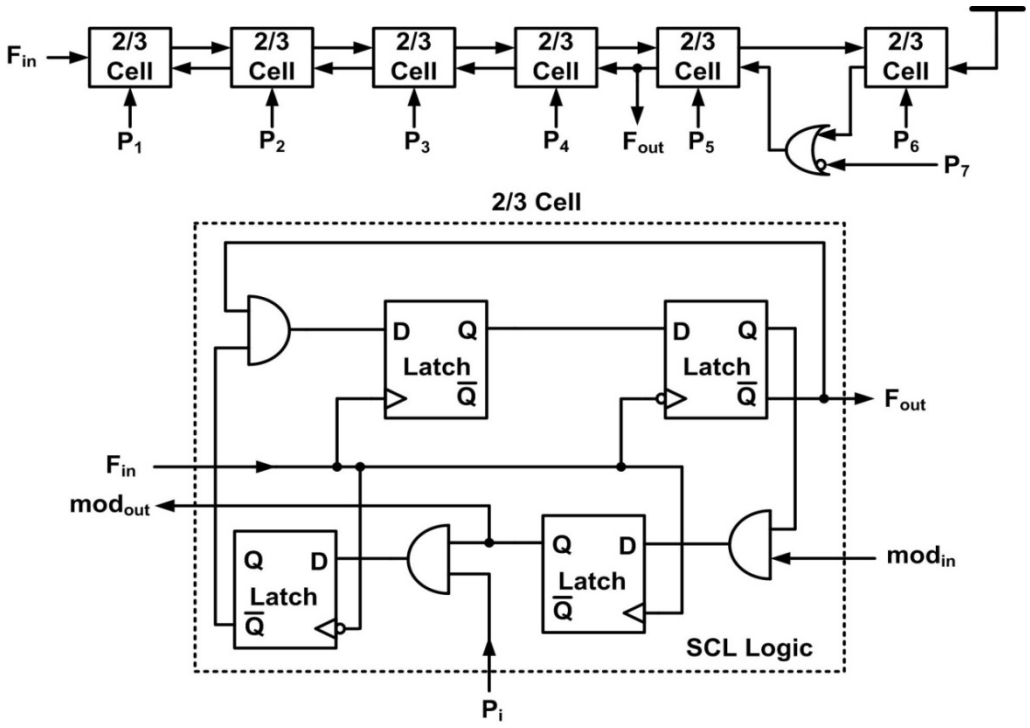


Fig. 8.2 Schematic of multi-modulus divider, divide-by-32~127.

In the SDR FGS, the multi-modulus divider's input can be connected to any point from node "III" to node "IX". A higher frequency is desirable to reduce the quantization step of the delta-sigma modulator and thus the quantization noise. And also all the divide-by-2 dividers preceding the multi-modulus divider have to be opened all the time to lock the loop, which would contribute sub-harmonic spurs at

the FGS's final output if the desired output frequency is higher than the multi-modulus divider's input frequency. However, the higher the input frequency, the larger power the multi-modulus divider needs to consume. As a result, the input frequency is selected to be from 1.5GHz to 3GHz, with an acceptable total current consumption of 6mA.

8.3 PFD and CP

Fig. 8.3 gives the schematic of the implemented PFD and CP with the first 2^{nd}-order loop filter as shown in Fig. 8.1. The tri-state PFD compares the coming edges of the reference clock and multi-modulus divider's output, and generates positive or negative voltage pulse with the pulse width proportional to the phase difference of the two input signals. The generated voltage pulse is then converted into the current pulse by the CP and injected into the loop filter. In practical case, the CP cannot do the conversion infinitely fast due to the switching delay, consequently, if the phase difference between reference clock and divider clock is small enough, the PFD and CP would fail to response to the coming signal, causing the dead zone problem. The open loop gain could be greatly reduced within the dead zone, lowering the noise filtering and even causing stability problem. And as mentioned above, nonlinear response of the phase comparison with the dead zone can also fold the out-band noise of delta-sigma modulator into the loop bandwidth. To eliminate the dead zone, tunable delays Δt_1 and Δt_2 are added into the feedback path of the tri-state PFD. And Δt_1 and Δt_2 can be adjusted to be different, to generate a time offset and further improve the linearity of PFD and CP under the case that the up-current and down-current of CP has mismatches [15][102].

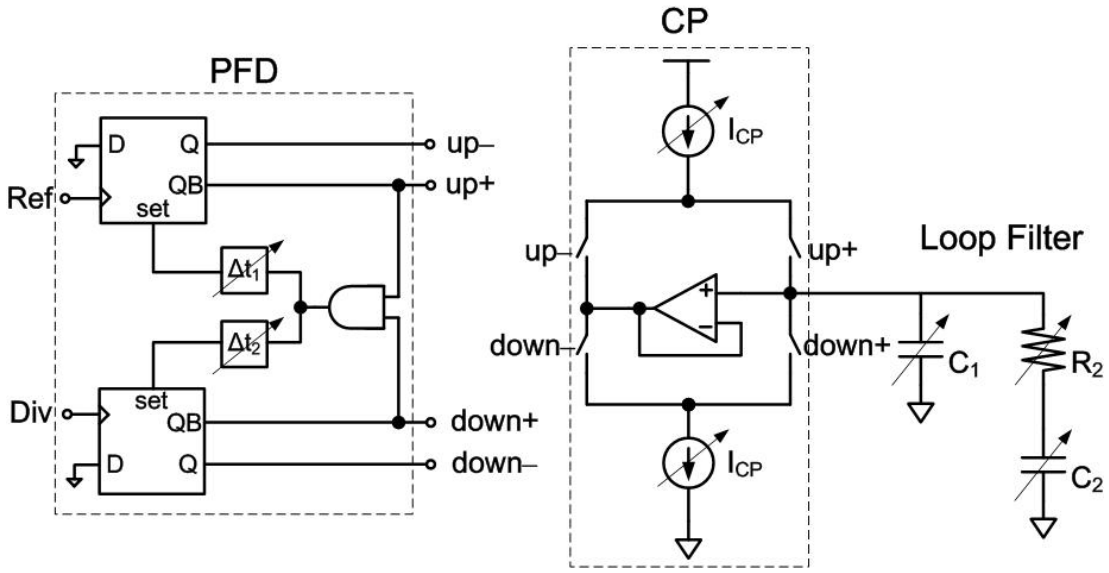


Fig. 8.3 Schematic of PFD, CP with the first loop filter

In Fig. 8.3, the up and down current source are also designed to be independently tunable, to adjust the open loop gain of the PLL and also to calibrate out the up and down current mismatch, which would induce the leakage current and cause reference spur at the VCO's output. To mitigate the charge sharing effect during the switching, a unity gain buffer is added between the two current-steering paths. And all the switches are implemented complementarily to reduce the spur due to the clock feed-through.

8.4 V2I Convertor

Fig. 8.4 shows the schematic of the voltage to current (V2I) convertor with the second loop filter (1^{st}-order) together. By regulating transistor M_1, the current flowing through M_1 can be well defined as V_{in}/R_{eff}, where R_{eff} is the effective resistance of the switched resistor array, which can be adjusted by 4 binary control bits. The converted current is mirrored and passed through SW_1 or SW_2 to control DB QVCO's Lower Band (LB) or Higher Band (HB) bias current, respectively. An

extra current I_{basic} is added into the current mirror network. As such, a minimum required bias current can be provided for the coupling pair of the Q-VCO, to guarantee the Q-VCO operating at quadrature mode and avoid the malfunction of the PLL.

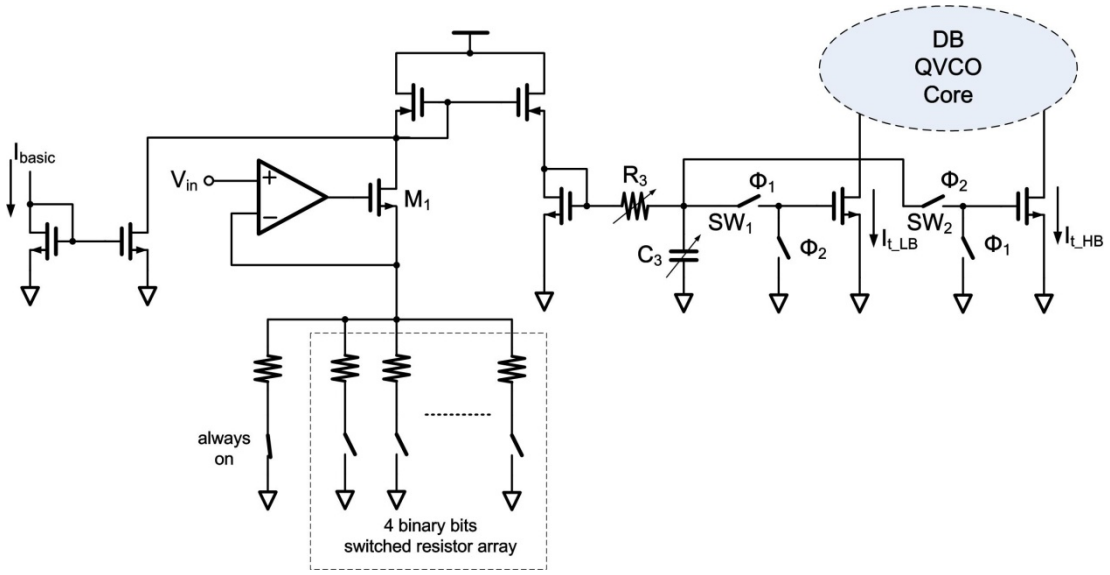


Fig. 8.4 Schematic of voltage-to-current (V2I) convertor with the second loop filter

The noise of the whole circuit needs to be carefully treated. As the circuit is placed after the 2nd order loop filter, the low frequency noise can be filtered out within the loop bandwidth of the PLL. For the V2I convertor, its high frequency noise is filtered out by R_3 and C_3, so the noise transfer function is band-pass characteristic. For the turn-on resistance of SW_1 and SW_2, the noise transfer function is the same as the one of VCO, high-passed. To reduce the noise contribution, the turn-on resistance has to be minimized. Unfortunately, this issue is not addressed during the tape-out. Small sized complementary switches are used for both SW_1 and SW_2, with the NMOS' W/L only being 2μm/0.12 μm and PMOS' W/L only being 5μm/0.12 μm. Spectre-RF Simulations show that the turn-on resistor contributes a typical value of as large as 50% of the QVCO's total noise power at 3MHz offset,

resulting in 3dB QVCO's phase noise degradation. The problem can be simply solved by increasing the switch size, as the induced parasitic is neglect able compared to C_3. By increasing the size to 20μm/0.12 μm for NMOS and 50μm/0.12 μm for PMOS, the contribution can be reduced to around 7%, equivalent to 0.32dB phase noise degradation. If increasing the size to 40μm/0.12 μm for NMOS and 100μm/0.12 μm for PMOS, the phase noise degradation can be reduced to less than 0.2dB.

8.5 Loop Dynamics

8.5.1 Transfer Function

The PLL can be conveniently analyzed by assuming that each building block operates linearly within a small range around the locking point. This linear approach is also proved to be accurate for fractional-N synthesizer with delta-sigma modulation [103].

Fig. 8.5 shows the linear model of the frequency synthesizer in frequency domain. The PFD and CP convert the input phase difference to a current signal by simply multiplying a coefficient K_D, which is equal to $I_{CP}/(2\pi)$ for the tri-state PFD. The current signal flows into the loop filter and corresponds to a controlling voltage of the VCO by multiplying the filter's impedance Z(s). Since phase is the accumulation of frequency, through the VCO, the controlling voltage is converted back to a phase signal by multiplying the coefficient K_{VCO}/s, where K_{VCO} is the gain of VCO with unit of rad/(S•V). At last, the divider divides down the VCO's output frequency and thus also the phase by N. Noticed that, in this model, the second loop filter in Fig. 8.1 is swapped with the V2I convertor, to allow the V2I convertor

combined with the dual-band QVCO (more exactly, CCO, current-controlled oscillator), with a linear transfer function of K_{VCO}/s. By doing so, the transfer functions of most building blocks remain exactly the same, except for the V2I convertor. The noise transfer function would become high-pass like from the original band-pass like. Simulation shows that, with the band-pass characteristic, the noise of V2I convertor is neglect ably small compared to the QVCO's noise, thereby, the modification of such noise does not affect the accuracy of noise analysis.

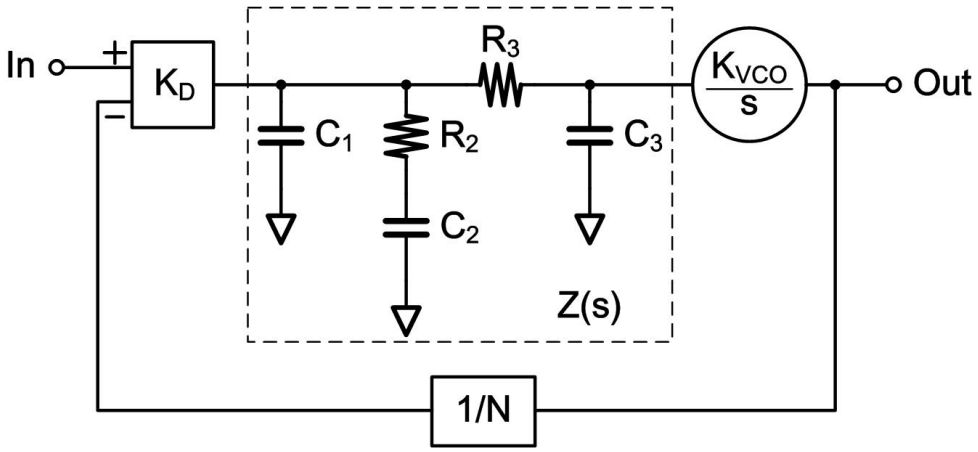


Fig. 8.5 Linear mode of frequency synthesizer

The open loop transfer function G(s) is equal to

$$G(s) = \frac{K_D K_{VCO} Z(s)}{s} \tag{8.1}$$

And the closed loop transfer function CL(s) is given by

$$CL(s) = \frac{G(s)}{1+G(s)H} \tag{8.2}$$

where H denotes the gain of the feedback path, equal to 1/N.

The loop bandwidth of the PLL ω_c is the angle frequency where the feed-forward gain is equal to unity, which is expressed as

$$|G(s)H| = 1 \tag{8.3}$$

Considering the transfer functions (TFs) for different sources, for the reference

and the divider, the TF is equal to CL(s). Since within the loop bandwidth, the open loop gain G(s) is typically very large to minimize the phase error, thereby CL(s) is approximate as N. While at frequencies much higher than ω_c, since G(s) is very small, CL(s) is approximated as G(s). As a result, the transfer function of reference and divider is low pass characteristic. The transfer function of PFD and CP is equal to $CL(s)/K_D$, has the similar characteristic with CL(s). The transfer function of VCO is equal to CL(s)/G(s), written as 1/(1+G(s)H). It is approximated as N/G(s) within the loop bandwidth and close to 1 at frequencies much higher than ω_c. Thereby, the TF of VCO is high pass characteristic.

8.5.2 Loop Filter Calculation

Because the order of delta-sigma modulator (MASH 1-1-1) is equal to 3, the order of loop filter is also selected to be 3 to make the roll-off of the out-band quantization noise match with the one of the VCO. With given loop bandwidth ω_c and phase margin φ, the parameters of the 3rd order loop filter cannot be fixed, and different parameter combinations are available. The calculation of the loop filter follows the procedures provided in [86], for completeness of the dissertation, it is reviewed here.

The impedance of the 3rd order loop filter can be derived as

$$Z(s) = \frac{1+T_2 s}{s(A_2 s^2+A_1 s+A_0)} \tag{8.4}$$

Or rewritten in the form of

$$Z(s) = \frac{1+T_2 s}{A_0 s(1+T_1 s)(1+T_3 s)} \tag{8.5}$$

with explicitly denoting the zero and pole locations.

Considering that C_2 is typically much larger than C_1 and C_3 to stabilize the loop,

the coefficients can be calculated as follows

$$A_0 = C_1 + C_2 + C_3 \tag{8.6}$$

$$T_1 \approx \frac{R_2 C_2 C_1}{A_0} \tag{8.7}$$

$$T_2 = R_2 C_2 \tag{8.8}$$

$$T_3 \approx R_3 C_3 \tag{8.9}$$

$$A_1 = A_0(T_1 + T_3) \tag{8.10}$$

$$A_2 = A_0 T_1 T_3 \tag{8.11}$$

At first, the two pole locations can be correlated with a fixed ratio, a good starting point is assumes T_3=0.5T_1. And then the phase margin φ can be calculated as

$$\varphi = \tan^{-1}(\omega_c T_2) - \tan^{-1}(\omega_c T_1) - \tan^{-1}(\omega_c T_3) \tag{8.12}$$

Another relationship is obtained by setting the derivative of φ equal to zero, so that the phase margin can be insensitive to the variation of the loop bandwidth. This gives the following equation

$$T_2 \approx \frac{2}{3\omega_c{}^2 T_1} \tag{8.13}$$

where the approximations are made that $\omega_c T_1 \ll 1$ and $\omega_c T_2 \gg 1$, which is typically true for a PLL with sufficient phase margin.

Taking Eq. (8.13) into Eq. (8.12), T_1 can be solved approximately as

$$T_1 \approx \frac{2\,[\sec(\varphi) - \tan(\varphi)]}{3\omega_c} \tag{8.14}$$

Therefore, T_1, T_2 and T_3 are all solved.

Next, making use of the definition of the unity gain frequency ω_c, the Eq. (8.3), and using Eqs. (8.1) and (8.5), A_0 can be solved as below

$$A_0 = \frac{K_D K_{VCO}}{N\omega_c{}^2} \sqrt{\frac{1+\omega_c{}^2 T_2{}^2}{(1+\omega_c{}^2 T_1{}^2)(1+\omega_c{}^2 T_3{}^2)}} \tag{8.15}$$

So far, 4 variables including A_0, T_1, T_2 and T_3 have been solved. But in order to find the final solution of the 3rd order loop filter, it still needs one extra identity. This can be done by choosing a C_1 to maximize the value of C_3, by doing so, the impact of VCO's parasitic capacitance can be minimized and the thermal noise of R_3 can maximally filtered out. It is also proved that the value of C_1 for maximum C_3 is very close to the value of C_1 for minimum R_3, which shows that such choice is optimal for minimizing R_3's noise [86]. Thereby, C_1 can be obtained as

$$C_1 = \frac{A_2}{{T_2}^2}\left(1 + \sqrt{1 + \frac{T_2}{A_2}(T_2 A_0 - A_1)}\right) \tag{8.16}$$

And other parameters of the loop filter can be solved as below

$$C_3 = \frac{-{T_2}^2 {C_1}^2 + T_2 A_1 C_1 - A_2 A_0}{{T_2}^2 C_1 - A_2} \tag{8.17}$$

$$C_2 = A_0 - C_1 - C_3 \tag{8.18}$$

$$R_2 = \frac{T_2}{C_2} \tag{8.19}$$

$$R_3 = \frac{A_2}{C_1 C_3 T_2} \tag{8.20}$$

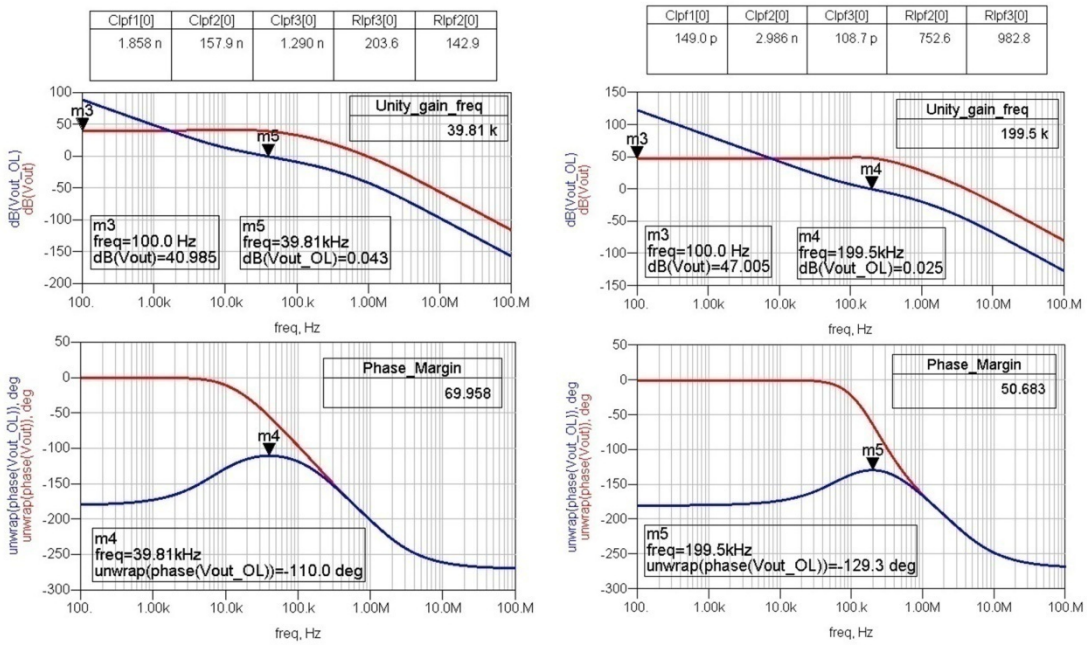
where A_1 and A_2 have been given by Eq. (8.10) and Eq. (8.11).

8.5.3 Behavioral Simulation of PLL

The calculation results are verified through the AC simulation in Agilent's Advanced Design System (ADS). The characteristics of the PFD, CP, VCO and dividers are modeled linearly through ideal voltage controlled voltage source, or voltage controlled current source.

With the equations in Section 8.5.2, the parameters of the loop filter are calculated using 40KHz loop bandwidth, 70° phase margin, 1mA CP current, 2π*200MHz/V K_{VCO} and total division number of 112 for the typical setting of the

PLL's narrow bandwidth mode. Fig. 8.6(a) shows the simulated frequency responses of the PLL, with the calculated filter component values listed at the top. It can be seen that simulated unity gain frequency and the phase margin are very close to the expected values, which proves the accuracy of the derived equations from [86]. Fig. 8.6(b) shows the simulated frequency responses with the typical setting of the PLL's wide loop bandwidth mode, where 200KHz loop bandwidth is used with 51° phase margin for the fastest channel settling response [104], and with 1mA CP current, 2π*400MHz/V K_{VCO} and a total division number of 224.



(a) (b)

Fig. 8.6 Simulated frequency responses of the SDR FS with, (a) 40KHz loop bandwidth and 70° phase margin, (b)200KHz loop bandwidth and 51° phase margin

The phase noise performance is simulated by adding frequency dependent current noise sources and voltage noise sources into the behavioral loop. These noise sources are set with the measured or simulated building block's noise data at different offset frequencies. Thereby, the noise behavior of each building block can be accurately depicted and simulated with the corresponding noise transfer functions

provided by the loop, as long as sufficient data points are used to plot the noise curve versus the offset frequency.

The loop bandwidth needs to be optimized carefully, because it decides all the performance of the PLL. A small loop bandwidth is helpful to depress the reference spur, the delta-sigma modulator's quantization noise, and allow less RMS phase error due to the reference referred noise (including noise from the reference source, PFD and CP, dividers). However, a reduced loop bandwidth also results in longer settling time, larger loop filter components and less suppression on the VCO's noise at low frequency offset, which is critical for CMOS process due to its inferior flicker noise. The trade-off related to the settling time can be greatly relaxed by applying adaptive bandwidth technique [105] or dual phase comparing path architecture [106]. Therefore, in the PLL design, the loop bandwidth is optimized to achieve minimum RMS phase error for each standard, under the condition that the reference spur is reasonably below -55dBc and the spot phase noise of the synthesizer can meet the requirement in Table 3.1.

Fig. 8.7 shows the simulated FGS output phase noise at 1.85GHz carrier frequency for DCS/PCS standard. The loop bandwidth is set around 40KHz to compromise different trades-off. It can be seen that, the total phase noise, as plotted using the thick red line, is mainly dominated by the VCO's phase noise from 1KHz up to 10MHz frequency offset. At lower offset frequencies below 1KHz, the phase noise is dominated by the reference noise (generated by Agilent's signal generator E5287D). And at offset frequencies larger than 10MHz, the phase noise is limited by the noise floor of divider-B, because the FGS output point is taken at the output of divider-B, its noise transfer function is also high-passed similar to the one of VCO. The total RMS phase error within the channel bandwidth is 0.663°. To reduce this

number the loop bandwidth needs to be increased to suppress the VCO's close-in phase noise. However, this is prohibited by the spot noise requirement of -139.5dBc/Hz at 3MHz for this standard. If the bandwidth is increased, the spot noise would be degraded due to the noise from delta-sigma modulator. Nevertheless, this trade-off can be relaxed by cancelling out the deterministic quantization noise as mentioned in Section 8.2, at some expense of chip area and power consumption.

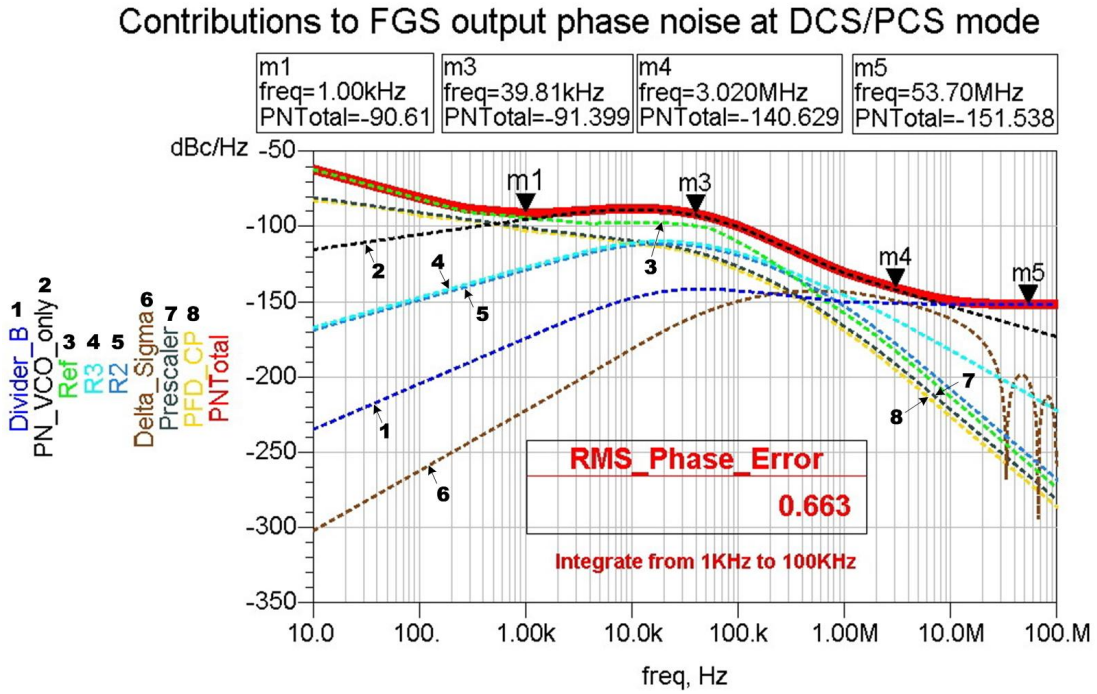


Fig. 8.7 Simulated the FGS output phase noise at 1.85GHz DCS/PCS mode

Fig. 8.8 shows the simulated FGS output phase noise at 2.45GHz carrier frequency for WLAN 11b/g mode. The loop bandwidth is set to be around 200KHz to optimize the RMS phase error. It is seen that with the larger loop bandwidth, the close-in phase noise is mainly contributed by the reference noise, which limits the in-band phase noise at around -95dBc/Hz. This noise contribution would become even more significant when the FGS output frequency is further increased, for example at 802.11a or UWB mode, because the increased division ratio results in

further amplification of the reference noise. The out-band phase noise is mainly contributed from the Q-VCO, delta-sigma modulator as well as the divider-A and divider-B at offset frequencies more than 30MHz. The integrated phase noise, within 10MHz, results in a RMS phase error of 0.731°.

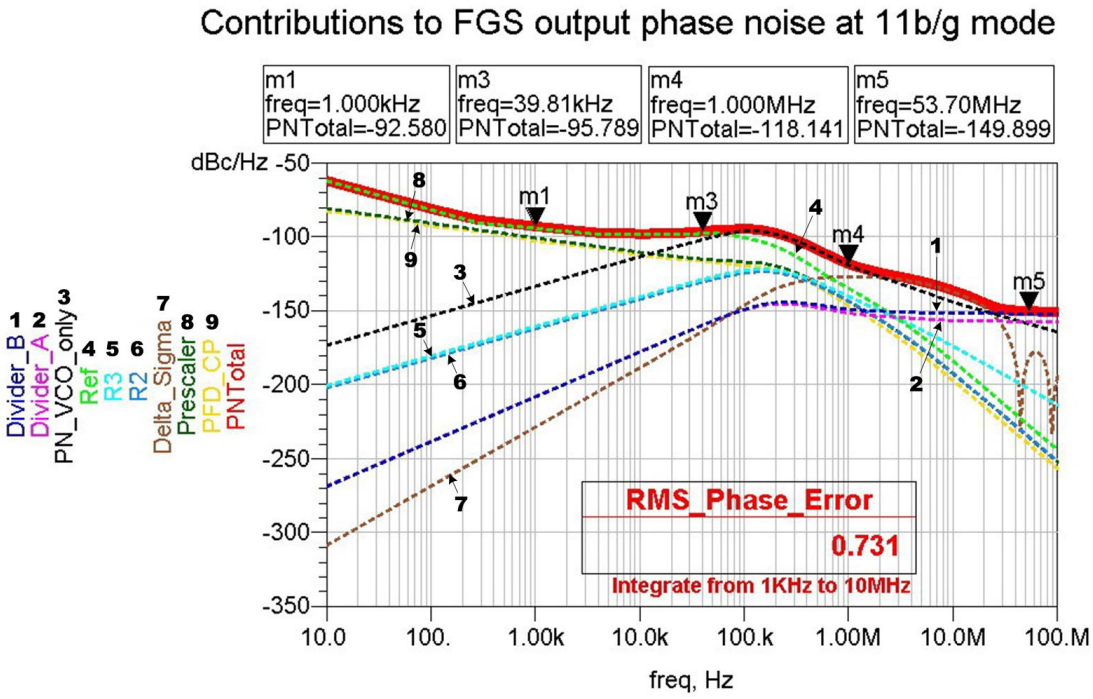


Fig. 8.8 Simulated the FGS output phase noise at 2.45GHz 802.11b/g mode

Chapter 9

Experimental Results of The SDR Frequency Generation System

9.1 System Integration

To verify the open loop performance of SDR FGS, a preliminary version was firstly fabricated in a 0.13μm CMOS technology. Fig. 9.1 shows the block diagram. The 60GHz output x27 ILFM chain is included for the direct-conversion MM-Wave transceiver for the standard 802.15.3c.

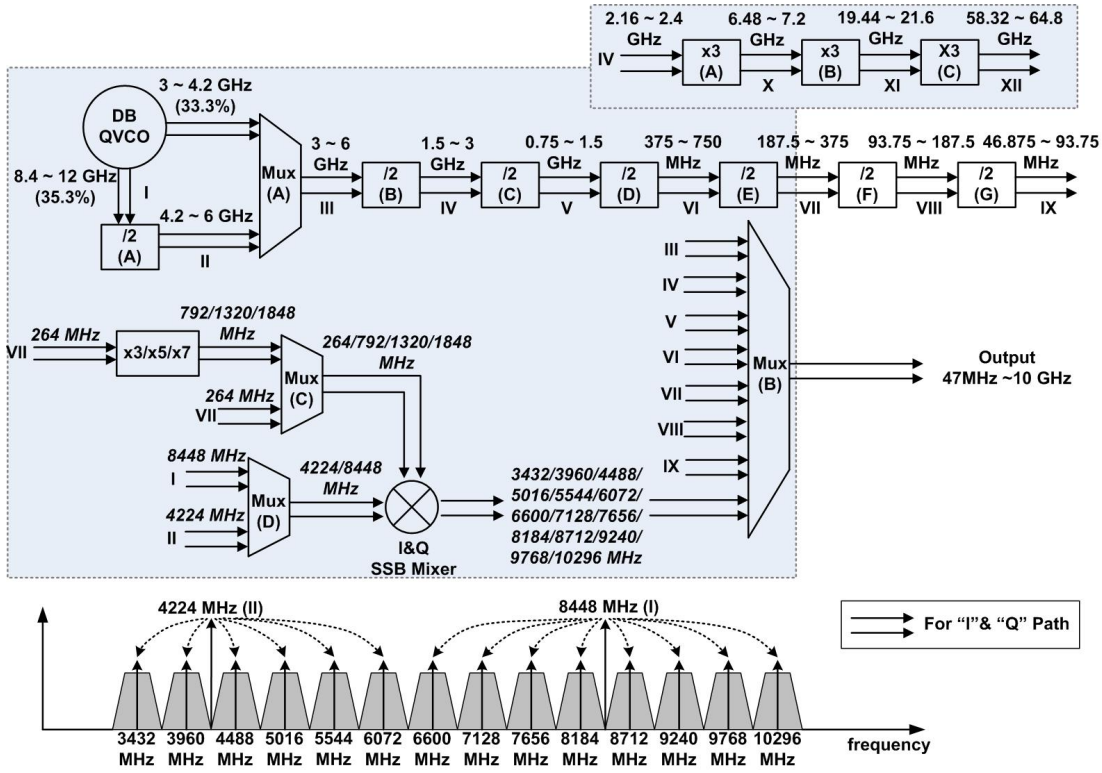


Fig. 9.1 Block diagram of preliminary SDR FGS fabricated in 0.13μm CMOS

The die photograph of the preliminary FGS chip is shown in Fig. 9.2. The open loop parts of the FGS are integrated within an area of 2mm by 1.2mm.

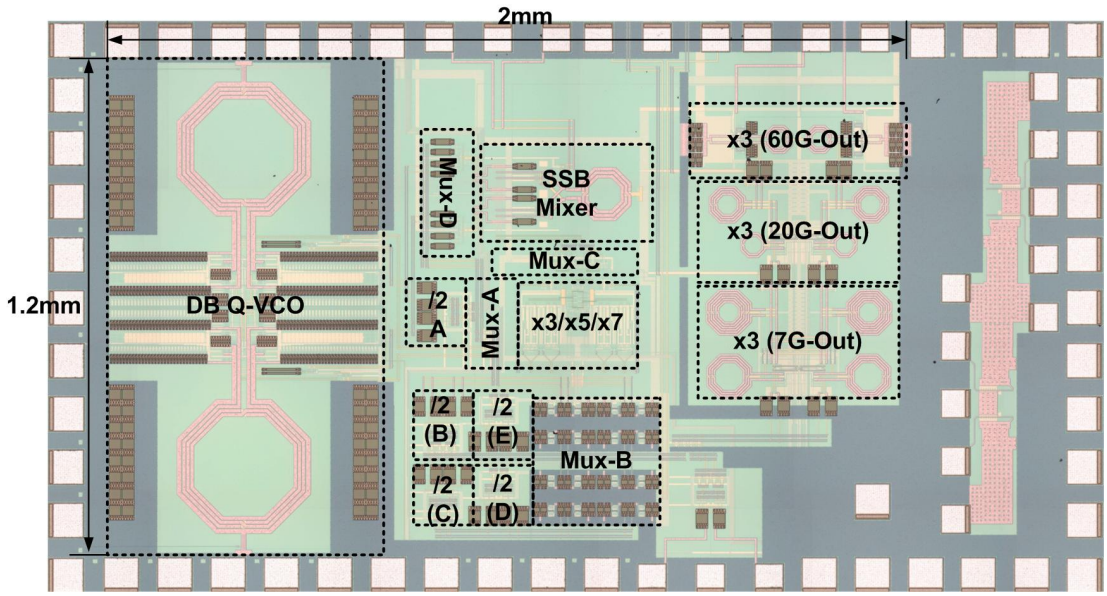


Fig. 9.2 Die photograph of preliminary SDR FGS fabricated in 0.13μm CMOS

With affirmative measurement results from the preliminary open-looped version, the final SDR FGS version is integrated and fabricated in the 0.13μm CMOS. Fig. 9.3 shows the block diagram. A reconfigurable phase locked loop is implemented with flexible loop dynamic adjustment as described in Chapter 8. Peak calibration circuits, introduced in Section 7.3.4, are integrated on chip to automatically calibrate the peak frequencies of 3 stage ILFMs in the chain, which generates the 20GHz and 40GHz LO frequencies for the dual-conversion MM-Wave transceiver. An up-conversion SSB mixer is integrated as the transmitter modulator to verify the IQ accuracy of the generated LO signals from the FGS. Besides, to mitigate the performance degradation due to the layout mismatches and process variations, other tunings like IQ coarse tuning, feed-through tuning are also implemented on chip with the control signals applied externally. Two groups of shift registers are incorporated to provide 120 digital control bits for the system, for simplicity, they are not drawn in Fig. 9.3.

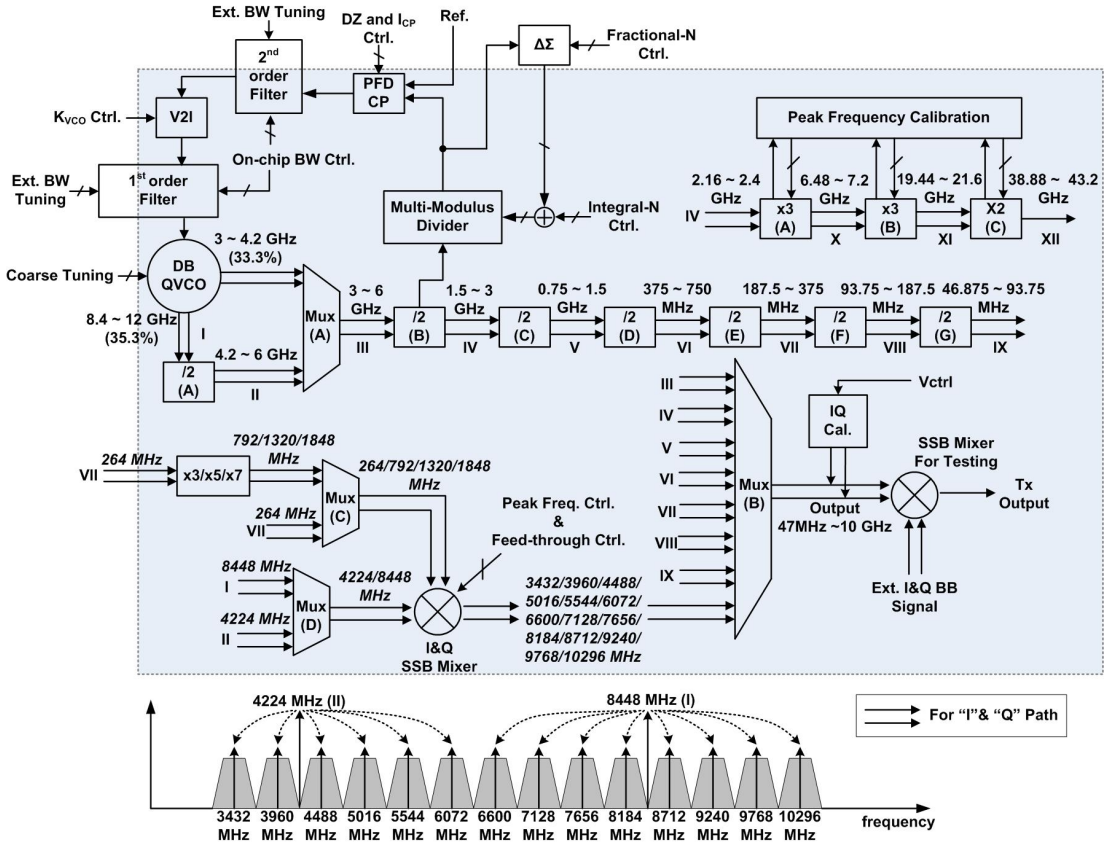


Fig. 9.3 Block diagram of the final SDR FGS fabricated in 0.13μm CMOS

Fig. 9.4 shows the die photo of the final SDR FGS. The whole system occupies an area of 2.5mm by 1.2mm.

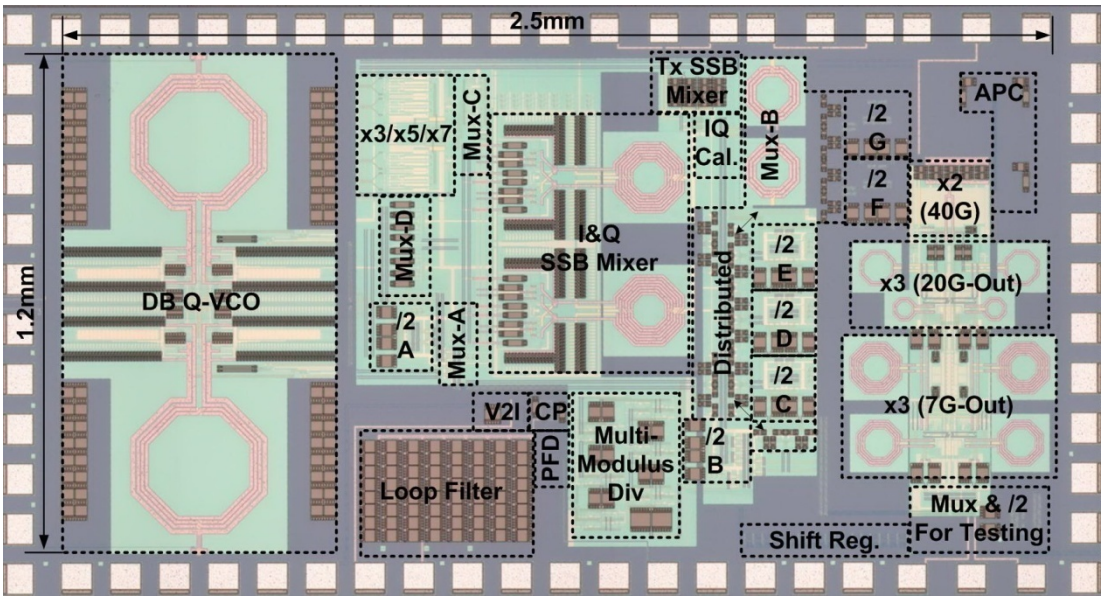


Fig. 9.4 Die photograph of final SDR FGS fabricated in 0.13μm CMOS

Based on the functionalities, the FGS can be divided into several sub-systems, including the dual-band Q-VCO with the PLL, the SCL divider chain, the x3/x5/x7 ILFM and SSB Mixers for MB-OFDM UWB carrier generation and the ILFM chain with APC for MMW carrier generation. Before the integration of the whole system, each of these sub-systems has been integrated and verified through post-layout simulations, with counting the associated loading effects from other sub-systems. The basic functions of the whole system are verified by the transient simulations. And the phase noise performance is verified through linear simulations in ADS as described in Chapter 8.

9.2 Measurement Setup

Fig. 9.5 shows the onsite photo of the typical FGS measurement setup. The reference signal is generated from Agilent's signal generator E8257D with close-in phase noise around -133dBc/Hz at 20KHz frequency offset. The output signals of the FGS are obtained by probing the die pads and measured by Agilent's spectrum analyzer E4440A with phase noise measurement personality. An oscilloscope is used to monitor the loop filter's control voltage and roughly measure the settling time of the PLL. I&Q baseband signals are generated by a vector signal generator (Agilent's E4438C), for measuring the side-band rejections at the output of the on-chip up-conversion SSB mixer. The digital controlling signals of the FGS are provided by a PC-controlled pattern generation device, and the critical analog biases are provided through an external PCB with tunable voltage or current biasing.

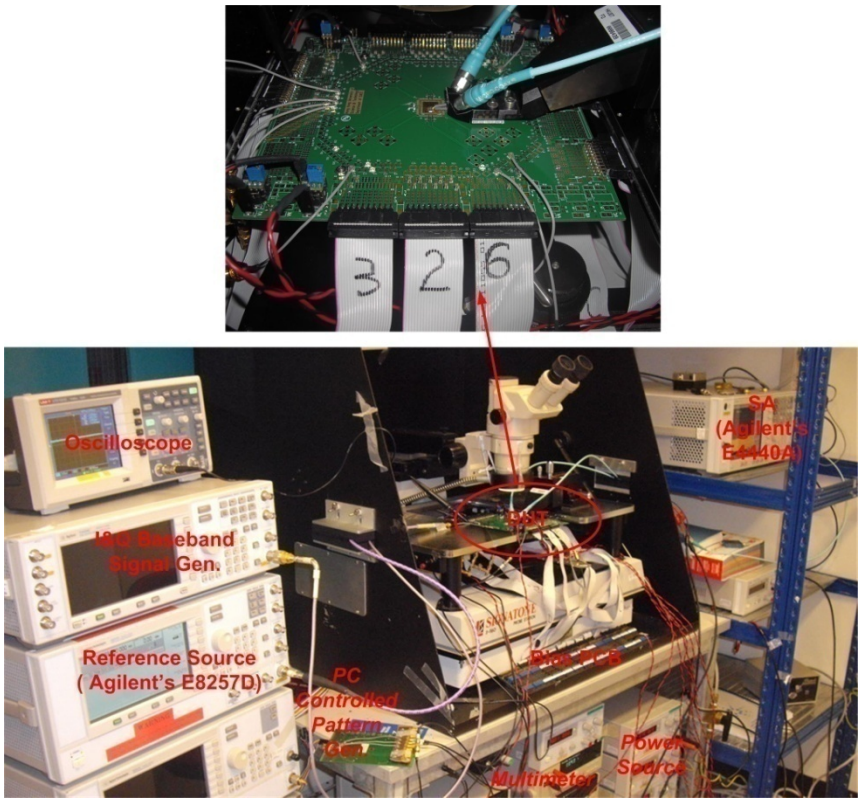


Fig. 9.5 On-site measurement setup of the SDR FGS

9.3 Coverred Frequency Range

In the measurement, the SDR FGS can successfully generate I&Q output signals continuously from 42MHz to 6.2GHz and from 18GHz to 22.5GHz, and differential output signals continuously from 36.9GHz to 44.1GHz. The FGS can also successfully generate all the 14-band carriers for the MB-OFDM UWB, from 3432MHz to 10296MHz with 528MHz spacing. Fig. 9.6 summarizes the covered frequency range by the SDR FGS in a log scale.

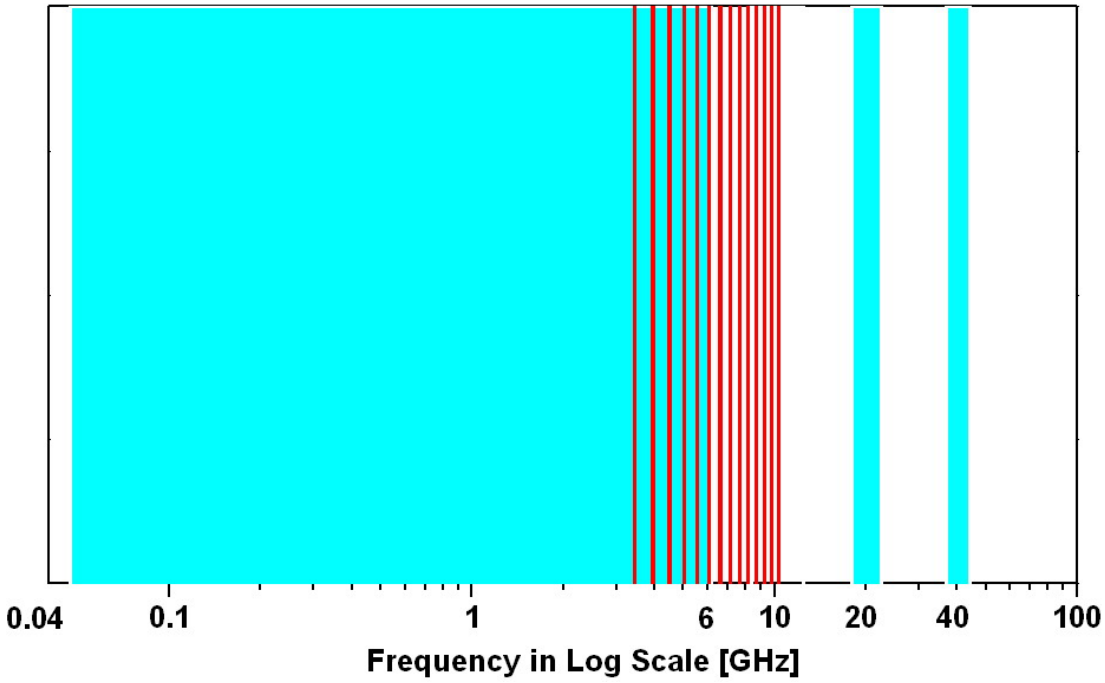


Fig. 9.6 Covered frequency range by the experimental FGS

9.4 Phase Noise

9.4.1 Open Loop Phase Noise

The open loop phase noise with free-running VCO was measured with the preliminary version of the SDR FGS, to verify the FGS' out-band phase noise values for different standards.

Fig. 9.7 shows the measured open loop phase noise of the carriers for WLAN, the green, blue and red curves are for the carrier frequencies of 2.4GH, 5.2GHz and 5.8GHz, respectively. The phase at 1MHz offset varies from -113dBc/Hz to -119dBc/Hz.

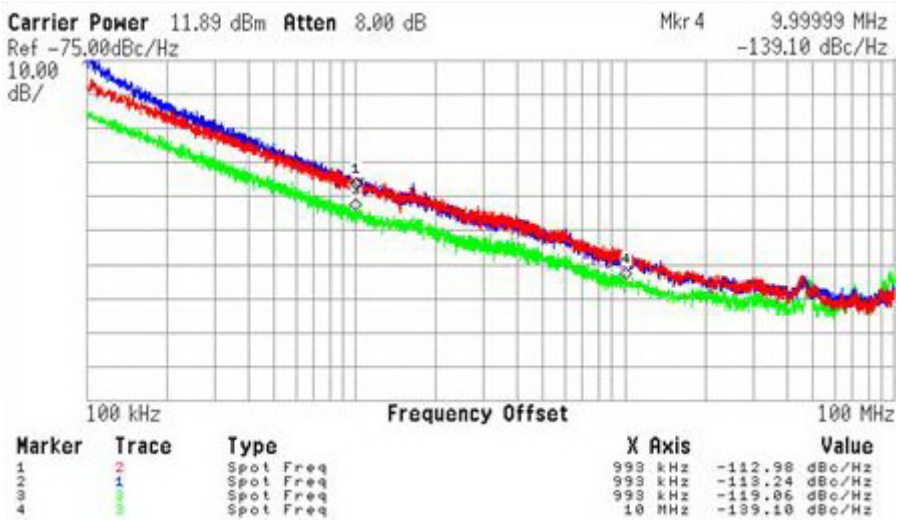


Fig. 9.7 Measured open loop phase noises of the carriers for WLAN

Fig. 9.8 shows the measured open loop phase noise of the carriers for MB-OFDM UWB standard, the blue, green and red curves are for the carrier frequencies of 3.4GH, 5GHz and 10.3GHz, respectively. The phase at 1MHz offset varies from -102dBc/Hz to -110.6dBc/Hz.

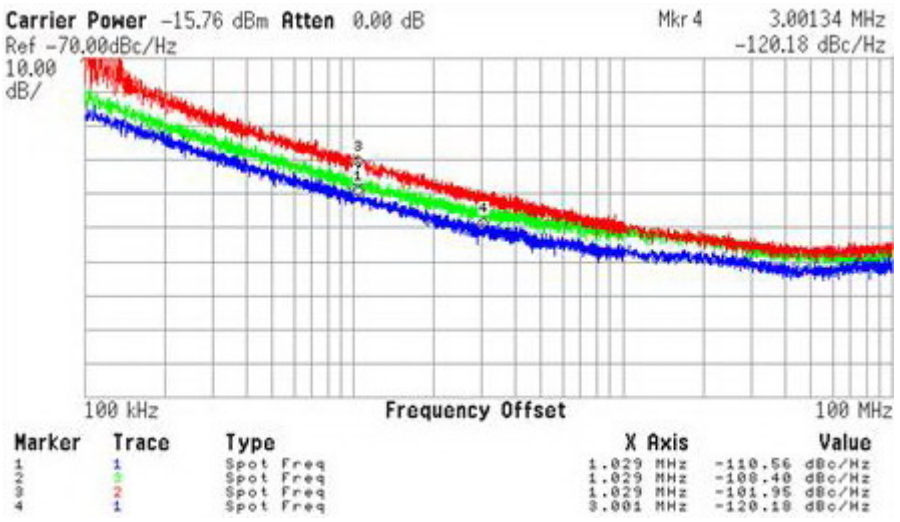


Fig. 9.8 Measured open loop phase noises of the carriers for MB-OFDM UWB

Fig. 9.9 shows the measured open loop phase noise of the carriers for Wimax. The green, blue and red curves are for the carrier frequencies of 2.4GH, 3.4GHz and 5.2GHz, respectively. The phase at 1MHz offset varies from -113dBc/Hz to -123.4dBc/Hz.

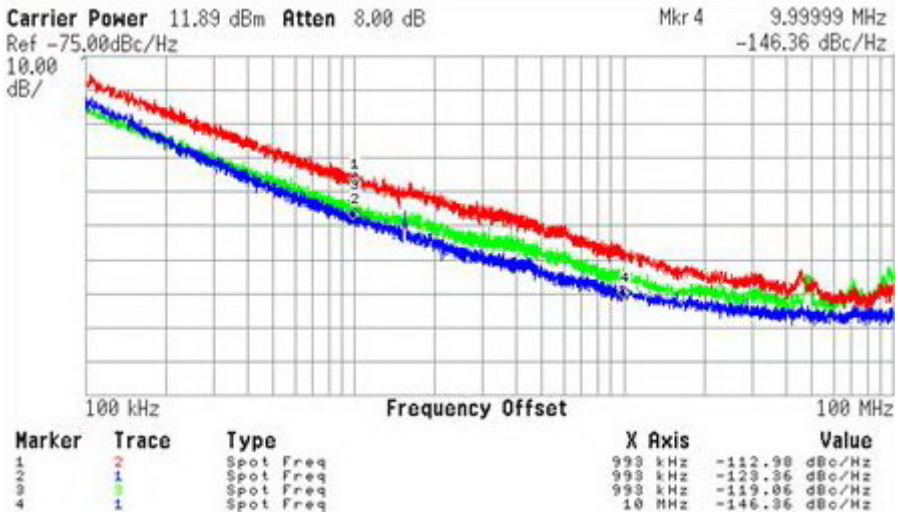


Fig. 9.9 Measured open loop phase noises of the carriers for Wimax

Fig. 9.10 shows the measured open loop phase noise of the carriers for cellular standards. The blue, red and green curves are for the carrier frequencies of 900MHz, 1.7GHz and 1.9GHz, respectively. The phase at 3MHz offset varies from -140.5dBc/Hz to -144.7dBc/Hz.

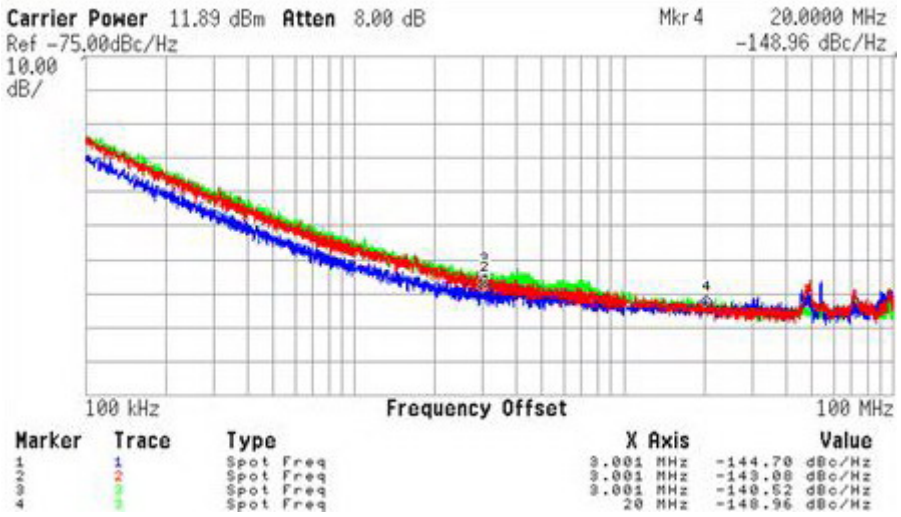


Fig. 9.10 Measured open loop phase noises of the carriers for cellular standards

Fig. 9.11 shows the measured open loop phase noise of the carriers for DTV applications. The yellow, cyan and purple curves are for the carrier frequencies of 470MHz, 498MHz and 870MHz, respectively. The phase at 1MHz offset varies from -128.1dBc/Hz to -135.8dBc/Hz.

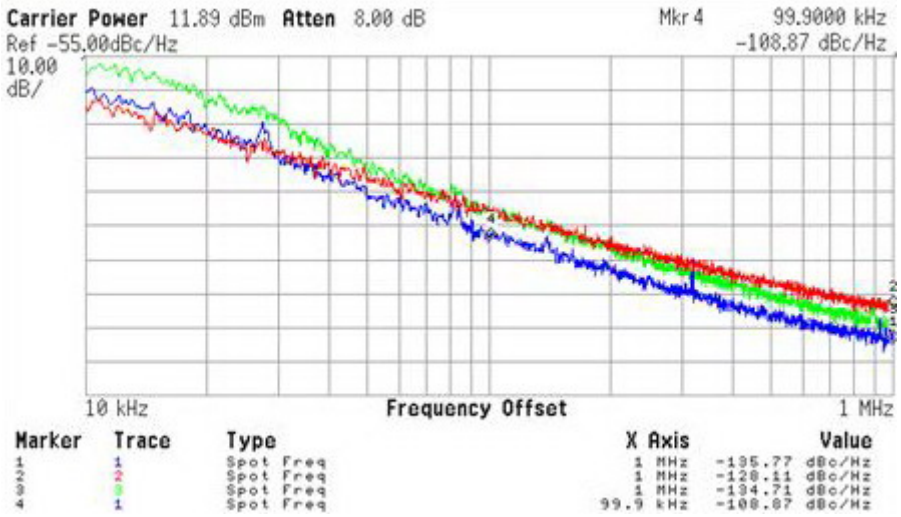


Fig. 9.11 Measured open loop phase noises of the carriers for DTV

9.4.2 Close Loop Phase Noise

When measuring the close loop phase noise of the final SDR FGS, the loop bandwidth is adjusted to achieve minimum RMS phase error for different standards as discussed in Section 8.5.3.

9.4.2.1 DTV

Fig. 9.12 shows the measured close loop spectrum and phase noise for DTV standard with DB Q-VCO consuming current around 10mA. At different frequency bands, the close-in phase noise at 10KHz offset varies from -91.7 to -107.7dBc/Hz. The out-band phase noise at 1MHz offset is measured as from -119.9 to -134.7dBc/Hz. The RMS phase error integrated from 1KHz to 4MHz frequency offset varies from 0.1° to 0.85°.

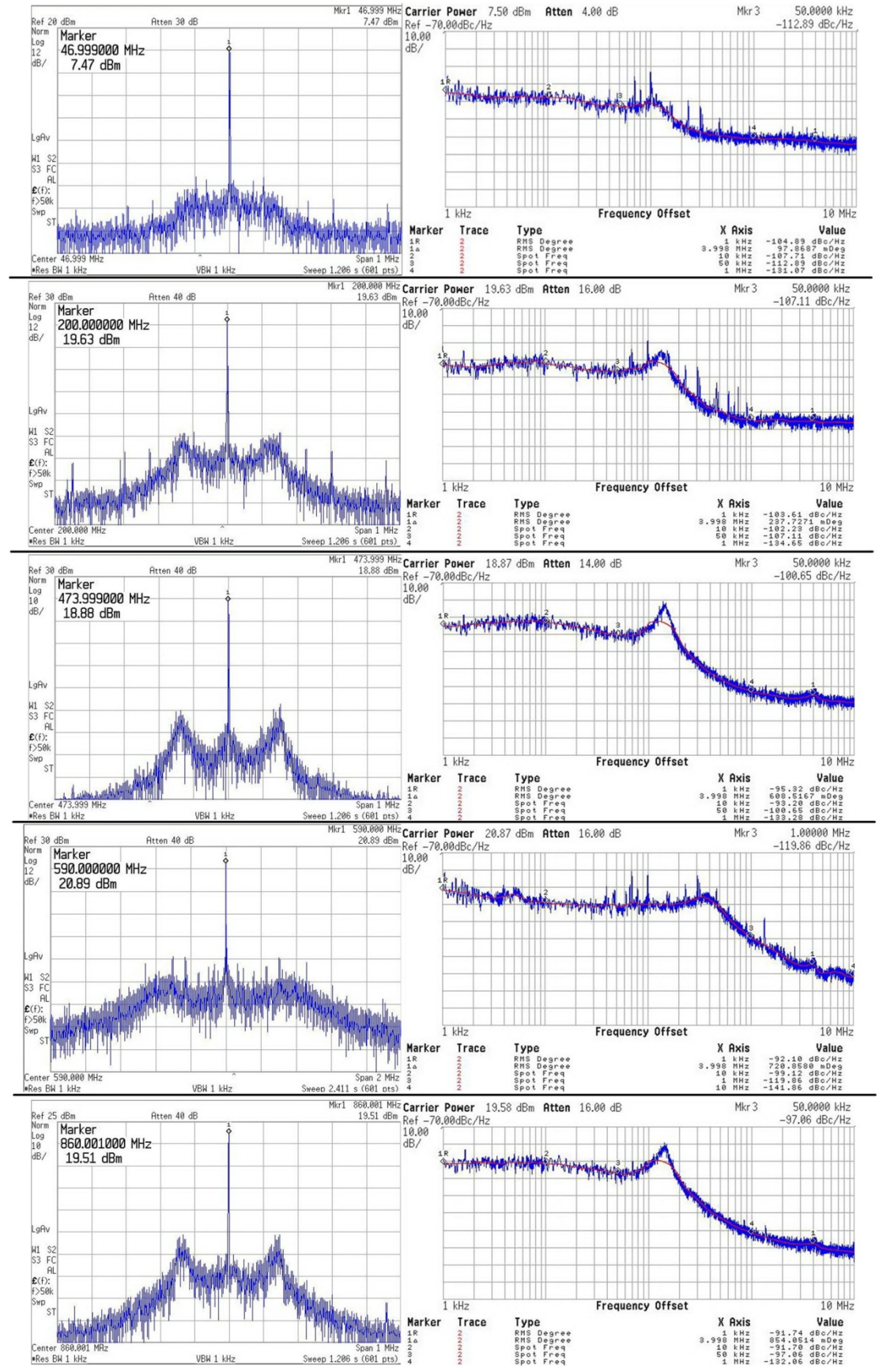


Fig. 9.12 Measured close loop spectrum and phase noise for DTV

9.4.2.2 GSM900

Fig. 9.13 shows the measured close loop spectrum and phase noise for GSM900 with DB Q-VCO consuming current of 20mA. The close-in phase noise at 50KHz offset is -97.9dBc/Hz. The out-band phase noise at 3MHz offset is measured as -141.7dBc/Hz. The RMS phase error integrated from 1KHz to 100KHz frequency offset is 0.4°.

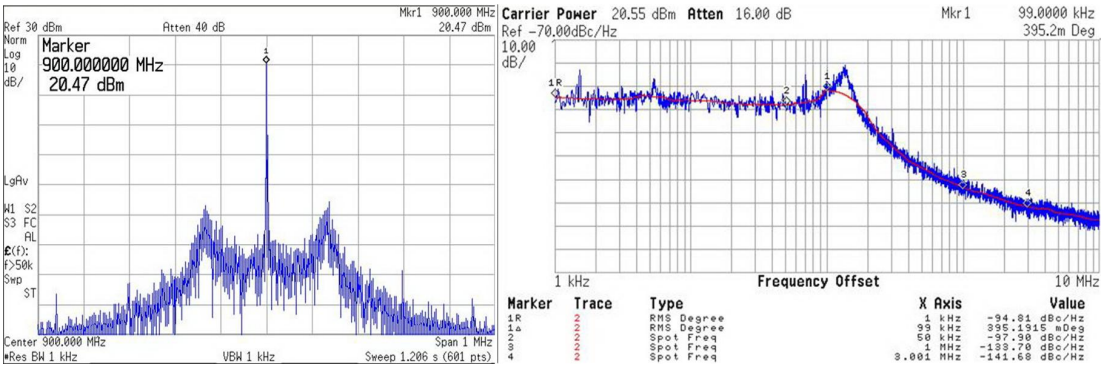


Fig. 9.13 Measured close loop spectrum and phase noise for GSM900

9.4.2.3 DCS/PCS

Fig. 9.14 shows the measured close loop spectrum and phase noise for DCS/PCS with DB Q-VCO consuming current of around 20mA. The close-in phase noise at 50KHz offset varies from -90.6 to -91.3dBc/Hz. The out-band phase noise at 3MHz offset is measured as from -137.2 to -139.6dBc/Hz. Noted that, the phase noise at 3MHz offset are around 3dB worse compared to the open-loop ones, due to the extra noise from the switches in the V2I convertor (refer to Section 8.4). With correcting the design mistake, the FGS' phase noise at 3MHz offset could marginally meet the requirement of DCS/PCS standards, while sufficiently fulfill the GSM900 requirement. Integrated from 1KHz to 100KHz frequency offset, the RMS phase error for the DCS/PCS mode is from 0.97° to 1.06°.

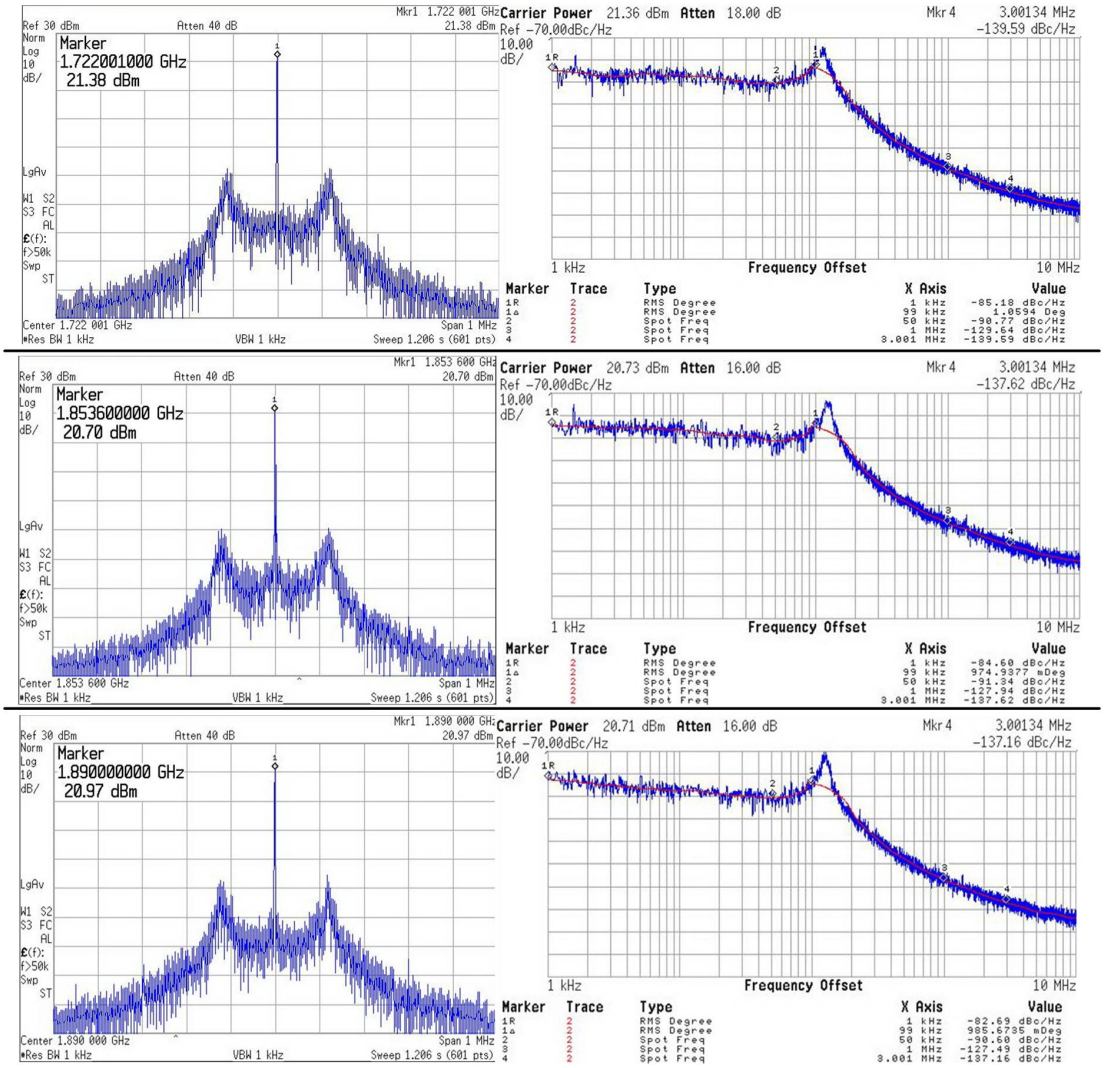


Fig. 9.14 Measured close loop spectrum and phase noise for DCS/PCS

9.4.2.4 UMTS

Fig. 9.15 shows the measured close loop spectrum and phase noise for UMTS with DB Q-VCO consuming current of 20mA. The close-in phase noise at 50KHz offset is -91.1dBc/Hz. The out-band phase noise are -136.3dBc/Hz and -145.7dBc/Hz at 3MHz and 20MHz offset, respectively. The RMS phase error integrated from 1KHz to 2.5MHz frequency offset is 1.32°.

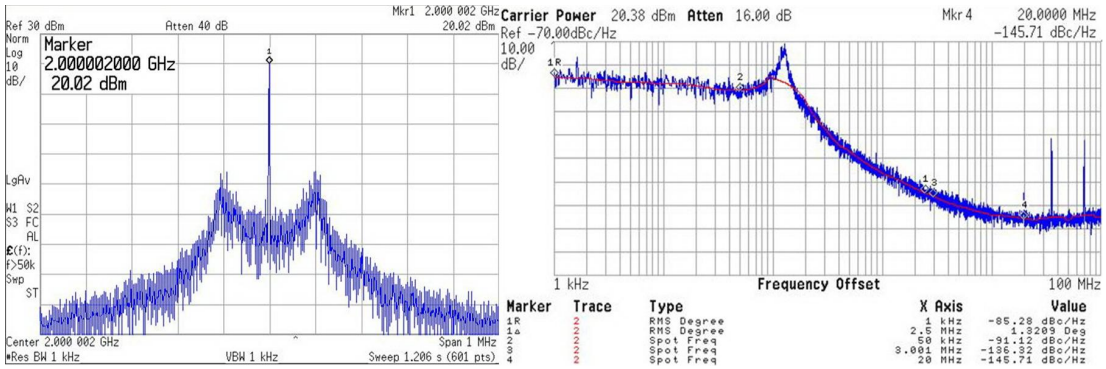


Fig. 9.15 Measured close loop spectrum and phase noise for UMTS

9.4.2.5 RFID

Fig. 9.16 shows the measured close loop spectrum and phase noise for UHF-RFID with DB Q-VCO consuming current of 20mA. The close-in phase noise at 50KHz offset is -96.2dBc/Hz. The out-band phase noise at 3.6MHz offset is measured as -144.3dBc/Hz. The RMS phase error integrated from 1KHz to 50KHz frequency offset is 0.3°.

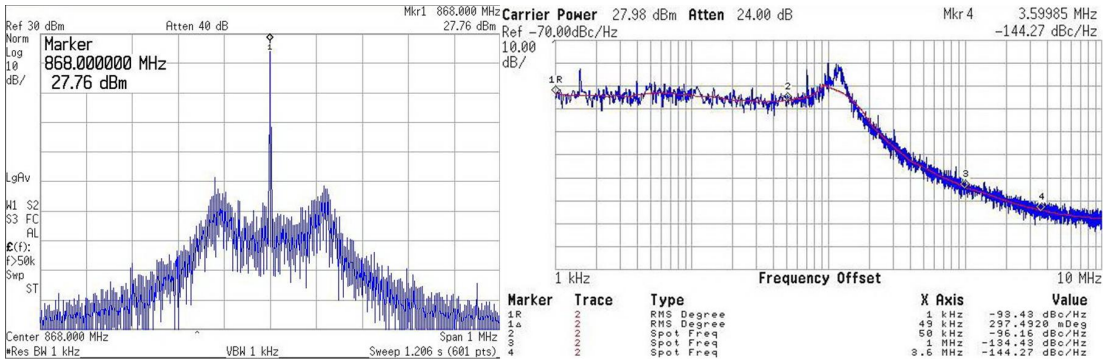


Fig. 9.16 Measured close loop spectrum and phase noise for UHF-RFID

9.4.2.6 DECT

Fig. 9.17 shows the measured close loop spectrum and phase noise for DECT with DB Q-VCO consuming current of 15mA. The close-in phase noise at 50KHz offset is -90.6dBc/Hz. The out-band phase noise at 4.7MHz offset is measured as

-137.9dBc/Hz. The RMS phase error integrated from 1KHz to 864KHz frequency offset is 1.58°.

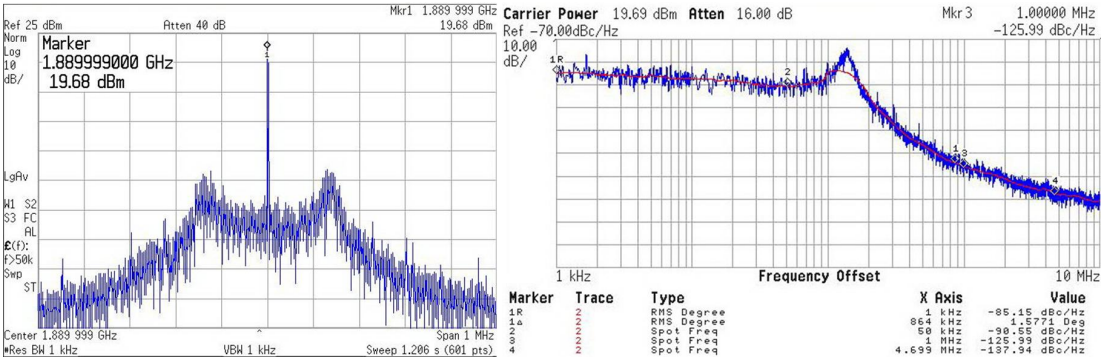


Fig. 9.17 Measured close loop spectrum and phase noise for DECT

9.4.2.7 GPS

Fig. 9.18 shows the measured close loop spectrum and phase noise for GPS with DB Q-VCO consuming current of 17mA. The close-in phase noise at 50KHz offset is -91.5dBc/Hz. The out-band phase noise at 1MHz offset is measured as -130.7dBc/Hz. The RMS phase error integrated from 1KHz to 511KHz frequency offset is 1.08°.

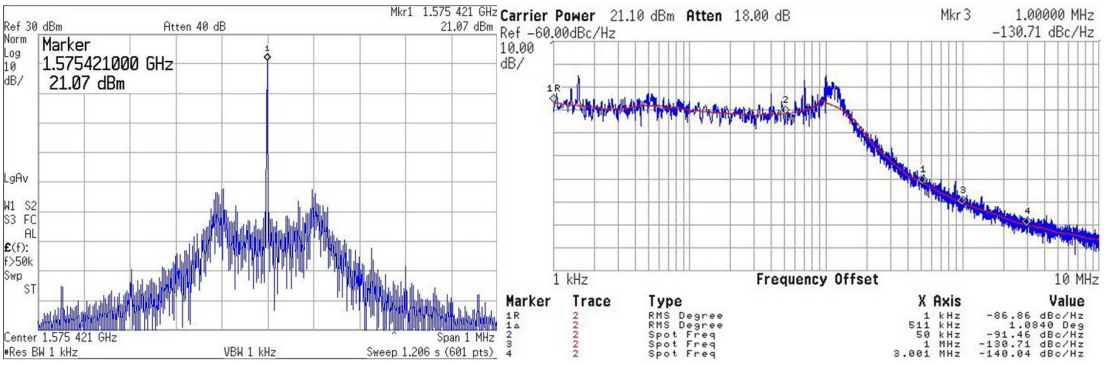


Fig. 9.18 Measured close loop spectrum and phase noise for GPS

9.4.2.8 WLAN

Fig. 9.19 shows the measured close loop spectrum and phase noise for WLAN standard with DB Q-VCO consuming current around 20mA. At different frequency

bands, the close-in phase noise at 100KHz offset varies from -89 to -95.8dBc/Hz. The out-band phase noise at 1MHz offset is measured as from -112.5dBc/Hz to -116.8dBc/Hz. The RMS phase error integrated from 1KHz to 10MHz frequency offset varies from 1.25° to 2.9°. Both the in-band phase noise and the RMS phase error are limited by the reference noise around -133dBc/Hz within the loop bandwidth. The higher the carrier frequency is, the more significantly the reference noise dominates the synthesizer's phase noise performance.

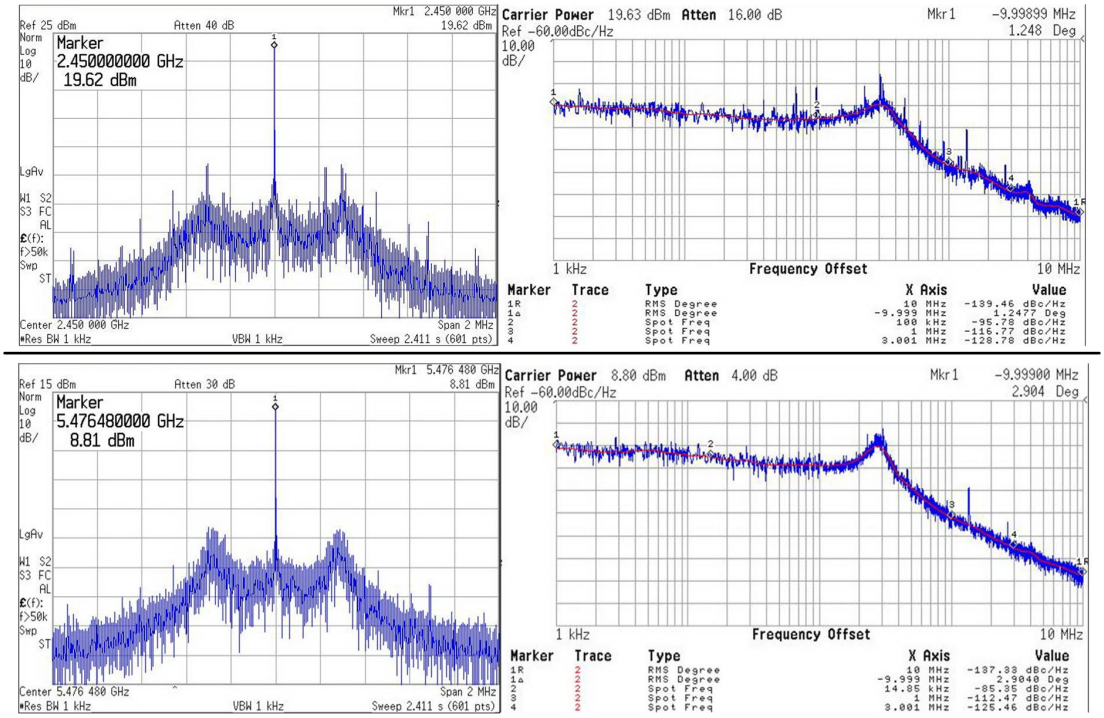


Fig. 9.19 Measured close loop spectrum and phase noise for WLAN

9.4.2.9 Wimax

Fig. 9.20 shows the measured close loop spectrum and phase noise for Wimax standard at 3.4GHz band and 5.2GHz band, when the DB Q-VCO consumes current around 18mA. Referring to the phase noise data from Fig. 9.19 as well, for different bands spanning from 2GHz to 6GHz, the close-in phase noise varies from -85.1 to

-95.8dBc/Hz. The out-band phase noise at 1MHz offset varier from -108.8dBc/Hz to -123.6dBc/Hz. The RMS phase error integrated from 1KHz to 14MHz frequency offset varies from 1.25° to 3.0°.

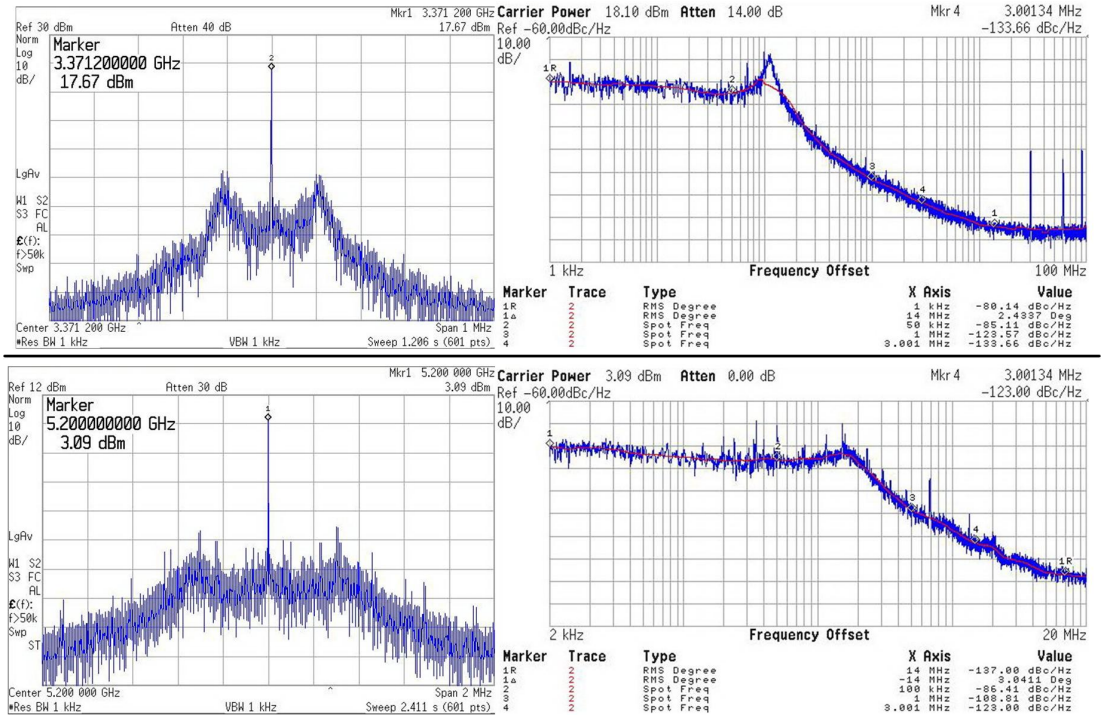


Fig. 9.20 Measured close loop spectrum and phase noise for Wimax

9.4.2.10 Zigbee and Bluetooth

Fig. 9.21 shows the measured close loop spectrum and phase noise at 900MHz band and 2.4GHz band, for low-end low-power standards Zigbee and Bluetooth. The Q-VCO's power consumption is reduced to around 6mA. The close-in phase noise varies from -80dBc/Hz to -95dBc/Hz. The out-band phase noise at 10MHz offset for Zigbee standrad is measured from -129.3dBc/Hz to -140.8dBc/Hz. The phase noise at 500KHz offset for Bluetooth is measured as -90.3dBc/Hz. The RMS phase error is 1.19° and 4.87°, for 900MHz band and 2.4GHz band respectively.

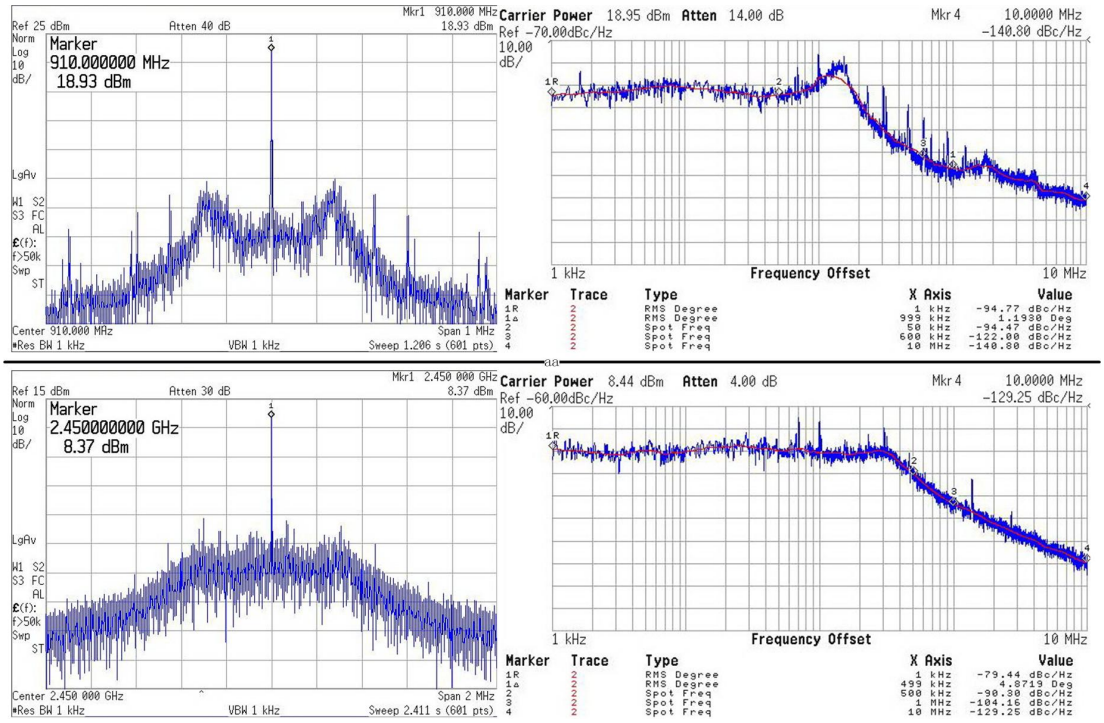


Fig. 9.21 Measured close loop spectrum and phase noise for Zigbee and Bluetooth

9.4.2.11 MB-OFDM UWB

Fig. 9.22 shows the measured close loop phase noise for MB-OFDM UWB standard. Since the reference noise dominates the close-in phase noise at carrier frequencies larger than 3GHz. A doubled reference frequency 66MHz is used to reduce the division number and mitigate the reference noise influence. With the DB Q-VCO consuming current around 16mA, at different frequency bands the close-in phase noise at 100KHz offset varies from -84.2 to -93.1dBc/Hz. The out-band phase noise at 1MHz offset is measured as from -100.1dBc/Hz to -109.8dBc/Hz. The RMS phase error integrated from 1KHz to 264MHz frequency offset varies from 2.09° to 5.38°. The RMS phase error should be improved effectively by employing a 66MHz crystal oscillator as the reference source.

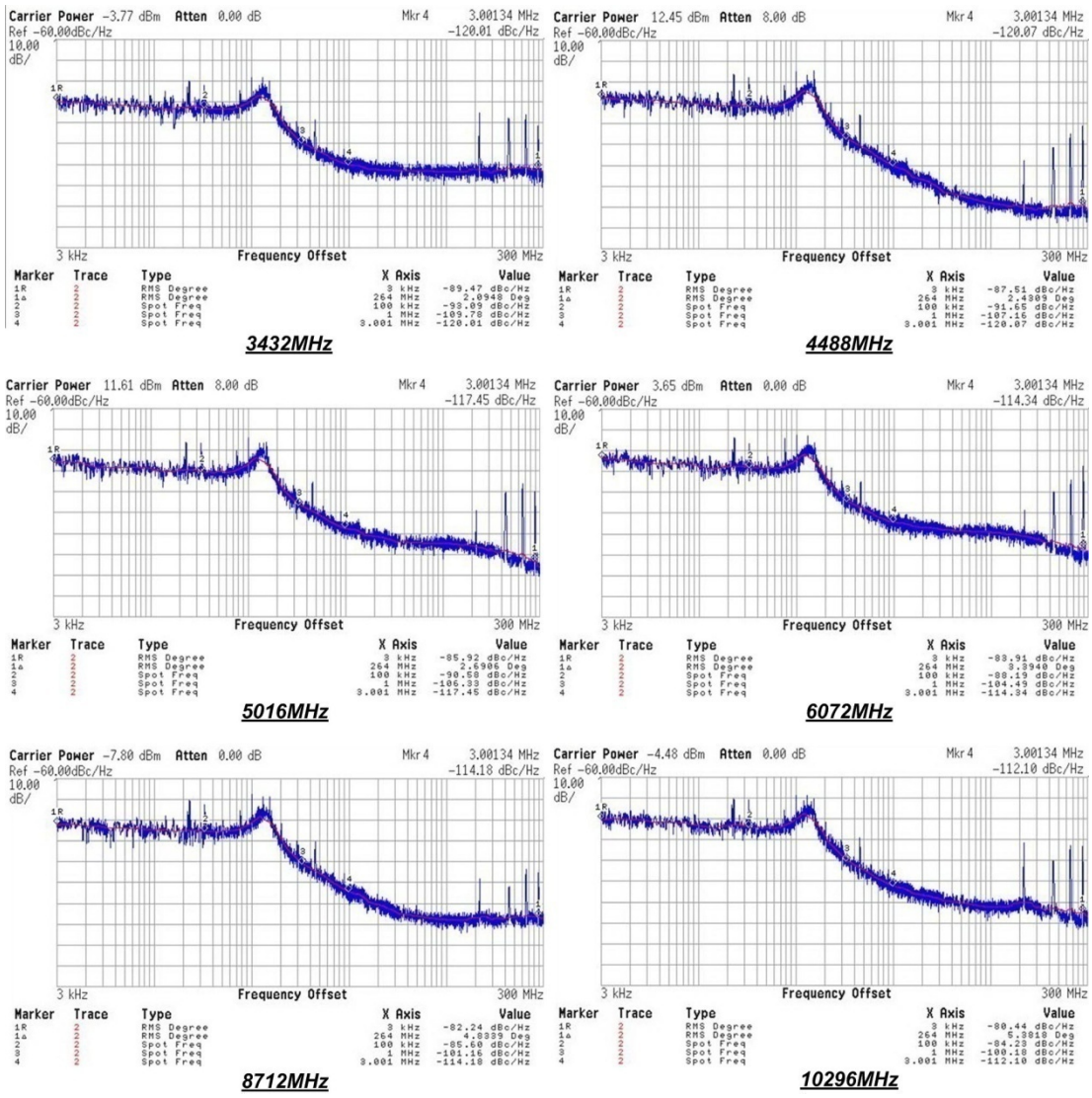


Fig. 9.22 Measured close loop phase noise for MB-OFDM UWB

9.4.2.12 UWB 802.15.3c

Fig. 9.23 shows the measured phase noise of the ILFM's chain with input signal generated on-chip and from external signal generator, where the top curve and the bottom curve are the phase noise of the 20GHz output signal and the one of the input signal, respectively. Consistent with the theory, the phase noise at 20.88GHz is around 19dB degraded compared to the 2.32GHz input, and around 13dB degraded compared to the 4.64GHz input from the signal generator. The close-in phase noise at 10KHz

offset of the 20GHz output signal is -75dBc/Hz and -108.7dBc/Hz with internal or external signal source, respectively. And the output-band phase noise at 1MHz offset is -97.2dBc/Hz and -128.1dBc/Hz, with internal or external signal source, respectively. The phase noise of the 40GHz output signal was measured by a dividing down the frequency by 2 through an external 40GHz-input frequency divider. The phase noise curve is very similar to the one of the 20GHz output. Considering 6dB difference for the phase noise of the 40GHz output signal, with input signals internally generated by the FGS, the in-band and out-band phase noise would be -69dBc/Hz and -91.2dBc/Hz, respectively. And with external signal source, the in-band and out-band phase noise would be -102.7dBc/Hz and -122.1dBc/Hz, respectively.

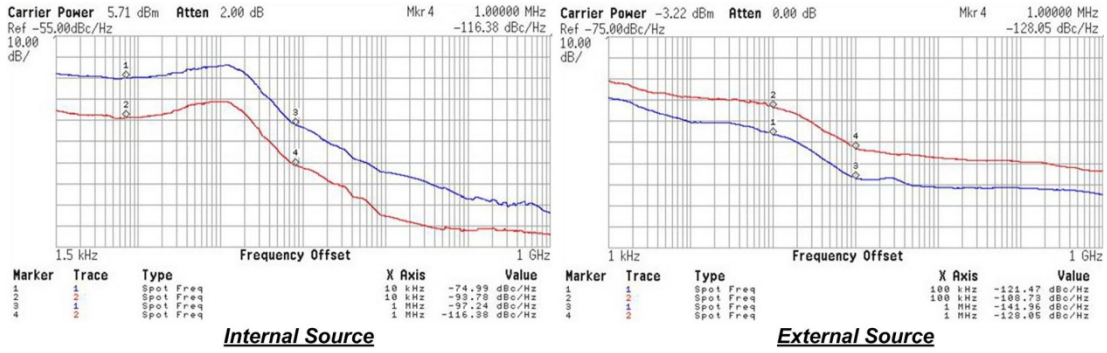


Fig. 9.23 Measured close loop phase noise for UWB 802.15.3c

9.5 Spur

Fig. 9.24 shows the typically measured output spectrums for at different carrier frequencies. Benefiting from the avoidance of using any mixers or fractional dividers for all the standard modes except UWB, the spurious tones other than the harmonics of the desired frequency are all below -50dBc. The harmonic tones would not affect the transceiver's performance, because the switching operation of the up-conversion

or down-conversion mixer is intrinsically nonlinear. For the UWB mode, the results are reported in Chapter 6, where the spurious tone level is below -31dBc for all the 14-band carriers.

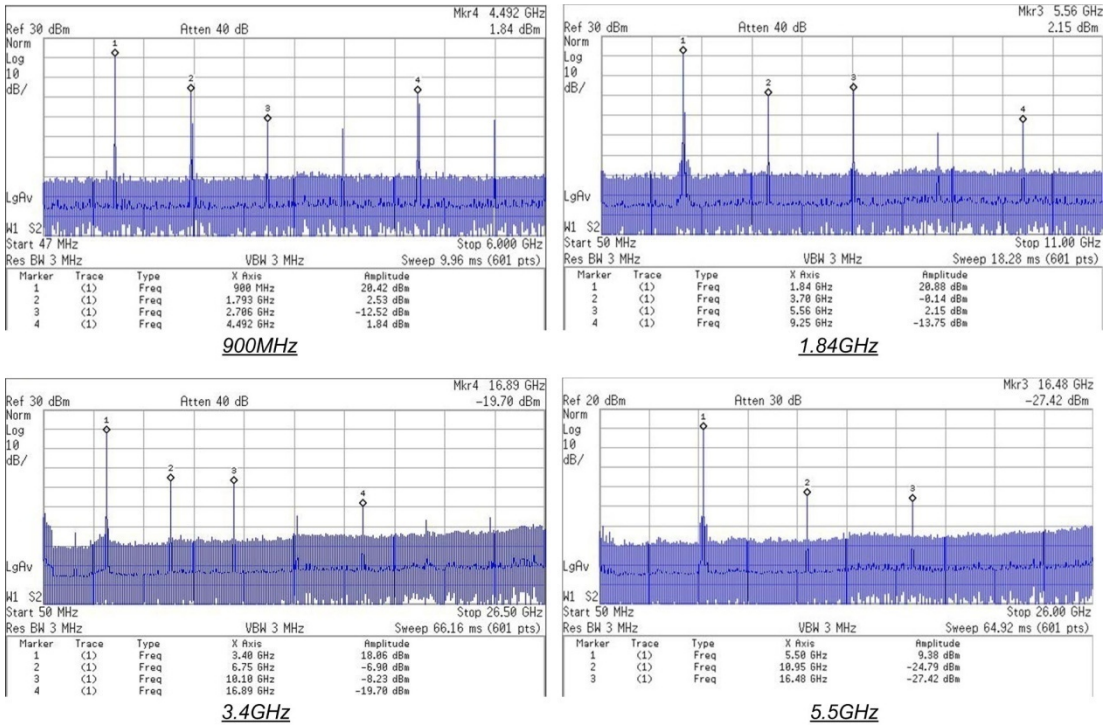


Fig. 9.24 Measured output spectrums at different frequencies

Fig. 9.25 shows the measured reference spurs at different carrier frequency. The loop bandwidth varies from 100KHz to 250KHz and the reference frequency is set from 30.2MHz to 72.5MHz. Under different conditions, the reference spur varies from -57.5dBc to -67.9 referred to the carrier power. During the measurement, the spur level is unchanged when fine tuning the up and down current of the CP, which indicates that the spur is mainly caused by reference clock feed-through. To further reduce the reference, layout techniques, such as ground shielding and guard ring, can be used to isolate the VCO's control line better. And the bonding wires connecting the chip and testing PCB need to be also carefully planned, to prevent the reference clock coupled to the VCO's control line externally.

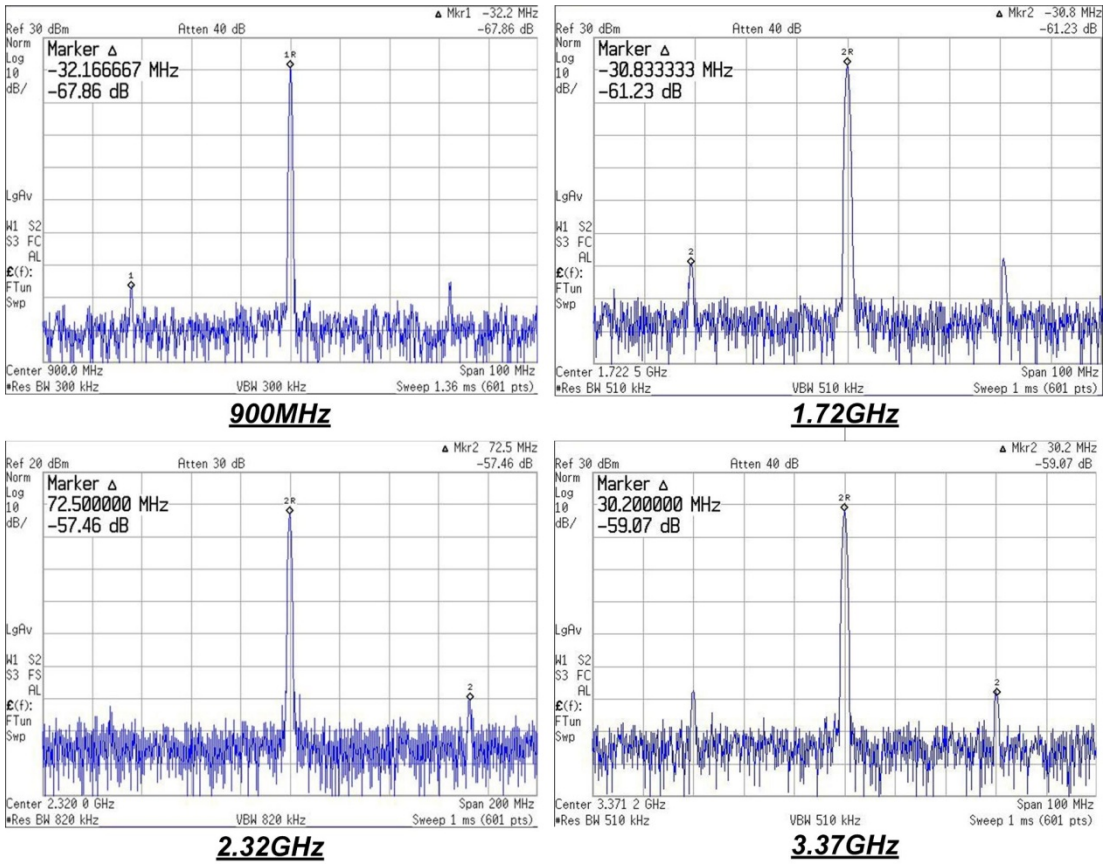


Fig. 9.25 Measured reference spurs at different conditions

9.6 Channel Settling Time

The channel settling time is estimated, through measuring the control voltage on the loop filter by an oscilloscope. Fig. 9.26 shows the captured picture from the oscilloscope. The output carrier frequency of the FGS is switched from 2470MHz to 2490MHz with a 20MHz channel space. From Fig. 9.26, the PLL can settle the channel frequency within 40μS, which is sufficient for all the standards including Bluetooth and Wimax.

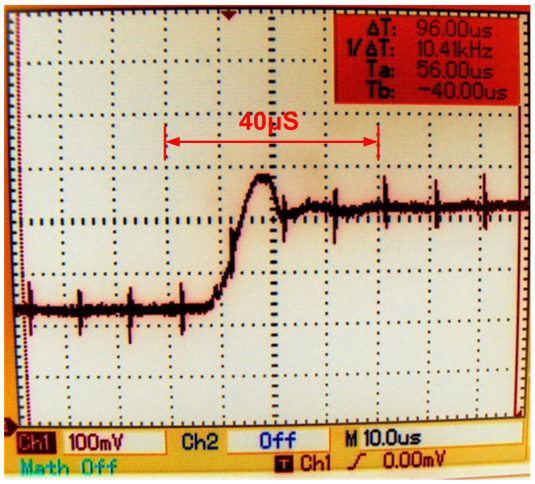


Fig. 9.26 Measured channel settling time by oscilloscope

To measure the channel settling time more accurately, an alternative method is used through the spectrum analyzer [107]. The center frequency of the spectrum analyzer is set exactly at the desired carrier frequency (2490MHz in the measurement), and the IF filter bandwidth of the spectrum analyzer is set based on the required carrier frequency accuracy associated with the channel settling time specification provided by given standard. For example, the WLAN standard requires the channel to be settled within 224 μS with a frequency accuracy of ±60KHz, therefore the bandwidth of the IF filter is set to be 120KHz such that the spectrum analyzer can detect the carrier when it settles into the required range.

Fig. 9.27 shows the measured settling time at different spectrum analyzer's IF bandwidth. With 500KHz IF bandwidth the PLL can settle down within 35.6 μS. When the IF bandwidth is increased to 200KHz, the settling time is increased to 61.2 μS. The measured settling time is 92.8 μS for a frequency accuracy of ±30PPM, which can well meet the 200 μS requirement of Bluetooth [108]. And the measured settling time is 94.8 μS for a frequency accuracy of ±60KHz, sufficiently fulfilling WLAN's specification.

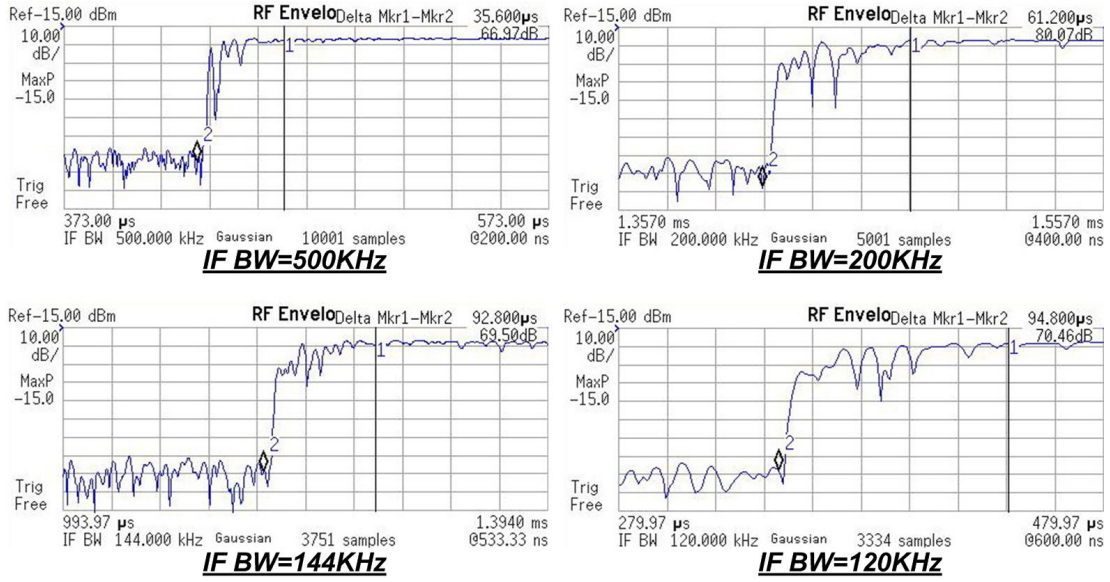


Fig. 9.27 Measured channel settling time by spectrum analyzer

Fig. 9.28 shows the measured channel hopping time through Agilent's Infiniium 90000A high speed oscilloscope, where the output frequency of the reconfigurable ILFM is hopping from 792MHz (x3 mode) to 1320 (x5 mode), and the output frequency of the UWB FS is hopping from 5016MHz (band-4) to 5544MHz (band-5). From the measured waveform, the estimated channel hopping time is less than 0.9nS. For the worst case, the open loop switching time is less than 3.7nS.

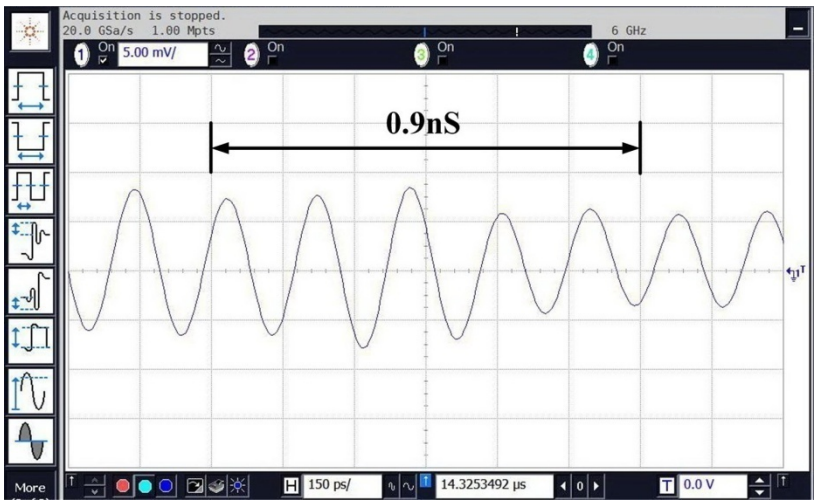


Fig. 9.28 Measured UWB channel hopping time by oscilloscope

9.7 IQ Mismatch

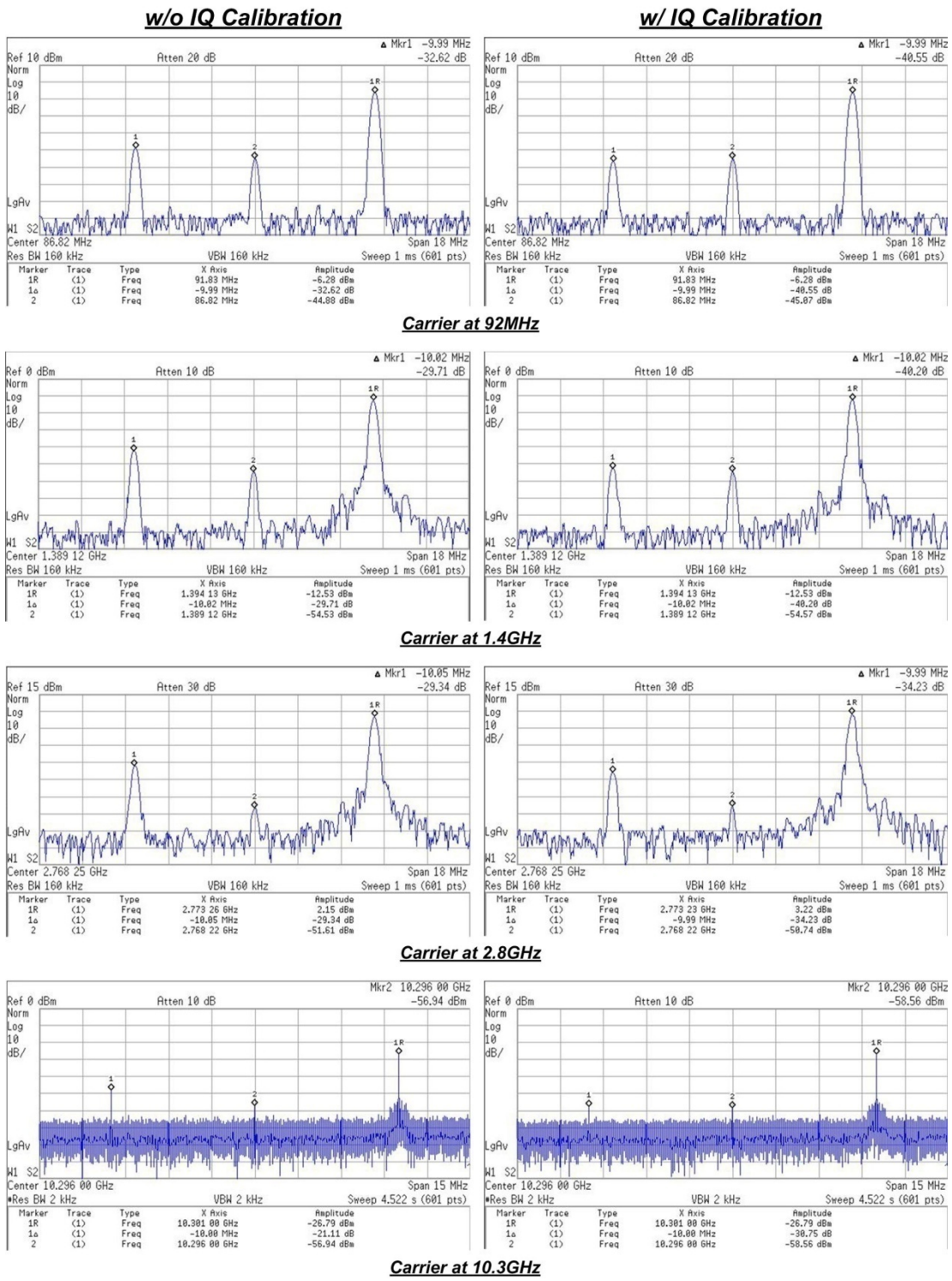


Fig. 9.29 Measured spectrums at Tx mixer's output w/ and w/o IQ calibration

Fig. 9.29 shows measured output spectrum at the transmitter mixer's output. 5MHz IQ baseband signals are used, and thereby it is reasonable to assume the IQ

mismatch of the baseband signals is neglect able. It can be seen that, the LO leakage level is around -30 to -50dBc for the carrier frequency from 100MHz to 10GHz. Fig. 9.30 summarizes the measured sideband rejection (SBR) ratios with different carrier frequencies. Without IQ calibration, the SBR varies from 19dB to 40dB, corresponding to IQ phase error of from 12.6° to 1.1° with no amplitude mismatch. After the IQ calibration, the SBR can be improved to from 30.3dB to 47dB, corresponding to IQ phase error of from 3.4° to 0.5°. This error should be able to be calibrated out by the digital baseband, which typically has a capability of 5°.

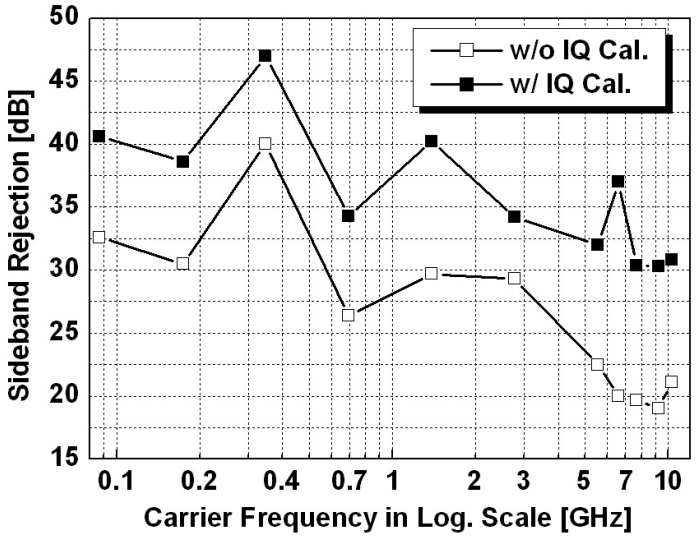


Fig. 9.30 Summary of measured sideband rejection w/ and w/o IQ calibration

9.8 Power Consumption

Table 9.1 summarizes the power consumption of the fabricated building blocks in the SDR FGS.

Table 9.1 Power consumption summary of the SDR FGS

Part	Building block Name	Current (VDD=1.2V) [mA]	Power [mW]
Main RF (I&Q)	DB-QVCO w/ buf	6 ~ 20	7.2 ~ 24
	Div-A w/ buf	6	7.2
	Div-B w/ buf	4	4.8
	Div-C w/ buf	2	2.4
	Div-D w/ buf	1	1.2
	Div-E w/ buf	1	1.2
	Div-F w/ buf	0.5	0.6
	Div-G w/ buf	0.4	0.5
	Mux-A	3~5	3.6~6
	Mux-B	6	7.2
	Multi-Modulus Div.	6	7.2
	PFD/CP	0.01 ~ 2	0.01 ~ 2.4
	V2I	0.02 ~ 0.1	0.02~0.1
PLL in total		**19 ~ 43**	**22.8 ~ 51.6**
RF part for I&Q in total		**25 ~ 54**	**30 ~ 64.8**
UWB (I&Q)	ILFM x1/x3/5/x7 w/ buf & Mux-C	5 ~ 6.7	6 ~ 8
	Mux-D	5.4	6.5
	SSB Mixer	4.4 * 2 = 8.8	10.5
UWB part for I&Q in total		**19.2 ~ 20.9**	**23 ~ 25.1**
MM-Wave (I&Q)	7G output X3 w/ buf	8.6	10.3
	20G output X3 w/ buf	13.6	16.3
	40G output X2 w/ buf	9.6	11.5
	APC (when opened)	1.6	1.9
MM_Wave part for I&Q in total		**33.4**	**40**

9.9 Performance Summary and Comparison

Finally, the measurement results of the SDR frequency generation system are summarized in Table 9.2.

Table 9.2 Measurement results summary of the SDR FGS

Standards		Out-Band Phase Noise [dBc/Hz]			In-Band Phase Noise [dBc/Hz]	RMS Phase Error
		Specification	Close Loop	Open Loop		
EGSM	850-900	-139.5 @3MHz	-141.7 @3MHz	-144.7 @3MHz	-97.9 @50KHz	0.4°
	DCS/PCS		-137.2~ -139.6 @3MHz	-140.5~ -143.1 @3MHz	-90.6~ -91.3 @50KHz	0.97° ~ 1.06°
UMTS	FDD	-120@3MHz	-136.3 @3MHz	-140@3MHz	-91.1 @50KHz	1.32°
	TDD	-145 @20MHz	-145.7 @20MHz	-149@3MHz		
WLAN 802.11	a b/g n	-102@1MHz	-112.5~ -116.8 @1MHz	-113~ -119.1 @1MHz	-89~ -95.8 @100KHz	1.25° ~ 2.9°
WIMAX 802.16	802.16-2004 TDD/ FDD	-102@1MHz	-108.8~ -123.6 @1MHz	-113~ -123.4 @1MHz	-85.1~ -95.8 @100KHz	1.25° ~ 3°
	802.16e-2005					
Bluetooth	802.15.1	-89 @500KHz	-90.3* @500KHz	-112 @500KHz	-80* @50KHz	4.87°*
DECT		-131 @4.7MHz	-137.9 @4.7MHz	-142 @4.7MHz	-90.6 @50KHz	1.58°
Zigbee	802.15.4	-110 @10MHz	-129.3* ~ -140.8* @10MHz	-139.1 ~-148.7 @10MHz	-80* ~ -95* @50KHz	1.19°* ~ 4.87°*
UWB	802.15.3a MB-OFDM	-100 @1MHz	-100.1 ~ -109.8 @1MHz	-102 ~ -110.6 @1MHz	-84.2 ~ -93.1 @100KHz	2.09° ~ 5.38°

UWB	MMW 802.15.3c	-88 @1MHz	20G: -97.2 40G: -91.2 @1MHz	60G: -93.2 @1MHz	20G: -75 40G: -69 @10KHz	1.7pS (Jitter)
Broad-casting	DVB-T/H	-87@10KHz -115@1MHz	-119.9* ~ -134.7* @1MHz	-128.1 ~ -135.8 @1MHz	-91.7* ~ -107.7* @10KHz	0.1°* ~ 0.85°*
Position	GPS	-105@1MHz	-130.7 @1MHz	-132.2 @1MHz	-91.5 @50KHz	1.08°
RFID	UHF	-144 @3.6MHz	-144.3 @3.6MHz	< -145.7 @3.6MHz	-96.2 @50KHz	0.3°

Spur	Switching Time	I&Q Accuracy
< -57dBc	Close Loop: 36μS ~ 95μS Open Loop: < 3.7nS	SBR: 30.3dB ~ 47dB

*Q-VCO's bias current is much reduced to save the power consumption for the associated standards

It can be seen that the proposed FGS is able to meet all the wireless communication standards' requirement, except for DCS/PCS, due to the 3dB phase noise degradation caused by the band selection switches in the V2I convertor. After fixing the design error, the FGS should be able to fulfill the DCS/PCS' specification as well, as proved in the open-loop measurement.

A more interesting way of evaluating the SDR FGS is to compare the system with the existing frequency synthesizers designed dedicated for a single standard. By doing so, the power consumption and chip area overhead as well as the performance trade-off can be fully assessed and understood for such SDR sub-system with high re-configurability and capability. Table 9.3 shows the comparisons.

Table 9.3 Comparisons between the SDR FGS and the existing frequency synthesizers dedicated for a single standard

Standard	Ref.	Tech.	Area [mm^2]	Power [mW]	In-Band PN [dBc/Hz] (Other)	Out-Band PN [dBc/Hz]	RMS Phase Error
GSM900	H. Lee JSSC 2004	0.5μm BiCMOS	4.6	55	-80	< -139 @3MHz	-
	This SDR FGS	0.13μm CMOS	3.0	50	-97.9	-141.7 @3MHz	0.4°
DCS /PCS	B. Muer JSSC 2002	0.25μm CMOS	4	70	-60/-80	-139 @3MHz	3°/1.7°
	This SDR FGS	0.13μm CMOS	3.0	48	-90.6~ -91.3	-137.2~ -139.6 @3MHz	0.97° ~ 1.06°
UMTS	E. Temp. JSSC 2004	0.18μm CMOS	3.4	28	-104	-129 @2MHz	0.32°
	This SDR FGS	0.13μm CMOS	3.0	48	-91.1	-136.3 @3MHz	1.32°
WLAN	A. Bonf. ESSCIRC 2007	0.13μm CMOS	0.41	51	< -90	< -108 @1MHz	<3°
	J. Rogers JSSC 2005	0.5μm BiCMOS	3.2	99	-98	-120@1MHz	0.35° ~ 0.86°
	This SDR FGS	0.13μm CMOS	3.0	56~61	-89~ -95.8	-112.5~ -116.8 @1MHz	1.25° ~ 2.9°
WIMAX 802.16	Y. Yang JSSC 2006	0.18μm CMOS	1.0	48	-100	-124@1MHz	0.41°
	H. Heda. JSSC 2009	0.18μm CMOS	3.2	47	-102	-130@3MHz	0.46°
	This SDR FGS	0.13μm CMOS	3.0	41~58	-85.1~ -95.8 @100KHz	-108.8~ -123.6 @1MHz	1.25° ~ 3°
Blue-tooth	D. Leena. JSSC 2003	0.18μm CMOS	1.1	15	-65	< -120 @3MHz	-
	This SDR FGS	0.13μm CMOS	3.0	36	-80	-90.3 @500KHz	4.87°

DECT	M. Perrott JSSC 1997	0.6μm CMOS	9.0	27	-75	-131 @5MHz	-
	This SDR FGS	0.13μm CMOS	3.0	42	-90.6	-137.9 @4.7MHz	1.58°
Zigbee	W. Raha. RFIC 2007	0.28μm CMOS	0.22	0.8	-55	-98@1MHz	-
	This SDR FGS	0.13μm CMOS	3.0	33~36	-80 ~ -95	-129.3 -140.8 @10MHz	1.19°~ 4.87°
UWB (MB-OFDM)	T. Lu ISSCC 08	0.18μm CMOS	5.5	117	SFDR>33dB Hopping-time<3.3nS	-98@1MHz	-
	This SDR FGS	0.13μm CMOS	3.0	79~81	SFDR>31dB Hopping-time<3.7nS	-100.1~ -109.8 @1MHz	2.09° ~ 5.38°
UWB (802.15.3c)	K. Scheir ISSCC 09	45nm CMOS	0.82	76~78	-75@1MHz	-82@3MHz	-
	This SDR FGS	0.13μm CMOS	3.0	83	20G: -75 40G: -69 @10KHz	20G: -97.2 40G: -91.2 @1MHz	1.7pS (Jitter)
DTV	M. Maru. ISSCC 06	0.11μm CMOS	1.9	18~20	-95 ~ -120	-130 ~ -150 @1MHz	-
	L. Lu ISSCC 09	0.18μm CMOS	1.6	25	-95	-126.5 @1MHz	0.6° ~ 1.05°
	M. Kon. ISSCC 10	65nm CMOS	0.3	11	-80 ~ -94	-119 @1MHz	-
	This SDR FGS	0.13μm CMOS	3.0	38~52	-91.7~-107.7 @10KHz	-119.9~-134.7 @1MHz	0.1° ~ 0.85°
GPS	G. Mont. JSSC 2003	0.18μm CMOS	0.8	16	-80 ~ -96	-95 @1MHz	7°
	This SDR FGS	0.13μm CMOS	3.0	44	-91.5 @50KHz	-130.7 @1MHz	1.08°
RFID (UHF)	W. Wang TCAS-I 08	0.18μm CMOS	1.7	4.9	-70	-121 @1MHz	-
	S. Chiu JSSC 2007	0.18μm BiCMOS	-	-	-78 ~ -82	-144 @3.6MHz	1.3° ~1.4°
	This SDR FGS	0.13μm CMOS	3.0	50	-96.2 @50KHz	-144.3 @3.6MHz	0.3°

From Table 9.3, it can be seen that for those high requirement standards including GSM/DCS/PCS, WLAN, UWB and RFID, the SDR FGS is very comparable to the associated dedicated synthesizers in terms of the chip area, power consumption and the performance. While for the low requirement standards like Bluetooth and Zigbee, the power consumption of the SDR FGS is relatively high. Nevertheless, for the reconfigurable multi-standard and software-defined radio applications, the SDR FGS prototype shows its great area and cost advantages over the multiple synthesizer solution.

Chapter 10

Conclusion and Future Work

10.1 Summary

In this dissertation, circuit techniques and system architectures are investigated to realize a wideband IQ LO generation system for software-defined radios. Chapter 1 and Chapter 2 introduce the background and transceiver architectures of the software-defined radio. The general considerations and the specifications of the frequency synthesizer for wideband SDR are summarized in Chapter 3.

In Chapter 4, complete analysis on both one-port and two-port dual-band oscillators using transformer-based fourth-order LC tanks is provided, from which critical parameters - including oscillation frequency, start-up condition, tank Q, phase noise - are analytically derived and compared. It is shown that one-port oscillators consume less power than two-port counterparts but may suffer from stability problem which can be solved by a notch-peak cancellation technique. On the other hand, compared to one-port oscillators, two-port oscillators need to consume more power to obtain the same output swing, but their phase noise can be improved more linearly with increasing bias current, and thus they can achieve lower phase noise at sufficiently large bias current. Based on the results, a dual-band quadrature voltage-controlled oscillator (Q-VCO) is systematically designed and implemented in a 0.13-μm CMOS process for software-defined-radio (SDR) applications. The prototype achieves a dual-band operation with in-phase and quadrature-phase (IQ) output signals from 2.7GHz to 4.3GHz and from 8.4GHz to 12.4GHz. At 3.6GHz and

10.4GHz, phase noise at 3MHz offset of -135.9dBc/Hz and -119dBc/Hz and sideband-rejection ratios (SBR) of 37dB and 41dB are measured, respectively.

Novel current-bleeding and current-reusing techniques are proposed in Chapter 5, to efficiently enlarge and maximize the locking ranges of injection-locked and Miller frequency dividers, without extra inductive component and extra power consumptions. Analysis shows that to achieve maximum locking range for the LC-based frequency dividers, the effective biasing current can be simply fixed to certain value so as to make the divider's self-oscillation amplitude equal to the specified minimum output amplitude. Implemented in a 0.13μm CMOS, two current-reusing ILFD prototypes achieve locking ranges of 6.02GHz to 8.45GHz and 59.6GHz to 66.96GHz, around 3 times and 2 times improvement than that of the conventional ILFDs, while consume 0.9mW and 1.6mW from a 0.8V supply, and a 60GHz current-bleeding Miller divider prototype shows significant locking range improvement of more than 5x compared to that of the conventional Miller divider, without extra inductor and extra power consumption.

In Chapter 6, new circuit topologies, including a reconfigurable injection locking based frequency multiplier, and transformer-based single-coil 3GHz-to-10GHz tunable narrow-band LC-tank for SSB mixers, are employed, to integrate a 14-band MB-OFDM UWB carrier generator into the FGS, in an area efficient way with only 2 extra inductive coils. In the experiment, the generator achieves sideband rejections better than 31dB for all the 14-band carriers.

A novel interpolative-phase-tuning technique is proposed in Chapter 7 to implement varactor-less multi-phase LC oscillators with wide tuning range and low phase noise at MMW frequencies. Two phase-tuning CCO prototypes, one with 8-phase 50GHz outputs and another with 4-phase 60GHz outputs, implemented in the

0.13μm CMOS process and operated at 0.8V supply, measure phase noise of -127.8dBc/Hz and -120.6dBc/Hz at 10MHz offset, FOMs of 186.4dB and 180.6dB, and FOM_Ts of 183dB and 179.7dB, respectively, which are much better compared to other state-of-the-art MMW oscillators using capacitive tuning.

An alternative way of using high frequency multipliers to synthesize the MMW LO frequencies is also investigated in Chapter 7. Two injection-locked based frequency multiplying chains are designed and demonstrated, providing LO signals for both direct-conversion and dual-conversion transceivers operating at 60GHz band. A proposed automatic peak calibration technique is implemented for the ILFM chain, which effectively improves the output swing and the spur rejection performance with low area and power consumptions.

Employing these circuit techniques and topologies, a wideband SDR frequency generation system, with reconfigurable phase-locked loop as described in Chapter 8, is proposed and demonstrated in a 0.13μm CMOS. The prototype successfully generates the LO signals from 47MHz to 10GHz, from 18GHz to 22.5GHz and from 37GHz to 44GHz. The detailed experimental results are provided in Chapter 9. It is shown that the proposed FGS is capable of meeting all the wireless communication standards' specifications including GSM900, DCS/PCS (after fixing the error as mentioned in Section 8.4), UMTS, WLAN, WiMAX, Bluetooth, DECT, ZigBee, DVB-T/H, GPS, UHF-RFID, MB-OFDM UWB and UWB 802.15.3c.

10.2 Contributions of The Dissertation

Firstly, the dissertation proposes the system architecture of an IQ LO signal generator, which fully supports a described ultra wideband SDR transceiver system,

covering all the wireless communication standards within the frequency band from 47MHz to 10GHz as well as the 60GHz band.

Secondly, the dissertation contributes the complete theory of transformer-based one-port and two-port dual-band oscillators, and proposes an optimized dual-band Q-VCO topology for the wideband SDR applications.

Thirdly, locking range enhancement techniques are proposed for the LC-based injection-locked frequency dividers and Miller dividers. And the associated locking range optimization theory is developed.

Fourthly, a varactor-less phase tuning technique is proposed to improve the performance of oscillators operating at high frequencies, like the millimeter-wave frequencies.

Fifthly, the dissertation proposes the circuit topologies of a reconfigurable x3/x5/x7 injection-locked frequency multiplier, and a transformer-based single-coil tunable narrow-band LC-tank. With the novel circuitries, it is demonstrated that the 14-band carriers of the MB-OFDM UWB standard can be generated with only two extra inductive coils based on a phase-locked VCO.

Sixthly, cross-injection and quadrature-input-differential-output topologies are proposed for injection-locked frequency multiplier circuits. Together with a novel automatic-peak control technique, it is demonstrated that the LO signals for the 57GHz-to-66GHz dual-conversion transceivers can be generated through the sub-harmonic injection-locking method, with sufficient locking range, LO swing and phase noise performance.

Finally, the dissertation contributes the design, integration and measurement results of the whole frequency generation system, which is the very first one successfully covering the frequency bands from 47MHz to 10GHz, 19GHz to 22GHz

and 38GHz to 44GHz.

10.3 Recommendations for Further Work

The main focus and the contributions of this work are in the open loop part for wide-band LO generations. Nevertheless, there are also some potential topics worthy to be investigated in the close loop part of the SDR FGS as well.

One issue is how to dynamically control the loop bandwidth of the PLL for different standards. Although the loop parameters such as K_{VCO}, loop filter parameters can be optimized in the measurement and then memorized in digital domain, such a method requires a long period and tedious experimental process which is not time and cost effective. Moreover, this method cannot realize real time calibration and thus the performance is limited by the PVT variations. To implement the real time loop bandwidth control, on chip measurement needs to be done to obtain the phase noise, settling time and spur information, in order to automatically calibrate the loop bandwidth, which is difficult to realize in analog domain. Thereby, all digital PLL would be the direction for implementing the fully self-adaptive and self-reconfigurable frequency synthesizer.

Another issue is to effectively reduce the channel switching time of the FGS. With proper design, the switching time of the open loop part can be controlled into nanosecond level, but what limits the total channel switching time is the PLL part. By using a large loop bandwidth together with quantization noise compensation or dynamic bandwidth control, the settling of the loop can be accelerated to tens of microseconds, however, considering a wide range of spectrum scanning for the future cognitive radio, many tens of microseconds would still be too long. Therefore,

novel techniques to further reduce the switching time are highly desirable.

Besides, the current PLL is based on single loop architecture, while dual loop or multiple loop architecture is worthwhile of investigations. One of the motivations to use an extra loop is to adjust the reference frequency as well, by doing so the resolution requirement of the main loop can be much relaxed.

In the designed SDR FGS, IQ LO signals are provided for typical transceiver architectures. On the other hand, to support harmonic rejection transceivers, half-quadrature phase LO signals are required. One potential method to generate 45° signals is adding more dividers in the divider chain and applying the IQ differential signals at each node to two following dividers, instead of summing I and Q signals and applying on a single following divider, as in the current way. By doing so, half-quadrature signals can be obtained at the two dividers' outputs. In this scheme, the phase sequence at the two dividers' outputs needs to be carefully dealt with. And more importantly, at Mux-B's output, the leakage signals at the harmonic frequencies of the desired signal should be treated as well, because such leakage signals can change the original phase relationship between fundamental tone and the harmonic tones of the desired LO signal, which would degrade the harmonic rejection ratio of the harmonic rejection transceivers.

For the SDR FGS, the power consumption is quite high for the low end standards like Zigbee and Bluetooth, while the phase noise, especially for Zigbee, still has much margin to be traded off with the power consumption. It is therefore desirable to improve the individual building block as well as the system architecture to further enhance the re-configurability of the whole system. And it would be wise to selectively group and integrate the standards with more common points into different sub-systems, to globally optimize the whole SDR.

Appendix-I

Design Flow of Inductor or Transformer

In this appendix, the computer aided design flow of inductive components will be provided, while the technical aspects of monolithic inductors and transformers, including the layout configurations, the physical analysis and the fitting models can be found in numerous literatures [109]-[113].

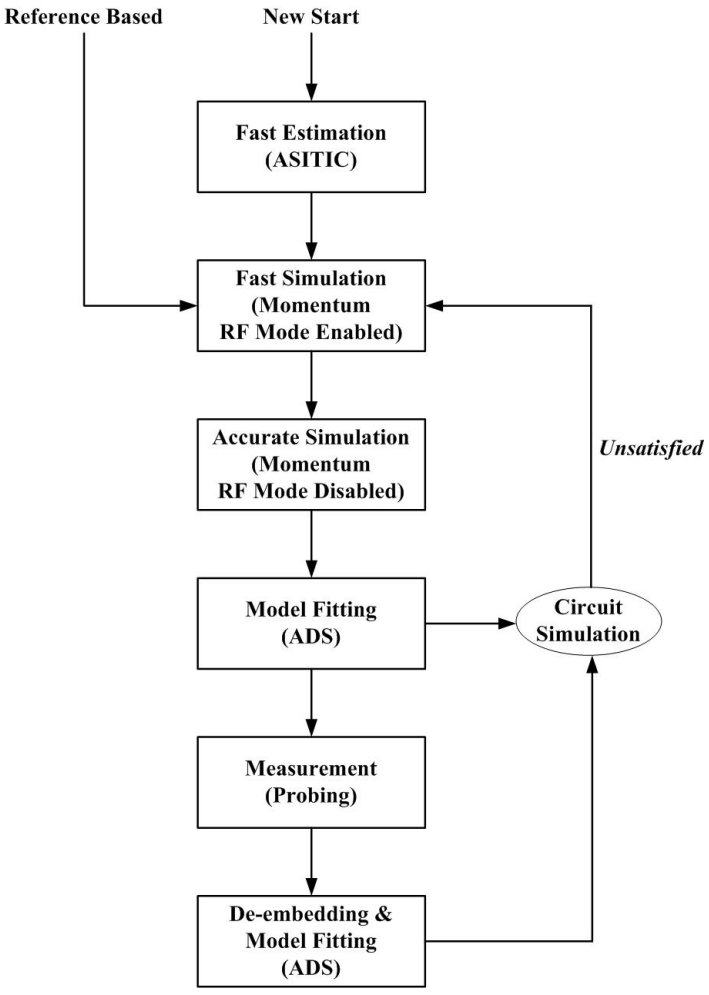


Fig. I-1 Design flow of inductive components

Fig. I-1 shows the design flow for the inductors and the transformers used in the

FGS. At the beginning, the component parameters like the inductance, Q and coupling coefficient can be quickly estimated and optimized using the tool ASITIC [114], with simulating different layout configurations and adjusting the physical parameters such as the turn number, the diameter, the metal width, the line spacing and so on. It should be noticed that the estimated Q from ASITIC is typically higher than the actual Q, especially at the frequencies above 5GHz. So enough design margins should be left for the inductive Q before moving to the next step.

After obtaining the basic physical parameters, the inductor or the transformer is then simulated in a 2.5D EM simulator Momentum commercialized by Agilent. In this step, the RF mode of the simulator is enabled to sufficiently save the simulation time, so that the physical parameters like the metal width and the line spacing can be fine tuned with a reasonable accuracy and without consuming too much time. When the layout is optimized and fixed, the component is simulated with the RF mode disabled. The simulation would take much longer time but become more accurate in particular at millimeter wave frequencies. Then, the simulated S-parameter data from Momentum are fitted into a discrete component model in ADS, so that the inductor or the transformer can be well simulated in the circuit simulators, such as Spice or SpectreRF. If the circuit performance with the designed inductor or transformer is satisfied, the design is done and the testing structures of the inductive component can be fabricated for measurement. If not, the flow needs to go back to the fine-tuning step, or even back to the first step with ASITIC if a new layout architecture needs to be used. Note that, if the characteristic of the desired inductor or transformer is similar to that of an existing design, the flow can start directly from the second fine-tuning step based on the reference.

Finally, the inductor or the transformer is measured based on the on-wafer

probing. Before measuring the data, the whole test environment needs to be calibrated through probing a calibration substrate for the associated probes. Then, the inductor or the transformer is measured by replacing the calibration substrate with the device under test. Since the measured raw data contain both the parasitic capacitance of the pads and the parasitic inductance of the interconnecting lines between the device and the pads, the testing structures of the open pads and short pads are also fabricated and measured, and then the de-embedding and the model fitting with the measured data are done in ADS. After that, the fitted model is verified again in the circuit level simulation, to find out the actual influence of the inductor or the transformer on the circuit performance, if necessary, the inductive component needs to be re-designed from the beginning.

Appendix-II

List of Publications

Conference papers:

1. **Sujiang Rong** and H. C. Luong, "A 1V 4GHz-and-10GHz transformer-based dual-band quadrature VCO in 0.18μm CMOS," *IEEE Custom Integrated Circuits Conference (CICC),* pp. 817–820, Sept. 2007.
2. **Sujiang Rong** and Howard C. Luong, "A 1.7mW 25GHz Transformer-Feedback divide-by-3 Frequency Dvider with Quadrature Outputs," *IEEE Asian Solid State Circuit Conference (ASSCC),* Nov. 2007.
3. **Sujiang Rong**, Alan W. L. Ng and Howard C. Luong, "0.9mW 7GHz and 1.6mW 60GHz Frequency Dividers with Locking-Range Enhancement in 0.13μm CMOS", *IEEE International Solid-State Circuits Conference (ISSCC), Dig. Tech. Papers*, pp. 96-97, Feb. 2009
4. Alan W.L. Ng, **Sujiang Rong**, Hui Zheng and Howard C. Luong, "Low-Voltage Transformer-Feedback CMOS VCOs and Frequency Dividers", *VLSI DAT*., 2009 (invited paper)
5. **Sujiang Rong** and Howard C. Luong, "V-Band Varactor-Less Interpolative –Phase-Tuning Oscillators with Multiphase Outputs," *IEEE Custom Integrated Circuits Conference (CICC),* Sept. 2010.
6. W. Wang, S. Lou, K. Chui, **S. Rong**, C. F. Lok, etc, "A Single-Chip UHF RFID Reader in 0.18-mm CMOS," *IEEE Custom Integrated Circuits Conference (CICC),* Sept. 2007.
7. **Sujiang Rong** and H. C. Luong, "A 57-to-72GHz Differential-Input Frequency Divider with Locking Range Optimization in 0.13μm CMOS," *IEEE Asian Solid State Circuit Conference (ASSCC),* Nov. 2010.
8. **Sujiang Rong** and Howard C. Luong, "A 47MHz-to-10GHz, 18GHz-to-22GHz and 37GHz-to-44GHz Frequency Generation System for Software-Defined Radios," To be submitted.

Journal papers:

1. **Sujiang Rong** and H. C. Luong, "A 2.7GHz-to-4.3GHz and 8.4GHz-to-12.4GHz Transformer-Based Quadrature-VCO for Software-Defined Radios," *IEEE J. Solid-State Circuits*, submitted.
2. W. Wang, S. Lou, K. Chui, **S. Rong**, C. F. Lok, etc, "A Single-Chip UHF RFID Reader in 0.18-μm CMOS," *IEEE J. Solid-State Circuits,* 2008.
3. **Sujiang Rong** and H. C. Luong, "Locking Range Optimizations for LC-Based Frequency Dividers," to be submitted.
4. **Sujiang Rong** and H. C. Luong, "Low Phase Noise Varactor-Less Interpolatvie Phase Tuning Oscillators for MM-Wave Applications," to be submitted.
5. **Sujiang Rong** and H. C. Luong, "A Wide-Band CMOS Frequency Generation System for Software-Defined Radios" to be submitted.

Patents:

1. **Sujiang Rong** and Howard C. Luong, "Injection-Locking-Range Enhancement Technique for Frequency Dividers", U.S. Patent Application, Serial No. 12/474,490, filed on May 2009.

2. **Sujiang Rong** and Howard C. Luong, "Method and Apparatus for Tuning Frequency of LC-Oscillators Based on Phase-Tuning Technique", applied for U.S., T.W., C.N. Patents.

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