A CMOS Digital Polar Transmitter with Low Noise ADPLL and High Linear PA

by

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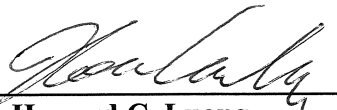

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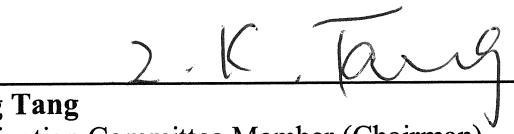

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Nomenclature

ACLR: Adjacent Channel Leakage Ratio

ACPR: Adjacent Channel Power Ratio

ACW: Amplitude Control Word

ADC: Analog-to-Digital Converter

ADPLL: All Digital Phase Lock Loop

ADTX: All Digital Transmitter

AM: Amplitude Modulation

BER: Bit Error Rate

BPSK: Binary Phase-Shift Keying

CF: Crest Factor

CMOS: Complementary metal–oxide–semiconductor

CP: Charge Pump

DAC: Digital-to-Analog Converter

DCC: Duty Cycle Correction

DCO: Digitally-Controlled Oscillator

DPA: Digitally-Controlled Power Amplifier

DPM: Digitally-Controlled Phase Modulator

EVM: Electronic Voting Machine

FCW: Frequency Control Word

FLL: Frequency Lock Loop

HRM: Harmonic Rejection Mixer

INL: Integral nonlinearity

ISF: Impulse-Sensitive Function

LSB: Least significant bit

MSB: Most Significant Bit

OFDM: Orthogonal frequency-division multiplexing

OSC: Oscillator

PA: Power Amplifier

PAE: Power Added Efficiency

PAPR: Peak-to-Average Power Ratio

PFD: Phase-Frequency Detector

PI: Phase Interpolation

PLL: Phase Lock Loop

PM: Phase Modulation

QAM: Quadrature Amplitude Modulation

QPSK: Quadrature Phase-Shift Keying

QVCO: Quadrature voltage-controlled oscillator

SCA: Switch-Capacitors Arrays

SFDR: Spurious-Free Dynamic Range

SSBM: Single-Sideband Mixer

TDC: Time-to-Digital Converter

VCO: Voltage-Controlled Oscillator

WCDMA: Wideband Code Division Multiple Access

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A CMOS Digital Polar Transmitter with Low Noise ADPLL and High Linear PA

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Abstract

Digitally-intensive RF design has attracted a lot of attention recently because it is highly programmable for multi-standard operation and enables high system integration with digital baseband and application processors on the same die. Moreover, many RF impairments could be repaired by using digital calibration.

This thesis presents a 65nm all digital polar transmitter with on chip LO generation, polar modulation and power amplification for WCDMA and WLAN application.

In the LO path, an all-digital phase lock loop (ADPLL) is designed for low noise and low spur carrier generation. To reduce the out-band phase noise, a quadrature phase digitally-controlled oscillator (QDCO) with quantization noise suppression technique is proposed and measured 6.6dB improvement of the out-band phase noise. The in-band phase noise of the ADPLL is minimized by using a statistical TDC with ultra-fine time resolution and a proposed phase-interpolated ΣΔ programmable divider

To reduce the DCO pulling effects, a quadrature output ÷1.5 divider is proposed for the LO frequency plan. This ÷1.5 divider employs 8-phases harmonic rejection mixing and duty-cycle correction techniques to minimize its output I-Q mismatch. For Wide-band and fine-resolution phase modulation, a 2-segments phase-interpolated ΣΔ digital phase modulator is employed with bandwidth extension and phase error calibration techniques.

In the AM path, a novel digital polar amplifier with switched-capacitor modulator and high linear PA-array is proposed to achieve the output power range for the target applications. A linearization technique is implemented by adaptively changing the PA bias voltage according to the RF envelope. Even without amplitude pre-distortion, the transmitter system measures RMS-EVM of 2.83% and 4.07% for WCDMA and WLAN 54-Mb/s 64-QAM OFDM respectively while providing a peak output power of 20.4dBm with PAE 32.3%.

CHAPTER 1 INTRODUCTION TO DIGITAL TRANSMITTER

1.1 Background

Microelectronics industry is geared toward an ever-expanding use of digital circuits, because digital data is easy to process and store; moreover, digital design can take immediate advantage of technology scaling down. In the past 30 years, MOS device size reduction has led to an exponential growth in integration density, with a 1.3~1.5 increase factor per year. This trend is known as “Moore's law” [1.1] which is the main driving force of timing schedule for the semiconductor industry [1.2].

With recent advances in CMOS technologies, integrating RF transceivers with digital baseband and application processor into a single chip has become feasible and attractive [1.3]-[1.5]. Such sing-chip integration offers many advantages, including:

- Cost reduction by using smaller bill of materials
- Increase system performance
- Lower power consumption and longer battery life
- Smaller form factor

However, the design flow and circuit technology for the RF transceiver are typically analog intensive and the process technologies they used are typically incompatible with the digital part. As a result, design of such highly integrated RF System-on-Chip (SoC) would face with a lot of great challenges: 1) As the technology scale down, the supply voltage becomes lower and the signal swing is limited; the

switching noises from the surrounding high speed digital blocks become more significant for the RF and analog signals. 2) The non-ideal effects of the deep sub-micron transistors such as: process mismatch, channel-length modulation, flicker noise and so on degrade the accuracy of the analog and RF signal processing. 3) The chip area occupied by the analog and RF building block cannot scale down, (for example, an inductor at 65nm costs around 300K digital gates) which affects the total system cost. 4) The complexities in the simulation and verification of the RF SoC increase aggressively, which presents a great difficulty in the development phase and result in much longer turnaround cycle.

On the contrary, the digital signal processing becomes more powerful because the increase of switching speed and logic gate density in the scale-down technology. Instead of having to struggle to design and implement analog components, such as: analog amplifier, charge pump, continues-time filter, analog mixer and so on; the RF SoC designers can employ digital intensive RF techniques to process RF signals with familiar and proven tools and processes. Such techniques include:

- Oversampling converter
- Digital frequency synthesizer
- Digital amplitude/phase modulator
- Digital power amplifier
- Digital calibration
- Digital filter
- …

These techniques employ high-performance digital circuits in deep-submicron CMOS and provide “digital assistance” to the RF front-end, such as increase in

programmability for multi-band/multi-mode operation and process mismatch compensation. Moreover, the advantages of conventional digital design flow can be taken, including:

- Predictable performance – much lower parameter variability than the analog circuits
- Higher testability – automatic functional testing with good error coverage
- Smaller silicon area and lower power consumption – keep improving in every new process node
- Fast design turnaround circle – By using automated CAD tools, including auto synthesis, auto place-and-route layout generation and accuracy timing-driven verification
- An excellent chance of first-time silicon success

1.2 Research Motivation

Given the advantages mentioned above, when implementing single-chip multi-band/multi-mode RF transceivers, designing of power amplifier (PA) still remains the most challenging [1.6] [1.7] not only because the PA tends to disturb the sensitive blocks such as VCO and LNA [1.8] [1.9] but also because it requires large output power and high efficiency. Moreover, for high data-rate communication with high spectrum efficiency, non-constant envelope modulation with large peak-to-average ratio (PAR) are used, such as quadrature amplitude modulation (QAM), orthogonal frequency division multiplexing (OFDM), and quadrature phase shift keying (QPSK) with root-raise cosine filtering. These applications require the PA to have sufficient linearity to meet their stringent specification.

The aim of this research program is to investigate the feasibility of an all-digital radio transmitter system with full-levels of integration in advance scale-down CMOS technology. The transmitter architecture and circuit implementation have been explored to achieve multi-standards operation with low-cost, low-noise, high-linearity, and high-efficiency.

1.3 Organization of this dissertation

- Chapter 2 provides a literature review of the RF transmitter design and overviews different kinds of transmitter architectures, including: direct-conversion, out-phasing and polar transmitter. Also, it will show you that the polar transmitter has not only a better trade-off between efficiency and linearity but also the possibility of realization in advanced scale-down CMOS technology. Finally, the system design of the proposed digital polar transmitter will be discussed.
- Chapter 3 introduces the basic concepts of the frequency synthesizer and explains the reason of using "all-digital" realization. Each building block of the ADFS will be discussed, including: A QDCO with embedded phase shifter and quantization noise filter, a statistical TDC with ultra fine resolution and a phase-interpolated ΣΔ fractional-N divider. Also, the design flow of the digital loop filter will be presented and there is a performance summary in the end.
- Chapter 4 introduces the VCO pulling effects and shows you these effects can be eliminated by choosing the VCO frequency and LO frequency carefully. After that the ÷1.5 divider with I-Q output is introduced with the techniques to

minimize the I-Q mismatches, including 8-phase harmonic rejection mixing based ÷1.5 divider with duty-cycle correction.

- Chapter 5 presents a digitally-controlled phase modulator. It employs 2-segments architecture and using high linear phase-interpolation and ΣΔ modulation to achieve wide-band operation with wide-range and fine-step phase tuning. After that, an all-digital phase calibration technique to reduce the phase mismatch will be introduced.
- Chapter 6 presents a new architecture of the digital polar amplifier. It is composed of a digital interpolation filter, a digital polar modulator and a high-linear PA. The limitations of existing linearization techniques for the polar PAs are discussed, including close-loop polar amplifier and digital pre-distortion polar amplifier. Then the proposed PA with AM replica feedback linearization is introduced with a performance summary and comparison in the end.
- Chapter 7 presents the experiment results of the transmitter, including: measurement setup, phase noise, spurs, output power, efficiency, emission mask, EVM and power consumption. These results will be compared with other state-of-the-art transmitters.
- Finally, conclusions will be draw and summary the contribution of the dissertation. The recommendation for the future work is presented in the end.

Bibliography

[1.1] Intel Corp., What is Moore's Law? Available at URL http://www.intel.com/intel/museum/hof/moore.htm

[1.2] Semiconductor Industry Association (SIA), the International Technology Roadmap for Semiconductors, 1999. Available at URL http://public.itrs.net/1999_SIA_Roadmap/Home.htm

[1.3] R. B. Staszewski and P. T. Balsara, "All-Digital Frequency Synthesizer in Deep-Submicron CMOS," Hoboken, NJ: Wiley, 2006.

[1.4] Darabi, H.; et al., "A Quad-Band GSM/GPRS/EDGE SoC in 65 nm CMOS" *IEEE J. Solid-State Circuits*, VOL.46, NO. 4, pp. 870–882, May 2011.

[1.5] R. B. Staszewski et al., "A 24 mm quad-band single-chip GSM radio with transmitter calibration in 90 nm digital CMOS," in *IEEE ISSCC* Dig. Tech. Papers, 2008, pp. 208–209.

[1.6] Kanda, K.; et al., "A fully integrated triple-band CMOS power amplifier for WCDMA mobile handsets" in *IEEE ISSCC* Dig. Tech. Papers, 2012, pp. 86–88.

[1.7] Kousai, S.; et al, "A 28.3mW PA-closed loop for linearity and efficiency improvement integrated in a +27.1dBm WCDMA CMOS power amplifier" in *IEEE ISSCC* Dig. Tech. Papers, 2012, pp. 84–86.

[1.8] Chandrashekar, K.; et al., "A 32nm CMOS all-digital reconfigurable fractional frequency divider for LO generation in multistandard SoC radios with on-the-fly interference management," in *IEEE ISSCC* Dig. Tech. Papers, 2012, pp. 352–354.

[1.9] S. Pellerano, et al., "A 4.75-GHz Fractional Frequency Divider-by-1.25 With TDC-Based All-Digital Spur Calibration in 45-nm CMOS," *IEEE J. Solid-State Circuits*, vol.44, no.12, pp.3422-3433, Dec. 2009

CHAPTER 2 TRANSMITTER OVERVIEW

2.1 Transmitter Fundamental

RF transmitter transmits signals through free space by electromagnetic radiation of a radio wave [2.1]. The transmitted data is carried by systematically changing some properties of the radiated wave, such as their amplitude, frequency, phase, or pulse width. In the digital wireless communication system, transmitter provides the interfaces for the digital baseband and the antenna; it performs modulation, up-conversion and power amplification [2.2].

Conventional modulation strategies use orthogonal vectors to describe a two-dimensional space. As shown in Fig. 2.1(a), the vector is typically referred to as in-phase, I and quadrature-phase, Q. The RF signal trajectory is mapped using *I(t)* and *Q(t)* baseband signals and up-converted using quadrature local oscillators:

$$v(t) = I(t)\sin(\omega_c t) + Q(t)\cos(\omega_c t) \tag{2.1}$$

where ω_c is the RF carrier frequency.

v(t) can be decomposed into the polar form shown in Fig. 2.1(b) using the amplitude and phase of the RF carrier. With a polar representation, *v(t)* is written as follows:

$$v(t) = A(t)\cos[\omega_c t + \phi(t)] \tag{2.2a}$$

$$A(t) = \sqrt{I(t)^2 + Q(t)^2} \tag{2.2b}$$

$$\phi(t) = \tan^{-1}\left(\frac{Q(t)}{I(t)}\right) \tag{2.2c}$$

where *A(t)* and $\phi(t)$ are the amplitude and the phase of the transmitted signals.

Importantly, complex representation of the transmitted signal allows many ways to encode the digital information.

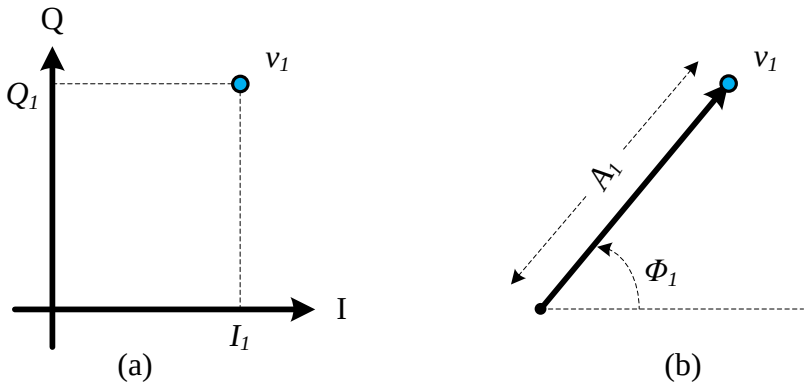


Fig. 2. 1 two views of a vector signal space (a) I-Q projections (b) polar form

2.2 Complex Modulation

Digital modulation scheme [2.3] encodes data in symbols which can be considered as vectors in a signal constellation with unique amplitude and phase. Each symbol can represent multiple bits of digital information; the number of bits per symbol depends on the complex of the constellation.

In phase-shift keying (PSK), the constellation points chosen are usually positioned with uniform angular spacing around a circle. This gives maximum phase-separation between adjacent points and thus the best immunity to corruption. They are positioned on a circle so that they can all be transmitted with a constant envelope carrier.

Two common examples are “binary phase-shift keying” (BPSK) which uses two phases and “quadrature phase-shift keying” (QPSK) which uses four phases, although any number of phases may be used. Since the data to be conveyed are usually binary, the PSK scheme is usually designed with the number of constellation points being a power of 2.

2.2.1 BPSK

BPSK (also sometimes called PRK, Phase Reversal Keying, or 2PSK) is the simplest form of phase shift keying (PSK). It uses two phases which are separated by 180 °and so can also be termed 2-PSK. It does not particularly matter exactly where the constellation points are positioned, and in Fig. 2.2 they are shown on the real axis, at 0 ° and 180 °. This modulation is the most robust of all the PSKs since it takes the highest level of noise or distortion to make the demodulator reach an incorrect decision. It is, however, only able to modulate at 1 bit/symbol, so it is unsuitable for high data-rate applications.

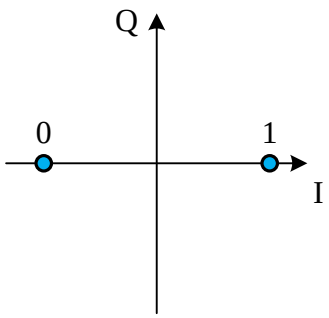


Fig. 2. 2 constellation diagram example for BPSK

2.2.2 QPSK

Quadrature phase-shift keying (QPSK) uses four points equally spaced around a circle on the constellation diagram. As shown in Fig. 2.3, with four phases, QPSK can encode two bits per symbol. The mathematical analysis shows that QPSK can be used either to double the data rate compared with a BPSK system while maintaining the same bandwidth of the signal, or to maintain the data-rate of BPSK but halving the bandwidth needed. In this latter case, the BER of QPSK is exactly the same as the BER of BPSK

Given that radio communication channels are allocated by agencies such as the

Federal Communication Commission (FCC) giving a prescribed (maximum) bandwidth, the advantage of QPSK over BPSK becomes evident: QPSK transmits twice the data rate in a given bandwidth compared to BPSK – at the same BER. The engineering penalty that is paid is that QPSK transmitters and receivers are more complicated than the ones for BPSK. However, with modern electronics technology, the penalty in cost is very moderate.

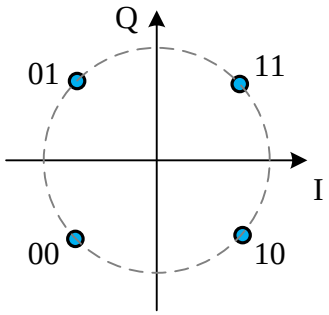


Fig. 2. 3 constellation diagram example for QPSK

2.2.3 QAM

To achieve higher symbol rate for a given spectrum bandwidth, both amplitude and phase modulation can be employed, as called “quardrature amplitude modulation” (QAM). In QAM, the constellation points are usually arranged in a square grid with equal vertical and horizontal spacing. Since QAM is usually square, the most common forms are 16-QAM (shown in Fig. 2.4), 64-QAM and 256-QAM. By moving to a higher-order constellation, it is possible to transmit more bits per symbol. However, if the mean energy of the constellation is to remain the same, the points must be closer together and are thus more susceptible to noise and other corruption; this results in a higher bit error rate and so higher-order QAM can deliver more data less reliably than lower-order QAM, for constant mean constellation energy.

If data-rates beyond those offered by 8-PSK are required, it is more usual to move to QAM since it achieves a greater distance between adjacent points in the I-Q plane by distributing the points more evenly. The complicating factor is that the points are no longer all the same amplitude and so the demodulator must now correctly detect both amplitude and phase, rather than just phase.

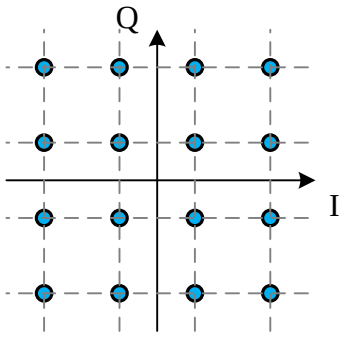


Fig. 2. 4 constellation diagram example for 16-QAM

2.3 Radio Transmitter Specification

2.3.1 Output power range and efficiency

Cellular systems which are based on CDMA define both a maximum output power and a power control range. The base station adjusts the transmitted power of the user's TX in order to accommodate the variable distance of the terminal. An active feedback control loop between the user's TX and the base station updates the gain setting of the TX. For instance, the WCDMA specifies 24dBm of maximum output power and 75dB of power control range [2.4]. While for the 802.11 b/g wireless LAN with 20 MHz-wide channel in the 2.4 GHz ISM band, to meet the 5 mW/MHz requirement of the EIRP (equivalent isotropically radiated power), the maximum output power of the transmitter should be 20dBm.

In general, the term efficiency signifies how efficiently the PA is converting the DC power from the supply to the RF output power. The DC power drawn from the supply can be simply expressed as:

$$P_{DC} = \frac{1}{T}\int_0^T V_{DD} i_{DD} dt = \frac{V_{DD}}{T}\int_0^T i_{DD} dt = V_{DD} I_{DD} \tag{2.3}$$

The average power delivered to a purely resistive load can also be calculated from the current and the voltage signal according to:

$$P_{out} = \frac{V_{out,RMS}^2}{R_L} = I_{out,RMS}^2 R_L \tag{2.4}$$

The drain efficiency is defined as:

$$\eta = \frac{P_{OUT}}{P_{DC}} \tag{2.5}$$

The drawback of drain efficiency is that it doesn't depend on the gain of the PA. If two PAs have the same output power and draw the same DC power they still might have different gain and input power. Hence, a different concept is often used to characterize the efficiency of the PA. It is called *PAE* (Power Added Efficiency) and it is defined as:

$$PAE = \frac{P_{OUT} - P_{IN}}{P_{DC}} \tag{2.6}$$

where *Pin* is the available input power. If the power gain is defined as:

$$G_P = \frac{P_{OUT}}{P_{IN}} \tag{2.7}$$

then the equation 2.6 can be rewritten as:

$$PAE = \eta * (1 - \frac{P_{IN}}{P_{OUT}}) = \eta * (1 - \frac{1}{G_P}) \tag{2.8}$$

It can be seen that if the two PAs have the same output power and DC power, the PA which has a higher gain will have a higher *PAE*.

The previous analysis is valid for the constant envelope signals. If an amplitude modulated signal is applied to the PA both the output power and the efficiency are also functions of the varying envelope signal.

The output is varying according to the amplitude modulated signal. This variation can be described by parameters like Crest Factor (*CF*) in case of voltage signals and by Peak to Average Power Ratio (*PAPR*) when the power signals are handled. The *PAPR* is defined as:

$$PAPR = \frac{P_{EP}}{P_{OUT}} \tag{2.9}$$

where P_{EP} stands for Peak Envelope Power and *Pout* is the average output power of the amplitude modulated signal. The peak envelope power is defined as the average power supplied to the antenna transmission line by a transmitter during one RF cycle at the crest of the modulation envelope, under normal operating conditions. The P_{EP} of the PA can be expressed as

$$P_{EP} = \max\{P_{OUT}\} = \frac{\max\{V_{out}^2(t)\}}{R_L} \tag{2.10}$$

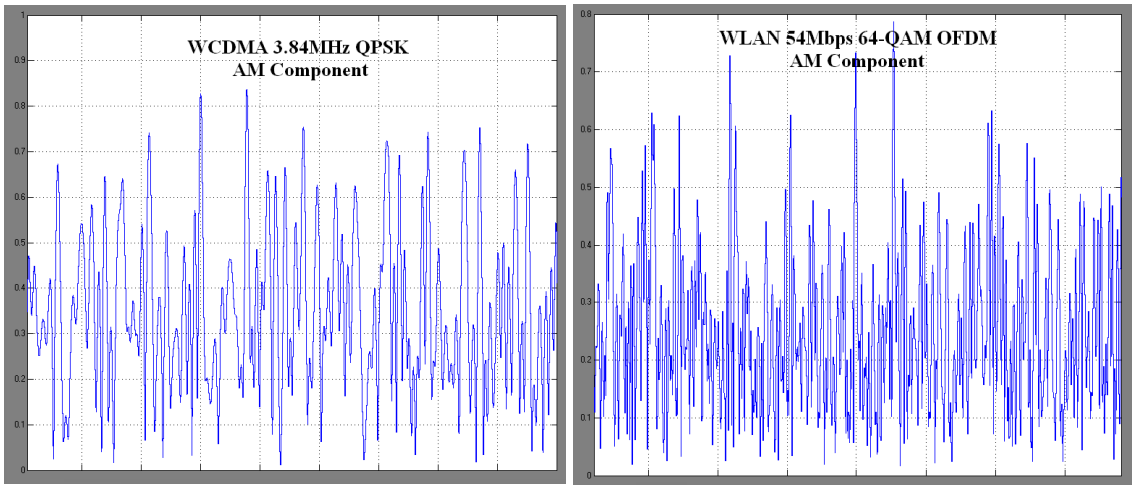
where V_{out} is the amplitude of the output voltage signal.

The Crest Factor (*CF*) is defined as the peak amplitude divided by the RMS value of the waveform. The PAPR equals to $PAPR = CF^2$

$$CF = \frac{\max\{V_{out}\}}{V_{out,RMS}} \tag{2.11}$$

Fig. 2.5 shows the example of the time varying amplitude modulated component of

the (a) WCDMA and (b) 20MHz WLAN signals.



(a) **(b)**

Fig. 2. 5 The AM component of (a) WCDMA and (b) WLAN signals

Generally, the efficiency of the PA which has to transmit a signal with a high PAPR will be much lower than the peak efficiency of the PA when it is saturated. The linear PA which has to amplify a modulated signal with high PAPR has to be capable to transmit the P_{EP} but the average output power will be much lower. The input power of the linear PA has to be decreased according to the PAPR of the modulated signal so that the signal can be transmitted without pushing the PA into saturation. This mode of operation is called power back-off. The power back-off linearization technique significantly decreases the overall efficiency of the PA and it is one of the major reasons why the linear PAs have such a low efficiency when they transmit complex modulated wireless signals with a high PAPR.

The efficiency of a PA is a function of the varying envelope signal A(t). Generally, the efficiency is always a function of the output power. Because the amplitude modulation modulates the output power it will also change the efficiency. To characterize this effect one can define the average drain efficiency as: [2.5]

$$\eta = \eta[A(t)] = \lim_{T\to\infty} \frac{1}{T} \int_{-T/2}^{T/2} \eta[A(t)]dt \tag{2.12}$$

Notice that the equation above gives an arithmetic average of drain efficiency and it is different from average efficiency calculated based on Eq. (2.3).

Another effect which directly influences the overall efficiency is the probability distribution function (PDF) of the output power [2.6]. The average output power level is usually set by the base station which is constantly evaluating the quality and power of the received signal. The active power control can be used to increase the battery life time of a mobile device but it can also be used by the wireless network to maximize its capacity (WCDMA). The period of the power level adjustment is different for each mobile standard. The PDF of the output power is obtained by long term measurements and it is usually specified for the different network environments (urban or rural). An example of the output power PDF in EDGE/WCDMA is shown in Fig. 2.6.

The drain efficiency can be expressed as a function of the PDF according to:

$$\eta = \int_{P_{out,\min}}^{P_{out,\max}} \eta(P_{out}) * PDF(P_{OUT}) dP_{OUT} \tag{2.13}$$

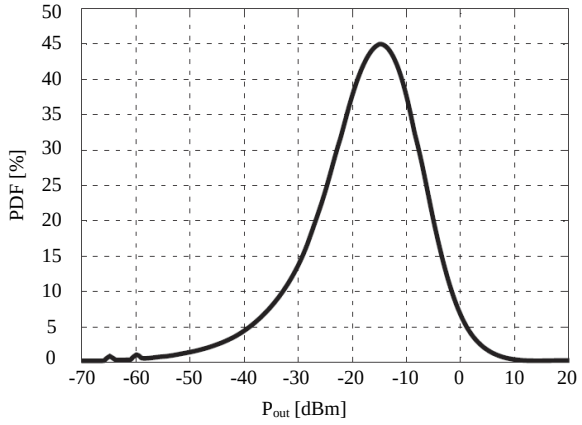


Fig. 2. 6 PDF versus output power of the WCDMA mobile station transmitter

2.3.2 Occupied bandwidth and adjacent channel power leakage (ACLR)

In order to make efficient use of the spectrum, cellular systems tend to have stringent specifications on the bandwidth that a signal within a channel occupies. As an outcome of the nonlinear signal distortion, the transmitted signal spectrum may grow and leak into the adjacent channel which degrades the adjacent-channel-leakage ratio (ACLR). Another source of ACLR degradation is the signal spurs which can be generated within the synthesizer or couple through the supply. Table 2.1 presents a list of channel bandwidths together with the ACLR requirements.

Table 2. 1 Channel bandwidths and ACLR

	GSM	EDGE	WCDMA	802.11 a/b/g
Channel BW (MHz)	0.2	0.2	5	20
ACLR (dB)	-30/60	-30/-54	-33/-44	-40

2.3.3 Spectral Mask

A similar metric to ACLR is spectral mask. The power spectral density of a RF transmitter is sometimes referred as spectral emission. A spectral mask is generally intended to reduce the interference by limiting excessive radiation at frequencies beyond the necessary bandwidth. Fig. 2.7 shows the spectral mask specified in the WCDMA/WLAN 802.11 standard. The graph illustrates the maximum allowed power density, normalized to the power density within the signal band, as a function of the frequency offset from the carrier.

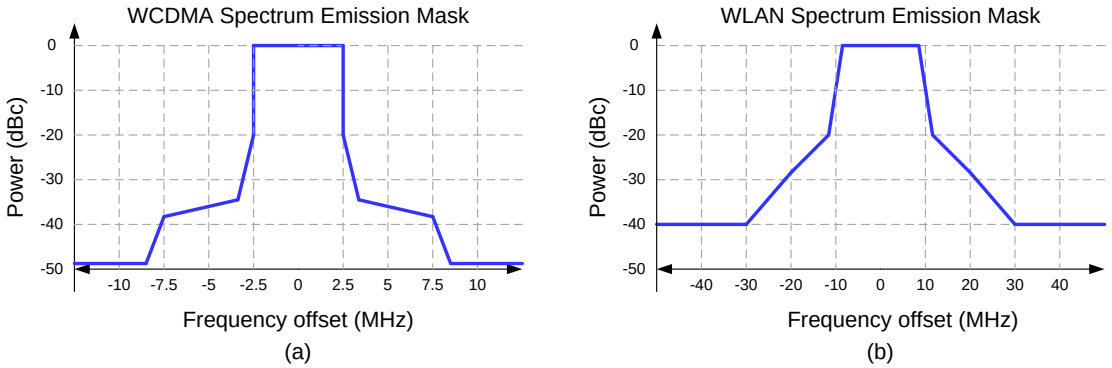


Fig. 2. 7 Spectral mask (a) WCDMA (b) WLAN 802.11 b/g

2.3.3 Constellation pattern and error vector magnitude (EVM)

The tradeoff with higher order modulation schemes is that more resolution is needed to represent the symbol. A metric which relates to the size of the constellation pattern is the error vector magnitude (EVM). Shown in Fig. 2.8, EVM describes how the transmitted or received constellation pattern differs from the ideal one. It is typically defined as a root-mean-squared quantity across a number of symbol measurements:

$$EVM = \frac{\sqrt{\frac{1}{N}\sum_{j=1}^{N}(V_e^2)}}{|V_m|} \tag{2.14}$$

where V_e is the magnitude of the error vector for each symbol, V_m is the magnitude of the desired symbol vector, and N is the number of measurements.

Sources of EVM degradation in a TX are the synthesizer phase noise, the carrier leakage, the I-Q imbalance and the baseband filter group delay variation. Furthermore, the EVM specification has to be satisfied within the whole power control range.

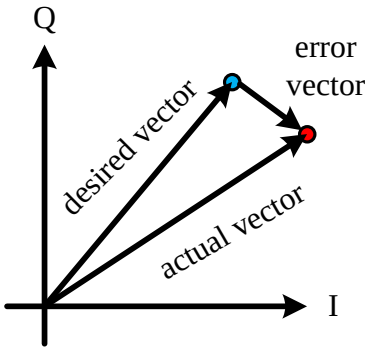


Fig. 2. 8 Error vector is the difference between the actual and ideal symbol vectors

Table 2.3 shows the EVM specification for different systems together with their crest factor. In OFDM modulated systems, EVM has to be very low because a larger constellation is more sensitive to errors.

Table 2. 2 System EVM and crest factor

	EDGE	WCDMA	802.11 a/b/g
EVM	9%	17.5%	5.6%
Crest factor (dB)	3	3.35-7.5	10-12

2.4 Transmitter Architecture

The choice of transmitter architecture is determined by many factors: the number of off-chip components, the restrictions on unwanted emission, and the trade-off between the output power and efficiency. Also, the required linearity directly impact on the transmitter topology and implementation of each circuit block. Furthermore, the disturbance from the transmit path to the transceiver's oscillators and receive path influence the frequency planning and the level of integration [2.7].

2.4.1 Direct-Conversion Transmitter

If the transmitted carrier frequency is equal to the local oscillator (LO) frequency, the architecture is called "direct conversion." Fig. 2.9 shows the block diagram of the direct conversion transmitter [2.8]-[2.10]. The signal *S(t)* at the transmitter output can be described as:

$$S(t) = I(t)\sin(\omega_c t) + Q(t)\cos(\omega_c t) \tag{2.15}$$

where *I(t)* and *Q(t)* are the I and Q digital baseband signals.

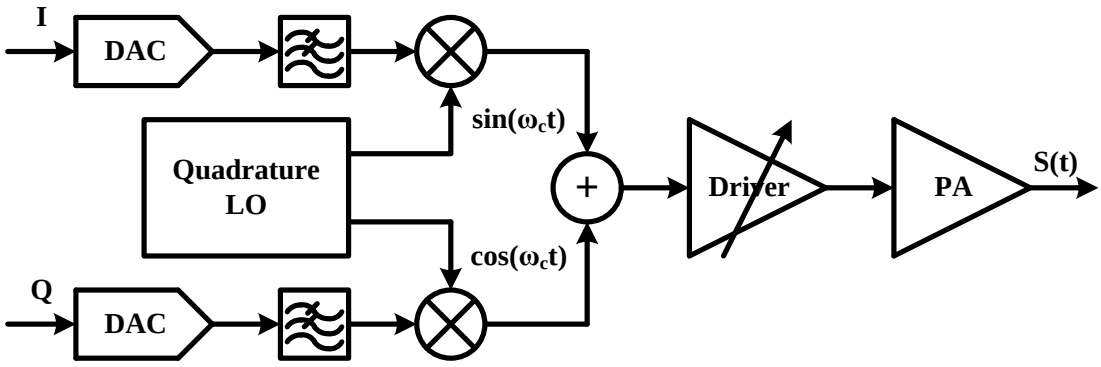


Fig. 2. 9 Block diagram of the direct conversion transmitter

There are some important issues in design of the direct conversion transmitter: 1) LO pulling. Due to the finite isolation between the VCO and the PA, the output spectrum of PA corrupts the oscillator purity through injection pulling. To tackle this problem, the VCO output frequency should be different from the RF frequency in the LO generation. 2) I-Q imbalance. 3) DC offset. The last two design issues are because the process mismatch in those analog and RF signal processing paths. Calibrations are needed to cancel out this non-ideality.

2.4.2 Outphasing Transmitter

An interesting approach to avoiding amplitude variations in a PA system is outphasing transmitter [2.11]-[2.12]. Illustrated in Fig. 2.10, the idea is that a bandpass signal *v(t)* can be expressed as the sum of two constant-amplitude phase-modulated signals *v1(t)* and *v2(t)*.

$$v(t) = a(t)\cos[\omega_c t + \phi(t)] \tag{2.16a}$$

$$v(t) = v_1(t) + v_2(t) \tag{2.16b}$$

$$v_1(t) = \frac{1}{2} V_o \sin[\omega_c t + \phi(t) + \theta(t)] \tag{2.16c}$$

$$v_2(t) = -\frac{1}{2} V_o \sin[\omega_c t + \phi(t) - \theta(t)] \tag{2.16d}$$

where $\theta(t) = \sin^{-1}[\frac{a(t)}{V_o}]$. Thus, $v_1(t)$ and $v_2(t)$ can be generated from the non-linear switch-PAs with high power efficiency.

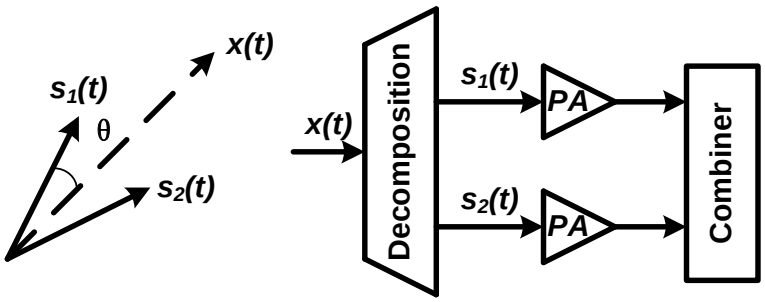


Fig. 2. 10 Block diagram of the outphasing transmitter

Outphasing transmitter must deal with two important issues. First, gain and phase mismatch between the two signal paths in Fig. 2.10 results in residual distortion. Second, the output adder introduces significant loss because it must achieve a high isolation between the two PAs.

2.4.3 Polar Transmitter

As mentioned in Eqs. (2.2a), (2.2b) and (2.2c), any bandpass signal can be represented as: $S(t)=A(t)\cos[\omega_c t+\phi(t)]$, that is by an envelope signal $A(t)$ and a phase signal $\phi(t)$. This observation leads to the idea of decomposing $S(t)$ into an envelope signal and a phase-modulated signal, amplifying each separately, and combining the result at the end.

2.4.3.1 Traditional Polar Transmitter Architecture

Fig. 2.11 shows the traditional polar transmitter architecture [2.13] [2.14]. In the PM path, the baseband PM signals control the analog phase lock loop to generate the phase-modulated LO for the PM carrier. In the AM path, the digital AM signal is converted to analog by a digital-to-analog converter (DAC) together with an analog reconstruction filter. A supply modulator receives the analog AM signal as a reference and generates the supply voltage for the PA. This PA operates at switch mode for the combination of the AM and PM signals.

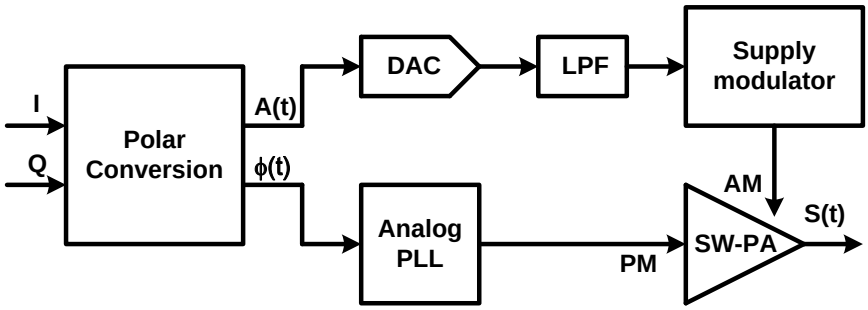


Fig. 2. 11 Traditional polar transmitter architecture

The polar transmitter relaxes the linearity requirement of the PA and then has a much better power efficiency. However, there are several drawbacks for this

architecture: First, the AM path has limited bandwidth due to the narrow-band supply modulator. Second, the time delays for the signal processing in the AM and PM paths are different. These time delays vary with the process variation and make it very difficult to synchronize the AM and PM signals. Third, the analog loop filter of the PLL and the DAC reconstruction filter occupy a large chip area; also, the supply modulator normally requires off-chip components.

2.4.3.2 All-Digital Polar Transmitter Architecture

Fig. 2.12 shows the all-digital polar transmitter architecture [2.15]-[2.17]. The PM signal is generated from an all-digital phase-lock-loop (ADPLL) and the RF envelope is controlled by tuning on/off sub-set of the PA cells according to the A(t). With the digital implementation, the time delay of the signal processing in AM and PM paths can be synchronized by the digital clock. In addition, the massive analog filters are removed in this architecture, so the chip area can be reduced aggressively and the integration level is much higher. Moreover, the digital images due to the sampling are pushed far away by the digital interpolation filter. So, wide band polar modulation can be achieved.

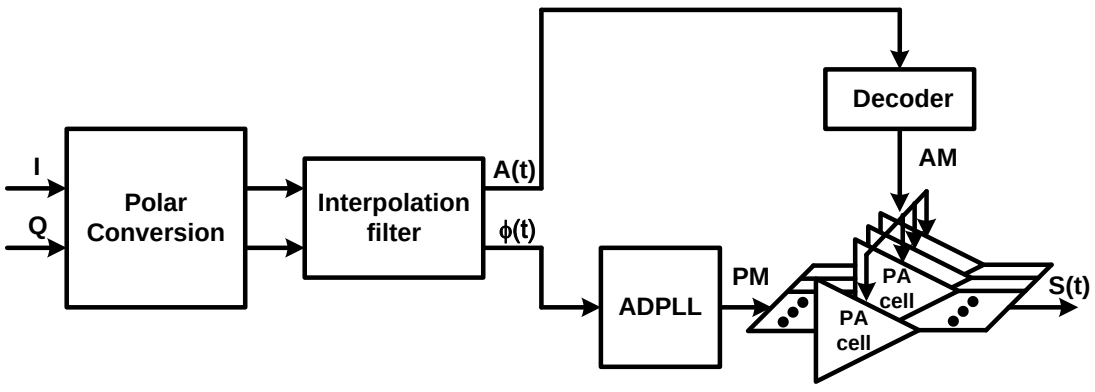


Fig. 2. 12 All-digital polar transmitter architecture

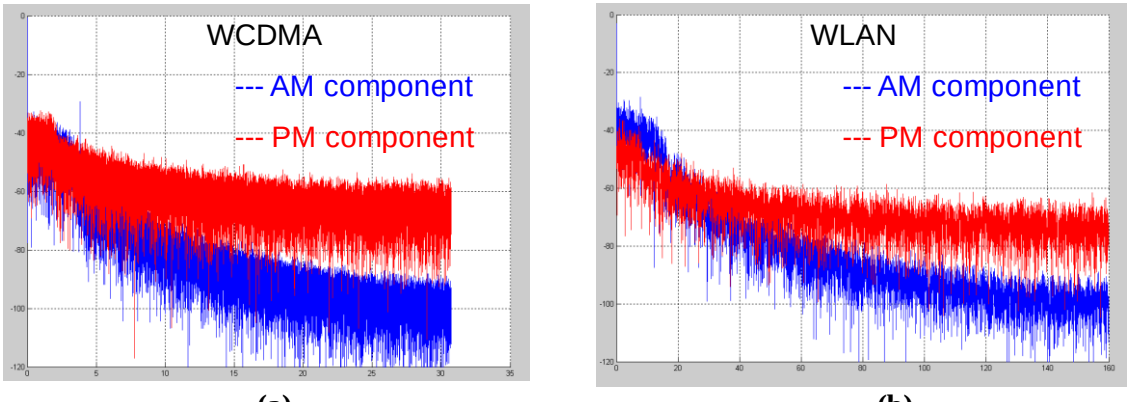
2.5 System design of the All Digital Polar Transmitter

The transmitter specifications for WCDMA and WLAN are summarized in Table 2.3. The most challenging parameters are marked in red color. For WCDMA, the required power control range is 75dB; while for WLAN 802.11 b/g, the maximum bandwidth is 20MHz.

Table 2. 3 Transmitter System specification

Standard	Frequency	Channel Bandwidth	Modulation	Max output power	PAPR	Power control range	EVM
WCDMA	1.92-1.98GHz 1.85-1.91GHz	5MHz	QPSK	24dBm	3.5-7dB	75dB	17.5%
WLAN IEEE 802.11 b/g	2.4-2.484GHz	20MHz (Max.)	BPSK, QPSK, 16-QAM, 64-QAM, OFDM	~20dBm	~10dB		5.6% (54Mbps 64-QAM OFDM)

The frequency spectrums of the AM and PM components for WCDMA and 20MHz WLAN are shown in Fig. 2.13. Table 2.4 summarizes their I-Q bandwidth and required AM and PM paths modulation bandwidth. In addition, the AM to PM time delay mismatch should be less than 2ns.



(a) **(b)**

Fig. 2. 13 Frequency spectrums of the AM and PM components for WCDMA and 20MHz WLAN

Table 2. 4 Bandwidth and delay mismatch requirements

Parameters	WCDMA	WLAN (54Mbps, 64-QAM OFDM)
I/Q path bandwidth	3.84MHz	16.7MHz
AM path bandwidth	7MHz	43MHz
PM path bandwidth	11MHz	67MHz
AM-PM time delay mismatch	<2nS	

As shown in Fig. 2.11, the limited AM and PM modulation bandwidth of the traditional polar transmitter architecture cannot meet this requirement. In addition, the AM – PM time delay mismatch will be much larger than 2ns. To enlarge the modulation bandwidth, a novel all digital polar transmitter architecture is proposed and shown in Fig. 2.14. For the PM carrier generation, an ADPLL is employed for low noise LO generation; a ÷1.5 divider is inserted to eliminated the LO pulling effect; to achieve wideband phase modulation, a digital phase modulator with phase interpolation and selection is designed to modulate the phase of the carrier. In the AM path, a high linear digital polar amplifier achieves wide band modulation by using oversampling. The AM and PM paths are synchronized by digital clock. The design parameters for the AM and PM paths are shown in table 2.5 and table 2.6 respectively.

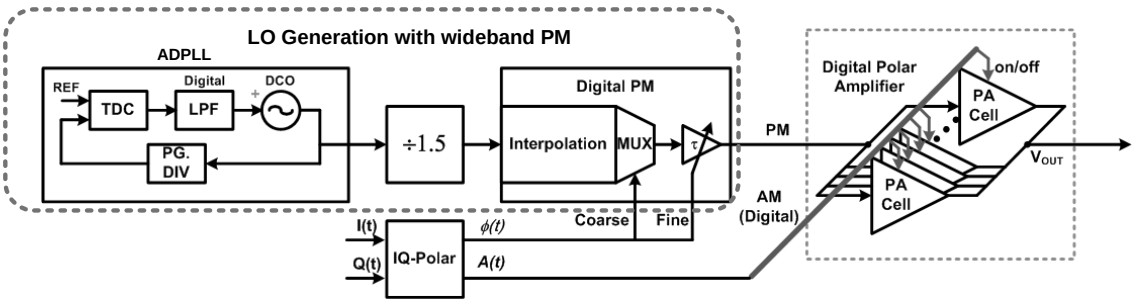


Fig. 2. 14 Proposed all digital polar transmitter architecture

Table 2. 5 Design parameters for LO generation with wideband PM

Parameters	WCDMA	WLAN (54Mbps)
OSC frequency (GHz)	2.77~2.97	3.6~3.73
Output frequency (GHz)	1.85~1.98	2.4~2.484
PM bandwidth	11MHz	67MHz
PM resolution	9-bit	10-bit
Phase noise (dBc/Hz)	-120@3MHz	-102@1MHz

Table 2. 6 Design parameters for the Polar PA

Parameters	WCDMA	WLAN (54Mbps)
Output power (dBm)	24	20
AM resolution	>8-bit	>6-bit
Gain control	75dB	~
AM-PM mismatch	<2ns	
AM-PM conversion	<5°	

The following sections of this thesis will focus on the design consideration of the all digital polar transmitter. Design trade-off and not-ideality of each building block and sub-system will be discussed. New architectures and circuit techniques are proposed to optimize the chip area, performance and power consumption.

Bibliography

[2.1] Dictionary of Electronics By Rudolf F. Graf (1974). Page 467.

[2.2] B. Razavi, RF Microelectronics, Upper Saddle River, NJ: Prentice-Hall, 1998

[2.3] Kundu Sudakshina, Analog and Digital Communications, Pearson Education India, pp. 163–184. ISBN 978-81-317-3187-1 2010

[2.4] 3GPP mobile broadband standard, available in http://www.3gpp.org/Technologies/ Keywords-Acronyms/article/w-cdma

[2.5] Patrick Reynaert.; et al., RF Power Amplifiers for Mobile Communications, Springer, 2006

[2.6] John F. S. "Statistical Characterization of RF Power Amplifier Efficiency for CDMA Wireless Communication Systems," Wireless Communications Conference, pages 110~113, 1997.

[2.7] B. Razavi, "RF Transmitter Architecture and Circuits" *IEEE Custom Integrated Circuits Conference*, page 197-204, 1999

[2.8] Brenna, G.; et al., A 2-GHz carrier leakage calibrated direct conversion WCDMA transmitter in 0.13-μm CMOS," *IEEE J. Solid-State Circuits*, vol.39, no.8, pp.1253-1262, Aug. 2004

[2.9] Perraud, L.; et al., "A direct-conversion CMOS transceiver for the 802.11a/b/g WLAN standard utilizing a Cartesian feedback transmitter," *IEEE J. Solid-State Circuits*, vol.39, no.12, pp.2226-2238, Dec. 2004

[2.10] Cassia, M.; et al., "A Low-Power CMOS SAW-Less Quad Band WCDMA/HSPA/HSPA+/1X/EGPRS Transmitter," *IEEE J. Solid-State Circuits*, vol.44, no.7, pp.1897-1906, July 2009

[2.11] Heidari, M.E.; et al, "All-Digital Outphasing Modulator for a Software-Defined Transmitter," *IEEE J. Solid-State Circuits*, vol.44, no.4, pp.1260-1271, April 2009

[2.12] Ravi, A.; et al, "A 2.4-GHz 20–40-MHz Channel WLAN Digital Outphasing Transmitter Utilizing a Delay-Based Wideband Phase Modulator in 32-nm CMOS" *IEEE J. Solid-State Circuits*, vol.47, no.12, pp.3184-3196, Dec. 2012

[2.13] Kitchen, J.N.; et al., "Combined Linear and Δ-Modulated Switch-Mode PA Supply Modulator for Polar Transmitters," *IEEE J. Solid-State Circuits*, vol.44, no.2, pp.404-

413, Feb. 2009

[2.14] Wu, P.Y.; et al., "A Two-Phase Switching Hybrid Supply Modulator for RF Power Amplifiers With 9% Efficiency Improvement," *IEEE J. Solid-State Circuits*, vol.45, no.12, pp.2543-2556, Dec. 2010

[2.15] van Zeijl, P.T.M.; et al., "A Digital Envelope Modulator for a WLAN OFDM Polar Transmitter in 90 nm CMOS," *IEEE J. Solid-State Circuits*, vol.42, no.10, pp. 2204 - 2211, Oct. 2007

[2.16] Presti, C.D.; et al., "A 25 dBm Digitally Modulated CMOS Power Amplifier for WCDMA/EDGE/OFDM with Adaptive Digital Predistortion and Efficient Power Control," *IEEE J. Solid-State Circuits*, vol.44, no.7, pp. 1883 - 1896, July 2009

[2.17] Kavousian, A.; et al., "A Digitally Modulated Polar CMOS Power Amplifier With a 20-MHz Channel Bandwidth," *IEEE J. Solid-State Circuits*, vol.43, no.10, pp. 2251 - 2258, Oct. 2008

CHAPTER 3 ALL-Digital Phase Lock Loop

3.1 Phase Lock Loop Overview

The local oscillation (LO) frequency generation is the "heart" of the radio transceiver system. The spectrum purity of the LO frequency will directly affect the performance of the whole transceiver system. Fig. 3.1 illustrates the phase noise influence on the transmitting signals. In the transmitter, when the IF signal is up-converted to the desired RF channel, due to the existence of phase noise, the transmitting signal is spread out and emits to the neighboring channels. In the scenario described in the plot, the transmitter with the desired channel f_{RF1} is far away from the receiver, while another transmitter operating at the neighboring channel f_{RF2} is much closer. Consequently, at the receiver, the wanted signal would be seriously corrupted by the emission from the neighboring channel.

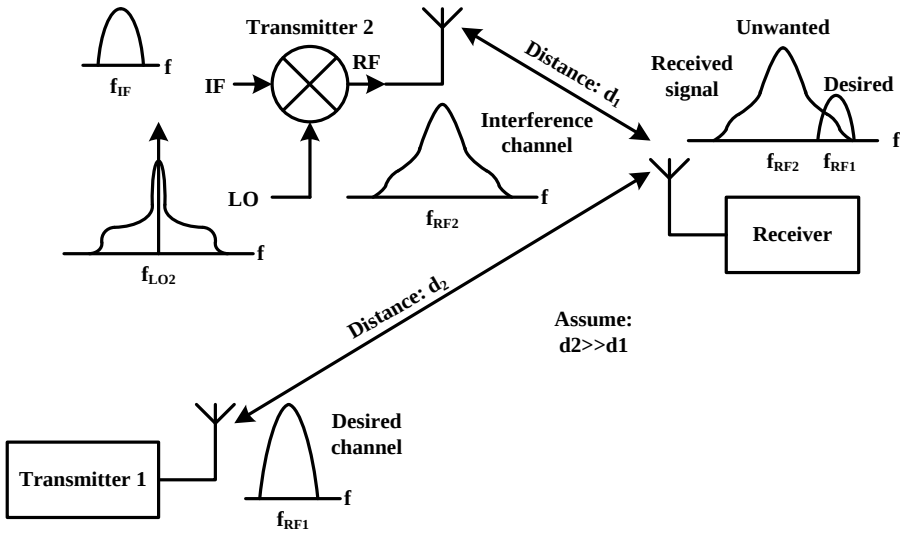


Fig. 3. 1 Phase noise influence on the transmitted signals

In order to guarantee proper communications, maximum allowable emission should be clearly specified for each wireless standard. Considering the worst case when the transmission signal power is maximal, the phase noise specification at different offset frequencies can be quickly calculated as below:

$$PN_{\max}(f_{offset}) = P_{emission}(f_{offset}) - P_{\max} - dB(IntegrationBW) \quad (3.1)$$

Here, an assumption is made that the phase noise over the channel bandwidth can be approximated flat with a uniform phase noise value equal to the one at the center frequency.

For the LO frequency generation system, phase lock loop technique is normally employed to stabilize the output frequency of the oscillator. Fig. 3.2 shows a block diagram of a traditional analog phase lock loop. The output frequency of the voltage controlled oscillator (VCO) f_{VCO} is divided down to f_{FB} by a programmable divider. Then the phase and frequency different between the f_{FB} and the input reference frequency f_{REF} is extracted by a phase frequency detector (PFD) and the up/dn controlled signals are generated for the charge pump (CP). The output current of the charge pump is injected to a low pass filter and generates a control voltage V_{ctrl} to tune the VCO output frequency. Due to the feedback control, we the loop is settled, the phase and frequency different at the PFD input is zero, and we have f_{VCO} to be:

$$f_{VCO} = N * f_{REF} \quad (3.2)$$

where N is the division ratio of the programmable divider. For the Fractional-N frequency synthesis, the fractional part of the frequency control word (FCW) will be truncated to the integer part by a ΣΔ modulator. Due to the ΣΔ modulation, the truncation error will be shaped to the out-of-band and suppressed by the PLL loop filter.

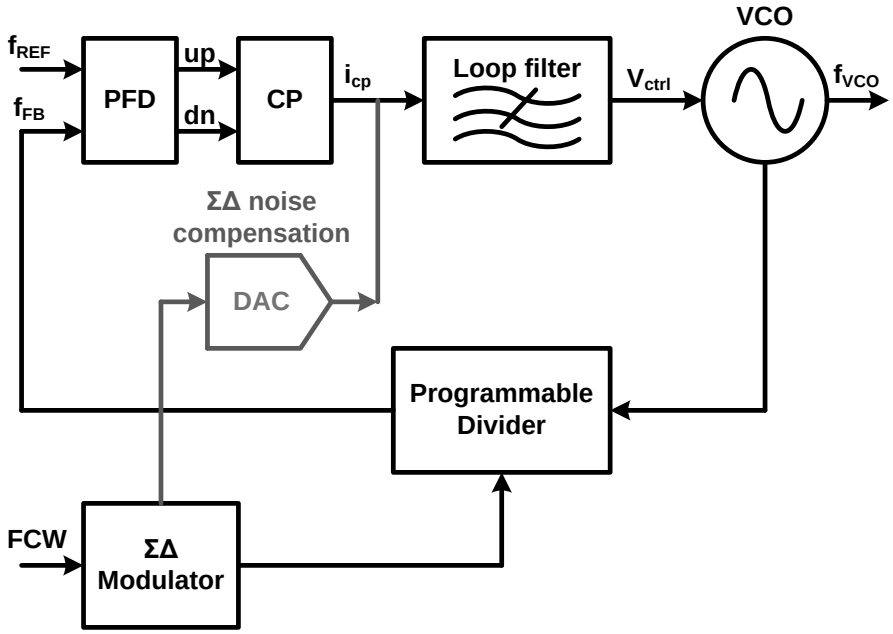


Fig. 3. 2 Block diagram of an analog PLL

In some applications, like frequency hopping communication, the settling time of the PLL is very critical and a large loop bandwidth is required. Also, large loop bandwidth can help to suppress the phase noise which is contributed by the VCO. However, when the loop bandwidth increases, the suppression for the ΣΔ noise may not enough and degrades the total phase noise performance of the PLL.

A noise compensation technique is used in [3.1], [3.2] for the wide-band fractional PLL. As shown in Fig. 3.2, the FCW truncation error will be calculated in digital domain and then converted to analog by a DAC. Then the FCW truncation error can be cancel out at the output of the charge pump.

To completely compensate the ΣΔ truncation error, the output magnitude of the CP and DAC should be match accurately. However, due to the process variation, the effectiveness of compensation degrades and normally a calibration for the gain mismatch is required.

3.2 ADPLL Motivation

As the CMOS technology scales down, all digital phase lock loop (ADPLL) attracts more and more research efforts [3.3]-[3.7]. Fig. 3.3 shows block diagram of an ADPLL. Compared to its analog counterpart, the PFD and CP in the analog PLL are replaced by a time-to-digital converter (TDC), so the leakage and process mismatch problems in the CP can be eliminated. In addition, the loop filter which consumes a large chip area in the analog PLL can be implemented in digital circuit. With the fast switching devices and high logic gate density in the advance process, the digital loop filter benefits not only cost reduction but also high programmability for multi-standard operation. Also, the ΣΔ noise compensation is much simpler because it is in digital domain.

Due to the reduction of the supply voltage, the varactor in scaled-down process technology becomes very non-linear and degrades the linear tuning range of the VCO. While in the ADPLL, the frequency control signals are in digital domain, so the digitally-controlled oscillator (DCO) can be employed to eliminate the non-linear varactor. Moreover, the DCO has much stronger noise immunity for the surrounding digital circuit which makes it more suitable for the high-level system integration.

Due to the quantization, the ADPLL has not only the intrinsic noise from the devices but also the quantization noise of the TDC and DCO. To design an ADPLL has a compatible or even better noise performance than the analog PLL, the quantization noise should be much lower than the device intrinsic noise, which make the design to be more challenging. In the following section, we will analysis how the quantization noise affect the PLL phase noise. Also, the design consideration and circuit implementation of each building block in the ADPLL will be discussed to optimize the performance and power consumption.

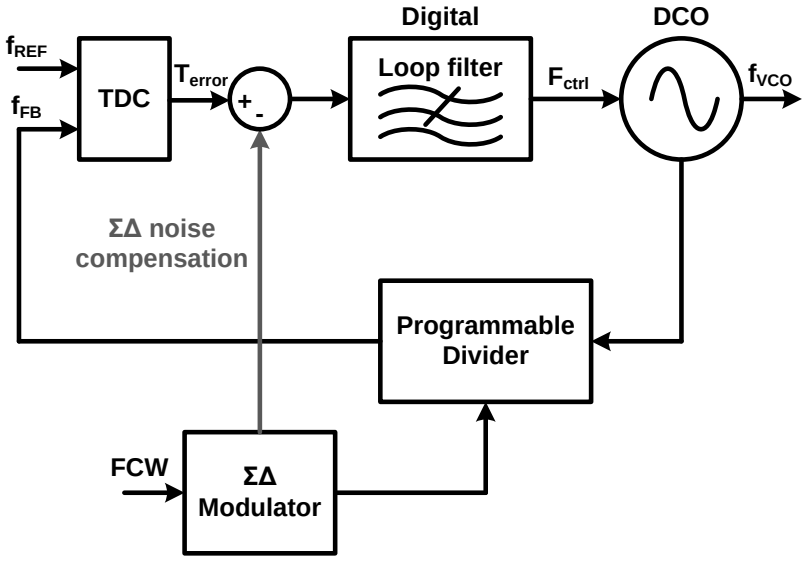


Fig. 3. 3 Block diagram of the ADPLL

3.3 Digitally-Controlled Quadrature Oscillator

Digitally-controlled oscillator (DCO) is one of the key building blocks in ADPLL. Due to the digital frequency tuning control, not only is its frequency resolution limited but also its phase noise is significantly degraded due to the quantization noise. Normally, in an LC oscillator, the LSB's capacitors are switched by a high-speed ΣΔ-modulated dither to reduce the effective DCO quantization step [3.8]. Depending on the dithering frequency, the out-of-band phase noise would increase due to the high-pass transfer function of the ΣΔ-modulator. In FDD system, like WCDMA, TX noise at the RX band has a very stringent requirement. Moreover, the co-existence of different wireless connectivity makes the out-of-band phase noise requirement more challenging.

This work presents a QDCO with 6.6dB out-of-band noise suppression without using a SAW filter. The QDCO operates in Class-C mode with current shaping for better DC-to-RF conversion efficiency. The embedded phase shifters between the I-Q coupling paths achieve better phase noise and I-Q phase accuracy without burning extra power.

3.3.1 Class-C Mode QVCO with Phase Shifter

A quadrature LC oscillator consists of two strongly coupled oscillators that are locked to the same frequency. Adding phase shifters in series with the I-Q coupling paths can improve the QVCO phase noise and make the I-Q phase accuracy less sensitive to the devices' mismatches [3.9].

Fig. 3.4 shows the block diagram of a quadrature LC oscillator and its current phasor diagrams. For the two coupled oscillators OSC_1 and OSC_2, the negative G_m cells generate currents i_1 and i_2 from the tank voltage v_1 and v_2 while the coupled G_{mc} cells generate currents i_{C1} and i_{C2}. In Fig. 3.4(b), without the phase shifter, a phase difference α is generated between the tank current i_{t1} and tank voltage v_1, which shifts the oscillation frequency ω_{OSC} away from the tank resonant frequency ω_0 and lowers the tank impedance. In Fig. 3.4(c), with the $90°$ phase shifter, the oscillation frequency is the same as the LC tank resonant frequency. As a result, the tank impedance is maximized, and the amplitude mismatches between the I-Q tanks do not affect the quadrature accuracy. Fig 3.5 shows the existing solution for the QVCO with phase shifter: In Fig. 3.5(a), they employed the common gate amplifier as the phase shifter [3.10], but the phase shifter will consume extra power and contribute more noise. In Fig. 3.5(b), they directly put the RC-CR filter in the tank to generate a phase shifter [3.9]. It is clear that this phase shifter will degrade the tank-Q and make the performance improvement of not effective. In Fig. 3.5(c), a buffer is used to drive the RC phase shifter [3.11], so the phase shifter does not load down the tank Q. However, the buffer will generate noise and consume extra power.

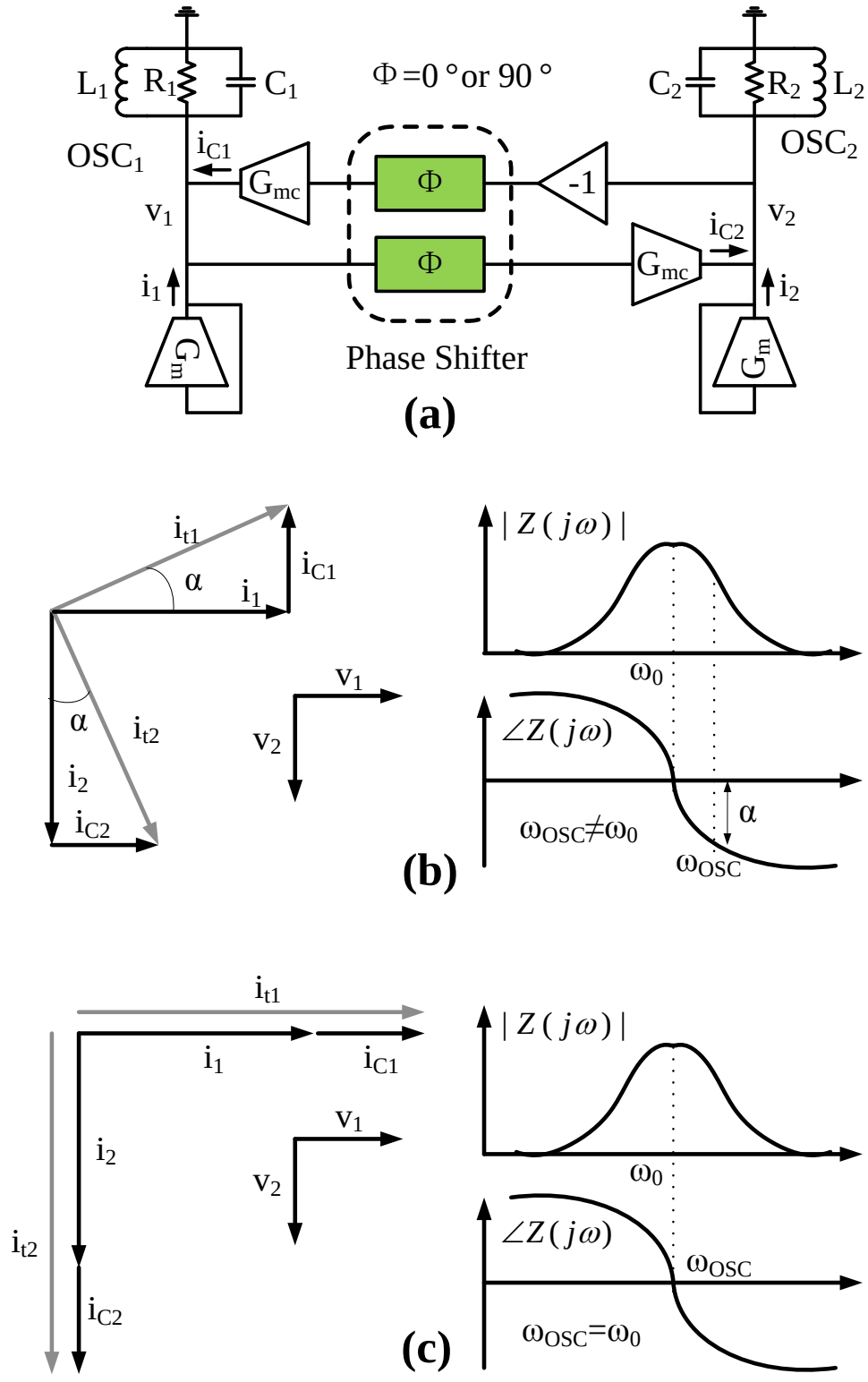


Fig. 3. 4 (a) Block diagrams of a quadrature LC oscillator; current phasor, amplitude and phase of tank impedance (b) without phase shifter; and (c) with 90 ºphase shifter.

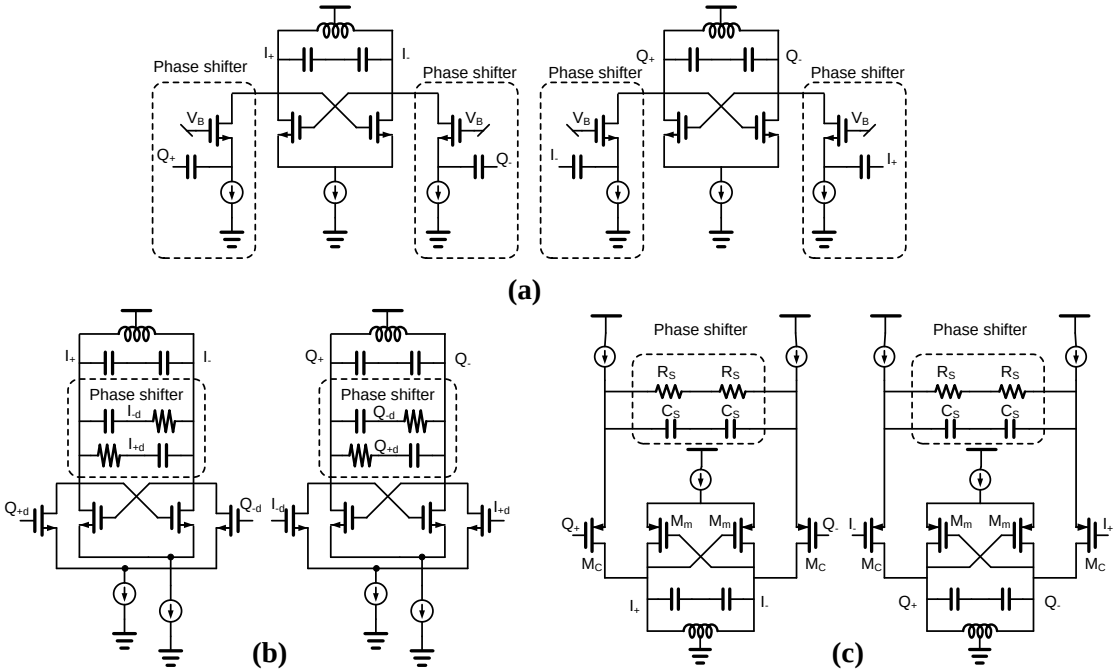


Fig. 3. 5 existing QVCO with phase shifter (a) Common gate amplifier as the phase shifter, (b) phase shifter in the tank, and (c) phase shifter with buffer and RC filter

Fig. 3.6 shows the schematic of the proposed transformer–coupled QVCO with embedded phase shifters to minimize power and noise contribution. The propose QVCO is based on a series-coupled QVCO [3.12], but the series-coupled devices are also used as the phase shifter. The transformer center tap V_g is biased to be lower than V_{DD} so that all the transistors are operated in Class-C and are only on for around half of the period. The primary coil of the transformer enlarges the voltage swing at the gate to enhance the switching effectiveness [3.13]. At the same time, the secondary coil reduces the voltage swing at the drain to maximize V_{ds} to prevent the transistors from operating in the linear region to improve phase noise. Capacitors C_{s1} are added not only for the current shaping in Class-C operation [3.14] but also as part of the phase shifter.

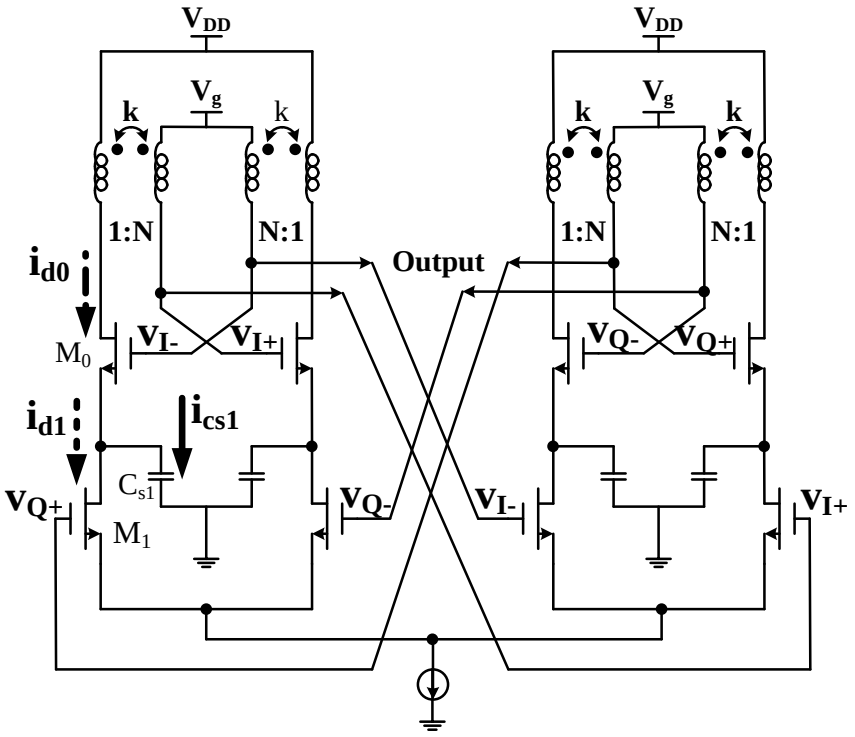


Fig. 3. 6 Proposed Class-C QVCO with phase shifters

Fig. 3.7 shows the current and voltage waveforms of M_0, M_1 and C_{s1} in the QVCO. The operation at the 4 critical moments can be explained as follows. At 0°, v_{I-} and v_{Q+} are low, and both M_0 and M_1 are off. At 90°, v_{Q+} increases, M_1 starts to conduct, and M_0 is still off. C_{s1} is discharged, and no current is injected to the tank. At 180°, M_0 starts to draw current from the tank. M_1 is still on, but its drain current is reduced since v_{ds} decreases, and C_{s1} starts to be charged. At 270°, v_{Q+} falls, M_1 is turned off, and all the current from the tank flows through M_0 to continue to charge C_{s1}. In the steady state, the currents charging and discharging C_{s1} become equal. The Q-phase coupled current is firstly stored in C_{s1} by M_1 and then synchronously injected to the I-phase tank by M_0, which effectively generates a 90° phase shift. Since this phase shifter reuses the active devices and the current of the quadrature series-coupled path, the performance is improved without extra noise and power.

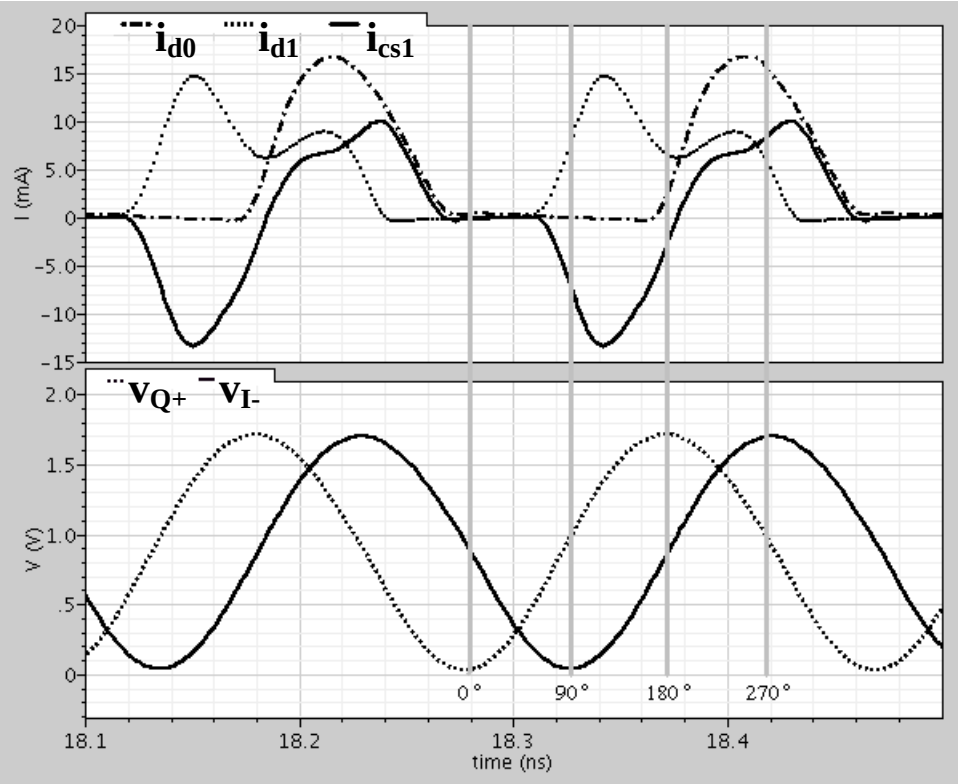


Fig. 3. 7 Transient current and voltage waveforms of M0 and M1

3.3.2 QDCO with ΣΔ Shaped Noise Suppression

Fig. 3.8 shows the block diagram of the QDCO which consists of the QVCO in Fig. 3.7 and digitally-controlled switched-capacitor arrays (SCAs) for frequency tuning. An 8-bit switched-MIM-capacitor array is employed in the primary coil for coarse tuning. Minimum-sized MOS capacitors are placed in the secondary coil instead of the primary coil to achieve finer tuning by exploiting the fact that the coupling coefficient is less than 1. In addition, since the voltage swing at the secondary coil is much smaller than that at the primary coil, the non-linearity effect of the tuning capacitors is significantly reduced. These MOS capacitors are controlled by a 10-bit integer signal and a 14-bit fractional signal. For the 10-bit integer signal, the 4 MSB's directly control

the binary-weighted MOS capacitors, and the 6 LSB's use thermometer code to control the 64 unit-weighted MOS capacitors. As a result, 1-LSB integer signal corresponds to an 80-KHz tuning step at 5GHz oscillation frequency. To reduce the quantization step, a 3rd-order ΣΔ modulator with 8-levels output is used for the 14-bit fractional control. This ΣΔ modulator operates at 1/16 of the oscillator frequency and achieves 5-Hz frequency resolution.

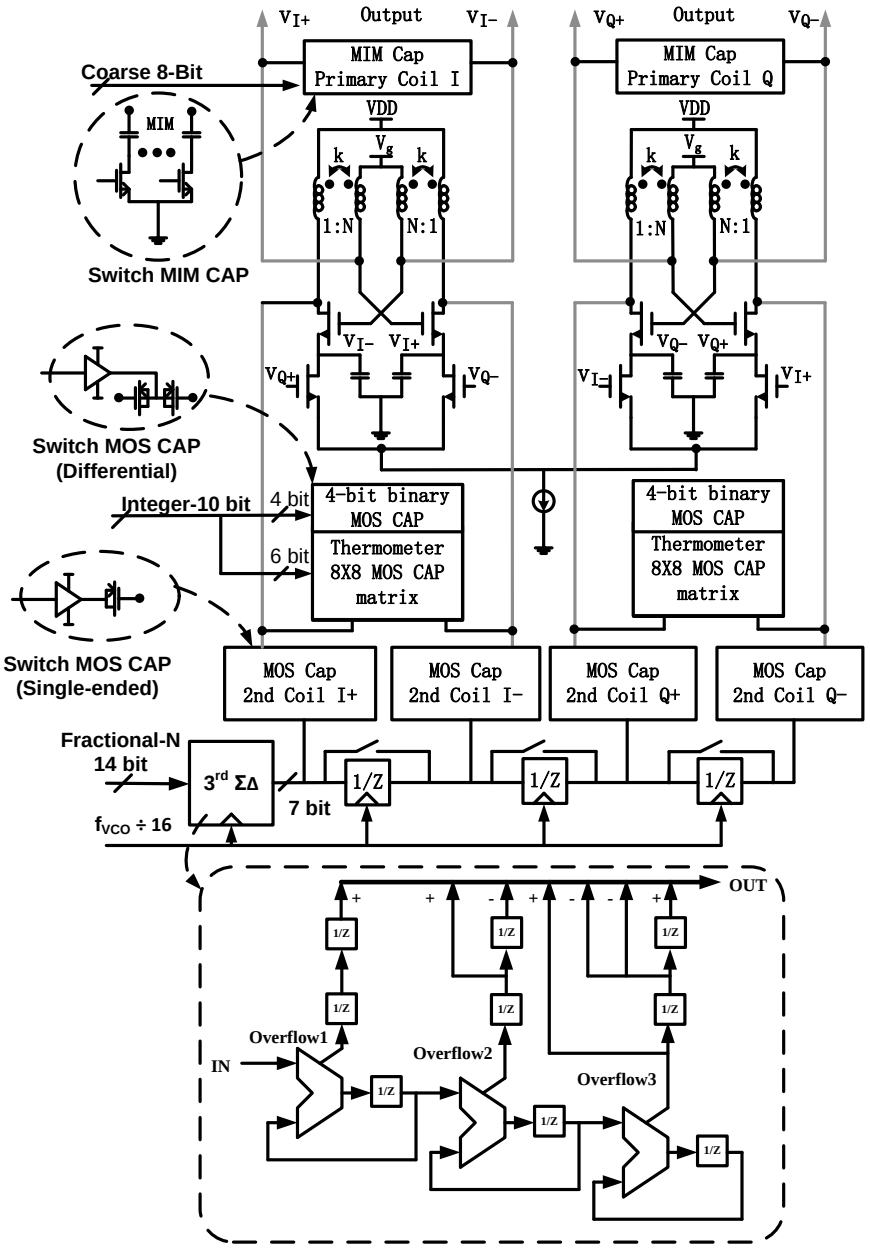


Fig. 3. 8 Schematic of the proposed QDCO with ΣΔ shaped quantization noise filter

To gain insight into the quantization effects of the finite DCO frequency resolution Δf_{res} on the RF output phase noise [3.8], consider its transfer function shown in Fig. 3.9(a). The infinite-precision tuning signal d is quantized to a finite-precision tuning word such that it matches the DCO frequency resolution Δf_{res}. The actual frequency deviation Δf_0 will be within $\Delta f_{res}/2$ away from ideal. The frequency deviation is then converted to phase through the $2\pi/s$ integration. The 2π multiplication denotes the conversion of a linear frequency to an angular frequency.

Since the tuning word normally spans multiple quantization levels, the DCO frequency quantization error is modeled in Fig. 3.9(b) as an additive uniformly distributed random variable $\Delta f_{n,0}$ with white noise spectral characteristics. Its variance is

$$\sigma_{\Delta f_0}^2 = \frac{(\Delta f_{res})^2}{12} \tag{3.3}$$

The total phase noise power is uniformly spread from DC to the Nyquist frequency, i.e., half of the reference frequency f_R. The single-sided spectral density of $\Delta f_{n,0}$ is, therefore, flat at

$$\frac{1}{2} S_{\Delta f} = \frac{\sigma_{\Delta f_0}^2}{f_R} \tag{3.4}$$

The transfer function from the frequency deviation quantization error $\Delta f_{n,0}$ to the phase ϕ_0 of the RF output is $2\pi/s$, so the single-sided power spectral density at the output is

$$\psi\{\Delta\omega\} = \frac{(\Delta f_{res})^2}{12 f_R} * \left(\frac{2\pi}{\Delta\omega}\right)^2 \tag{3.5}$$

It could be rewritten as:

$$\psi\{\Delta f\} = \frac{1}{12} * \left(\frac{\Delta f_{res}}{\Delta f}\right)^2 * \frac{1}{f_R} \tag{3.6}$$

Actually, the DCO input samples are not impulses to justify the white noise assumption above but are held constant between the updates. Consequently, (3.6) needs to be multiplied by the sinc function corresponding to the Fourier transform of the zero-order hold operation

$$\psi\{\Delta f\} = \frac{1}{12} * \left(\frac{\Delta f_{res}}{\Delta f} \right)^2 * \frac{1}{f_R} * \left(Sinc \frac{\Delta f}{f_R} \right)^2 \tag{3.7}$$

Equation (3.7) gives rise to the same 20 dB/dec attenuation characteristics as the up-converted thermal noise region of the oscillator phase, except for the protective notches at the DCO input sampling rate and its multiples. Without the ΣΔ modulation, even with the finest varactor resolution of the tracking bank, the resulting phase noise will normally be too high for wireless applications.

The spectrum of the nth ΣΔ-shaped frequency deviation

$$S_{\Delta f}\{\Delta f\} = \frac{(\Delta f_{res})^2}{12} * \frac{1}{f_{\mathrm{mod}}} * \left(2\sin \frac{\Delta f}{f_{\mathrm{mod}}} \right)^{2n} \tag{3.8}$$

Consequently, we obtain the phase noise spectrum as:

$$\psi\{\Delta f\} = \frac{1}{12} * \left(\frac{\Delta f_{res}}{\Delta f} \right)^2 * \frac{1}{f_{\mathrm{mod}}} * \left(2\sin \frac{\pi \Delta f}{f_{\mathrm{mod}}} \right)^{2n} \tag{3.9}$$

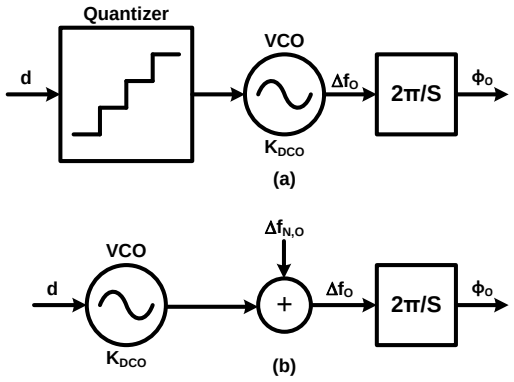


Fig. 3. 9 DCO quantization noise model (a) Behavior model and (b) mathematic model

Due to the noise-shaping effect of the modulator, the out-of-band noise floor is dominated by the modulator's shaped noise. For a fixed frequency tuning step, the noise level depends on the order and the dither frequency of the modulator. Reducing the order can improve the out-of-band phase noise, but in-band noise would become worse and generate more tones and spurs. Increasing the dither frequency can help to improve the quantization noise, but it would require more power and contribute more switching noise.

For our proposed QDCO, a clock delay is inserted in the 4-phase fractional MOS capacitors to implement an embedded 3rd-order sinc filter. With this filter, the phase noise spectrum as:

$$\psi\{\Delta f\} = \frac{1}{12} * \left(\frac{\Delta f_{res}}{\Delta f}\right)^2 * \frac{1}{f_{\mathrm{mod}}} * \left(2\sin\frac{\pi\Delta f}{f_{\mathrm{mod}}}\right)^{2n} * \frac{1}{4}(1 + Z^{-1} + Z^{-2} + Z^{-3}) \qquad (3.10)$$

where $Z=e^{j2\pi fmod}$; The embedded filter generates 3 zeros at ¼, ½ and ¾ of the ΣΔ modulation frequency to suppress the quantization noise. For comparison, the delay cells for the 4-phase fractional MOS capacitors are either selected or bypassed. Then the embedded filter can be reconfigurable to 0^{th}, 1^{st} and 3^{rd} orders.

For example, for a frequency quantization step of 80 KHz, DCO operation frequency is 5GHz and the ΣΔ operation frequency is 350MHz. As shown in Fig. 3.10, without any filter, the peak of ΣΔ quantization noise is -146.8dBc/Hz. With 1st sinc filter, the noise peak goes down to -151.8dBc/Hz and -158.1dBc/Hz for 3rd filter. The 1st-order and the 3rd-order embedded filters help suppress the out-of-band quantization noise by 5dB and 11.3dB, respectively. As we seen from Fig. 3.10, with proposed 3rd filter, the ΣΔ quantization noise can be at least 6dB lower than the intrinsic noise of the VCO for any frequency offset.

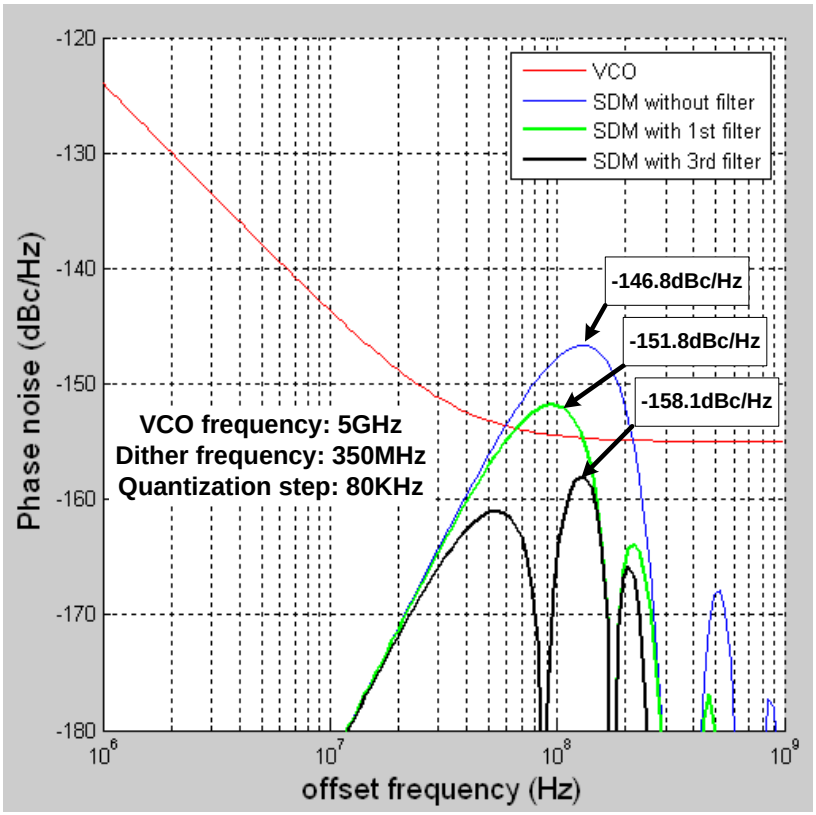


Fig. 3. 10 Phase noise simulation of the proposed QDCO

3.3.3 QDCO Measurements and Summary

A QDCO prototype is fabricated in a 65nm 1P6M LP CMOS process. It draws 15mA from 1.2V and achieves a tuning range of 45% from 4.08 to 6.52GHz. From Fig. 3.11, phase noise of -145.3dBc/Hz at 10MHz offset is measured at 4.9 GHz with ΣΔ dither power off, corresponding to FoM of 186.6 dB and FoMT of 199.8 dB. As shown in Fig. 3.12, the phase noise is measured across the turning range and has a variation less than 3dB. The worst case sideband rejection measured with an on-chip Single-Side-Band (SSB) up-mixer for 5 samples is 39.7dB, corresponding to an I-Q phase error of 1.2 °.

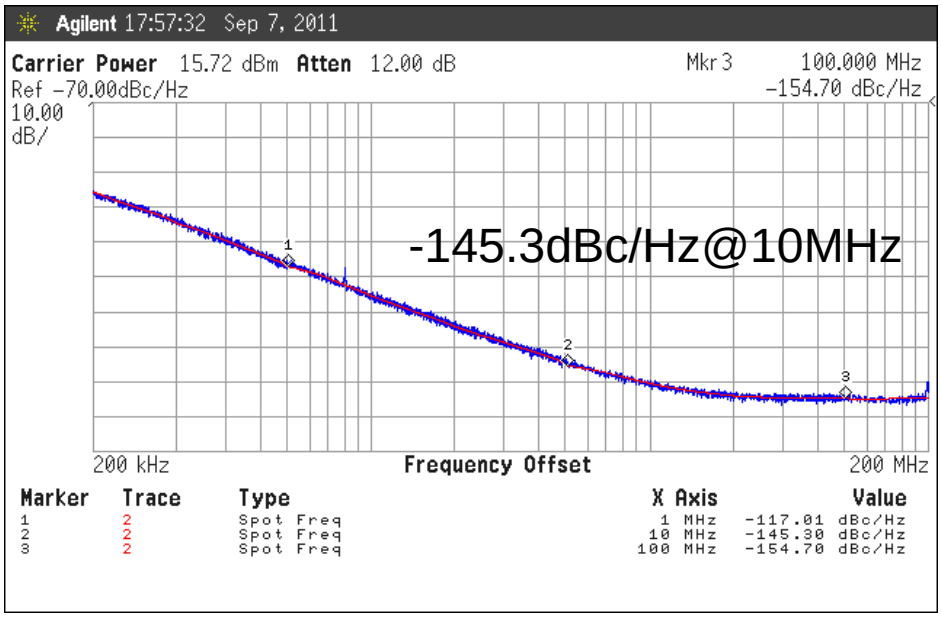


Fig. 3. 11 QDCO phase noise measure at 4.9GHz

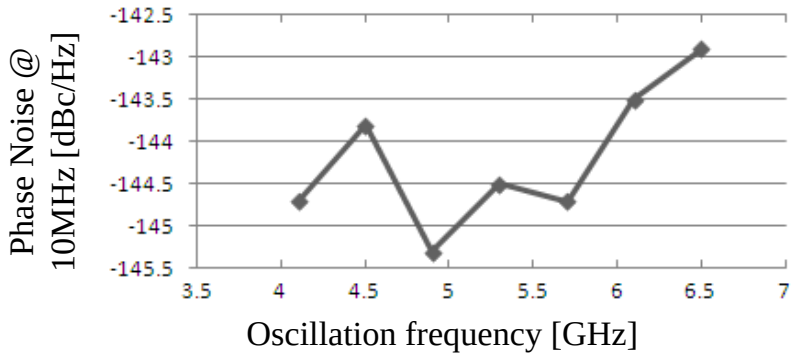


Fig. 3. 12 Measured phase noise at 10MHz offset frequency across the entire frequency tuning range

To verify the effectiveness of the embedded ΣΔ-shaped noise filter, the delay cells for the 4-phase fractional MOS capacitors are either selected or bypassed. Fig. 3.13 compares the out-of-band phase noise measurements in 3 different cases: a) ΣΔ modulator turns on without filter by bypassing all the delay cells, d) ΣΔ modulator turns on with 1st-order filter by bypassing the first and the last delay cells, and c) ΣΔ

modulator turns on with 3rd-order filter by turning on all the delay cells. The QDCO operates at 5.6GHz and has an integer step 87-KHz. When the modulator turns on, the noise floor increases by 11.8dB without filter. However, the 1st-order and the 3rd-order embedded filters help suppress the out-of-band quantization noise by 4.5dB and 6.6dB, respectively. As we seen in Fig.3.13, there are some spurs at the frequency offset of $\frac{1}{4} * f_{dither}$, $\frac{1}{2} * f_{dither}$, f_{dither}, $2*f_{dither}$ … These spurs are generated from a divider chain at the QDCO output. The divider chain is designed for the f_{dither} generation and it shares the same supply voltage with the QDCO output buffer. If they have a separate supply, then the spurs would become much lower.

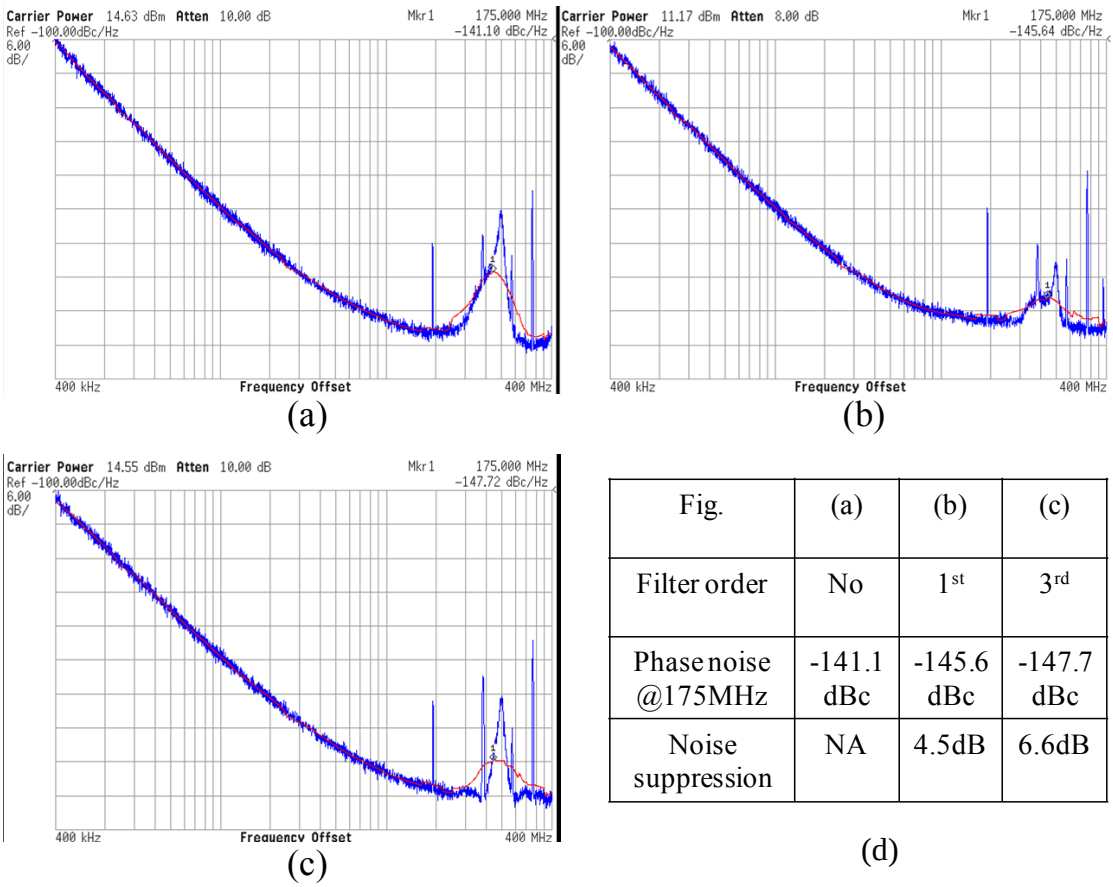


Fig.	(a)	(b)	(c)
Filter order	No	1st	3rd
Phase noise @175MHz	-141.1 dBc	-145.6 dBc	-147.7 dBc
Noise suppression	NA	4.5dB	6.6dB

(d)

Fig. 3. 13 QDCO out-band phase noise measurements: (a) ΣΔ modulator turns on without filter, (b) ΣΔ modulator turns on with 1st-order filter, and (c) ΣΔ modulator turns on with 3rd-order filter (d) Summary of the performance

The measured performance of the QDCO is summarized in Table 3.1. Fig. 3.14 shows the chip photo, which occupies a core area of 1.0 x 0.4mm2.

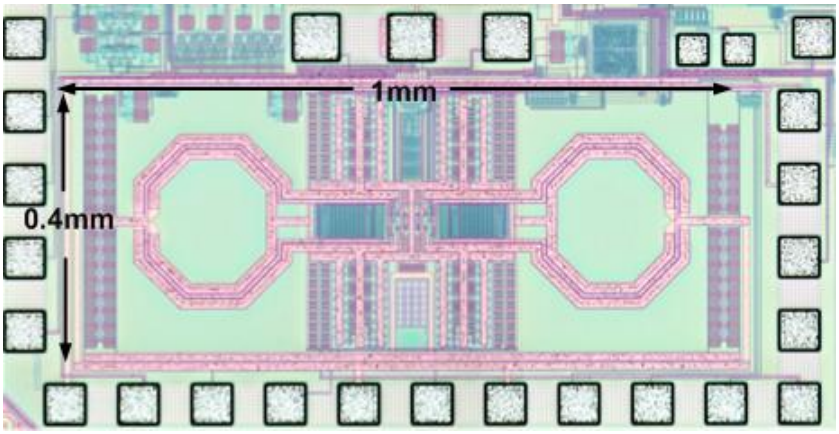


Fig. 3. 14 QDCO Die photograph

Table 3. 1 Performance Summary and Comparison

Ref.	JSSC 07 Allan [3.13]	JSSC 08 Mazzanti [3.14]	ISSCC 10 Fanori [3.15]	This work
Type	QVCO	Class-C VCO	DCO	Class-C QDCO
Technology	180nm CMOS	130nm CMOS	65nm CMOS	65nm CMOS
Supply voltage	1	1	1.8	1.2
Frequency	14.8~17.6 GHz	4.9~5.65 GHz 4.5~5.5 GHz	2.62~3.3 GHz	4.1~6.5 GHz
Phase noise (Normalized to 10MHz offset)	-130 dBc/Hz	-140 dBc/Hz	-147.5 dBc/Hz	-145 dBc/Hz
Frequency resolution	N/A	N/A	150Hz*	5Hz**
Tuning range	16.5%	14.2% 20%	26%	46%
Power consumption	5mW	1.4mW	28.8mW	18mW
Phase error	1.4 °	N/A	N/A	1.3 °
FoM	187.6 dBc/Hz	193.5/196 dBc/Hz	183 dBc/Hz	186.6 dBc/Hz
FoM_T	191.9 dBc/Hz	196.5/202 dBc/Hz	191.3 dBc/Hz	199.8 dBc/Hz

* without ΣΔ Modulation ** with ΣΔ Modulation

In Conclusion, we present a Class-C mode QDCO with embedded phase shifters and ΣΔ-shaped quantization noise filter. The embedded phase shifters use the same coupling devices and reuse the current of the quadrature series-coupled paths to improve the phase noise and IQ phase accuracy without extra power. Moreover, an embedded 3rd-ordered sinc filter is achieved by inserting one clock delay between the 4-phase fractional tuning capacitors to suppress the out-band noise by 6.6dB. A QDCO prototype was fabricated and measured to prove the proposed solution and achieves state-of-the-art performance.

3.4 Time-to-Digital Converter

Time-to-Digital converter is one of the key building blocks of the ADPLL because the in-band phase noise depends on the TDC resolution. Assuming that the period of the reference signal T_{REF} remains unchanged over time, the time resolution of the TDC Δt_{res} can be converted into a phase resolution of $\Delta\Phi$:

$$\Delta\Phi = \frac{2\pi\Delta t_{res}}{T_{REF}} \tag{3.11}$$

Fig. 3.15 shows a representative characteristic of the TDC, where the input phase difference is noted as Φ_{error}. The phase resolution of the TDC determines the applicability of a linear analysis for the ADPLL. If Φ_{error} is smaller than the resolution of the TDC, the behavior of the TDC is no different from a bang-bang phase detector. A linear analysis is not applicable in this case and thus the bandwidth in a strict sense is not defined. On the other hand, if the input phase error Φ_{error} is much larger than the resolution of the TDC, the input phase error is digitized in a linear manner. The TDC can be modeled as a gain of $1/\Delta\Phi$ plus quantization noise as in Fig. 3.16. Having a

linear phase detector allows us to use linear techniques for the analysis of ADPLLs. The noise contribution of a TDC is given in [3.16].

$$PN = 10\log\left(\frac{1}{T_{REF}} * (2\pi N)^2 * \frac{\Delta t_{res}^2}{12}\right) \tag{3.11}$$

where the phase noise has a unit of dBc/Hz and N is frequency division ratio between the DCO and reference in the ADPLL.

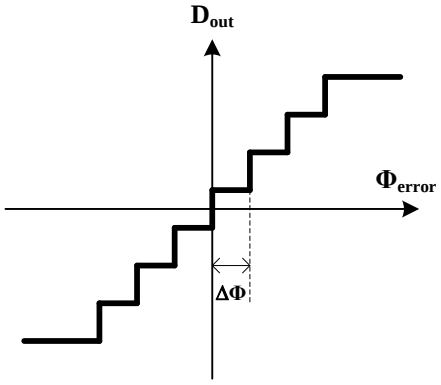


Fig. 3. 15 Transfer characteristic of the TDC

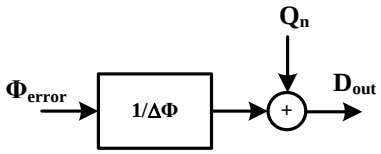


Fig. 3. 16 Linear model of the TDC

3.4.1 TDC with Vernier delay line

The resolution of the basis TDC structure is determined by the minimum gate delay of the process. In deep sub-micron CMOS, the minimum gate delay is in the range of few tens picoseconds. For example, there is a 20ps of the minimum gate delay with fan-out of 2 in 65nm CMOS. There are some techniques to reduce the TDC quantization steps to be lower than one minimum gate delay. Vernier delay line [3.17] is one of the

examples. As shown in Fig. 3.17, the delay line with the delay unit $\tau 1$ is for the start signal while the delay line with the delay unit $\tau 2$ is for the stop signal. By design $\tau 1$ to be different from $\tau 2$, then the TDC can ideally have a resolution of $|\tau 1 - \tau 2|$, which can be much smaller than the minimum gate delay. But due to the process variation, the time-delay mismatches which are not only in the delay cells but also in the DFFs limit the achievable resolution to be around few picoseconds.

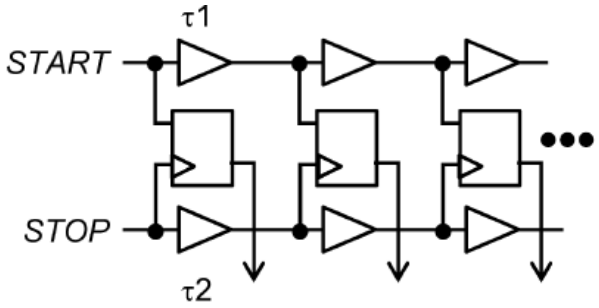


Fig. 3. 17 Vernier delay line based TDC

3.4.2 Two-step TDC

Similar to the Analog-to-Digital converter (ADC), the TDC can make use of the time amplifier (TA) to improve its resolution [3.18]. Fig. 3.18 shows the TDC architecture. To enlarge the measurement range, the operation of the TDC is split into 2 steps: In step 1, the TDC quantizes the time input with quantization step τ and selects the delayed start signal for the next stage. In step 2, the residual quantization error in step 1 are amplified by the gain G of the TA and then be quantized by the same quantization step τ. Then we can calculate the effective quantization step of the TDC is: τ/G. Unfortunately, G is not constant and varies as input change, which degrades the linearity of the TDC.

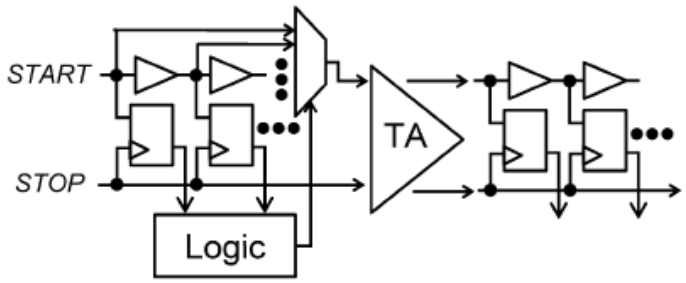


Fig. 3. 18 Two-step TDC with time amplifier

3.4.3 Statistical TDC

As we seen, the non-idealities of offset, mismatch, non-linearity … in the circuits limit the achievable TDC quantization step. On the contrary, the statistical TDC [3.19] makes use of the process mismatch and achieves much smaller quantization step. Fig. 3.19 shows the architecture of the statistical TDC. The 1023 time comparators are used to compare the same input. Due to the process variation, the comparators have different input offset voltages which have a Gaussian distribution. Depends on the slew rate, the input offset voltage translates to the input time offset. Assume a linear rise edge at the input, the time offset is also Gaussian distributed. By changing the slew rate of the rising edge, we can achieve different resolutions and measurement ranges.

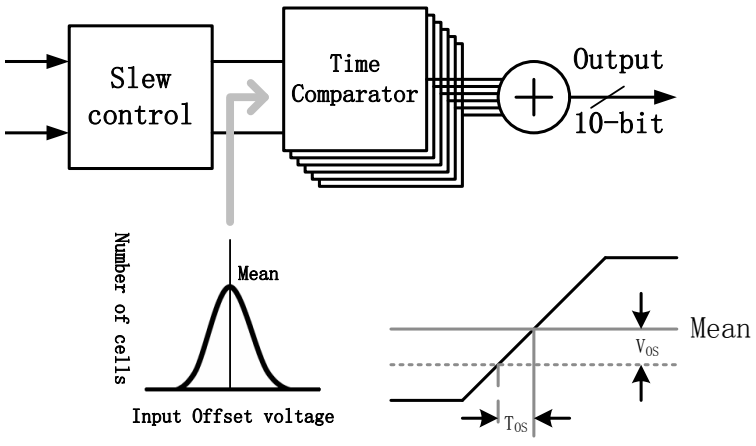


Fig. 3. 19 Statistical TDC with gain control

As shown in Fig. 3.20, the TDC input and output characteristic and be calculated by its offset distribution function. Due to the Gaussian distribution, the linear range of the TDC is approximately equal to the offset stand deviation which can be estimated by Monte-Carlo simulation.

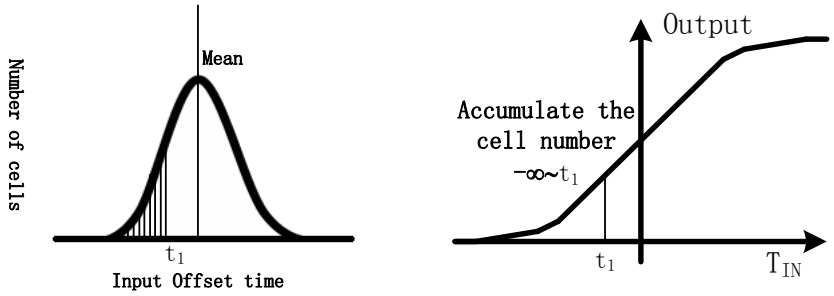


Fig. 3. 20 Time offset distribution and TDC input-output characteristic

Fig. 3.21 shows the schematic of the time comparator. When the inputs IN+ and IN- are low, the comparator is in reset state. If IN+ goes to high first, it will pull down the LTb and make Q to be high. After that, even when IN- goes to high, it cannot change the LTb. So, this time comparator can determine which input has the leading rising edge.

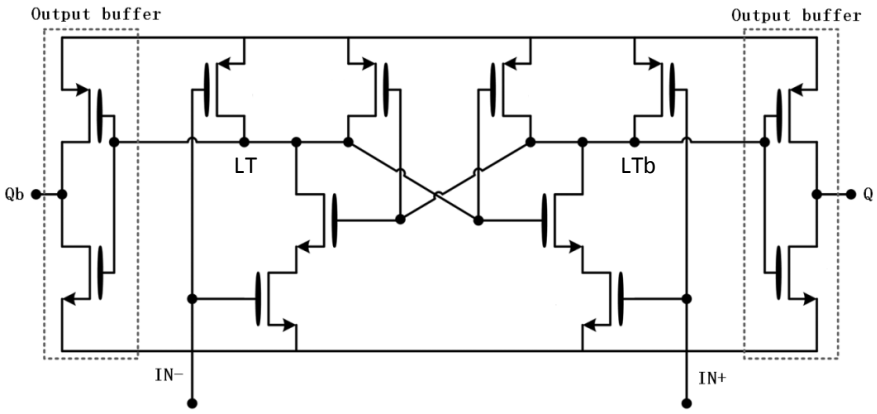


Fig. 3. 21 Time comparator for the TDC

A statistical TDC prototype is fabricated in a 65nm 1P6M LP CMOS process. The micro photograph is shown in Fig. 3.22 and Fig. 3.23 shows the measured input to

output characteristic with 3 different slew rates. By setting the TDC gain to be 4 (maximum value is 7), the linear input range is from -32pS to 32pS with 68.7fs/LSB resolution.

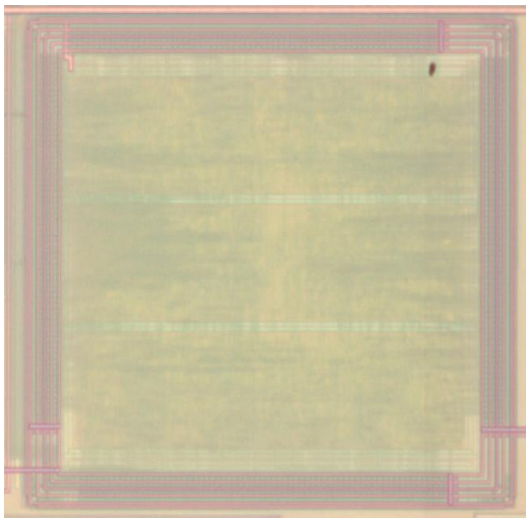


Fig. 3. 22 Micro photograph of the statistical TDC

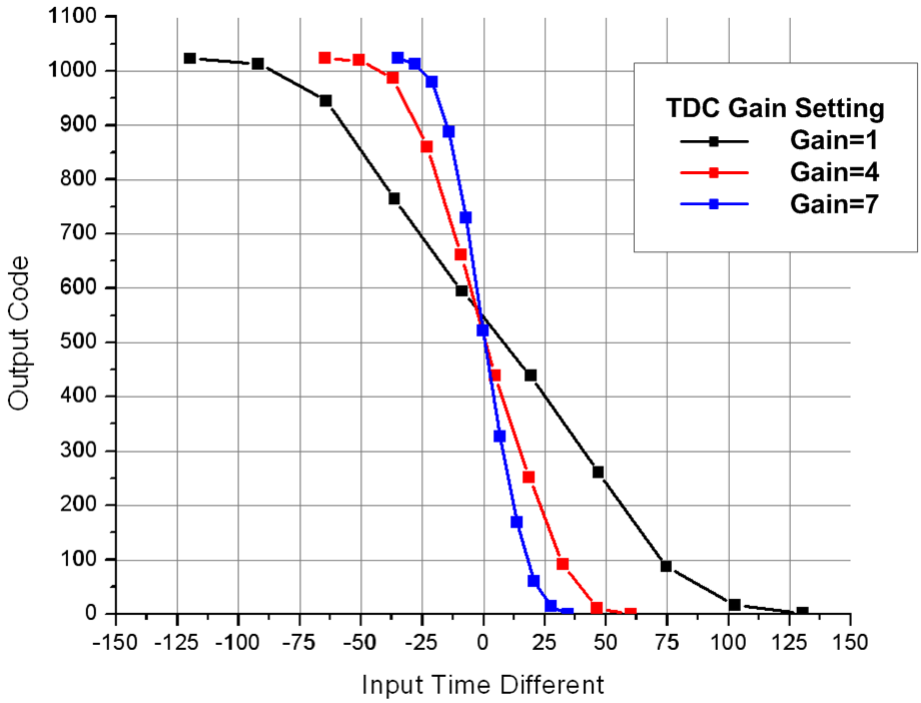


Fig. 3. 23 Measured TDC input-output characteristic with different slew rate

The Measured INL error of the TDC over an input range of -32ps to 32ps is shown in Fig. 3. 24, the maximum INL error is 2.1ps with a TDC gain of 4.

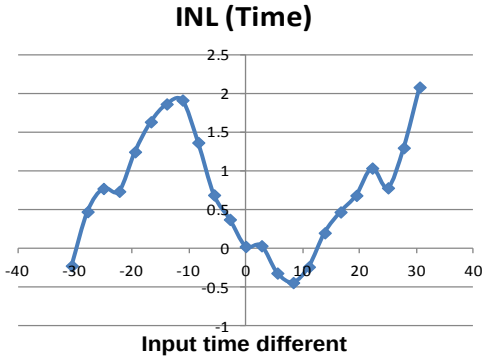


Fig. 3. 24 Measured INL error with TDC gain = 4

As Fig. 3. 25 shown, due to the noise of time comparators, there is a variation in the threshold voltage and it generates noise at the TDC output. Fig. 3. 26 shows the measured the TDC output with a fixed input time delay. There is a RMS noise of 1.5ps at the output when the TDC gain is 4.

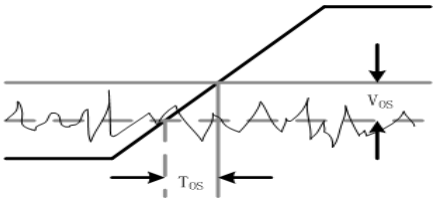


Fig. 3. 25 TDC noise due to the noise of the time comparator

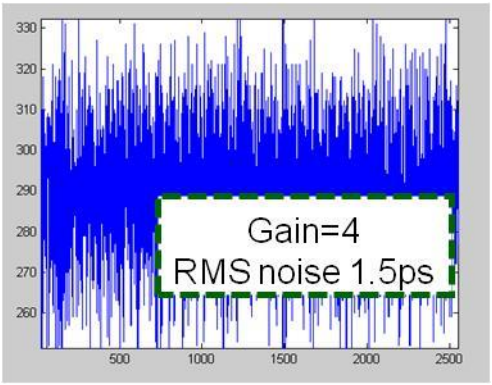


Fig. 3. 26 Measured TDC output with a fixed input

3.4 Phase-Interpolated Programmable Divider

For a classical fraction-N PLL, the input range of the TDC at the locked state is $K_{\Sigma\Delta}*T_{VCO}$. T_{VCO} is the VCO period and $K_{\Sigma\Delta}$ is the output levels of the ΣΔ modulator which are determined by the structure of the ΣΔ modulator. For example, there are 3 output levels for 2^{nd} orders error-feedback ΣΔ modulator. If the ΣΔ modulator contains more output levels, then its output patents are more random and have less spurs in its spectrum. However, it requires the TDC to have a wider input range and higher linearity. In section 3.3, we have seen that the high resolution TDCs normally have a limited input range. Increase the input range will increase the TDC power and degrade the resolution.

With the fixed $K_{\Sigma\Delta}$, the TDC input range can be reduced by using a programmable divider with a sub-integer N division ratio [3.7]. As shown in Fig. 3.27, a phase interpolation block is added to the output of the programmable divider to achieve sub-integer N division ratio. Its block diagram is shown in Fig. 3.28. First, the QDCO output frequency is divided by the programmable divider. Then the output of the divider is retimed to the phases 0°, 90°, 180°, 270° and 360° of the QDCO. After that, these 5 phases are interpolated to 32 phases by a 3-steps phase interpolator. The sub-integer division ratio is achieved by selecting one of the phases to the MUX output. Fig. 3.29 shows an example of divide by N+1/32 to explain its operation. In the first reference period, phase P_0 is selected to the output, while in the next reference period P_1 is selected so that their interval is $(N+1/32)*T_{VCO}$. By keep doing this, and then after 32 reference periods, the last phase P_{31} is selected. To maintain the same time interval, the integer division ratio is increased by 1 and P_0 is selected again to the output. With this phase interpolated programmable divider, a $1/32*T_{DCO}$ output frequency resolution can

be achieved and the input range of the TDC is reduced to: $1/32*K_{\Sigma\Delta}*T_{VCO}$. For our application, given a 2nd ΣΔ modulator with 3 output levels and a 320ps of the T_{VCO}, the required the TDC input range is only 30ps. Then a fine-resolution statistical TDC can cover this input range.

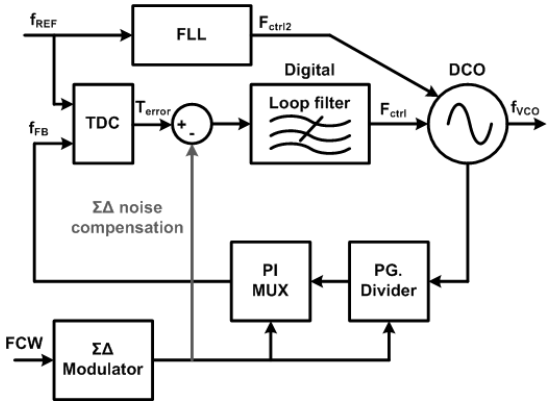


Fig. 3. 27 Technique to reduce the input range of the TDC

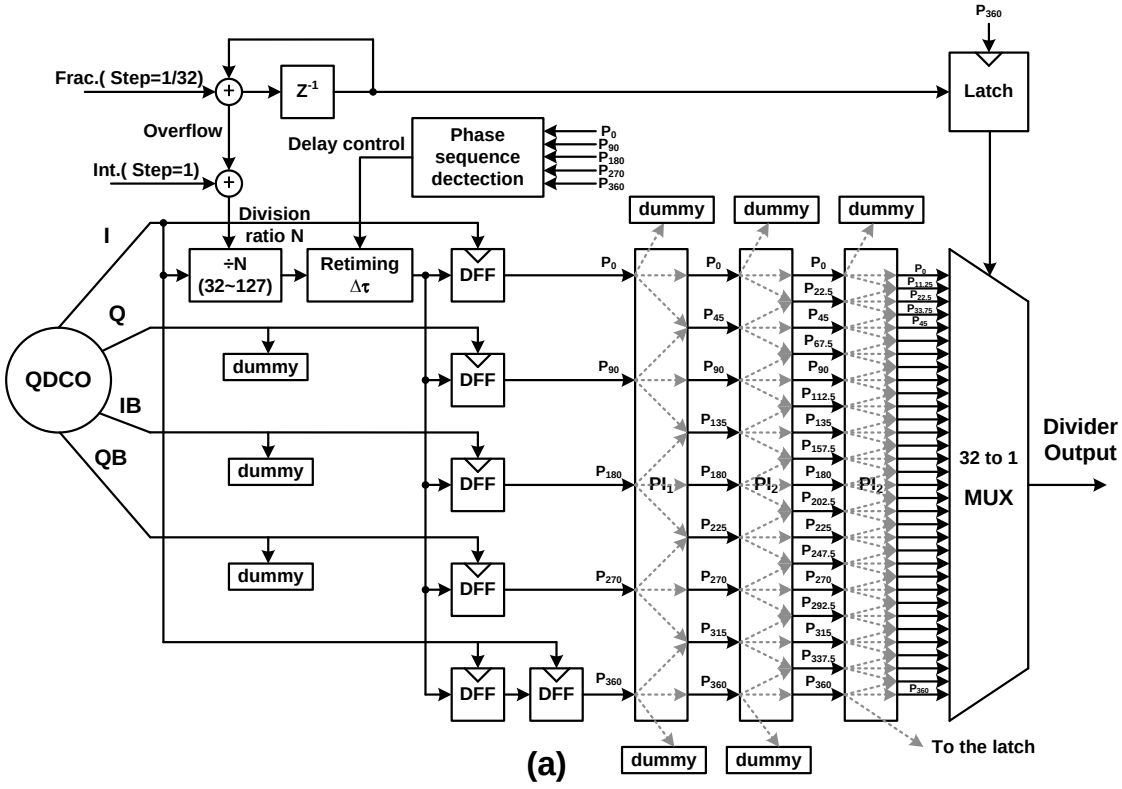


Fig. 3. 28 System block diagram of the Phase-interpolated programmable divider

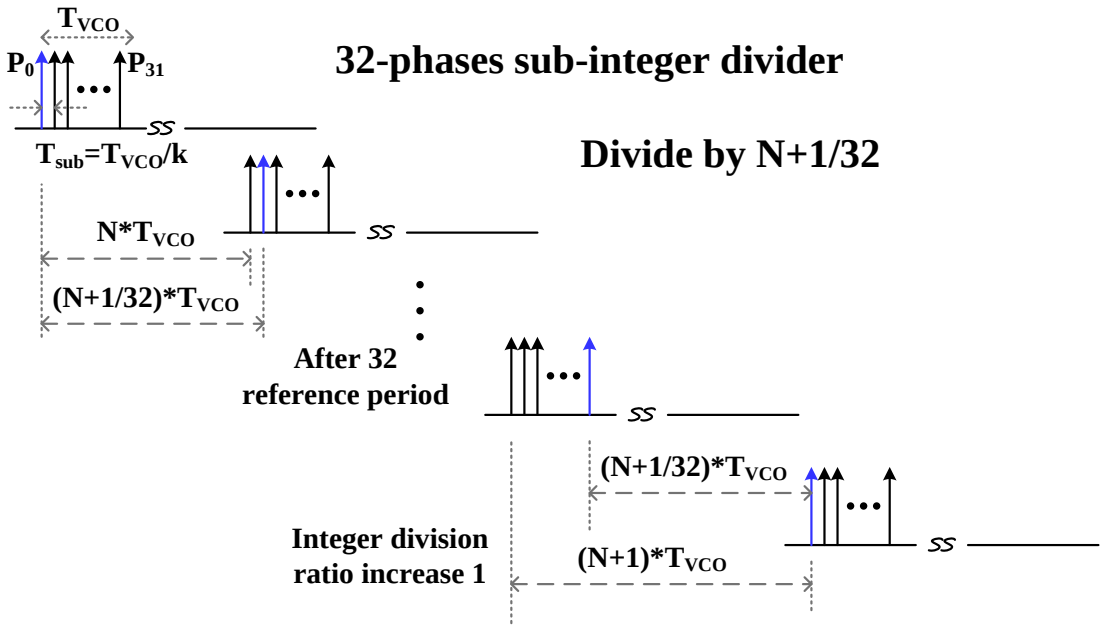


Fig. 3. 29 Operation principle of the Phase-interpolated programmable divider

As shown in Fig. 3.30(a), there is a phase sequence problem in the 5 retiming signals: P_0, P_{90}, P_{180}, P_{270} and P_{360} when P_0 is not right after the rising edge of DIV_1. To correct this error, a sequence detection circuit is designed and shown in Fig. 3.30(b). The leading phase is sampled by its following phase, if the DFF output is "1", then the phase sequence is correct, otherwise the AND gate will output "0". Then the selection logic circuit will tunes the output delay of the programmable divider until the AND gate output is "1".

The circuit implementation of the phase interpolator is shown in Fig. 3.31(a). Inv1 and Inv4 are standard inverters with size of (W/L), PI has two inverters Inv2 and Inv3 whose outputs are connected directly and whose gate widths are k*(W/L). By optimizing the coefficient k of these invertors, the intervals of the output phases can be equal. Fig. 3.31(b) shows the transient waveform of the phase interpolator and Fig.3.31(c) is the simulation of its output phase error over different input phase.

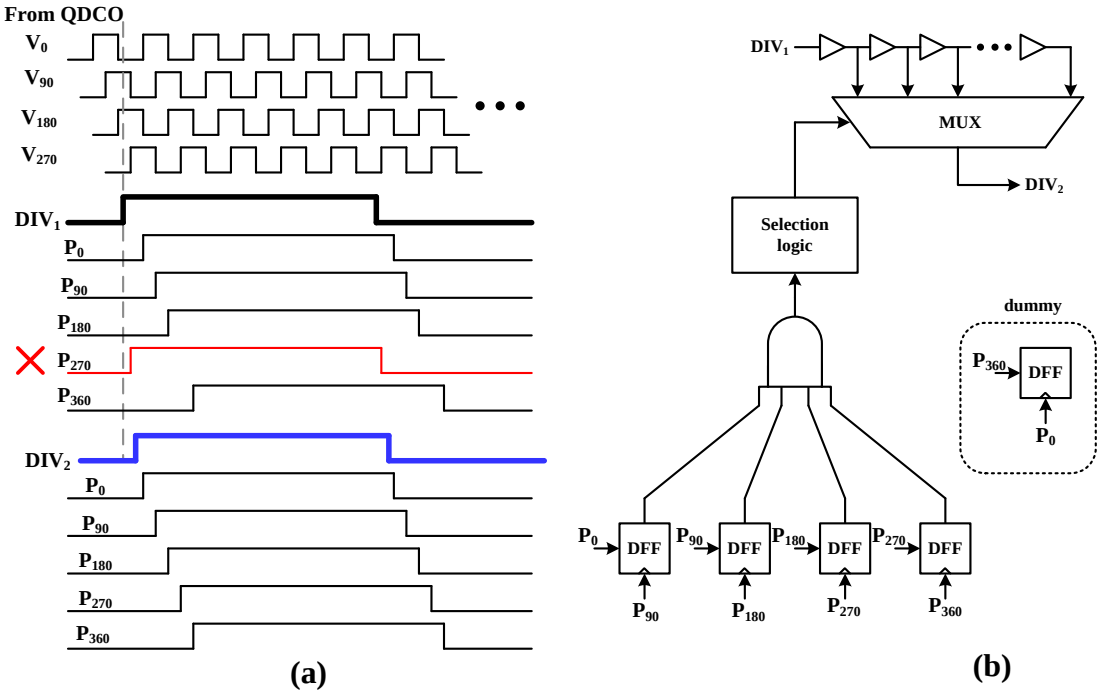


Fig. 3. 30 Phase sequence correction (a) timing diagram (b) circuit implementation

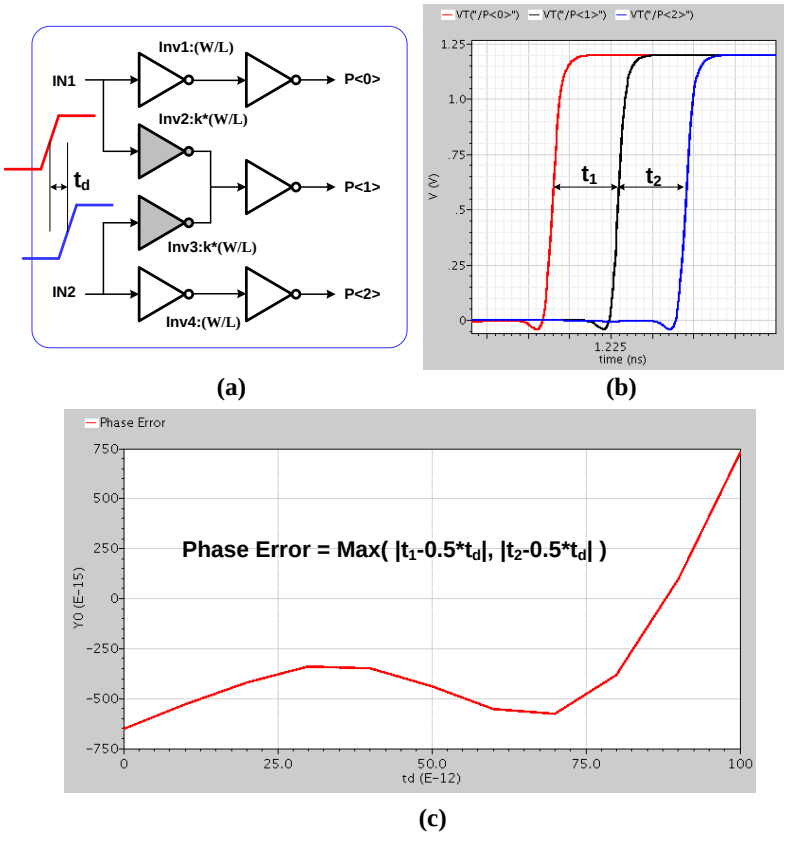


Fig. 3. 31 Phase interpolator (a) simplify implementation, (b) Transient simulation and (c) Simulation of the Phase Error

The simulation result of the 32-phases interpolator is shown in Fig. 3.32(a) and its phase error under different PVT condition are shown in Fig. 3.32(b). From Fig. 3.32(b), the phase error of the ΣΔ phase interpolated divider is less than 1.6ps in all cases.

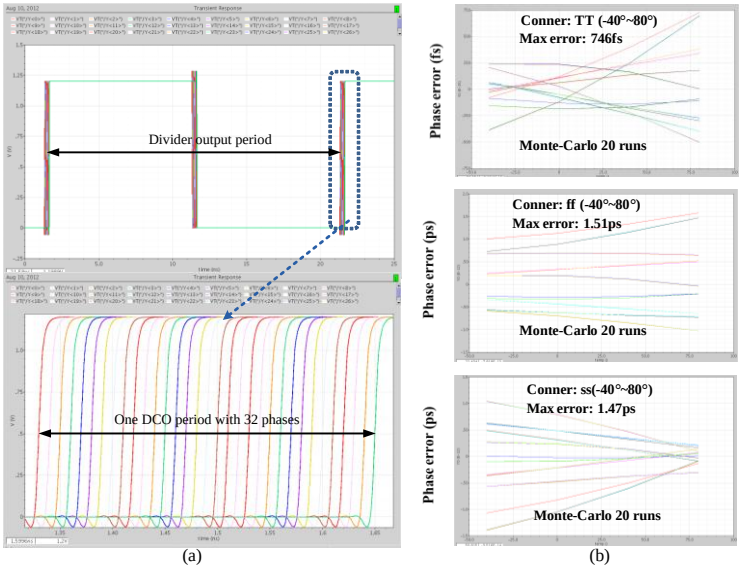


Fig. 3. 32Simulation result of the 32-phase interpolator (a) 32-phase output waveform and (b) phase error under different conditions

The measured output spectrum of the sub-integer divider is shown in Fig.3.33. The worst case spur is -71dBc with a division ratio of 32+1/32, which means all the phase errors in the PI will be selected to the output. The measured equivalent phase error is1.36ps, which is 0.0125% of the output period.

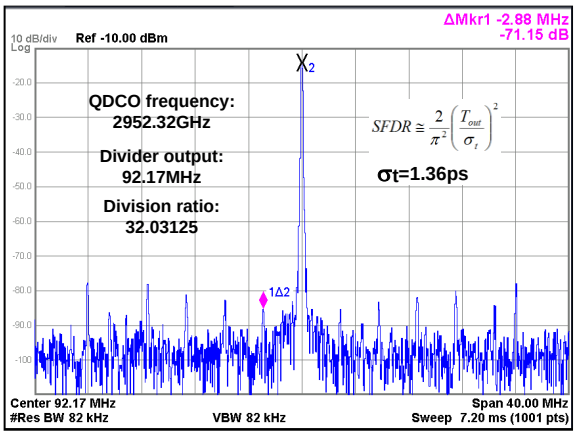


Fig. 3. 33 The measured output spectrum of the sub-integer divider

3.5 ADPLL System Design

3.5.1 Continuous-Time Approximation of Digital PLL

For continuous-time approximation of a digital PLL, at low frequency (i.e., |sT|<<1), we can use the first order term of a Taylor series expansion to approximate:

$$z^{-1} = e^{-sT} \approx 1 - sT \quad \text{and} \quad s = \frac{1 - z^{-1}}{T} \tag{3.12}$$

The ADPLL equivalent model [3.20] is shown in Fig. 3.34. The parameters which need to be determined here are K_1, K_2, and α. K_1 and K_2 are two gain factors used to determine the overall filter gain and zero position, respectively. The value of α determines the cut off frequency of the first-order IIR.

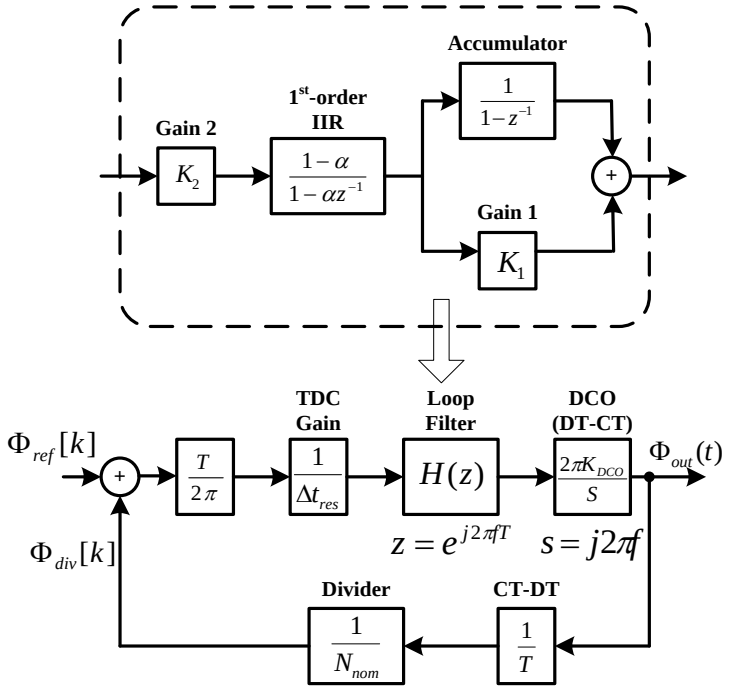


Fig. 3. 34 ADPLL equivalent model

In a classical PLL, the approximated S-domain open-loop transfer function is:

$$A(s) = \frac{K}{S^{type}} * \frac{1+\frac{s}{\omega_z}}{1+\frac{s}{\omega_p}} \tag{3.13}$$

where *type* is one or two for a Type-I and Type-II PLL, respectively, ω_z and ω_p are the zero and pole frequencies. For example: given a 100KHz bandwidth, type=2, 2nd order roll-off, we have:

$$K=3*10^{10};\ \omega p=2\pi*1.53*10^{5}\ (Hz);\ \text{and}\ \omega p=2\pi*10^{4}\ (Hz)$$

The open-loop transfer function of our ADPLL is:

$$\begin{aligned} A(S) &= \frac{T}{2\pi} * \frac{1}{\Delta t_{res}} * H(Z) * \frac{2\pi K_{DCO}}{S} * \frac{1}{N_{nom}} \\ &= \frac{T}{\Delta t_{res}} * \frac{K_{DCO}}{N_{nom}} * \frac{1}{S} * H(Z) \end{aligned} \tag{3.14}$$

$$\begin{aligned} H(Z) &= K_2 * \frac{1-\alpha}{1-\alpha z^{-1}} * (K_1 + \frac{1}{1-z^{-1}}) \\ &= K_2 * \frac{1-\alpha}{1-\alpha z^{-1}} * \frac{K_1 - K_1 z^{-1} + 1}{1-z^{-1}} \end{aligned} \tag{3.15}$$

By using the approximation of $z^{-1} = e^{-sT} \approx 1 - sT$, the S-domain filter transfer function can be approximated as:

$$\begin{aligned} H(Z) &= H(Z)|_{z=1-sT} \\ &= K_2 * \frac{1-\alpha}{1-\alpha(1-sT)} * \frac{K_1 - K_1(1-sT) + 1}{sT} \\ &= \frac{K_2}{sT} * \frac{1}{1+\frac{s\alpha T}{1-\alpha}} * (1+sK_1T) \end{aligned} \tag{3.16}$$

Now, we can plug equation 3.16 into equation 3.14 to obtain the final S-domain open-loop transfer function of our ADPLL:

$$A(S) = \frac{K_2}{\Delta t_{res}} * \frac{K_{DCO}}{N_{nom}} * \frac{1}{S^2} * \frac{1+sK_1T}{1+\frac{s(\alpha T)}{1-\alpha}} \tag{3.17}$$

The last step is to compare the open-loop transfer function of our PLL (equation 3.14) with the desired open-loop transfer function (equation 3.13) to obtain the following relationships:

$$K_1 = \frac{1}{\omega_z T} = \frac{1}{2\pi f_z T} \tag{3.19}$$

$$K_2 = K * \Delta t_{res} * \frac{N_{nom}}{K_{DCO}} \tag{3.20}$$

$$\alpha = \frac{1}{1+\omega_p T} = \frac{1}{1+2\pi f_p T} \tag{3.21}$$

Given the value of f_z and f_p, the final value of K_1, K_2, and α can be determined. To leverage the fact that a gain factor of a power of two can be easily implemented as bit-shifting in the hardware.

3.5.2 Noise Analysis of the ADPLL

Fig. 3.35 illustrates the modeling of the proposed digital frequency synthesizer with the TDC and DCO models, including their various noise sources [3.20]. As shown in this figure, the main noise sources in the overall system are: 1) TDC quantization noise $t_q[k]$, 2) Reference noise $\phi_{ref}[k]$, 3) Divider ΣΔ quantization noise $n[k]$, 4) DCO intrinsic phase noise $\phi_n(t)$ and 5) DCO quantization noise $q_{DCO}[k]$.

First, we derive the individual noise transfer functions, then characterize the spectral noise density of each noise source, and finally calculate the PLL output phase noise contributed from each of them. Before being able to do it in a systematic way, we need to define several transfer functions and terms in advance.

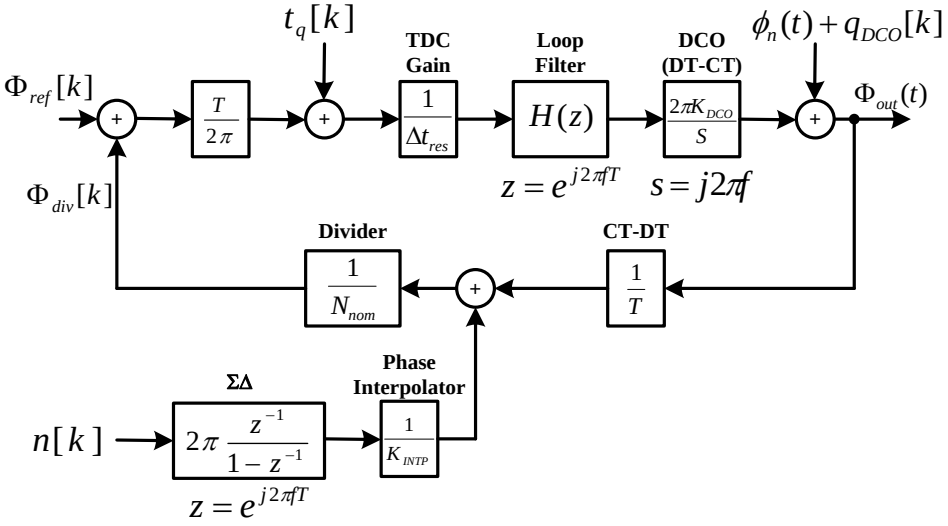


Fig. 3. 35 Noise model of the ADPLL

The open-loop and closed-loop transfer functions are defined as:

$$A(f)=\frac{T}{2\pi}*\frac{1}{\Delta t_{res}}*H(Z)*\frac{K_{DCO}}{j\cdot f}*\frac{1}{N_{nom}} \tag{3.21}$$

$$G(f)=\frac{A(f)}{1+A(f)} \tag{3.22}$$

Since $A(f)$ is low-pass in nature with an infinite gain at DC, $G(f)$ is a low-pass filter with a low-frequency gain of one.

We define the noise transfer functions from the reference-referred and DCO-referred noises to the PLL output as following:

$$\frac{\phi_{out}}{\phi_{ref}}=T\cdot N_{nom}\cdot|G(f)| \tag{3.23}$$

$$\frac{\phi_{out}}{\phi_{DCO}}=|1-G(f)| \tag{3.24}$$

As we seen, the key difference of these two equations is that although the reference referred noise is filtered by the low-pass filtering action of the PLL (i.e., G(f)), the DCO-referred noise is high-pass filtered by 1-G(f). In addition, the reference-referred

noise is amplified by a factor of T*N_{nom}, but the DCO referred-noise is not.

Then we derive the phase noise contribution of each building block:

1) TDC noise:

$$S_{out,tdc}(f) = \frac{1}{T} |2\pi N_{nom} G(f)|^2 \, (2\sin(\pi f T))^2 \cdot \frac{(\Delta T_{res})^2}{12} \tag{3.25}$$

2) Reference noise:

$$S_{out,ref}(f) = |N_{nom} G(f)|^2 \cdot S_{ref}(f) \tag{3.26}$$

where $S_{ref}(f)$ is the input reference noise;

3) Divider ΣΔ Quantization noise:

$$S_{out,div}(f) = \left(\frac{1}{K_{INTP}}\right)^2 \cdot T |2\pi G(f)|^2 \, (2\sin(\pi f T))^{2(m-1)} \cdot \frac{1}{12} \tag{3.27}$$

where K_{INTP} is the interpolation ration of the phase interpolator;

4) DCO noise:

$$S_{out,DCO}(f) = |1 - G(f)|^2 \cdot S_{DCO}(f) \tag{3.28}$$

where $S_{DCO}(f)$ include the intrinsic noise of the oscillator and the quantization noise due to the finite resolution of the DCO;

Because the above noises are uncorrelated to each other, the overall noise spectral density at the PLL output can be obtained by summing the above results:

$$S_{out,all}(f) = S_{out,tdc}(f) + S_{out,ref}(f) + S_{out,div}(f) + S_{out,DCO}(f) \tag{3.29}$$

To observe the relative contribution of each noise component, a MATLAB script, is developed to plot the overall PLL noise with the result illustrated in Fig. 3.36. The parameters used in this calculation are listed in Table 3.2.

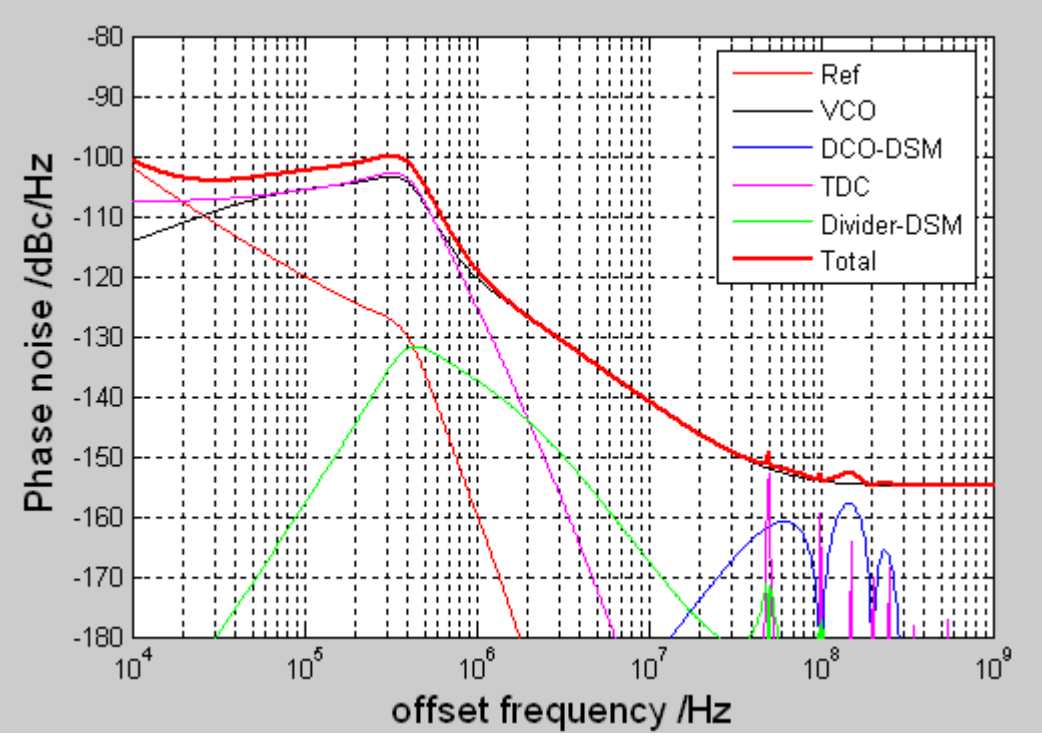


Fig. 3. 36 Phase noise simulation of the ADPLL

Table 3. 2 Parameter used for the ADPLL phase noise simulation

Parameter	Value
Reference CLK f_{ref}	50MHz
Division ratio N_{nom}	66
TDC resolution ΔT_{res}	1 ps
TDC noise floor ΔT_{floor}	2 ps
Reference noise	-156 dBc/Hz at 100 kHz offset
DCO intrinsic noise	-120 dBc/Hz at 10 MHz offset, 400-kHz flicker noise corner
DCO resolution	50KHz
ΣΔ Divider order	2
Phase interpolation ratio	32
Loop bandwidth	450KHz

3.6 Measurement Result

The open-loop phase noise of the ADPLL is measured by setting all the digital control of the QDCO to be 0. As shown in Fig. 3.37, for a carrier frequency of 2.93GHz, the measured phase noise at 100 KHz offset is -93.8dBc/Hz and -142.8dBc/Hz at 10 MHz offset, the flicker noise corner is at 500 KHz.

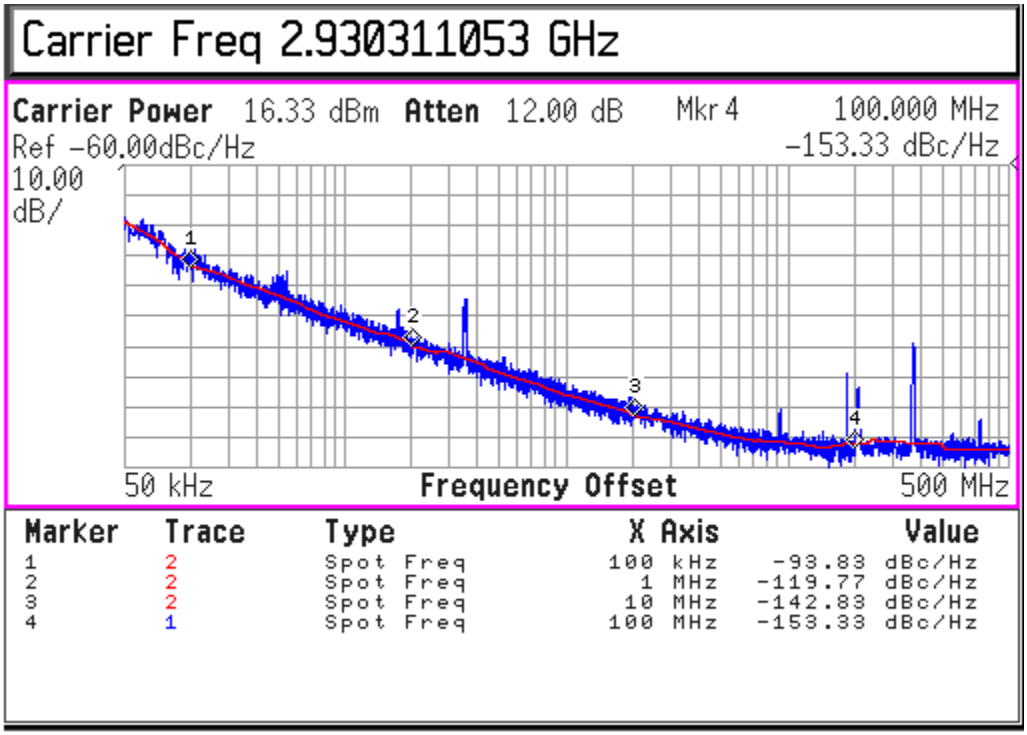


Fig. 3. 37 ADPLL open-loop phase noise

The measured close-loop phase noise of the ADPLL at 3.3GHz is shown in Fig.3.38. The in-band phase noise at 100 KHz offset is -100.3dBc/Hz and out-band phase noise at 10 MHz offset is -140.8dBc/Hz. Fig. 3.39 (a) shows the measured in-band fractional spurs with a maximum value of -49.5dBc at frequency offset 26.1 KHz. The reference spurs is shown in Fig. 3.39 (b), it is -71dBc at 50 MHz frequency offset. Table 3.3 summarizes and compares the performance of the proposed ADPLL with other of state-of-the-art solutions.

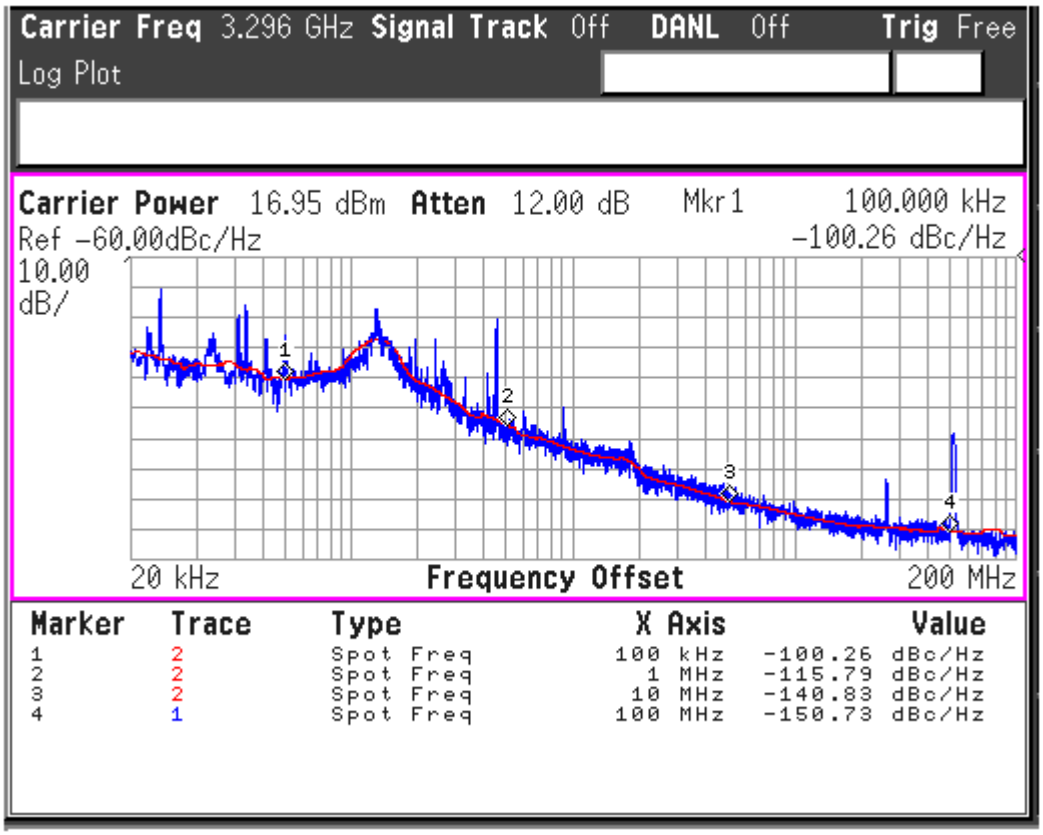
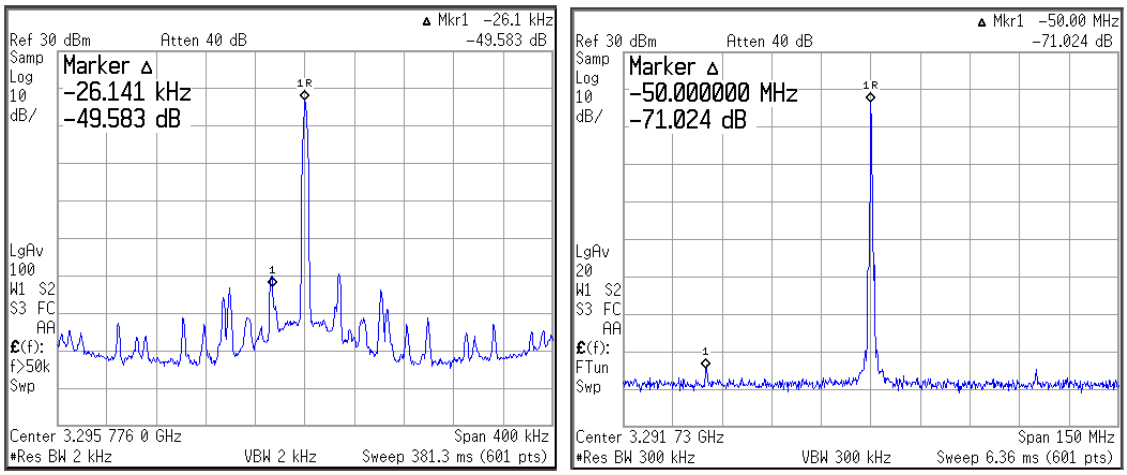


Fig. 3. 38 The measured phase noise of the ADPLL



(a) **(b)**

Fig. 3. 39 Measured ADPLL spurs (a) in-band fractional spurs and (b) reference spurs

Table 3. 3 Parameter used for the ADPLL phase noise simulation

Parameter	This work	JSSC 11 Zanuso [3.7]	ISSCC 11 Pavlovic[3.21]	ESSCIRC 12 Allan [3.22]
Technology (nm)	65nm	65nm	65nm	65nm
Supply Voltage (V)	1.2	1.2	1.2	1.2
Reference Frequency (MHz)	50	40	48	50
Carrier Frequency (GHz)	3.1	3.6	5.8	4.5
Tuning Range (GHz)	2.5~3.7	-	4.9~6.9	4.1~6.5
Loop bandwidth (KHz)	450	3200	500	800
Phase Noise (in-band) (dBc/Hz)	-100	-104	-96	-100
Phase Noise (10MHz) (dBc/Hz)	-141	-118	-134	-139
Reference Spurs (dBc)	-71	-65	-67	-65
Fractional Spurs (dBc)	-50	-57	-45	-48
Power Consumption (mW)	29	80	20	26

Bibliography

[3.1] Temporiti, E.; et al., "A 700-kHz bandwidth ΣΔ fractional synthesizer with spurs compensation and linearization techniques for WCDMA applications," *IEEE J. Solid-State Circuits*, vol.39, no.9, pp. 1446 - 1454, July 2009

[3.2] Meninger, S.E.; et al., "A fractional- N frequency synthesizer architecture utilizing a mismatch compensated PFD/DAC structure for reduced quantization-induced phase noise," *IEEE Circuits and Systems II*, vol.50, no.11, pp. 1446 - 1454, Nov 2003

[3.3] Temporiti, E.; et al., "A 3.5 GHz Wideband ADPLL with Fractional Spur Suppression through TDC Dithering and Feedforward Compensation," *IEEE J. Solid-State Circuits*, vol.45, no.12, pp. 2723 - 2736, Dec. 2010

[3.4] Liangge Xu; et al., "A 2.4-GHz Low-Power All-Digital Phase-Locked Loop," *IEEE J. Solid-State Circuits*, vol.45, no.8, pp. 1513 - 1521, Aug. 2010

[3.5] Staszewski, R.B.; et al., "Spur-Free Multirate All-Digital PLL for Mobile Phones in 65 nm CMOS," *IEEE J. Solid-State Circuits*, vol.46, no.12, pp. 2904 - 2919, Dec. 2011

[3.6] Temporiti, E.; et al., "A 3 GHz Fractional All-Digital PLL With a 1.8 MHz Bandwidth Implementing Spur Reduction Techniques," *IEEE J. Solid-State Circuits*, vol.44, no.3, pp. 824 - 834, Mar. 2009

[3.7] Zanuso, M.; et al., "A Wideband 3.6 GHz Digital ΔΣ Fractional-N PLL With Phase Interpolation Divider and Digital Spur Cancellation," *IEEE J. Solid-State Circuits*, vol.46, no.3, pp. 627 - 638, Mar. 2011

[3.8] Staszewski, R.B.; et al., "A digitally controlled oscillator in a 90 nm digital CMOS process for mobile phones" *IEEE J. Solid-State Circuits*, vol. 40, no. 11, pp. 2203-2211, Nov. 2005.

[3.9] Mirzaei, A..; et al., "The Quadrature LC Oscillator: A Complete Portrait Based on Injection Locking," *IEEE J. Solid-State Circuits*, vol. 42, no. 9, pp. 1916-1932, Sep. 2007.

[3.10] van der Tang, J.; et al., "Analysis and design of an optimally coupled 5-GHz quadrature LC oscillator," *IEEE J. Solid-State Circuits*, vol. 37, no. 5, pp. 657 - 661, May 2002.

[3.11] Deping Huang; et al., "A Frequency Synthesizer With Optimally Coupled QVCO and Harmonic-Rejection SSBmixer for Multi-Standard Wireless Receiver," *IEEE J. Solid-State Circuits*, vol. 46, no. 6, pp. 1307 - 1320, June 2011.

[3.12] Andreani, P.; et al., "Analysis and design of a 1.8-GHz CMOS LC quadrature VCO"

IEEE J. Solid-State Circuits, vol. 37, no. 12, pp. 1737-1747, Dec 2002.

[3.13] Ng, A.W.L.; Luong, H.C.; A. "A 1-V 17-GHz 5-mW CMOS Quadrature VCO Based on Transformer Coupling" *IEEE J. Solid-State Circuits*, vol. 42, no. 9, pp. 1933-1941, Sep. 2007.

[3.14] Mazzanti, A.; Andreani, P.; "Class-C Harmonic CMOS VCOs, With a General Result on Phase Noise" IEEE J. Solid-State Circuits, VOL. 43, NO. 12, Dec 2008

[3.15] Fanori, L.; et al., "3.3GHz DCO with a frequency resolution of 150Hz for All-digital PLL" *IEEE ISSCC* Dig. Tech. Papers, pp. 48-49, 2010

[3.16] R. B. Staszewski and P. T. Balsara, "All-Digital Frequency Synthesizer in Deep-Submicron CMOS," Hoboken, NJ: Wiley, 2006.

[3.17] Dudek, P.; et al., "A high-resolution CMOS time-to-digital converter utilizing a Vernier delay line," *IEEE J. Solid-State Circuits*, vol. 35, no. 2, pp. 240 - 247, Feb 2000.

[3.18] Minjae Lee; et al., "A 9 b, 1.25 ps Resolution Coarse–Fine Time-to-Digital Converter in 90 nm CMOS that Amplifies aTime Residue," *IEEE J. Solid-State Circuits*, vol. 43, no. 4, pp. 769 - 777, April 2008.

[3.19] V. Gutnik, et al., "On-chip picosecond time measurement," in *IEEE VLSI* Dig. Tech Papers, Jun. 2000, pp. 52–53

[3.20] Michael H. perrott "ISSCC 2008 Tutorial on Digital Phase-Lock-Loop,"

[3.21] Nenad Pavlovic, et al., "A 5.3GHz Digital-to-Time-Converter-Based Fractional-N All-Digital PLL," *IEEE ISSCC* Dig. Tech. Papers, pp. 54-55, 2011

[3.22] Alan W.L. Ng, et al., "A 4.1GHz-6.5GHz All-Digital Frequency Synthesizer with a 2nd-Order Noise-Shaping TDC and a Transformer-Coupled QVCO," *IEEE ESSCIRC* Dig. Tech. Papers, pp. 189-192, 2012

CHAPTER 4 Quadrature-In/Quadrature-Out ÷1.5 Divider

4.1 Introduction of LO Pulling

A common issue when integrating the power amplifier together with the RFIC is the "pulling" of the VCO by the strong power amplifier signal [4.1]. The injection pulling experienced in the VCO, i.e., the victim circuit, caused by interference originating in the PA, the aggressor circuit, can degrade the transmitter's performance to the extent that it fails its targeted specifications. There are three main types of coupling paths between the PA and the VCO:

1) Resistive couple due to the low resistive substrate
2) Magnetic couple from the inductor and bond wire
3) Capacitive coupling due to the connection.

4.1.1 LO Pulling Mechanism

The injection pulling expression can be derived from first principles of a feedback oscillator [4.2], the essential components of which is an active device (amplifier) and a feedback network. Such system which satisfies the Barkhausen Criteria will oscillate. The key mechanism behind the oscillation is the fact that the amplifier starts up by amplifying its noise, which transits from the output back to the input through a network with certain gain and phase response. The Barkhausen criteria state that the gain of the feedback network has to be 1. The gain is large at the time oscillation starts but as the oscillator signal amplitude grows, the gain reduces to 1. The second constraint is that the phase shift caused by the network has to be 360 ° for common-gate or common-drain

and 180 ° for common-source amplifier. This will ensure that the signals at the input and output are in-phase allowing the signal to grow until the circuit reaches saturation point. The frequency at which these two criteria are satisfied will be the oscillation frequency of the system.

With this understanding, the behavior of VCO under injection of an AM aggressor can be studied using fundamental principles of feedback oscillators [4.3]. Assume a feedback oscillator with amplitude V_{OSC} and a composite vector V_T shown in Fig. 4.1(a). In the absence of any interference V_{inj}, the phasor V_{OSC} and the composite vector V_T are rotating at same speed and in phase. The Barkhausen criteria are satisfied at frequency ω_0. When the system undergoes the modulation, an aggressor V_{inj} is injected into the VCO. The phasor representation of this scenario is shown in Fig. 4.1(a). From Fig. 4.1(c) it is clear that the aggressor is generated by the polar amplifier (PA) (If a divider are used to generate the LO with division ratio n, then the aggressor is the n^{th} harmonic of the PA output) that finds its way to the VCO through a coupling path represented by a transfer function H(s). This will result in an angular displacement ϕ between the composite vector V_T and V_{OSC}

At steady state, the aggressor V_{inj} and victim V_{OSC} move at the same rate with a constant angular displacement between them. This additional phase ϕ that is introduced in the feedback oscillator will violate Barkhausen criteria at ω_0 and, therefore, the oscillation will shift to another frequency along the curve shown in Fig. 4.1(b). If *Vinj(t)* is a time-varying signal due to the AM-modulation, which results in a time-varying $\phi(t)$ and consequently a time-varying in $\omega(t)$. In this way, AM-FM conversion is experienced by the DFC.

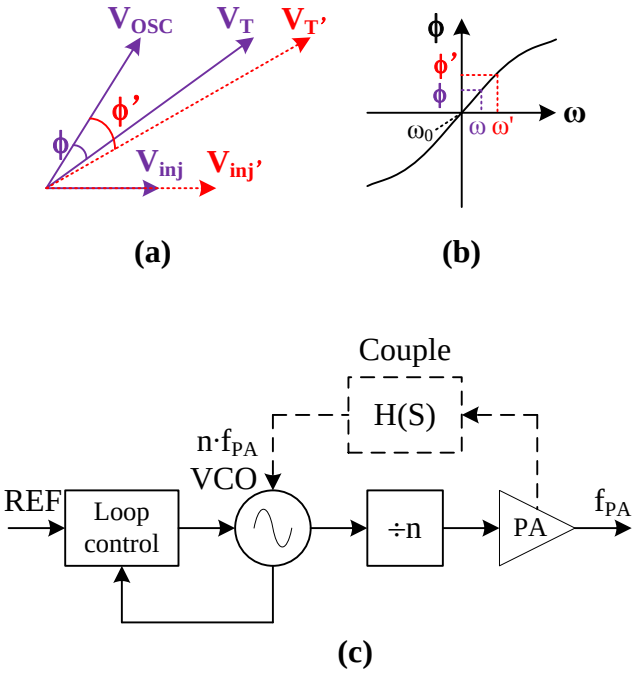
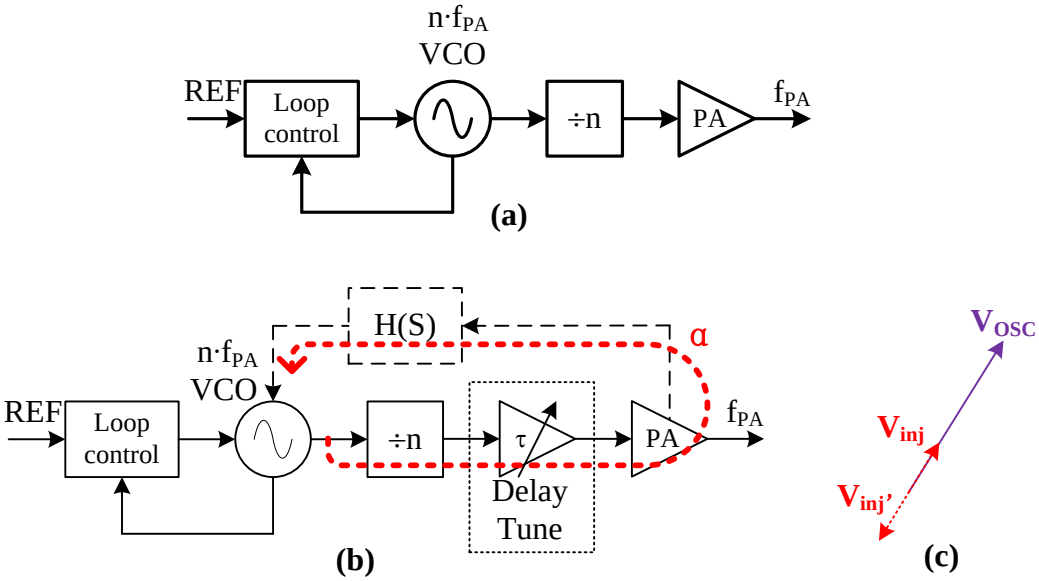


Fig. 4. 1 LO pulling mechanism (a) Phasor representation of signals in the VCO (b) Phase response of the resonance tank (c) Block diagram of the LO pulling mechanism

4.1.2 LO Pulling Reduction Techniques

A number of techniques have been used to offset the VCO operating frequency from the PA output frequency to prevent this effect [4.4]-[4.5]. 1) The LO is generated the by integer division (typically division by two) of the VCO signal. As shown is Fig. 4.2(a), this prevents direct PA pulling without introducing undesired spurs. However, it might still suffer of pulling from the harmonics of the PA, which can be rather high especially when the PA operates in overdriven mode for better efficiency. This might limit the applicability of the technique of Fig. 4.2(a) to systems with lower output power or off-chip PA. Integer division ratios higher than two could reduce the harmonic pulling, but result in much higher operation frequency of the VCO and higher power consumption. 2) In fig. 4.2(b), a programmable delay is added in the LO generation path and the phasor diagram is shown in fig. 4.3(b). By tuning the delay, the interference

vector Vinj and the oscillator vector VOSC can be controlled to have a phase angle of 0 ° or 180 ° to eliminate the pulling effect. This technique will require a calibration procedure to fine an optimal tuned delay to make the phase angle to be 0 °or 180 °. Because there are more than one coupling path between the PA and VCO, these interferences from different coupling paths will have different phases. However the added delay can only tune one of the phase to be 0 °or 180 °, then the pulling effect can't eliminate completely. This might limit the output power of the on-chip PA. In addition the phase delay will be affected by the PVT condition which makes the calibration procedure to be very complicate. 3) As shown in Fig. 4.2(d), If the LO generation divider can provide a fractional frequency division ratio, then the direct and harmonic pulling can be completely eliminated. For fractional frequency division, it will generate spurs because the divider is based on single-side-band mixing. Phase calibration may be employed to suppress these spurs. For most of the application, quadrature phase LO is required and this should be co-design with the fractional divider.



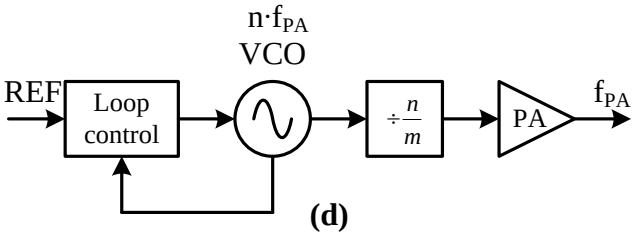


Fig. 4. 2 Pulling reduction techniques for LO generation: (a) Integer frequency division, (b) tunable delay for in/out phase pulling, (c) phase diagram of in/out phase pulling, and (d) fractional frequency division

4.2 Fractional Frequency Division with Quadrature Phase Output

Multiphase signal can be used to implement a fractional frequency division [4.6]-[4.9]. These multiphase signals (normally, 4-phases: 0°, 90°, 180° and 270°) can be generated from a multiphase oscillator or poly-phase filter. There are mainly 2 types of fractional frequency division techniques: 1) phase-rotating frequency division and 2) single-side-band mixing. Both techniques will be discussed in detail.

4.2.1 Phase-Rotating Frequency Division

Fig. 4.3(a) shows a case that implements a division by 1.25 [4.10]. A 4-to-1 MUX is used to cyclically select one of the input phases (0°-90°-180°-270°-0°-…), such that only one of them is connected to the output at one time. In the example in Fig. 4.3(a), every time the output signal produces a falling edge, the next phase is selected in the MUX. Since the input phases are $T_{in}/4$ apart (T_{in} being the period of the input signal), this operation will stretch the input period by 25%, generating an output period $T_{out}=1.25*T_{in}$. This is equivalent to a frequency division by 1.25. Different division

ratios can be obtained with four phases. If, for example, In the Fig. 4.3(b), the phase sequence is inverted (270 °-180 °-90 °-0 °-270 °-…), a division by 0.75 is implemented. When more than four phases are available, a wider number of fractional division ratios can be synthesized.

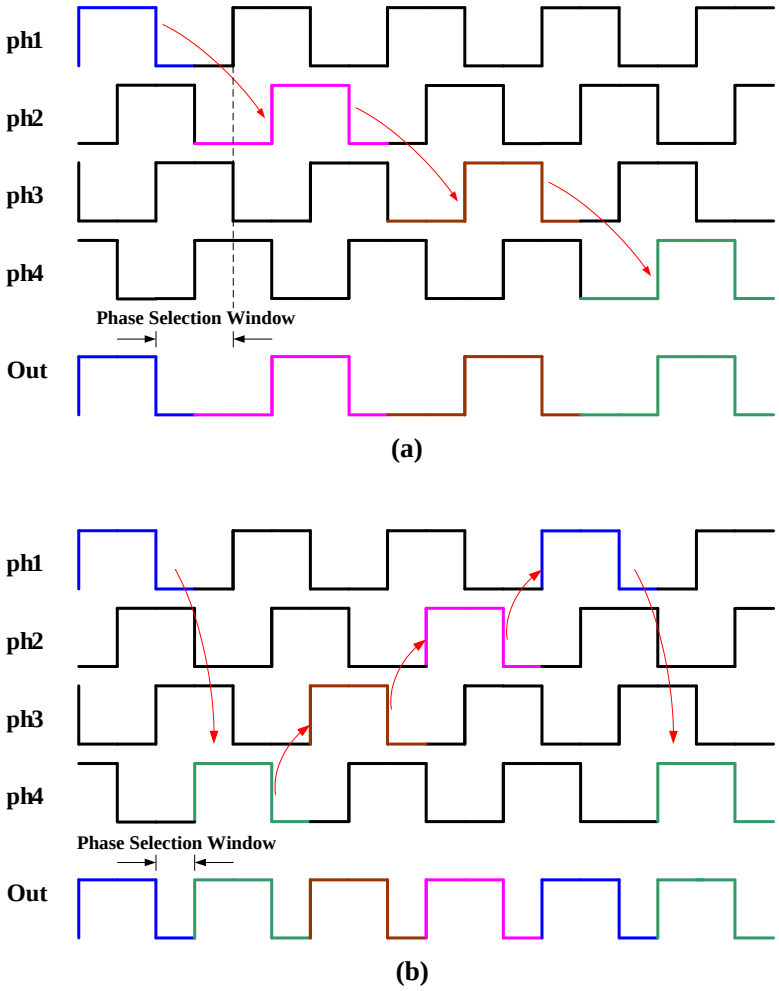


Fig. 4. 3 Phase-Rotating Frequency Division (a) divide by 1.25 and (b) divide by 0.75

For ÷1.5 frequency division with quadrature phase output, we can cascade a phase-rotating ÷0.75 divider and a ÷2 divider. To achieve accurate quadrature phase output, the input signal of the ÷2 divider has to be 50% duty-cycle. However, as we seen in Fig.

4.3(b), in the ideal case, the duty-cycle of the output signal is 2/3. So, after divide by 2, the I-Q mismatch will be $30°$ which is not acceptable for most of the wireless application.

4.2.2 Fractional Frequency Division with Sing-Side-Band Mixer

Fig. 4.4 shows the block diagram of the ÷1.5 divider with quadrature phase output [4.11]. The divider takes the 4-phases input from a QVCO. A single-side-band mixer (SSBM) and two ÷2 dividers form a feedback loop for the fractional frequency division. Its operation is explained by the following equation: (For simplicity's sake, we assume the sinusoidal wave at each node, at the harmonics will be considered later)

The input signal for the QVCO is:

$$I_a = \sin(\omega_a t) \tag{4.1a}$$

$$Q_a = \cos(\omega_a t) \tag{4.1b}$$

Assume the output of the SSBM is:

$$V_b = \sin(\omega_b t + \phi) \tag{4.1c}$$

Then the first divider output is:

$$I_c = \sin(\frac{\omega_b}{2} t + \frac{\phi}{2}) = \sin(\omega_c t + \frac{\phi}{2}) \tag{4.1d}$$

$$Q_c = \cos(\frac{\omega_b}{2} t + \frac{\phi}{2}) = \cos(\omega_c t + \frac{\phi}{2}) \tag{4.1e}$$

And the second divider output is:

$$I_d = \sin(\frac{\omega_b}{4} t + \frac{\phi}{4}) = \sin(\omega_d t + \frac{\phi}{4}) \tag{4.1f}$$

$$Q_d = \cos(\frac{\omega_b}{4} t + \frac{\phi}{4}) = \cos(\omega_d t + \frac{\phi}{4}) \tag{4.1g}$$

The operation of the SSBM is:

$$V_b = I_a \cdot Q_d + Q_a \cdot I_d \tag{4.1h}$$

From equation (4.1a) to (4.1h), we have: $\omega_b=\omega_a+\omega_b/4$, then $\omega_b=4/3\omega_a$ and $\omega_c=2/3\omega_a$. So, divide by 1.5 can be achieved.

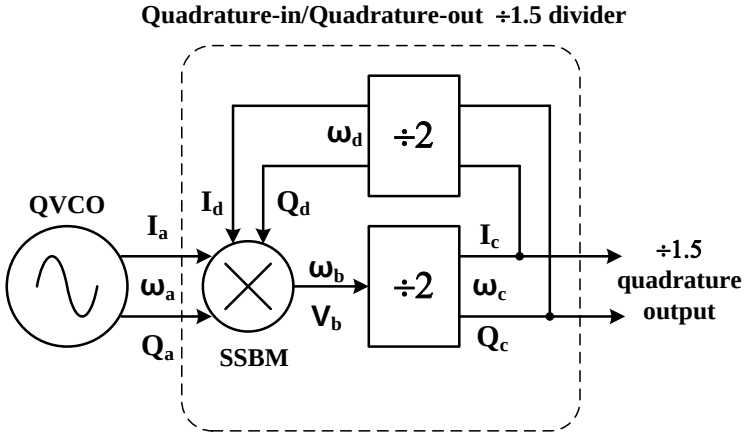


Fig. 4. 4 Block diagram of a Quadrature-in/Quadrature-out ÷1.5 divider

As Fig.4 shown, the quadrature output signals I_C and Q_C are generated by dividing V_b by 2. So, V_b should have 50% duty cycle to guarante quadrature output of the divider. Assume the SSBM and ÷2 divider are all using differential implementation, and then all the even-order harmonics are cancelled. For the SSBM, due to the nonlinear of its switch, odd-order harmonics mixing is unavoidable. Considering I_d and Q_d contrain 3rd order harmonic and I_d and Q_d are supposed to be delayed by a time delay Δt with respect to I_a and Q_a, then I_d and Q_d can be express as:

$$I_d = \sin\left[\frac{\omega_a}{3}(t+\Delta t)\right] + C\sin\left[\omega_a(t+\Delta t)\right] \tag{4.2a}$$

$$Q_d = \sin\left[\frac{\omega_a}{3}(t+\Delta t+\frac{T_d}{4})\right] + C\sin\left[\omega_a(t+\Delta t+\frac{T_d}{4})\right] \tag{4.2b}$$

Where T_d is the period of I_d and Q_d, and $T_d=2\pi/(\omega_a/3)$; C is the coefficient of the 3rd

order harmonic. Applying equation (4.2a) and (4.2b) to (4.1h), we have:

$$V_b = \sin\left[\frac{4\omega_a}{3}(t+\Delta t)\right] + C\sin(\omega_a \Delta t) \tag{4.2c}$$

From equation (4.2c), a DC offset $Csin(\omega_a \Delta t)$ is presented at the output of the SSBM and therefore the duty cycle is not 50% and depends on the QVCO frequency ω_a and the delay Δt.

Fig. 4.5 shows a classical circuit implementation of the SSBM, the bottom row of transistors convert the input voltage I_a and Q_a to current and then I_d and Q_d control the top row of transistors to steer the current to R_+ or R_- to generate the output voltage V_{b+} and V_{b-}. From equation (4.2c), there is a DC offset between V_{b+} and V_{b-}. This DC offset generates not only non-50% duty cycle of the output but also amplitude mismatch between V_{b+} and V_{b-}. The amplitude mismatch is due to the unequal current bias for the transistor connected to V_{b+} and V_{b-}. The duty cycle error and amplitude mismatch cause the quadrature mismatch of the final output which is generated by dividing V_b by 2.

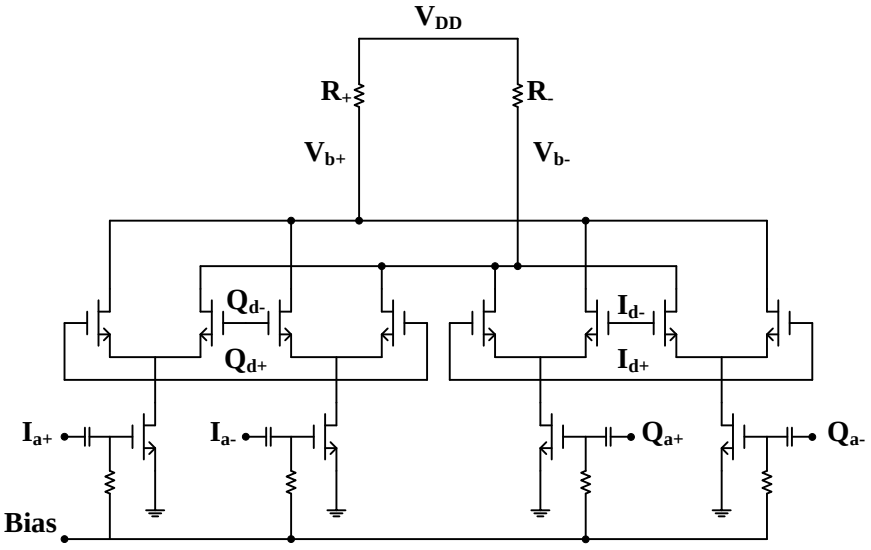


Fig. 4. 5 a classical circuit implementation of the SSBM

The duty cycle error and amplitude mismatch of the SSBM are simulated and shown in Fig. 4.6. The duty cycle is 38% and the amplitude mismatch is 22%. After ÷2, there is a 22.6 ºquadrature mismatch of the final output.

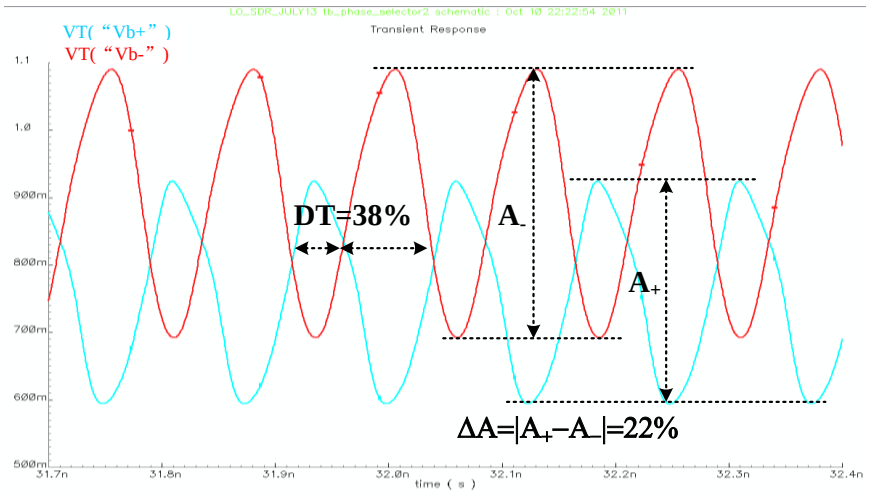


Fig. 4. 6 simulated SSBM output

To solve the duty cycle error and amplitude mismatch problem, we need to eliminate the DC term: $Csin(\omega_a \Delta t)$ in equation (4.2c). As we seen, there are 2 solutions to make this term to be 0: 1) Make $\omega_a \Delta t$ to be the multiple of π. ω_a is the QVCO frequency which has a wide range of operation for our application. Δt is due to the propagation delay of the SSBM and divider. Δt is process dependent and varies under different PVT condition. So, this solution is not suitable. 2) Make the coefficient C to be zero. We know C is due to the 3rd harmonic mixing of I_d and Q_d, then harmonic rejection mixer (HRM) [4.12] can be employed to solve this problem.

Fig. 4.7 shows the proposed Quadrature-in/Quadrature-out ÷1.5 divider with HRM and duty cycle correction (DCC). The HRM together with the three ÷2 dividers form a

feedback loop to perform ÷1.5 frequency division with quadrature input and quadrature output. To reject the 3rd harmonic of ω_d, the 8-phases signals with $\pi/4$ space are generated by dividing V_b by 4. Duo the process mismatch, there is some phase mismatches for the 8-phases signals and the HRM will have a finite harmonic rejection ratio. The residual duty cycle error at V_b will be calibrated by a DCC loop. With the accurate 50% duty cycle of V_b, the quadrature error of the final output phase is minimized.

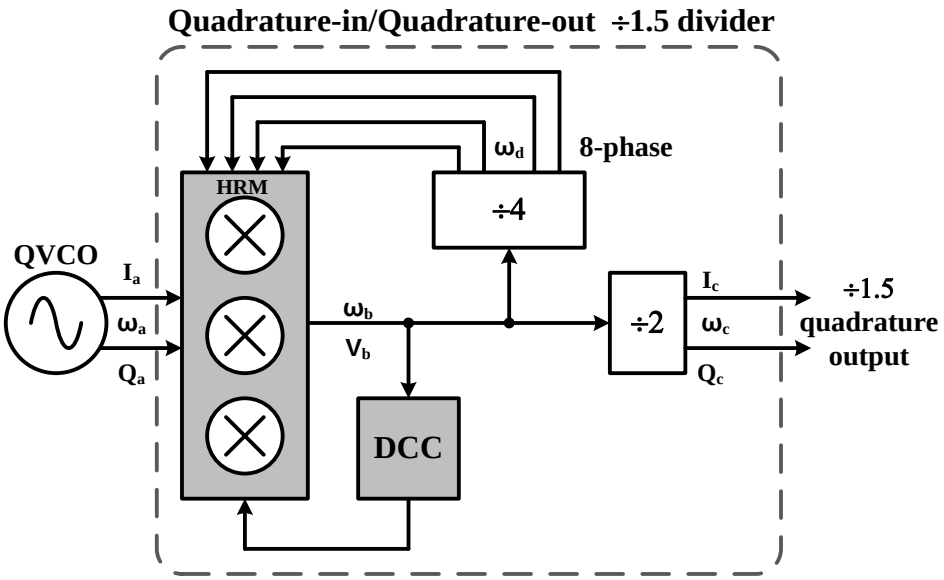


Fig. 4. 7 block diagram of the proposed Quadrature-in/Quadrature-out ÷1.5 divider

Fig. 4.8 shows the implementation of the HRM and DCC. Two differential-to-single ended (D-S) buffer are added at V_{b+} and V_{b-}, with the output: $V_{out+} = (V_{b+} - V_{b-})$ and $V_{out-} = (V_{b-} - V_{b+})$. An error amplifier (EA) amplifies the duty cycle errors V_E which are extracted by a 1st order RC filter and control the mount of DC current feed to the HRM. With the feedback loop, V_E is 0 when the loop is settled and the duty cycle of V_{out+} and V_{out-} is 50%.

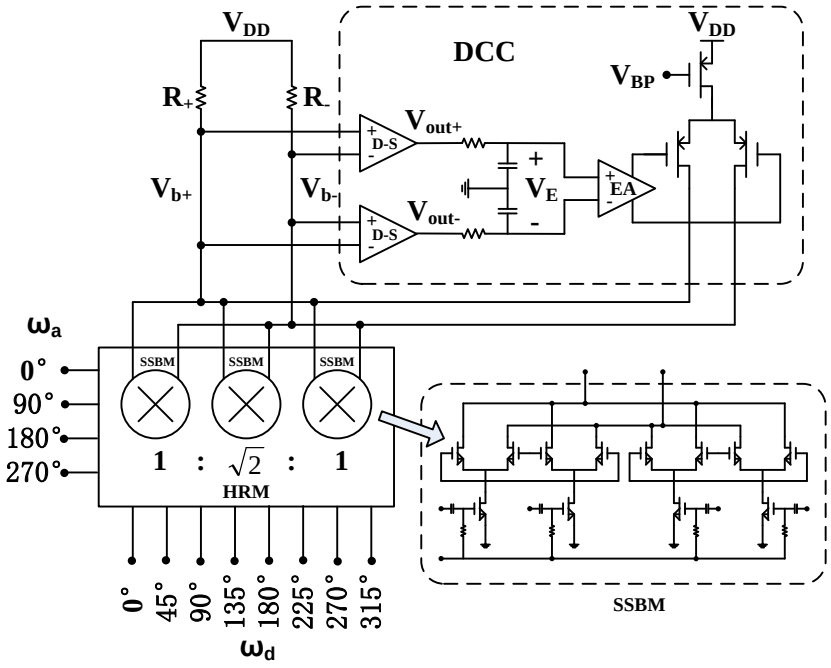


Fig. 4. 8 Implementation of the HRM and DCC

Fig. 4.9 shows the implementations of the differential-in/quadrature-out ÷2 divider and differential-in/8-phase-out ÷4 divider. They use dynamic divider architecture to achieve low power consumption and low phase noise. Fig. 4.10 shows the simulated HRM output with the proposed error correction techniques. The duty cycle is 48.3% and the amplitude mismatch is 3.7%.

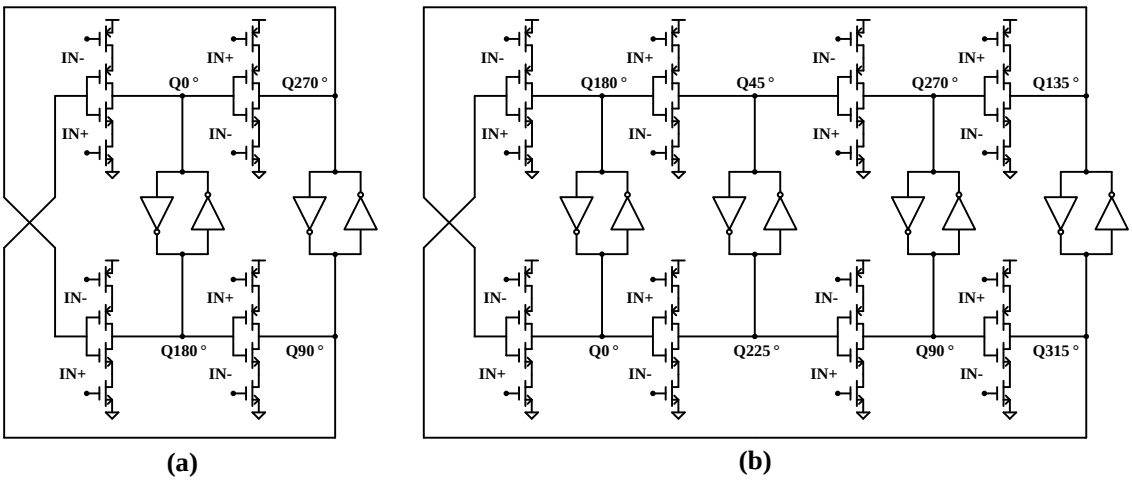


Fig. 4. 9 implementation of the divider (a) ÷2, 4-phases and (b) ÷4 8-phases output

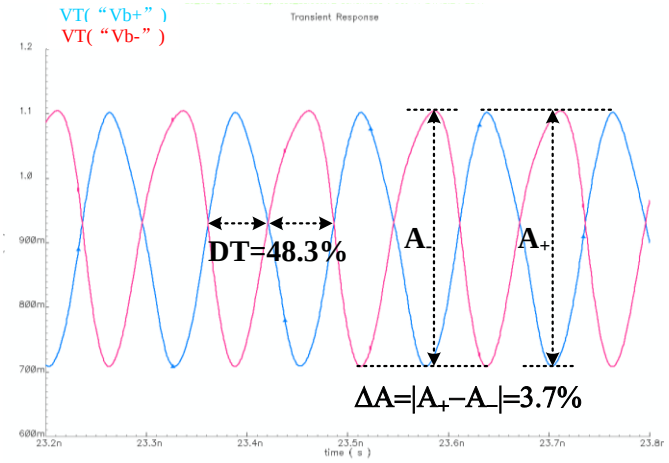


Fig. 4. 10 simulated HRM output

Table 4. 1 performance summary of the ÷1.5 divider

Parameter	Value
Input frequency	1~4GHz
Quadrature error without HRM and DCC	22.6 ℃@3GHz
Quadrature error with HRM and DCC	1.3 ℃@3GHz
VDD	1.2
Power consumption	5mW
Process Technology	CMOS 65nm

Bibliography

[4.1] B. Razavi, RF Microelectronics, Upper Saddle River, NJ: Prentice-Hall, 1998

[4.2] R.Adler, "Astudy of locking phenomenona in oscillators," Proc. IEEE, vol. 61, pp. 1380–1385, Oct. 1973.

[4.3] Imran Bashir, et al., "A Novel Approach for Mitigation of RF Oscillator Pulling in a Polar Transmitter," *IEEE J. Solid-State Circuits*, vol. 46, no. 2, pp. 403 - 415, Feb. 2011.

[4.4] O. Degani et al., "A 1 × 2 MIMO multi-band CMOS transceiver with an integrated front-end in 90 nm CMOS for 802.11a/g/n WLAN applications," in Proc. *IEEE ISSCC* Dig. Tech. Papers, Feb. 2008, pp. 356–357.

[4.5] H. Darabi et al., "A 2.4-GHz CMOS transceiver for bluetooth," *IEEE J. Solid-State Circuits*, vol. 36, no. 12, pp. 2016–2024, Dec. 2001.

[4.6] J. Craninckx and M. S. J. Steyaert, "A 1.75-GHz/3-V dual-modulus divide-by-128/129 prescaler in 0.7- um CMOS," *IEEE J. Solid-State Circuits*, vol. 31, pp. 890–897, Jul. 1996

[4.7] B. A. Floyd, "Sub-integer frequency synthesis using phase-rotating frequency dividers," *Trans. Circuits and Systems I*, vol. 55, pp.1823–1833, Aug. 2008.

[4.8] N. Krishnapura and P. R. A. Kinget, "5.3-GHz programmable divider for HiPerLAN in 0.25- um CMOS," *IEEE J. Solid-State Circuits*, vol. 35, no. 7, pp. 1019–1024, Jul. 2000.

[4.9] K. Shu, E. Sanchez-Sinencio, J. Silva-Martinez, and S. H. K. Embabi, "A 2.4-GHz monolithic fractional-N frequency synthesizer with robust phase-switching prescaler and loop capacitance multiplier," *IEEE J. Solid-State Circuits*, vol. 38, no. 6, pp. 866–874, Jun. 2003.

[4.10] Stefano Pellerano, et al., "A 4.75-GHz Fractional Frequency Divider-by-1.25 With TDC-Based All-Digital Spur Calibration in 45-nm CMOS," *IEEE J. Solid-State Circuits*, vol. 44, no. 12, pp. 3422–3433, Dec. 2009.

[4.11] Davide Guermandi, et al., "A 0.83–2.5-GHz Continuously Tunable Quadrature VCO," *IEEE J. Solid-State Circuits*, vol. 40, no. 12, pp. 2620–2627, Dec. 2005.

[4.12] Weldon, J.A.; et al., "A 1.75-GHz highly integrated narrow-band CMOS transmitter with harmonic-rejection mixers," *IEEE J. Solid-State Circuits*, vol. 36, no. 12, pp. 2003 - 2015, Dec. 2001.

CHAPTER 5 Digitally-Controlled Phase Modulator

5.1 Phase Modulator Overview

Phase modulation (PM) is a form of modulation that represents the information as the variations in the instantaneous phase of the carrier. Suppose the message signal is *m(t)* and the carrier signal is *c(t)*,

$$c(t) = A_c \sin(\omega_c t + \phi_c) \tag{5.1}$$

Where A_C is the carrier amplitude, ω_C is the carrier frequency and ϕ_C is the carrier phase shift. Then we have the modulated signal:

$$y(t) = A_c \sin(\omega_c t + m(t) + \phi_c) \tag{5.2}$$

$$y(t) = A_c \sin\left(\left(\omega_c + \frac{dm(t)}{dt}\right)t + \phi_c\right) \tag{5.3}$$

Eq. (5.2) and (5.3) shows that we can use *m(t)* to modulate the phase of RF carrier directly or use *dm(t)/dt* to modulate the frequency of the RF carrier.

When apply the Phase Lock Loop (PLL) for the PM, its output frequency f_{PLL} is:

$$f_{PLL} = f_{REF} \times FCW \tag{5.4}$$

Where f_{REF} is the reference frequency which usually supposed to be a constant; FCW is the digital frequency control word which controls the feedback division ratio to set the PLL output frequency. Fig. 5.5 shows its block diagram. N_C is for carrier selection. Then the FCW is:

$$FCW = N_c + \frac{d\phi(t)}{dt} \tag{5.5}$$

Then we can achieve $\phi(t)$ at the VCO output.

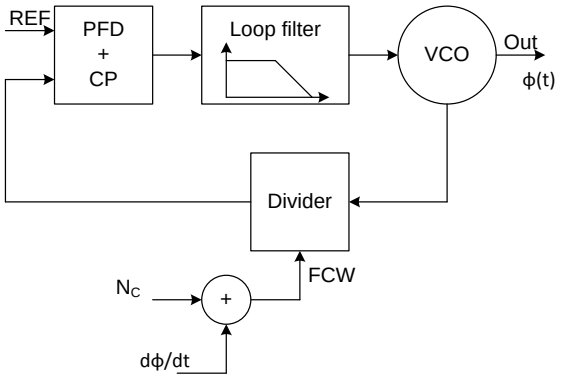


Fig. 5. 1 Block diagram of PLL based PM

This PM method works well only when the $\phi(t)$ is much lower than the cut-off frequency of the loop filter. Since the PLL is a feedback system, the PM is intrinsic linear even the VCO has a non-linear frequency tuning behavior. When the bandwidth of $\phi(t)$ becomes higher than the loop filter, the high frequency component of $\phi(t)$ is attenuated and cause distortion in the output PM signal.

Fig. 5.2 shows the block diagrams of the high bandwidth PM generation [5.1]. The digital PM signal is spitted into 2 parts: the low frequency components are sent to a pre-emphasis filter which has inverse frequency respond of the loop filter before adding to the FCW; while the high frequency components are converted to analog by a DAC and then directly modulate the VCO, so the modulation bandwidth can be enlarged.

For this wide band PM architecture, there are several drawbacks: 1) The PLL loop filter is in analog domain, its frequency respond would be varied due to the process variation, so the digital pre-emphasis filter can't completely match with it. 2) The time delay from the FCW input to the loop filter output can't be predicted accurately and products error when the two PM signals are combined with time mismatch. 3) The non-linear frequency tuning behavior of the VCO degrades the PM linearity. 4) The DAC gain and K_{VCO} should be normalized.

As we see, the main drawback of the above PM architecture is due to the analog passive loop filter of the PLL, which can be replaced by a digital filter in ADPLL.

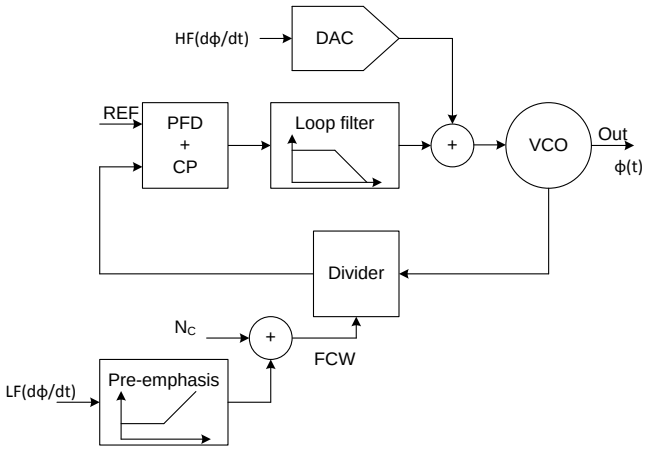


Fig. 5. 2 Block diagram of PLL based wide band PM

5.2 PM Generation with ADPLL

A lot of research efforts are devoted to the All-Digital Phase Look Loop (ADPLL) [5.2]-[5.4] recently main because the traditional analog PLL in deep sub-micron CMOS process shows many drawbacks: 1) The output range of the charge pump is limited due to the reduction of the supply voltage; 2) The varactors become more non-linear and compress the linear tuning range of the VCO; 3) The on-chip passive loop filter which consumes a lot of silicon area can't not scale down in the advanced process technology. On the contrary, the performance and chip area of the digital blocks depend on the time delay and logic gate density, so it can be fully benefited with the scaling in the process technology. In addition, the ADPLL performs more robustness when it integrates with the digital baseband and application processor due to its good digital switch noise immunity.

Fig. 5.3 shows the block diagrams of an ADPLL for the wide-band PM [5.6], [5.7]. Unlike the traditional analog PLL, the phase/frequency detector (PFD) is replaced

by a time-to-digital converter (TDC) to compare the input reference phase and the PLL feedback phase; the phase error is filtered by a digital loop filter and then directly controls a digitally-controlled oscillator (DCO).

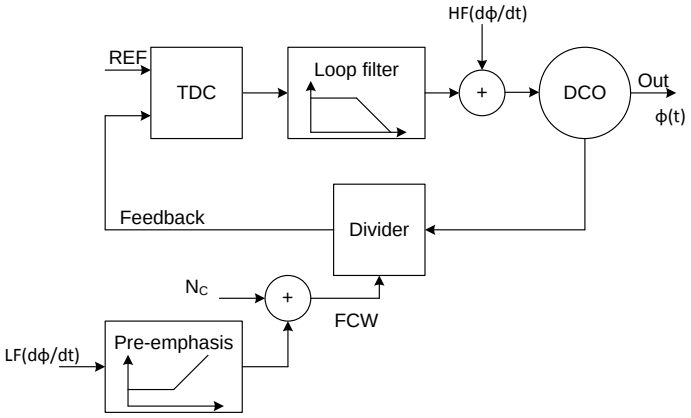


Fig. 5. 3 Block diagram of an ADPLL for the wide-band PM

As we seen at Fig. 5.3, because the loop filter is digital, its inverse function can be very accurate and well matches with the pre-emphasis filter. Also, the time delay of the two-path (LF and HF) injected PM signals is well controlled by digital clock synchronization. This ADPLL based PM modulators have been demonstrate in the application of GSM, Bluetooth, EDGE and WCDMA [5.5]-[5.7]. For the wide band application, such as 20MHz WLAN and LTE, the non-linearity frequency tuning of the DCO degrades the PM linearity significantly because the main part of the PM signal in its spectrum is outside the PLL loop bandwidth. In addition, the two-path PM signals eventually go to the TDC, which requires the TDC to have a larger linear input range. Fig. 5.4 shows the PM components of a WLAN 54Mbps 64-QAM OFDM transmitted signal. To achieve the required PM, the DCO should have a frequency variation of +/-150MHz. which corresponds to +/-6% at a 2.4GHz carrier. Such large linear frequency tuning range is unachievable in design of the DCO even with K_{VCO} calibration.

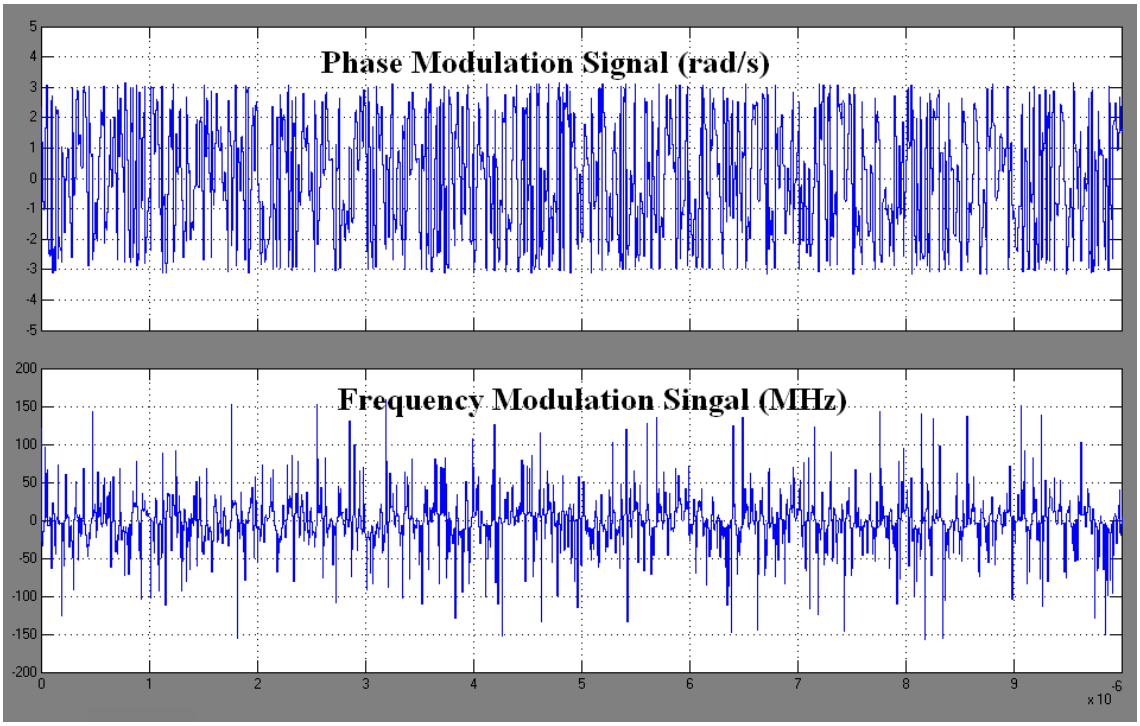


Fig. 5. 4 PM components of a WLAN 54Mbps 64-QAM OFDM transmitted signal (a)Required PM and (b) required DCO frequency variation

5.3 Proposed Phase Interpolated Digital Phase Modulator

The block diagram of the proposed phase interpolated digital phase modulator is shown in Fig. 5.5. The phase modulator uses 2-segments structure, the coarse segment employs phase interpolation and selection and obtains a 0~360 °phase tuning range with a resolution of 5.625 °. A digital-controlled phase-tuning buffer is designed for the fine segment and achieves 0.1 °resolution. The 11-bits digital PM signals are sent to the 2^{nd} order ΣΔ modulator with a 6-bit quantizer. The quantizer's outputs are for the coarse segment while the 5-bit quantization errors are for the fine segment. The phase mismatches of the coarse segment are measured and calibrated in the fine segment. The gain error between the 2 segments is also calibrated and the residual error will be shaped to out-of-band duo to the ΣΔ modulation. Because this phase modulator uses open-loop architecture, it has much higher bandwidth than the PLL based modulator.

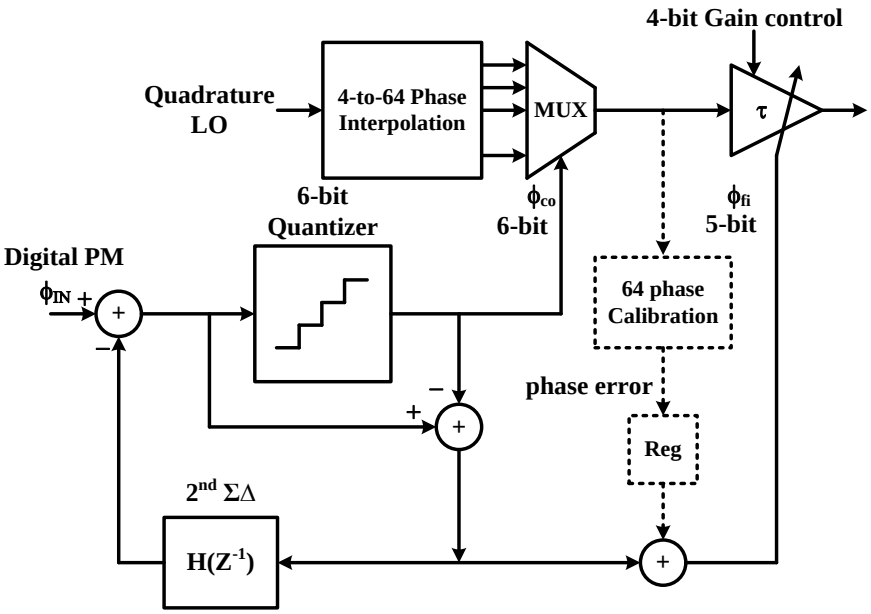


Fig. 5. 5 proposed phase interpolated digital phase modulator

5.3.1 Implementation of the coarse segment

Fig. 5.6 shows the coarse segment of the phase modulator. It is composed of a 3-steps 4-to-32 phase interpolator and a 64-phases selection MUX with 32 phases input.

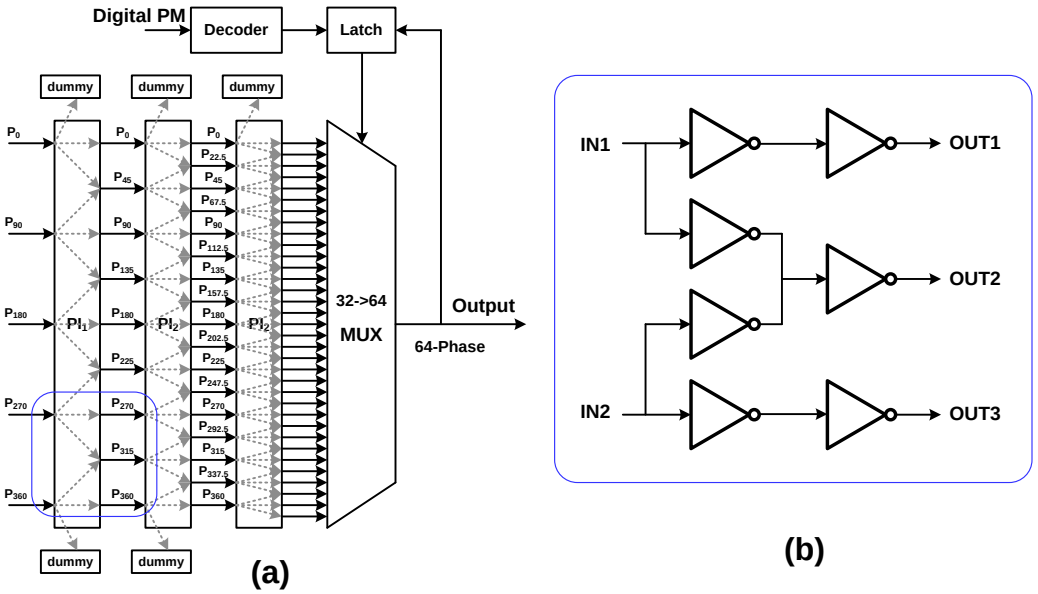


Fig. 5. 6 coarse segment of the phase modulator (a) Block diagram and (b) PI-cell

The 64-phases selection MUX is shown in Fig. 5.7(a). It contains a LC tank and 64 switch transconductance (gm) cells with every 2 cells connected to one of the 32 input phases. The operation of this MUX can be explained as: if P_0 is selected to the output, then the 2 gm cells with P_0 as their input are on, and the other gm cells are off. If $P_{0.5}$ is selected to the output, then one P_0 gm cells and one P_1 gm cells are on, the other gm cells are off. With this operation, the phase modulator achieves 64 output levels with 32 phase input.

The amplitude mismatch due to the phase interpolation MUX is shown in Fig. 5.7(b). The error is only 2% and the AM-PM distortion can be ignored.

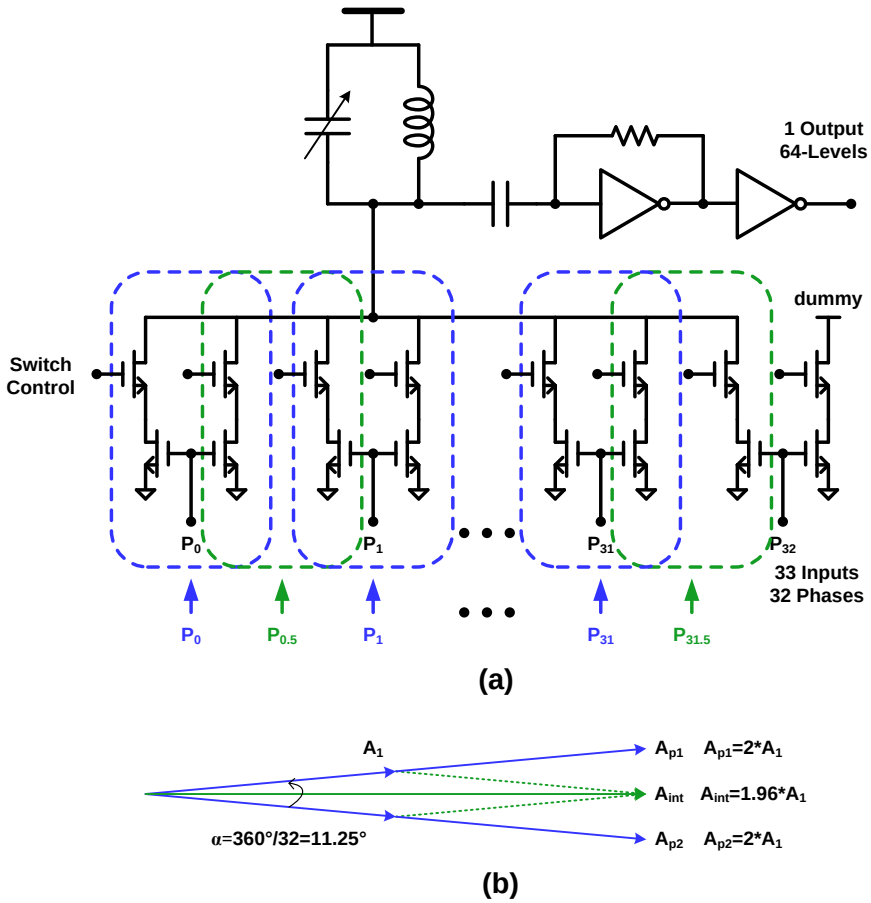


Fig. 5. 7 64-phases selection MUX (a) Implementation and (b) amplitude mismatch

5.3.2 Implementation of the fine segment

Fig. 5.8 shows the implementation of the fine-tune segment [5.8]. Fine resolution phase tuning can be achieved by tuning the digitally controlled loading capacitor. For the different gain setting, the driving capability of the buffer-array can be programmable by on/off sub-set of the buffer cells.

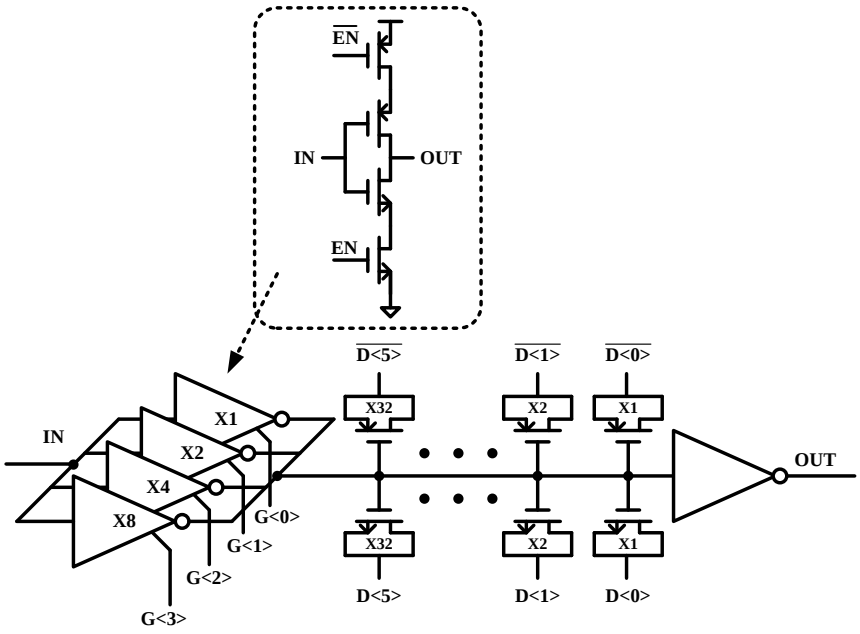


Fig. 5. 8 fine segment of the phase modulator

5.4 ALL-Digital Phase Calibration

Fig. 5.9 shows the blocks diagram of the all digital phase calibration [5.9]. We use 8-phase as an example to explain its operation principle. The 8-phase signals from the frequency synthesizer drive the phase tunable buffer and go to two 8-to-1 MUXs. The output of MUX1 drives a fixed-delay buffer before the TDC input1 while the second one goes directly to the TDC input2. The TDC converts the time delay between the two inputs to digital. An off-chip FPGA receives the TDC output and generates the control signals for the MUXs and phase tuning buffers.

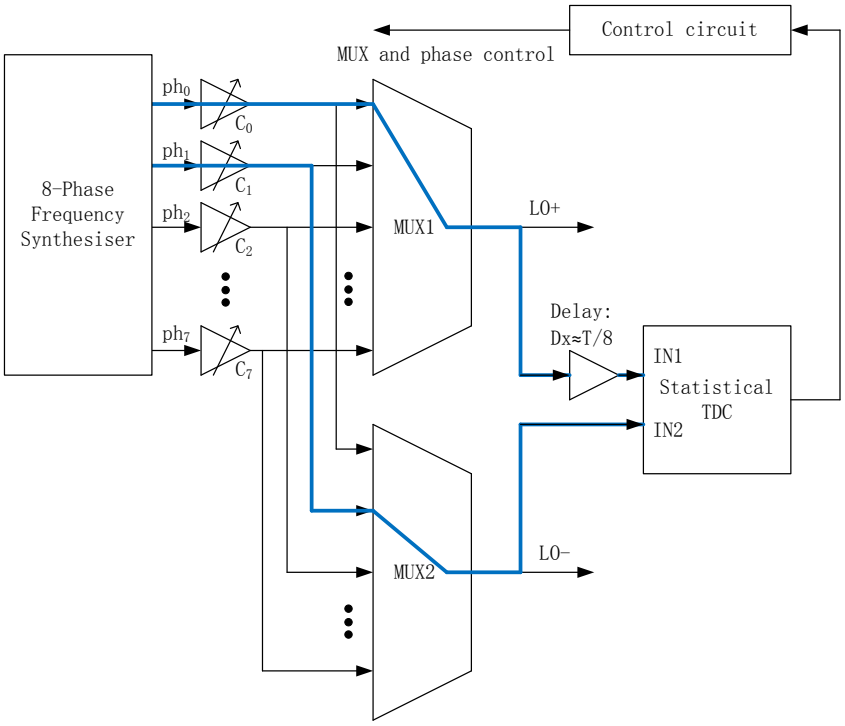


Fig. 5. 9 Blocks diagram of the phase selection and calibration

As the phase sequences are known, we can select the phase to the output of MUX1 always lead to MUX2. By inserting a fix delay with around 1/8 period between MUX1 and IN1 of the TDC, the phase different at the TDC inputs is reduced, so the TDC input range can be minimized to optimize its resolution. Fig. 24 shows the operation principle of the calibration. First, we select phase ph_0 and ph_1 to the output of MUX1 and MUX2; then we have a TDC output TO_0. The actual phase different between ph_0 and ph_1 is $D_0=D_X+TO_0$; we use the same method and measure D_1, D_2 … D_7. We calculate the average phase to be:

$$D_{avg}=\frac{D_0+D_1+...D_7}{8}=D_X+\frac{TO_0+TO_1+...TO_7}{8} \tag{5.6}$$

We define TO_{avg} to be:

$$TO_{avg}=\frac{TO_0+TO_1+...TO_7}{8} \tag{5.7}$$

After that, we select phase ph_0 and ph_1 to the TDC again, and control the phase tuning buffer C_1 to let the TDC output to be TO_{avg}. By repeating this process, all phases can be calibrated. The phase accuracy after calibration depends on the resolution of the TDC and the phase tuning buffers.

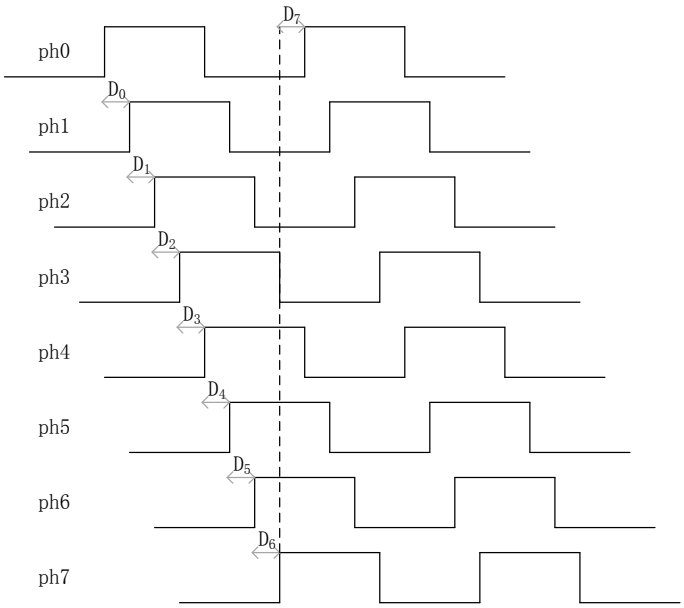


Fig.5.10 8-phase to be calibrated

Bibliography

[5.1] Shih-An Yu; Kinget, P. "A 0.65-V 2.5-GHz Fractional-N Synthesizer With Two-Point 2-Mb/s GFSK Data Modulation," *IEEE J. Solid-State Circuits*, vol. 44, no. 9, pp. 2411 - 2425, Sep. 2009.

[5.2] Temporiti, E.; et al., "A 3.5 GHz Wideband ADPLL with Fractional Spur Suppression through TDC Dithering and Feedforward Compensation," *IEEE J. Solid-State Circuits*, vol.45, no.12, pp. 2723 - 2736, Dec. 2010

[5.3] Liangge Xu; et al., "A 2.4-GHz Low-Power All-Digital Phase-Locked Loop," *IEEE J. Solid-State Circuits*, vol.45, no.8, pp. 1513 - 1521, Aug. 2010

[5.4] Staszewski, R.B.; et al., "Spur-Free Multirate All-Digital PLL for Mobile Phones in 65 nm CMOS," *IEEE J. Solid-State Circuits*, vol.46, no.12, pp. 2904 - 2919, Dec. 2011

[5.5] Temporiti, E.; et al., "A 3 GHz Fractional All-Digital PLL With a 1.8 MHz Bandwidth Implementing Spur Reduction Techniques," *IEEE J. Solid-State Circuits*, vol.44, no.3, pp. 824 - 834, Mar. 2009

[5.6] Giovanni Marzin, et al., "A 20 Mb/s Phase Modulator Based on a 3.6 GHz Digital PLL With −36 dB EVM at 5 mW Power," *IEEE J. Solid-State Circuits*, vol. 47, no. 12, pp. 2974 - 2988, Dec. 2012.

[5.7] Staszewski, R.B.; et al., "All-digital TX frequency synthesizer and discrete-time receiver for Bluetooth radio in 130-nm CMOS," *IEEE J. Solid-State Circuits*, vol. 39, no. 12, pp. 2278 - 2291, Dec. 2004.

[5.8] Madoglio, P.; et al., "A 20dBm 2.4GHz digital outphasing transmitter for WLAN application in 32nm CMOS," *IEEE ISSCC* Dig. Tech. Papers, pp. 168-170, 2012

[5.9] Stefano Pellerano, et al., "A 4.75-GHz Fractional Frequency Divider-by-1.25 With TDC-Based All-Digital Spur Calibration in 45-nm CMOS," *IEEE J. Solid-State Circuits*, vol. 44, no. 12, pp. 3422–3433, Dec. 2009.

CHAPTER 6 High-Linear Digital Polar Modulator and Power Amplifier

6.1 Introduction to Digital Polar Transmitter

With recent advances in CMOS technologies, integrating RF transceivers with digital baseband and application processor into a single chip has become feasible and attractive [6.1]-[6.5]. Such sing-chip integration offers many advantages including: 1) increased system performance, 2) smaller form factor, 3) cost reduction due to smaller bills of material, and 4) lower power and longer battery life. However, in implementing single-chip RF transceivers, designing of power amplifier (PA) still remains the most challenging [6.6]-[6.10] not only because the PA tends to disturb the sensitive blocks such as VCO and LNA [6.11] but also because it requires large output power and high efficiency. Moreover, for high data-rate communication with high spectrum efficiency, non-constant envelope modulation with large peak-to-average ratio (PAR) are used, such as quadrature amplitude modulation (QAM), orthogonal frequency division multiplexing (OFDM), and quadrature phase shift keying (QPSK) with root-raise cosine filtering. These applications require the PA to have sufficient linearity to meet their stringent specification.

In contrast, transistors in deep-submicron CMOS processes have poor linearity of transconductance and output impedance. Moreover, low supply voltages due to the transistors' low break-down voltage would inevitably limit the output power and degrade the linearity. As a result, an on-chip integrated CMOS PA usually achieves inferior performance compared to external PAs implemented in non-CMOS processes.

On the other hand, digital signal processing in scaled CMOS technologies becomes more powerful due to the increase of the device switching speed and the logic gate density. More and more research efforts have focused in digitally intensive RF design [6.1]-[6.5] because of its high programmability for multi-standard operation and its capability to repair RF impairments and improve RF performance by digital calibration.

Digital polar transmitter [6.13]-[6.19] is a good example. As illustrated in Fig. 6.1, the Cartesian I and Q input signals are converted to polar coordinates according to:

$$A(t) = \sqrt{I(t)^2 + Q(t)^2} \tag{6.1}$$

$$\phi(t) = \tan^{-1}\left(\frac{Q(t)}{I(t)}\right) \tag{6.2}$$

where $A(t)$ and $\phi(t)$ are the envelope and the phase of the transmitted signals.

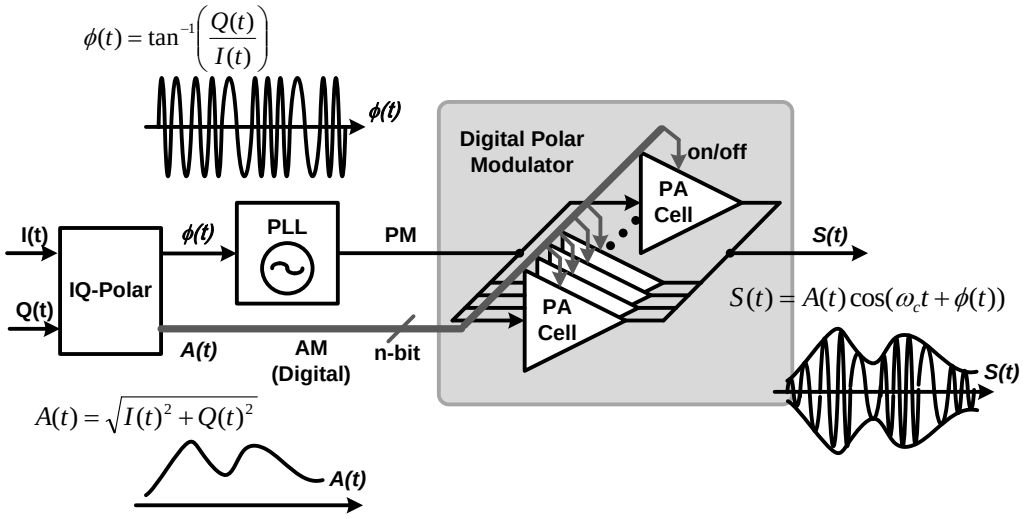


Fig. 6. 1 Block diagram of a typical digital polar modulator architecture

Normally, for phase modulation (PM), a phase-locked loop (PLL) can be used to modulate the output phase of the carrier. On the other hand, for amplitude modulation (AM), a digital polar modulator (DPM) employs an array of PA cells to amplify the PM

carrier and performs AM by tuning on or off a sub-set of the PA cells according to the input digital amplitude-control word (ACW) [6.13][6.14]. Compared to a traditional supply modulator [6.9], DPM is more compatible with digital processes and achieves much higher integration level. Furthermore, for DPM, wider modulation bandwidth can be obtained by over-sampling, and the time delay mismatch between the AM path and PM path can be well controlled by digital circuits. However, the non-linearity in the AM path due to the code-dependent impedance of the PA cells would cause AM-AM and AM-PM distortions. These distortions together with PM-PM distortions in the PM path significantly degrade the accuracy of the transmitted signals.

Solutions have been demonstrated to improve the DPM linearity such as close-loop polar architecture [6.8][6.15] and digital pre-distortion [6.2][6.13][6.14]. The close-loop polar transmitter is shown in Fig. 6.2(a). The PA output is down-converted with proper gain control. The phase and amplitude are then extracted and compared with the modulated signal to regulate the PA. With these feedback loops, the PA is linearized and becomes insensitive to variations in the load, temperature, supply, etc. However, the feedback techniques of [6.8] and [6.15] increase the implementation complexity, occupy larger chip area, and consume larger power. In addition, due to the stability issues, the modulation bandwidth is limited. For the digital pre-distortion solution shown in Fig. 6.2(b), the non-linearity of the PA will be measured by the receiver and stored in a look-up table (LUT) during the calibration stage. The input signal is pre-distorted accordingly to compensate for the measured non-linearity. Although the receiver can be reused within the transceiver, the LUT and the signal processing circuits required for the pre-distortion still significantly affect the overall system cost, especially when the transmitter needs to be operated in a wide range of changing conditions including the

variations of temperature, output power, and PA aging. Finally, the effectiveness of the pre-distortion technique highly depends on the linearity of the receiver and thus is typically limited.

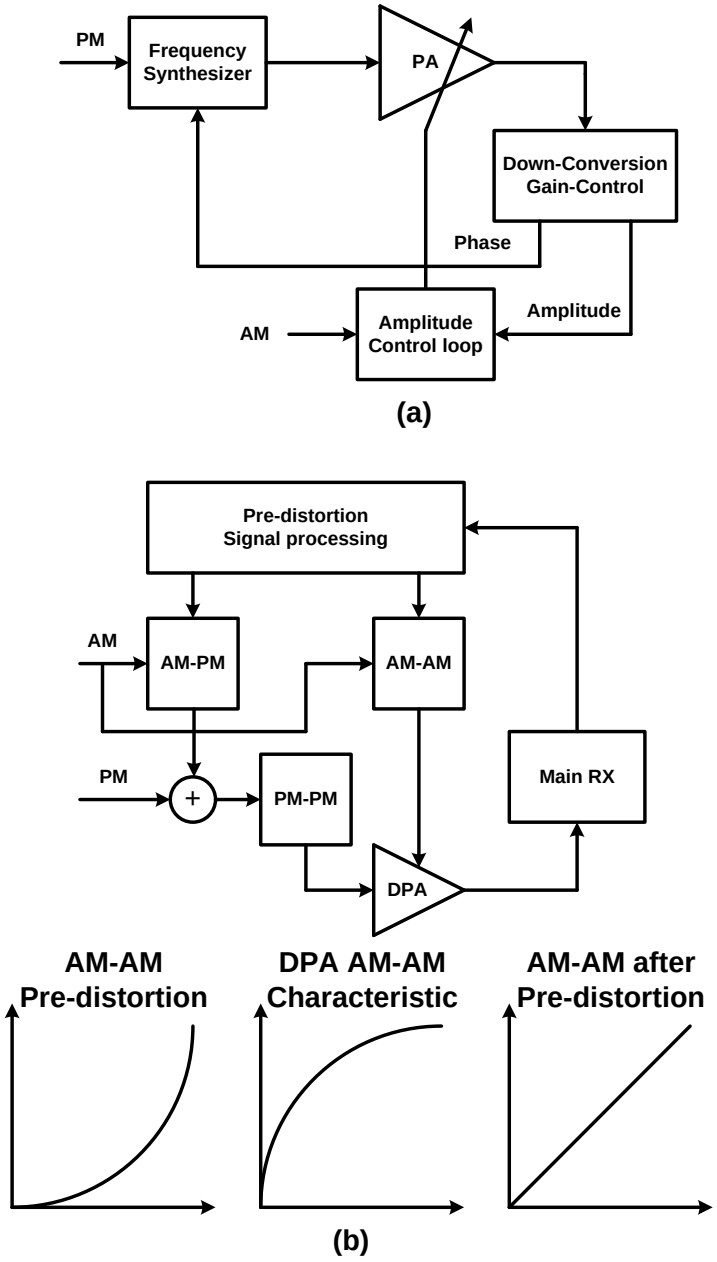


Fig. 6. 2 existing transmitter linearization techniques (a) close-loop transmitter and (b) digital pre-distortion

In this chapter, an amplitude linearization technique for digital polar transmitters is

proposed and demonstrated to eliminate the amplitude pre-distortion. The paper is organized as follows. Section II describes the proposed digital polar transmitter architecture with the proposed linearization technique. Section III presents the design considerations and the circuit implementations of the critical building blocks, including the digital polar modulator, the power amplifier, and the digital interpolation filter. Experimental results are discussed in Section IV, and conclusion is given in Section V.

6.2 Proposed Polar Transmitter Architecture

6.2.1 Non-Idealities Effect of Switched-Current DPM

Switched-current technique [6.1][6.2][6.13] and [6.14] is widely used for the DPM and its operation principle is illustrated in Fig. 6.3 The transistors at the bottom convert the phase-modulated LO carrier to current while the cascode transistors are controlled by the input digital amplitude-control word (ACW) to turn on and off corresponding current sources to reconstruct the RF envelope with good efficiency. A transformer is added between the output of the current sources and R_L to provide proper impedance transformation to achieve high output power.

Due to the finite AM resolution, the quantization error generates white noise and corrupts the spectral purity. As a result, the number of bits in a DPM is determined by the spectral mask of the target standards, and normally some extra bits are added for AM-AM pre-distortion and power control. Additional power control can be obtained by tuning the output amplitude of the PM carrier's buffers.

The DPM architecture shown in Fig. 6.3 is simple but suffers from a problem of nonlinearity, which causes AM-AM and AM-PM distortions and is responsible for

spectral regrowth and non-zero error-vector-magnitude (EVM). The AM-AM distortion is mainly due to the finite output resistance of the DPM. The output voltage V_{OUT} of the DPM can be expressed as:

$$V_{OUT} = V_{LO} * ACW * G_{mo} * (\frac{R_L}{N^2} \| \frac{R_{D0}}{ACW}) * N \tag{6.3}$$

where V_{LO} is the LO carrier amplitude, G_{m0} and R_{D0} are the equivalent transconductance and the output resistance of one LSB cell, R_L is the load resistance, and N is the transformer's turn ratio. Although the cascode device M_{20} is used to increase the output impedance, large swing of V_{OUT} would cause it to enter the triode region and degrade the improvement. Another problem is the code-dependent parasitic capacitance. For example, the input capacitance C_{IN} can be written as:

$$C_{IN} = ACW * C_{G0\_ON} + (2^n - 1 - ACW) * C_{G0\_OFF} \tag{6.4}$$

where C_{G0_ON} and C_{G0_OFF} are the gate capacitances of the LSB cells that are selected to be on and off, respectively, and n is the number of bits in the DPM. It is clear that C_{IN} changes as a function of ACW, which generates not only the load-pull effect of the VCO but also AM-PM distortion.

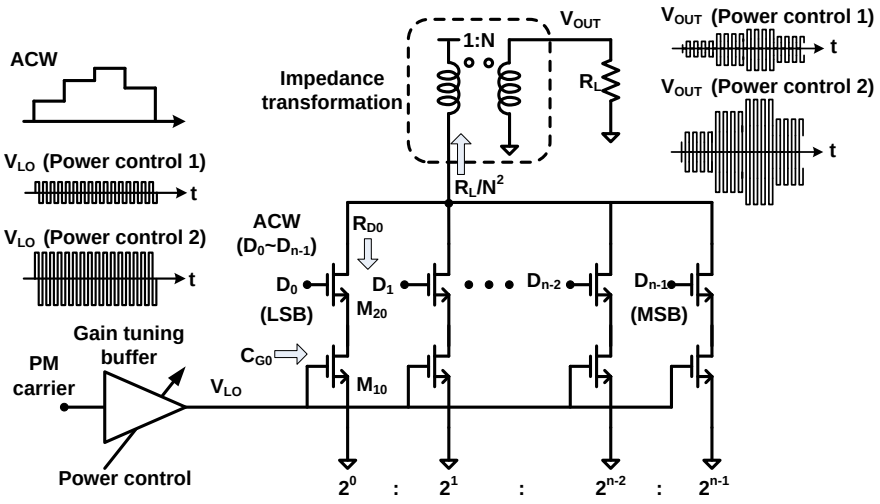


Fig. 6. 3 Illustration of the operation of the switched-current DPM

6.2.2Proposed Digital Transmitter Architecture

To reduce the AM-AM distortion without using pre-distortion, the output resistance of the PA cells should be increased, which can be accomplished by increasing the channel length of the transistors, but the gate capacitance would also be increased and the AM-PM distortion would get worse. Another way to improve the output resistance is to use negative feedback regulation. However, it cannot be operated directly at RF frequencies. In addition, constant input and output capacitance values are also required to minimize the AM-PM distortion.

In this work, a novel digital polar transmitter architecture is proposed to solve these problems. As shown in Fig. 6.4, the 9-bit ACW is first up-sampled by a digital interpolation filter to push the digital sampling image far away not to affect the desired RF spectrum. Instead of using switched-current DPM, a highly linear charge-mode switched-capacitor DPM is employed to modulate the amplitude of the PM carrier according to ACW and to provide constant input and output capacitance. To achieve the desired output power range for the target applications, the DPM output is amplified by a 6-bit PA array with an AM-adaptive bias for linearization. To generate this bias, the RF envelope of the PA input is extracted by a DAC which converts the input digital ACW to analog. A replica of the PA which only needs to operate at the AM frequency senses the RF envelope and regulates the output bias with an analog feedback loop to minimize the distortion in the AM path.

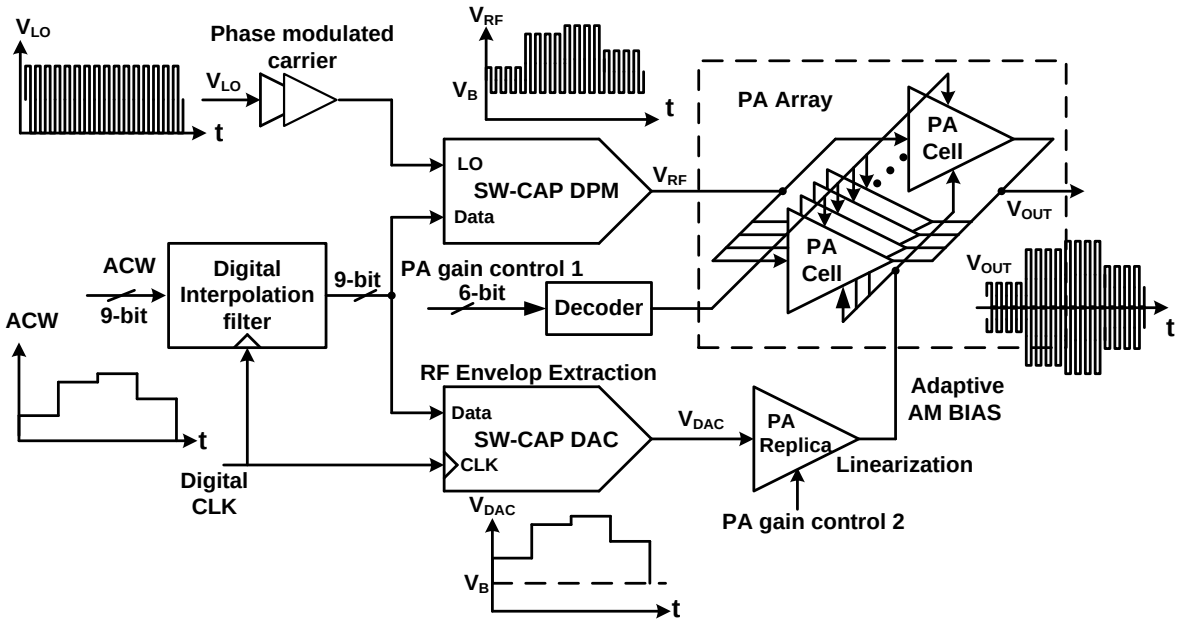


Fig. 6. 4 Block diagram of the proposed digital polar transmitter

6.3 Circuit Implementation

6.3.1 Switched-Capacitor Digital Polar Modulator (SC-DPM)

With CMOS technologies being aggressively scaled, the switched-capacitor technique can be applied for RF applications directly. A digital power amplifier employing switched-capacitor technique (SCPA) was demonstrated in [6.17]. Compared to the switched-current DPA, the SCPA does not require any voltage headroom so the output signals can be maximized from rail to rail. In addition, capacitors in CMOS processes not only are area-efficient but also have good matching with good layout techniques. Fig. 6.5 shows the operation principle of a SCPA, which can be regarded as an AC-voltage capacitive-division network. The AND gates select and connect an appropriate set of capacitors C_a to the PM carrier V_{LO} with a fixed amplitude while

connecting the rest of the capacitors C_b to GND. As such, the phase of the SCPA output is the same as the phase of V_{LO}, but its amplitude is modulated by ACW. To generate high output power, a matching network at the top-plate of the capacitors transforms the impedance of the antenna to R_{opt}. This matching network also provides band-pass filtering for the modulated signal. Since the top-plate capacitance is constant versus ACW, the frequency response of the band-pass matching network is not affected by ACW.

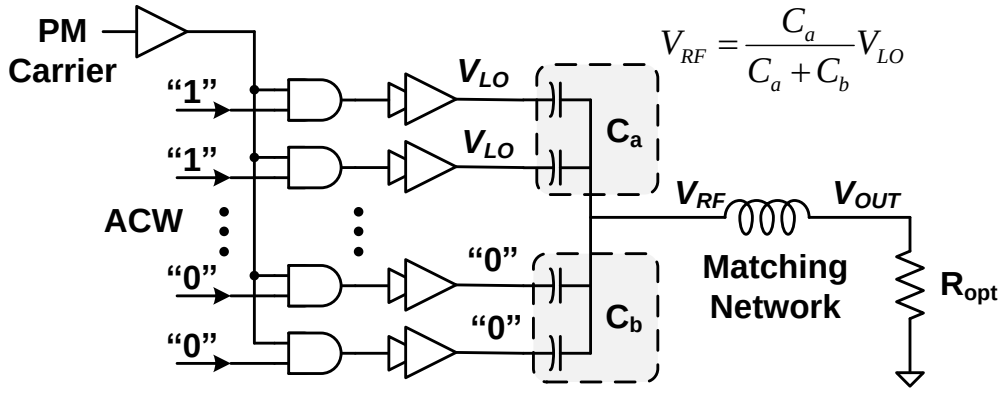


Fig. 6. 5 Block diagram of the SCPA [6.17]

To further enlarge the output power, cascode switches are employed so that the V_{DD} can be increased to twice of the standard supply voltage [6.17]. Like a Class-D PA, the turn-on resistances of the switches in SCPA need to be much lower than R_{opt}. Consequently, the size of the switches needs to be very large (especially for the PMOS transistors), and driving these large switches at the RF frequency would consume large power. Moreover, the effective source resistance seen from the output matching network is code-dependent if there is a mismatch of the turn-on resistances of the PMOS and NMOS switches. Such effect degrades the SCPA linearity and generates AM-AM and AM-PM distortion. Lastly, the power control provided by the SCPA is limited because

the amplitude of the V_{LO} has to be rail-to-rail.

To provide the power control for the application and to improve the linearity, a common-source programmable-gain PA is inserted between the SC-DPM and the matching network. The simplified circuit implementation is shown in Fig. 6.6(a). Since the SC-DPM does not need to deliver high output power, a simple digital inverter can be used for the switch to reduce the power consumption and to improve the linearity. To minimize the distortion of the whole system, the transistors M_{1A} and M_{1B} should be designed to have not only constant gate capacitance and transconductances but also high output resistance over the entire RF envelope amplitude range. The linearization technique for this common-source PA will be discussed in detail in the next section.

As shown in Fig. 6.6(a), when the output voltages of SC-DPM, V_{RF+} and V_{RF-}, are lower than the threshold voltages of M_{1A} and M_{1B}, the PA does not generate any output current and wastes the signal swing of the SC-DPM. To generate the gate bias voltage for M_{1A} and M_{1B}, a reset signal RST shown in Fig. 6.6(b) is created to pull V_{RF} to V_B when V_{LO} becomes low. So, V_{RF} can be level-shifted by V_B and expressed as:

$$V_{RF} = \frac{ACW * C_0}{C + C_{IN}} * V_{LO} + V_B \tag{6.5}$$

where C_0 is the unit capacitance of the LSB cells, C is the total input capacitance of the SC-DPM, and C_{IN} is the input gate parasitic capacitance of the common-source PA. Because C_{IN} varies with the RF envelope amplitude, C is designed to be much larger than the maximum variation to achieve good linearity, but the power required to charge and discharge the capacitors is also larger:

$$P_{SC} = ACW * C_0 * f_{LO} * V_{DD}^{\ 2} \tag{6.6}$$

where P_{SC} is the dynamic power of the switched capacitors and f_{LO} is the LO carrier

frequency. The value of *C* is designed to be 3.6pF to optimize the power consumption and the linearity.

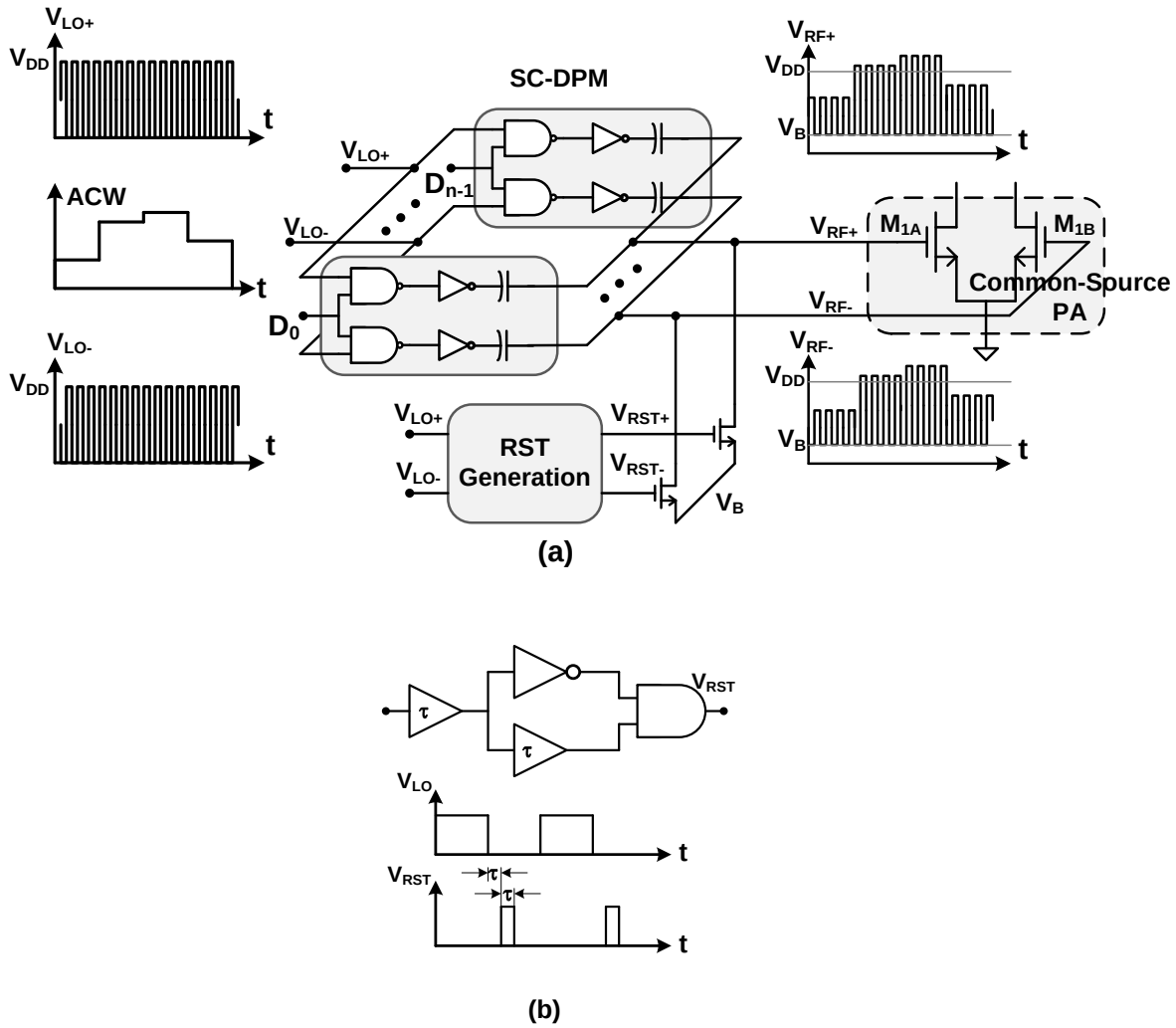


Fig. 6. 6 Block diagram of (a) the proposed SC-DPM, and (b) its RST generation circuit

To linearize the following common-source PA, the envelope of V_{RF} is extracted by a switched-capacitor DAC (SC-DAC), which is shown in Fig. 6.7. During $\phi 1$, the input ACW is sampled, and, during $\phi 2$, the charge of the capacitors is re-distributed to generate the desired output voltage. Both SC-DPM and DAC are designed to be 9 bits each with 6 thermometer-coded MSBs and 3 binary-coded LSBs. Since this DAC is synchronized with the DPM by using the same digital clock, both are designed to have

the same transfer function as shown in Eq. (6.5) to minimize the amplitude mismatches.

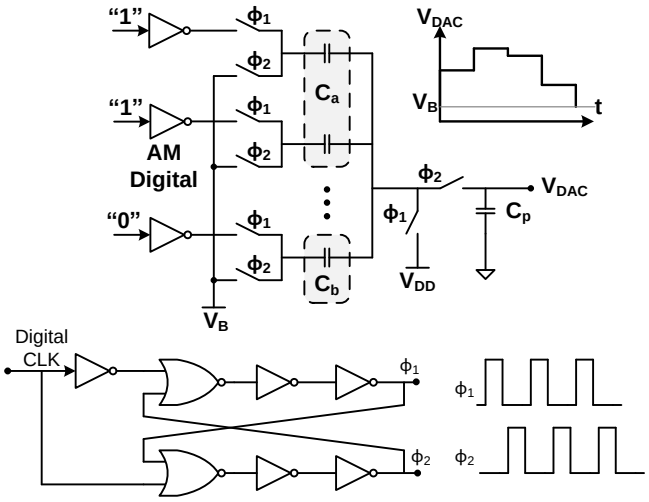


Fig. 6. 7 Schematic of the proposed SC-DAC circuit

6.3.2 Proposed PA with Linearization

An on-chip PA-array, as shown in Fig. 6.8, is added after the SC-DPM to achieve the desired gain control and output power. It operates in the Class-AB mode to optimize the linearity and efficiency. The transistors M_{1A}, M_{1B}, M_{2A} and M_{2B} form a differential cascode common-source PA, and its output is connected to an on-chip transformer which provides both output impedance transformation and differential-to-single-ended conversion. The cascode devices M_{2A} and M_{2B} are implemented using thick-gate-oxide transistors with the minimum gate length of 280nm so that it can operate at 2V V_{DD} to enlarge the output power.

To achieve high linearity, the common-source PA is desired to have constant transconductance and constant input capacitance for M_{1A} and M_{1B} over the whole amplitude range of the RF envelope. At the same time, the output resistance of M_{2A} and M_{2B} should be high. All these requirements can be achieved with the proposed AM replica linearization feedback techniques shown in Fig. 6.8. The transistors M_{1C} and

M_{2C} together with the opamp A_1 and the resistor R_C form a scaled replica of the main PA. By sizing M_{1C} and M_{2C} to be 1/k of M_{1A} and M_{2A} and choosing R_C to be k times of the effective loading resistance R_{eff}, a scaling ratio of 1:k is achieved.

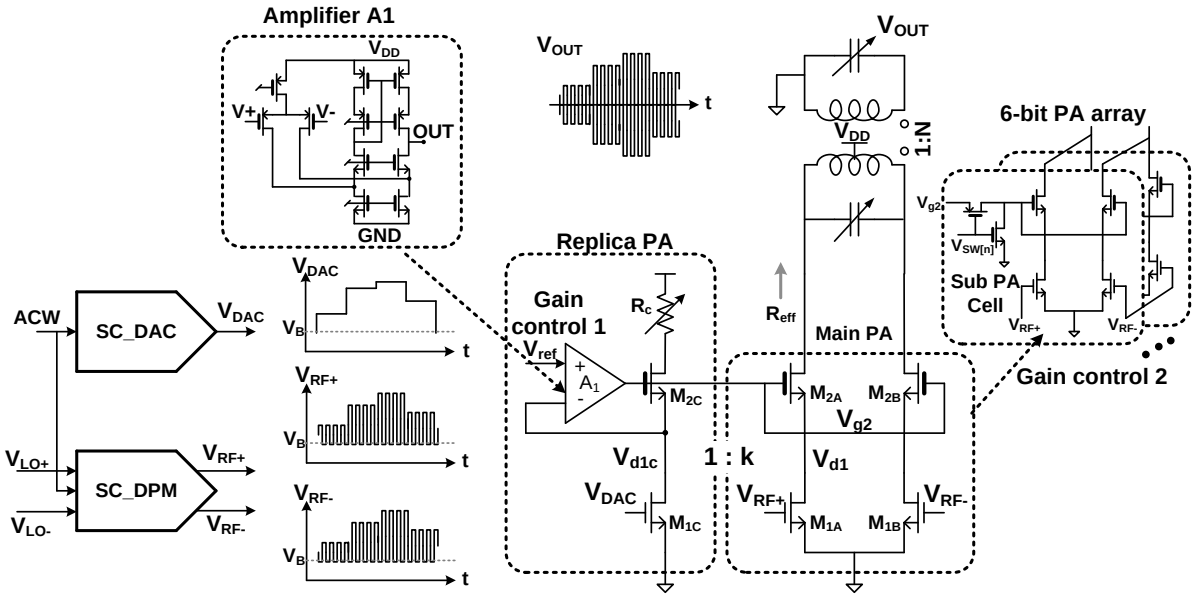


Fig. 6. 8 Schematic of the proposed PA with AM replica linearization

The DC operating point of the replica PA and the main PA are set by the bias voltage V_B from the SC-DAC and DPM. With M_{1C} being operated in the linear region, the opamp A_1 ensures that V_{d1C} is equal to V_{ref} to keep transconductance G_{M1C} of M_{1C} to be a constant value given by:

$$G_{M1C} = \mu C_{ox} \frac{W}{L} V_{REF} \tag{6.7}$$

Consequently, the replica PA is linearized. By applying V_{DAC} to the gate of M_{1C}, the cascode bias V_{g2} is changed according to the envelope of V_{RF} to stabilize transconductance of M_{1A} and M_{1B} as:

$$G_{M1} = k * G_{M1C} = k\mu C_{ox} \frac{W}{L} V_{REF} \tag{6.8}$$

Regarding the input capacitance, the PA can be modeled as shown in Fig. 6.9(a). The channel charge of M_1 is lumped into 3 capacitors: gate-to-bulk capacitor (C_{gb1}), gate-to-source capacitor (C_{gs1}) and gate-to-drain capacitor (C_{gd1}). These capacitors are not constant because their values depend on the region of operation. As shown in Fig. 6.9(b), in the accumulation region, the gate-channel capacitance is equal C_{gb1}, $C_{gb1}=C_{OX}WL$, and $C_{gs1}=C_{gd1}=C_{overlap}=$ constant where $C_{overlap}$ is the overlapping capacitance between the gate and source/drain diffusion regions. However, when in the saturation region, $C_{gb1}=0$, $C_{gs1}=(2/3)C_{OX}WL$, and $C_{gd1}=C_{overlap}$. Moreover, when in the linear region, $C_{gb1}=0$, and $C_{gd1}=C_{gs1}=0.5C_{OX}WL$. Clearly, the total input capacitor has a variation from less than $0.5C_{OX}WL$ to $C_{OX}WL$ as V_{gs1} changes from GND to V_{DD}.

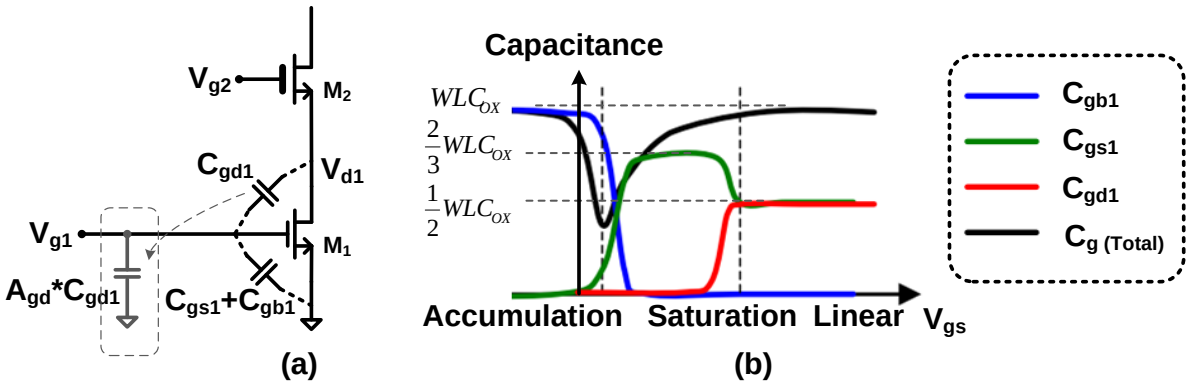


Fig. 6. 9 Common-source cascode PA: (a) schematic showing input capacitances, and (b) the input gate capacitance versus Vgs

For the PA shown in Fig. 6.9(a), when the cascade bias is fixed, the drain voltage V_{d1} of the transistor M_1 changes versus its input gate voltage V_{g1}. Whether M_1 operates in the saturation or the linear region depends on the amplitude of the RF envelope when M_1 is switched on. As a result, all the gate parasitic capacitance C_{gb1}, C_{gd1} and C_{gs1} are dependent on the input codes. Moreover, due to the Miller effect, C_{gd1} is amplified by the gain A_{gd1} between V_{g1} and V_{d1} when it is modeled as a capacitor between V_{g1} and

GND. Since the A_{gd1} changes with the input gate voltage, the variation of the total input capacitance becomes larger. With the AM replica feedback, M_1 is fixed in the linear region with a constant V_{d1} when it is switched on, which not only eliminates the Miller effect but also keeps the capacitances C_{gb1}, C_{gd1} and C_{gs1} constant. Consequently, the total input capacitance remains constant. In addition, the output resistance of the main PA is increased by the gain of the amplifier A_1, which further improves the linearity.

Fig. 6.10 and Fig. 6.11 show the simulation results of the input transconductance and the input capacitance of the main PA versus the ACW. Obviously, without linearization, the PA's transconductance G_M varies from 710μS to 38μS, and the input capacitance C_{IN} varies from 2.55pF to 1.96pF. In contrast, with the proposed linearization technique, the variation of the G_M is from 451uS to 372uS while the variation of C_{IN} is from 1.93pf to 1.98pf.

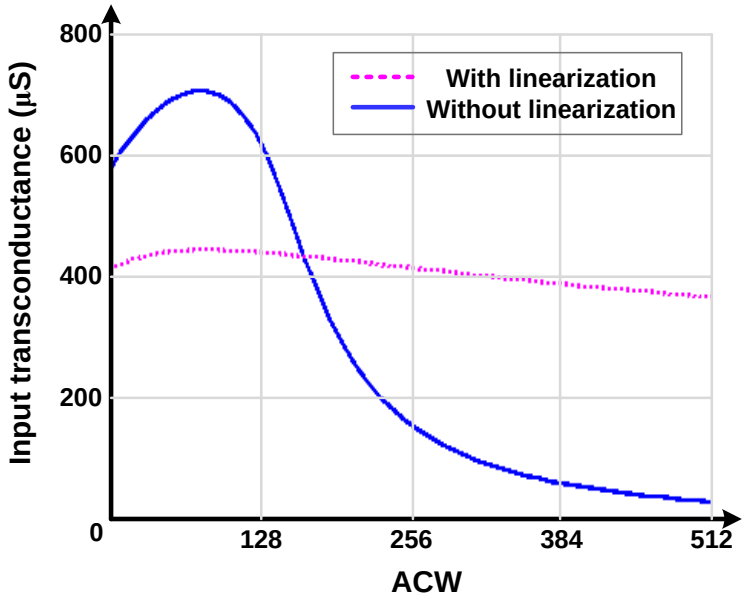


Fig. 6. 10 Simulated PA input transconductance versus ACW

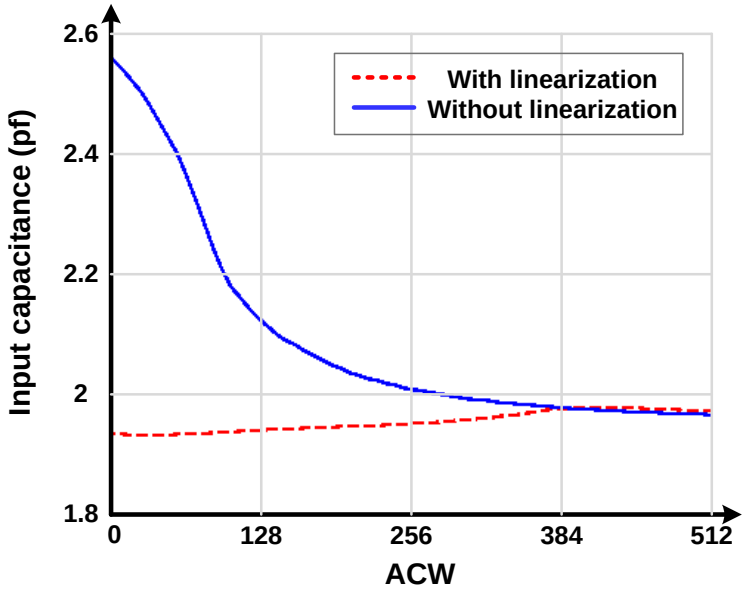


Fig. 6. 11 Simulated PA input capacitance versus ACW

The gain of the PA is controlled by tuning the bias voltage V_{ref} and turning on and off the 6-bit sub-PA cells according to the gain control word (GCW). The 4 MSBs control 16 unit-weighted PA cells while the 2 LSBs are binary-weighted. The total gain control range of the PA-array is 76dB with 1dB step. According to the Eq. (6.5) and (6.8), the final output voltage V_{OUT} of the proposed digital polar transmitter system, including the SC-DPM and the PA, can be written as:

$$\begin{aligned} V_{OUT} &= V_{RF} * G_{M1} * (R_{OUT} \parallel R_{eff}) * N \\ &= \left(ACW * V_{LO} \left(\frac{C_0}{C + C_{IN}} \right) \right) * GCW * \mu C_{ox} \left(\frac{W}{L} \right)_{unit} V_{REF} * (R_{OUT} \parallel R_{eff}) * N \end{aligned} \quad (9)$$

where C_{IN} is the input gate capacitance of the main PA, $(W/L)_{unit}$ represents the unit size of M_1 controlled by every LSB of GCW, R_{OUT} is the output resistance of the main PA, and N is the transformer turn ratio. High linearity can be ensured by designing C and R_{OUT} to be much larger than the variation of C_{IN} and R_{eff}, respectively.

6.3.3 Digital Interpolation Filter

Fig. 6.12 shows the block diagram of the digital interpolation filter [6.20]. It consists of a cascade of four finite-impulse-response (FIR) filters to provide a programmable up-sampling ratio of 1, 2, 4, 8 and 16.

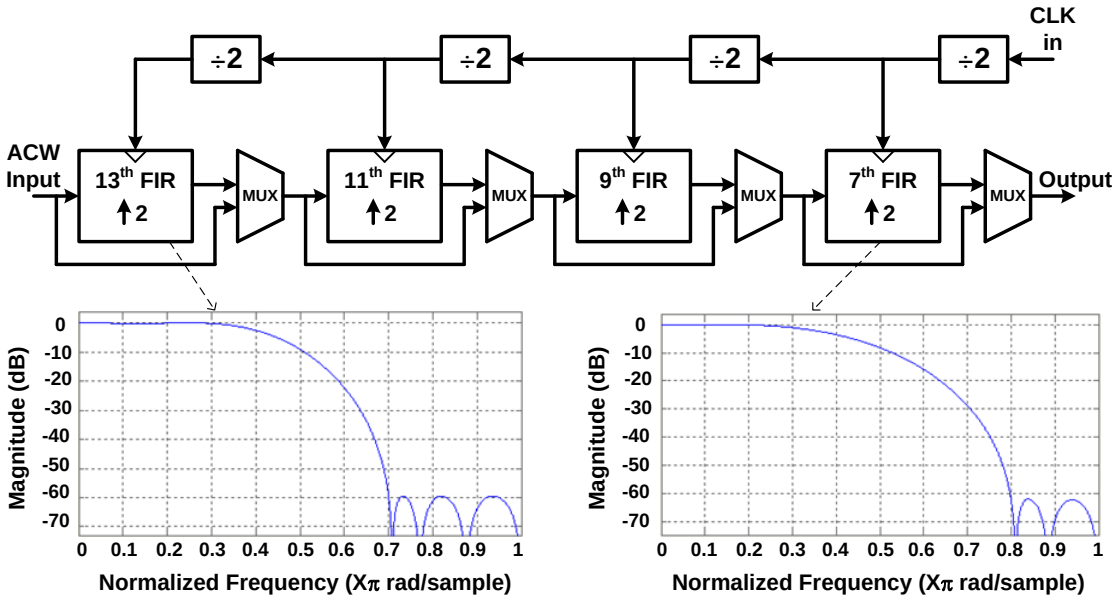


Fig. 6. 12 Block diagram of the proposed digital interpolation filter

Each stage of the filter is driven by a clock signal progressively divided from an external clock with the maximum frequency of 640MHz. For the first stage, a 13^{th}-order FIR is used which has a pass-band corner of 0.3 and stop-band edge of 0.7 normalized to its sampling frequency. The pass-band has a ripple less than 0.5dB while the stop band provides around 60dB attenuation. Its implementation is shown in Fig. 6.13. It uses a direct-form-FIR structure with symmetrical coefficients to reduce the number of multiplications. To further reduce the power consumption and optimize the operation speed, the filter coefficients are decomposed to sums of multiples of 2 so that the multiplication can be implemented by the shift-and-add operations only. For the later

stages, since the frequency spacing between the signal band and the image becomes larger, the filter transition band can be relaxed, and the filter order can be reduced. The orders of the 2^{nd}, 3^{rd} and 4^{th} FIR filter stages are designed to be 11^{th}, 9^{th}, and 7^{th}, respectively, to reduce the chip area and power consumption. Each filter stage is also designed with a bypass mode so that the up-sampling ratio is programmable for different input sampling rates.

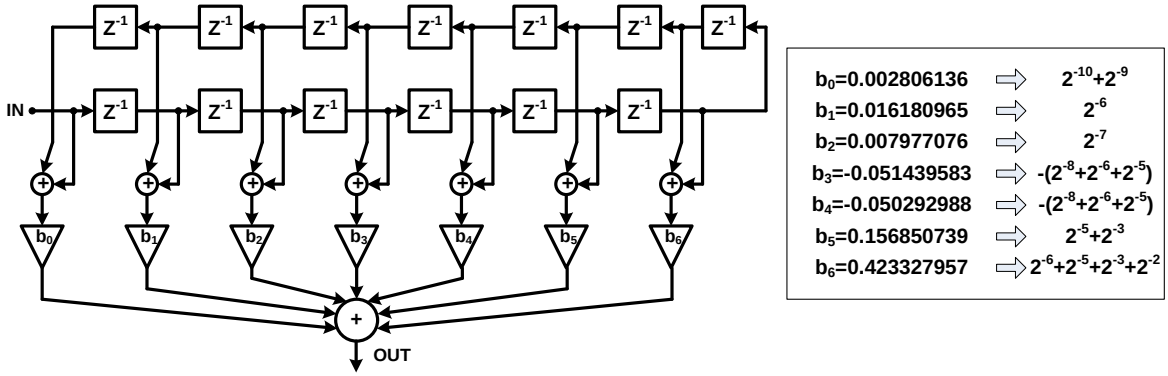


Fig. 6. 13 Implementation of the first-stage FIR filter

6.4 Measurement Results

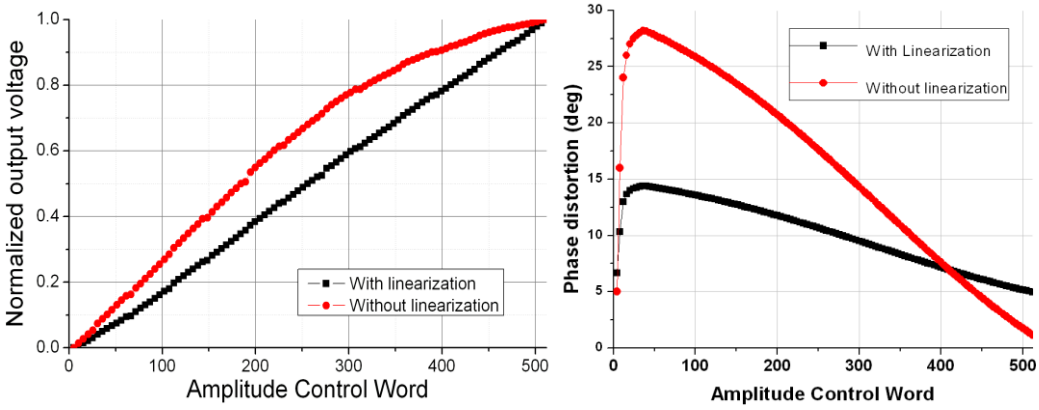
The digital polar transmitter was fabricated in a 65nm 1P6M CMOS process. The digital filters and the DAC consume 4mA, and the DPM together with the LO buffers consume 18mA at 1.2V while the PA-array consumes 14mA at 2V when delivering 0dBm to the output. The power consumption break down is summarized in Table I.

To verify the effectiveness of the AM replica feedback regulation technique in improving the PA linearity, the replica PA can be disabled while biasing M_{2A} and M_{2B} with a fixed voltage. Fig. 6.14 shows the measured static AM-AM and AM-PM transfer characteristic. Without the linearization, there is an AM-AM INL error of 18.6% and a

27.1° of AM-PM phase distortion because the PA's input transconductance and capacitance vary significantly with ACW. In contrast, with the linearization, the PA measures an AM-AM INL error of only 3.2% and an AM-PM distortion of 9.6° for a peak output power of 13.7dBm. As such, the AM-AM pre-distortion can be eliminated, and only AM-PM pre-distortion may be required. The measured peak output power and PAE values at different frequencies are shown in Fig. 6.15, which exhibits maximum output power of 20.4dBm at the maximum gain setting.

Table 6. 1 Power consumption break down when delivering 0dBm output power

Block	Supply Voltage [V]	Power Consumption [mW]
Digital Filter	1.2	2.5
SW-CAP DAC	1.2	2.5
DPM	1.2	10
LO Buffer	1.2	12
Replica Bias	2	12
PA array	2	16
Total	--	55mW



(a) (b)

Fig. 6. 14 Measured static transfer characteristic with 2GHz output and 13.7dBm peak output power: (a) AM-AM and (b) AM-PM

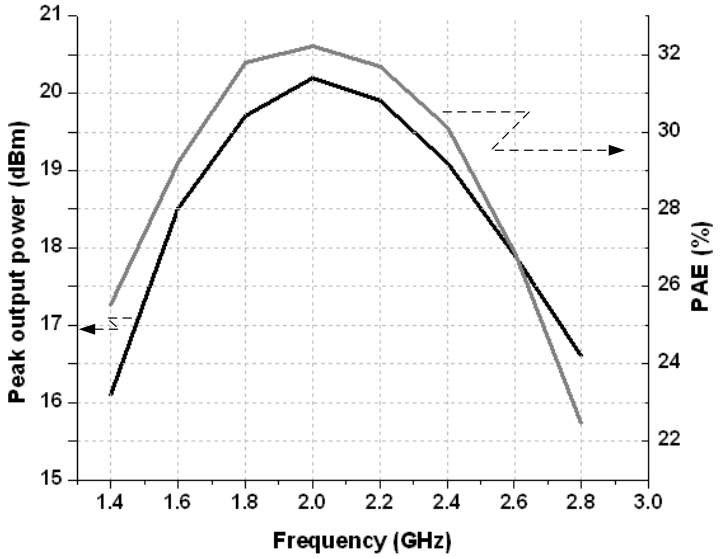


Fig. 6. 15 Measured peak output power and PAE as functions of the RF frequency

To measure the spectral mask and the EVM of the transmitted WCDMA and WLAN signals, a 16902A logic analyzer is used to generate the data patterns of the input ACW and phase signals. The 9-bit ACW signal is directly applied to the digital polar transmitter while the 10-bit phase signal is converted to an analog signal by a DAC ADV7127 and then modulates the RF signal generator to generate the phase-modulated carrier. The output of the transmitter is measured by an MXA signal analyzer N9020A. Fig. 6.16 shows the measured spectral masks and RMS EVM of 2.83% and 4.07% for WCDMA and WLAN 64-QAM OFDM signals, respectively. The measured performance is summarized and compared with existing state-of-the-art wideband digital polar transmitters in Table 6.2, from which it is clear that the proposed transmitter achieves comparable performance even without AM-AM pre-distortion. Fig. 6.17 shows the micrograph of the proposed transmitter which occupies an active area of 0.77mm2.

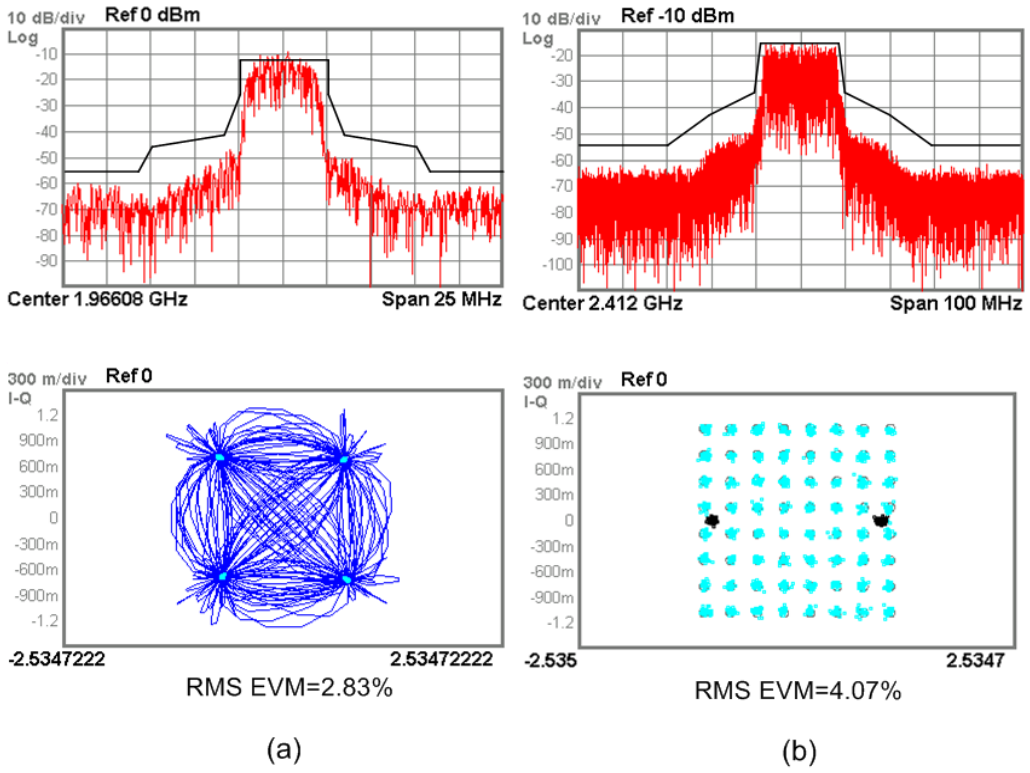


Fig. 6. 16 Measured spectral mask and EVM for: (a) WCDMA, and (b) WLAN 802.11g 54-Mb/s 64-QAM OFDM data

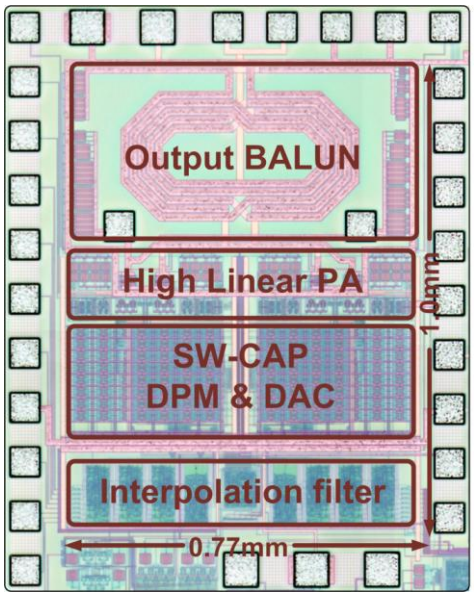


Fig. 6. 17 Die micrograph of the proposed transmitter

Table 6. 2 Performance summaries and comparison with other digital polar transmitters

Reference	This work	JSSC 09 Calogero [6.14]	JSSC 11 Sang [6.17]	JSSC 11 Chowdhury [6.18]
Technology	65nm CMOS	130nm CMOS SOI	90nm CMOS	65nm CMOS
Frequency [GHz]	1.5~2.7	0.8~2	1.8~2.8	~2.25
Supply Voltage [V]	1.2/2	1.2/2.1	1.5/3	1
Modulation	WCDMA 20M WLAN	EDGE WCDMA WiMax	20MHz WLAN	20MHz WLAN
AM-AM*	3%	41%	8%	44%
AM-PM*	9 °	24 °	50 °	17 °
Amplitude Pre-distortion	No	Yes	Yes	Yes
EVM (RMS)	2.8% (WCDMA) 4.1% (WLAN)	1.53% (5MHz-WiMax)	2.6%	4%
Output Matching Network	On-chip	Off-chip	Off-Chip	On-Chip
Peak output power **[dBm]	20.4	25	25.2	21.7
Peak PAE**	32.3%	47%	45%	36%
TX Power Control [dB]	76	>70	N/A	N/A
Area with PAD (mm2)	1.3	1.1	1.1	3.1

* Without pre-distortion; ** Test with single-tone

The AM-AM and AM-PM distortion are the common problems for the DPA. Fig. 6.18 shows the AM-AM and AM-PM characteristic of reference [6.14], [6.17] and [6.18]. Without pre-distortion, the AM-AM error is more than 40% for the current-mode DPA [6.14] and [6.18]; and 8% for the charge-mode DPA [17]. By using the proposed linearization technique, the AM-AM error is only 3%. So that the AM pre-distortion can be eliminated and have a more robust performance.

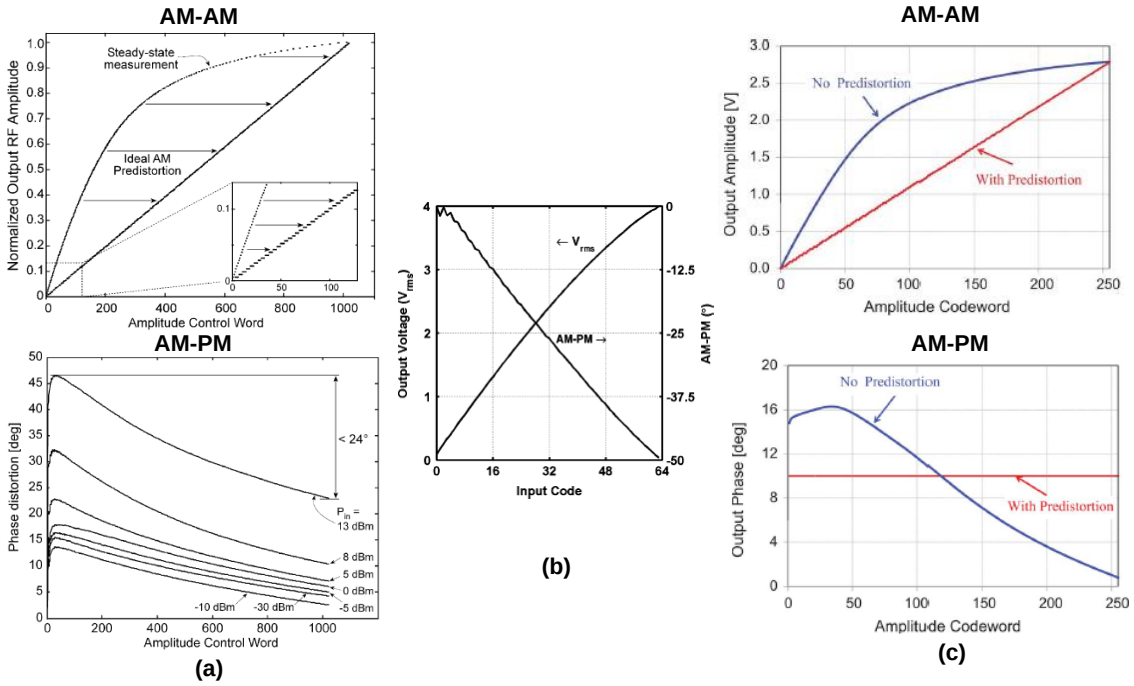


Fig. 6. 18 AM-AM and AM-PM characteristic of reference (a):[6.14], (b):[6.17] and (c):[6.18]

6.5 Conclusion

A 65nm CMOS digital polar transmitter for WCDMA and WLAN is presented. The proposed transmitter architecture employs an AM replica linearization technique to keep both the input transconductance and the input capacitance of the PA constant over the entire amplitude range of the RF envelope. In addition, the output resistance of the PA is boosted to further reduce the AM-AM and AM-PM distortion. Even without AM-AM pre-distortion, the performance of the proposed transmitter system is comparable with the existing state-of-the-art solutions.

Bibliography

[6.1] Staszewski, et al.; “All-digital TX frequency synthesizer and discrete-time receiver for Bluetooth radio in 130-nm CMOS ”, *IEEE J. Solid-State Circuits*, vol. 39, no. 12, pp. 2278-2291, Dec. 2004.

[6.2] Staszewski, et al.; “All-digital PLL and transmitter for mobile phones”, *IEEE J. Solid-State Circuits*, vol. 40, no. 12, pp. 2469-2482, Dec. 2005.

[6.3] Muhammad, K et al.; “The First Fully Integrated Quad-Band GSM/GPRS Receiver in a 90-nm Digital CMOS Process”, *IEEE J. Solid-State Circuits*, vol. 41, no. 8, pp. 1772-1783, Aug. 2006.

[6.4] Staszewski, et al.; “A 24mm2 quad-band single-chip GSM radio with transmitter calibration in 90nm digital CMOS,” *IEEE Int. Solid-State Circuits Conf. (ISSCC)* Dig. Tech. Papers, pp. 208–209, 607, Feb. 2008.

[6.5] Staszewski, et al.; “Software Assisted Digital RF Processor (DRP™) for Single-Chip GSM Radio in 90 nm CMOS ”, *IEEE J. Solid-State Circuits*, vol. 45, no. 2, pp. 276-288, Feb. 2010.

[6.6] Gang Liu, et al, “Fully Integrated CMOS Power Amplifier with Efficiency Enhancement at Power Back-Off,” *IEEE J. Solid-State Circuits*, vol. 43, no. 3, pp. 600-609, Mar. 2008.

[6.7] Chowdhury, D.; “A Fully Integrated Dual-Mode Highly Linear 2.4 GHz CMOS Power Amplifier for 4G WiMax Applications” *IEEE J. Solid-State Circuits*, vol. 44, no. 12, pp. 3393-3402, Dec. 2009.

[6.8] R. Pullela, et al.; “An integrated closed-loop polar transmitter with saturation prevention and Low-IF receiver for quad-band GPRS/EDGE,” in *IEEE Int. Solid-State Circuits Conf. (ISSCC)* Dig. Tech. Papers, 2009, pp. 112–113

[6.9] Shrestha, R. et al.; “A Wideband Supply Modulator for 20 MHz RF Bandwidth Polar PAs in 65 nm CMOS ” *IEEE J. Solid-State Circuits*, vol. 44, no. 4, pp. 1272-1280, Apr. 2009.

[6.10] P. Reynaert et al.; “A 1.75 GHz polar modulated CMOS RF power amplifier for GSM-EDGE,” *IEEE J. Solid-State Circuits*, vol.40, no. 12, p. 2598, Dec. 2005

[6.11] I. Bashir, et al.; “A Novel Approach for Mitigation of RF Oscillator Pulling in a Polar Transmitter” *IEEE J. Solid-State Circuits*, vol. 46, no. 2, pp.403-415, Feb. 2011.

[6.12] Darabi, H.et al.; “Analysis and Design of Small-Signal Polar Transmitters for Cellular Applications ” *IEEE J. Solid-State Circuits*, vol. 46, no. 6, pp. 1237-1249, Jan. 2011.

[6.13] A. Kavousian, et al, “A Digitally Modulated Polar CMOS Power Amplifier With a 20-MHz Channel Bandwidth” *IEEE J. Solid-State Circuits*, vol. 43, no. 10, pp. 2251-2258, Oct. 2008.

[6.14] Calogero D. et al.; “A 25 dBm Digitally Modulated CMOS Power Amplifier for WCDMA/EDGE/OFDM with Adaptive Digital Predistortion and Efficient Power Control” *IEEE J. Solid-State Circuits*, vol. 44, no. 7, pp.1883-1896, Jul. 2009.

[6.15] J. Lopez, et al.; “Design of Highly Efficient Wideband RF Polar Transmitters Using the Envelope-Tracking Technique” *IEEE J. Solid-State Circuits*, vol. 44, no. 9, pp.2276-2294, Sep. 2009.

[6.16] M. Youssef, et al.; “A Low-Power GSM/EDGE/WCDMA Polar Transmitter in 65-nm CMOS” *IEEE J. Solid-State Circuits*, vol. 46, no. 12, pp.3061-3074, Dec. 2011.

[6.17] Sang-Ming. Y, et al.; “A Switched-Capacitor RF Power Amplifier” *IEEE J. Solid-State Circuits*, vol. 46, no. 12, pp.2977-2987, Dec. 2011.

[6.18] D. Chowdhury, et al.; “An Efficient Mixed-Signal 2.4-GHz Polar Power Amplifier in 65-nm CMOS Technology” *IEEE J. Solid-State Circuits*, vol. 46, no. 8, pp.1796-1809, Aug. 2011.

[6.19] D. Chowdhury, et al.; A Fully-Integrated Efficient CMOS Inverse Class-D Power Amplifier for Digital Polar Transmitters” *IEEE J. Solid-State Circuits*, vol. 47, no. 5, pp.1113-1122, May. 2012.

[6.20] Xin He, et al., “A 45nm WCDMA transmitter using direct quadrature voltage modulator with high over sampling digital front-end,” *IEEE Int. Solid-State Circuits Conf. (ISSCC)* Dig. Tech. Papers, pp. 62–63, Feb. 2010.

CHAPTER 7 Measurement Results and Conclusion

7.1 System Integration

Fig. 7.1 shows the system block diagram of the digital polar transmitter. It is composed of a 2.5GHz to 3.7GHz ADPLL with quadrature output, a quadrature-in/quadrature-out ÷1.5 frequency divider, a wide-band digital phase modulator and a high linear digital polar amplifier. The transmitter is designed for WCDMA and 54M bps WLAN. The chip prototype is fabricated in TSMC 65nm 1P9M CMOS.

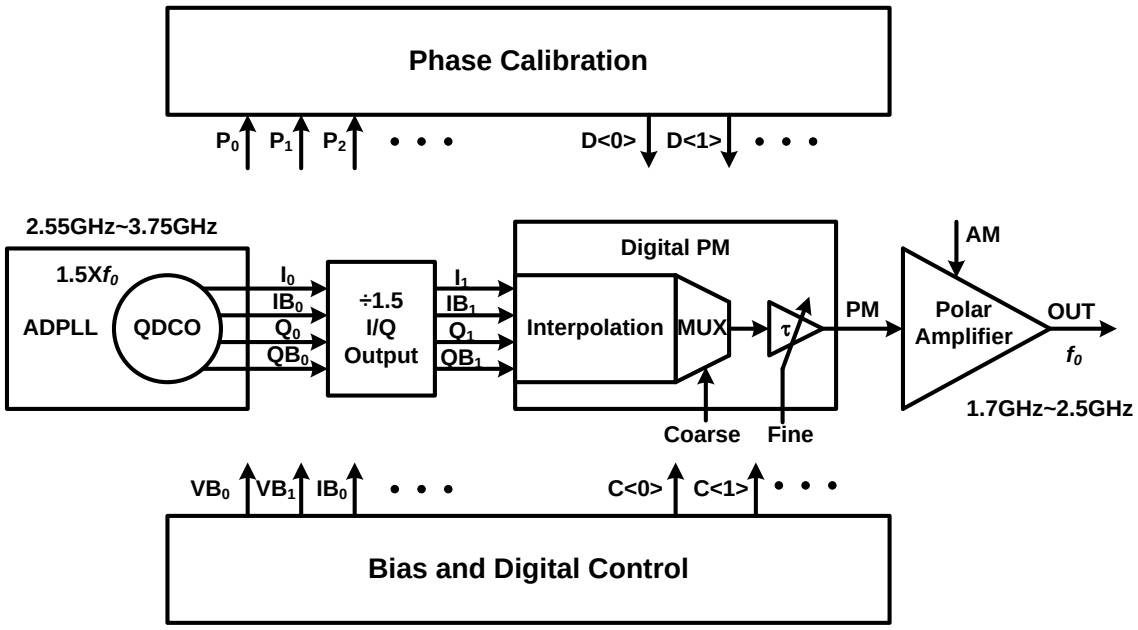


Fig. 7. 1 System block diagram of the digital polar transmitter

The layout of the transmitter system is shown in Fig. 7.2. It occupies a core area of 2.45 X 1.05 mm^2. The digital AM and PM control signals are generated from a high-speed pattern generator IO-3200 and sent to the transmitter in parallel. While an on-chip shift registers circuit is employed for other slow digital control signals. The RF signals are captured through on-wafer probing. The S-G-S probe is for the QDCO and G-S-G

probe is for the PA. The captured RF signals are sent to a MXA signal analyzer 9020A for demodulation and measurement. The whole testing setup is shown in Fig.7.3.

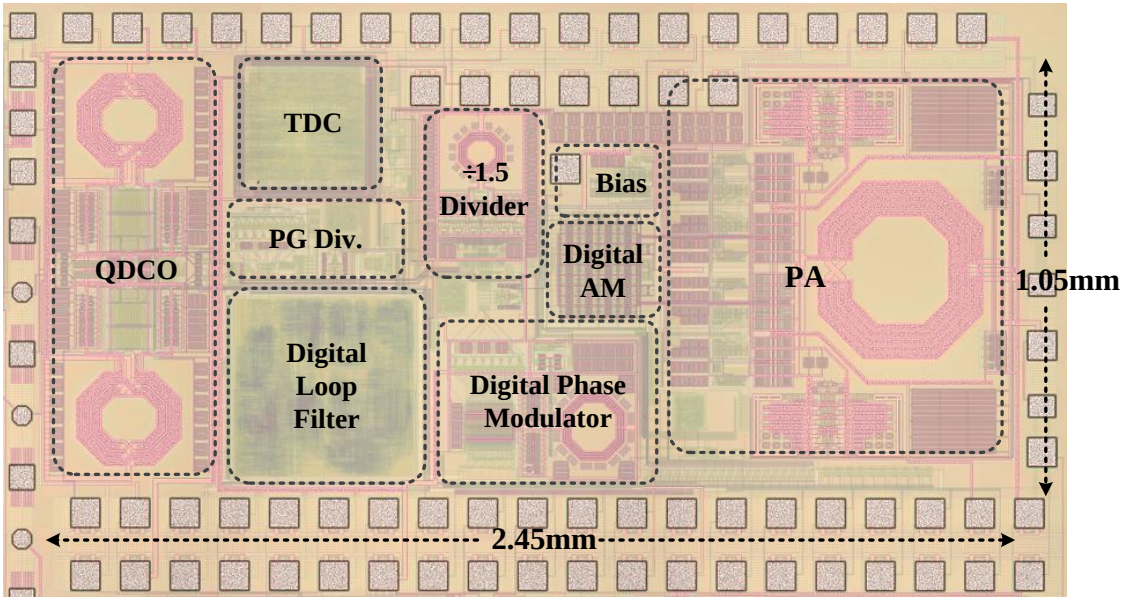


Fig. 7. 2 layout of the transmitter system

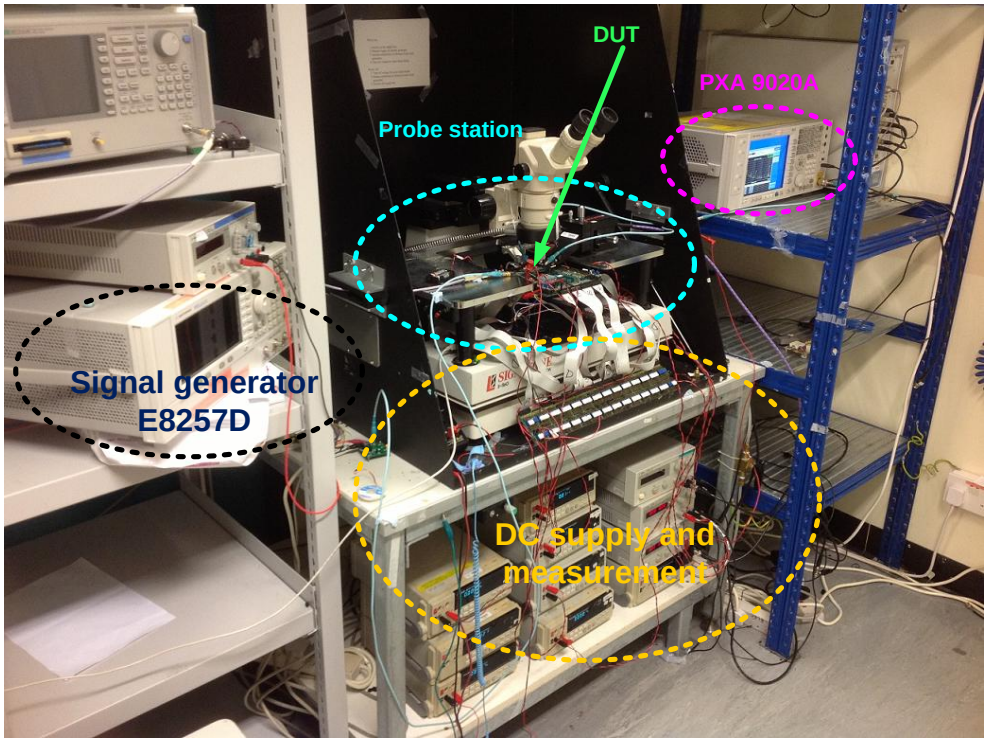


Fig. 7. 3 Measurement setup for the all digital polar transmitter

7.2 Measurement Results

Before the system measurement, each building block is characterized and the performances of the key building blocks will be discussed and compared with the simulation. After that, the measurement result of the three sub-systems is shown, includes: LO generation, digital modulation and power amplification. And finally, we have the result of the whole system.

7.2.1 QDCO

In the frequency range measurement, the QDCO can generate the quadrature signal from 2.5GHz to 3.7GHz. After the 1.5 frequency division, it can cover the frequency range of 1.67GHz to 2.47GHz. Fig. 7.4 shows the measured spectrum in the low-side and high-side of the required frequency range.

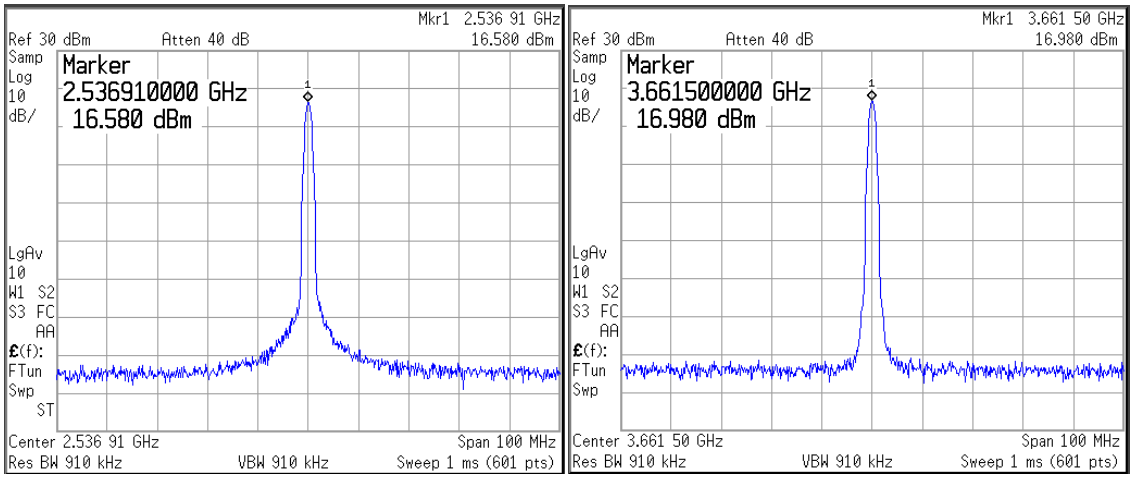


Fig. 7. 4 QDCO output frequency range

The phase noise of the QDCO is shown in Fig. 7.5. For a carrier frequency of 2.93GHz, the measured phase noise at 1MHz offset is: -119.77dBc/Hz, the flicker noise corner is round 500kHz.

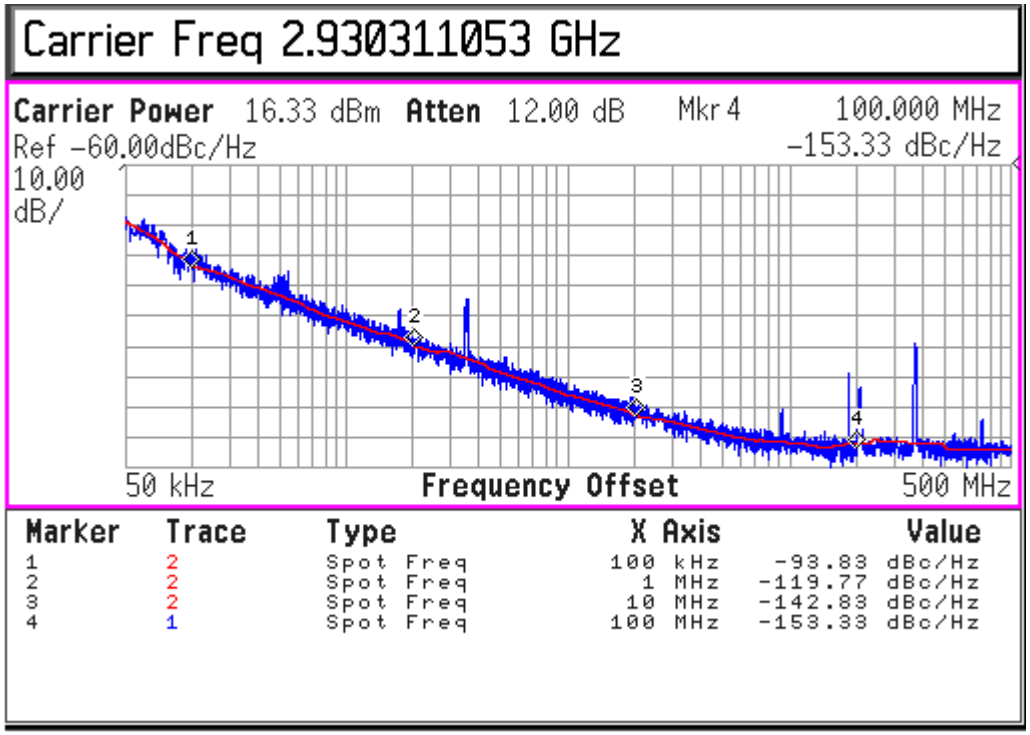


Fig. 7. 5 QDCO output phase noise

The quadrature mismatch of the QDCO was measured by using an on chip single-side-band-mixer. A 20MHz quadrature baseband (BB) signal are generated from an off-chip 80MHz reference signal with on-chip ÷4 frequency division. Then the BB signal is up-converted to the QDCO output frequency. The side-band-rejection was measured to calculate the quadrature error of the QDCO.

As Fig. 7.6 shown, the side-band-rejection before phase calibration is 41.8dB and after phase calibration is 56.3dB. Then the phase error can be calculated [1] by:

$$IR = 10 \cdot log\left(\frac{1 + A^2 - 2A\cos\theta}{1 + A^2 + 2A\cos\theta}\right)$$

where A and θ are the amplitude and phase mismatch.

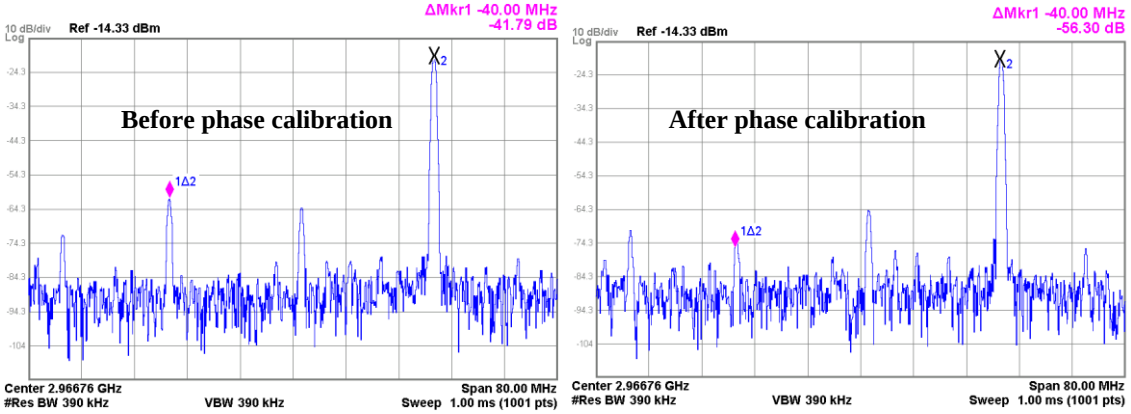


Fig. 7. 6 QDCO quadrature error measurement (a) before phase calibration (b) after phase calibration

7.2.2 Phase Interpolated Sub-Integer Programmable Divider

In this measurement, the programmable ratio is set to a fractional number and then the spectrum of divider output was measured. Fig. 7.7 shows the worst case output spurs which are caused by the non-linearity of the phase interpolation

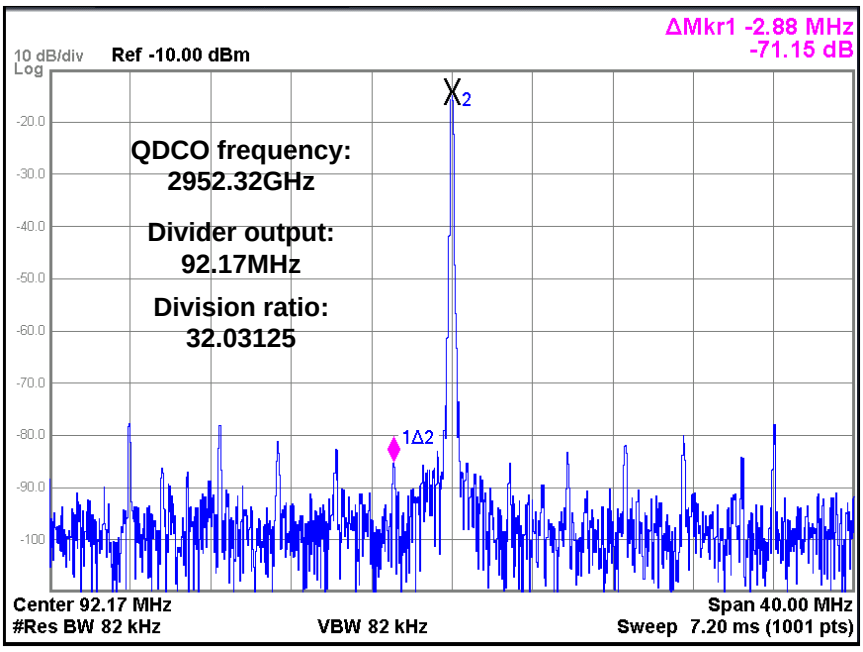


Fig. 7. 7 Worst case output spurs of the sub-integer programmable divider

7.2.3 ADPLL

The measured phase noise of the ADPLL is shown in Fig. 7.8 and Fig 7.9 shows the in-band fractional spurs and reference spurs.

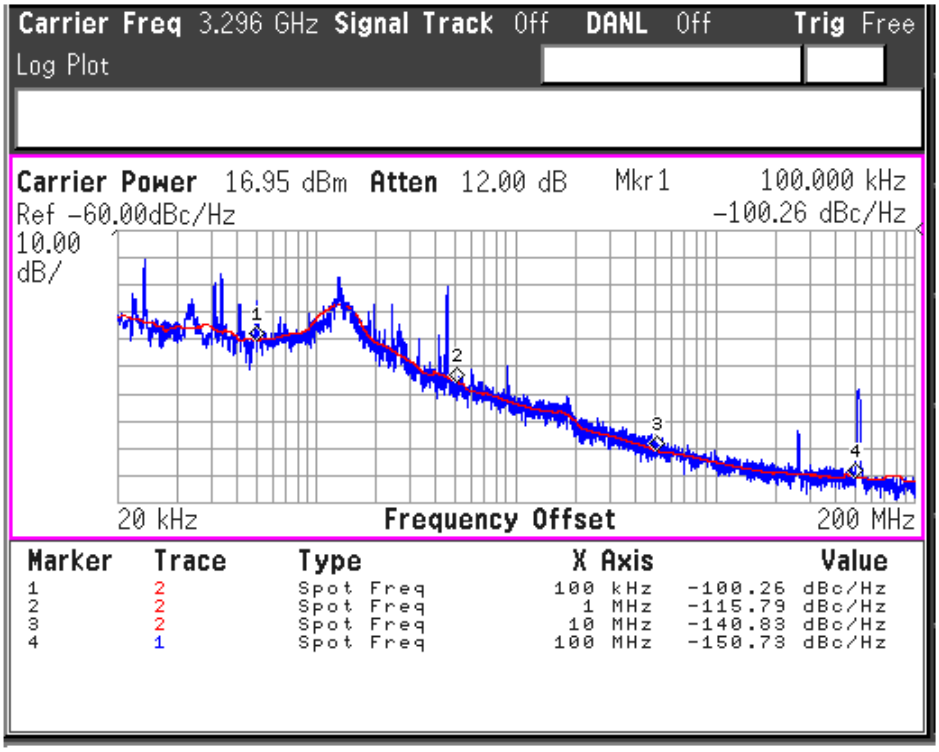
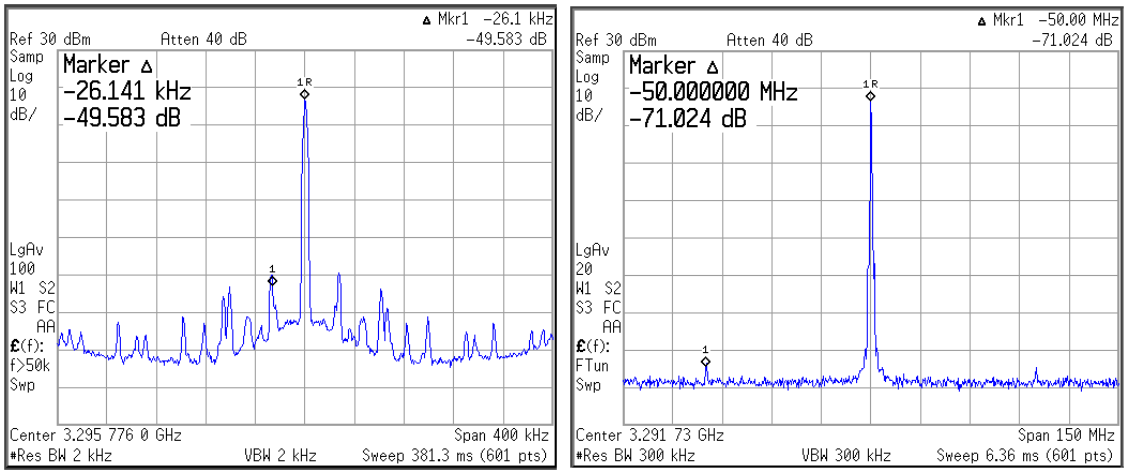


Fig. 7. 8 The measured phase noise of the ADPLL



(a) **(b)**

Fig. 7. 9 Measured ADPLL spurs (a) in-band fractional spurs and (b) reference spurs

7.2.4 ÷1.5 Quadrature Output Divider

Fig. 7.10 shows the output range of the ÷1.5 divider, it can cover the output range of the QDCO. Its output quadrature mismatches with/without the duty cycle correction (DCC) are shown in Fig 7.11. The DCC can improve the IR by

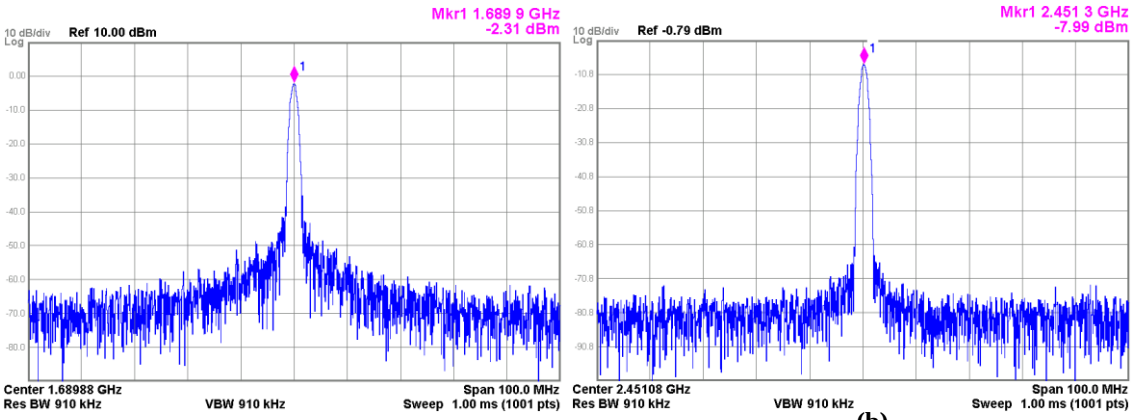


Fig. 7. 10 Measured output frequency range of the ÷1.5 divider (a) minimum frequency and (b) maximum frequency

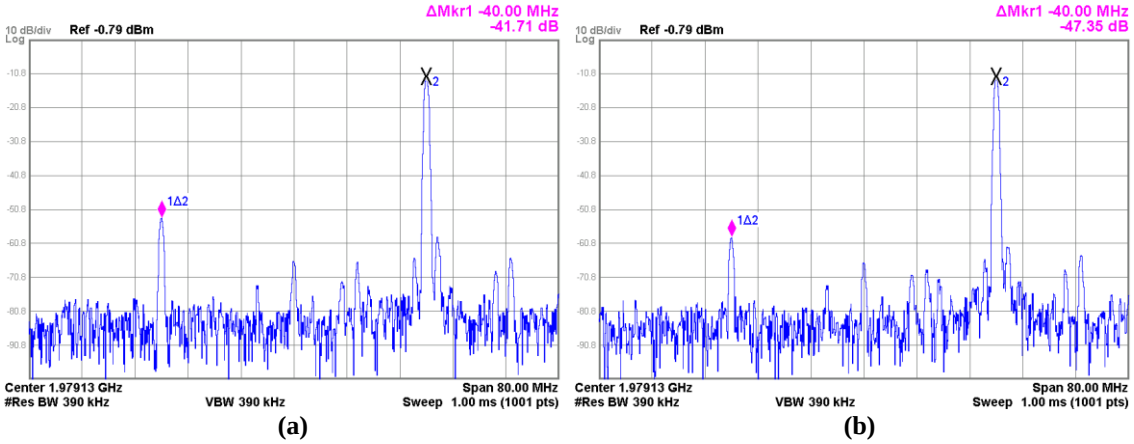


Fig. 7. 11 Measured quadrature error of ÷1.5 divider (a) without DCC and (b) with DCC

7.2.5 Digitally-Controlled Phase Modulator

To measure the phase tuning range of the digitally-controlled phase modulator, a digital dual-slope ramp signal (generated by an up-down counter) is used to modulate the output phase of the carrier for -180 °to 180 °. Then we use a PXA to demodulate this PM signal and show its output is in Fig. 7.12. We can see that the DPM has a phase tuning range of 360 °.

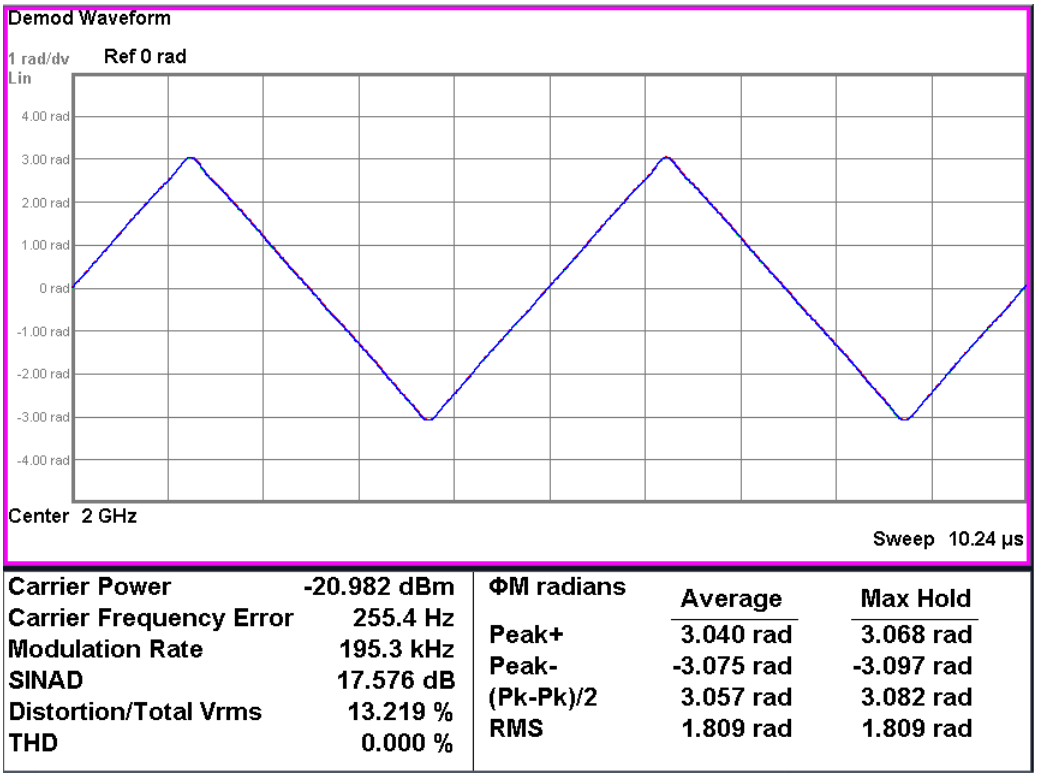


Fig. 7. 12 Demodulated dual-slope ramp PM signal

To measure the DPM linearity, we rotate the output phase of the carrier with a constant rate, then we can shift the carrier frequency. By measure the spectrum purity of the frequency-shifted carrier, we can calculate the phase error of the DPM. Fig. 7.13 shows the spectrum of a 2GHz carrier with its phase rotating at round 0.4rad/µs. The

phase error is shown in Fig. 7.14 with a RMS phase error of 1.23 °.

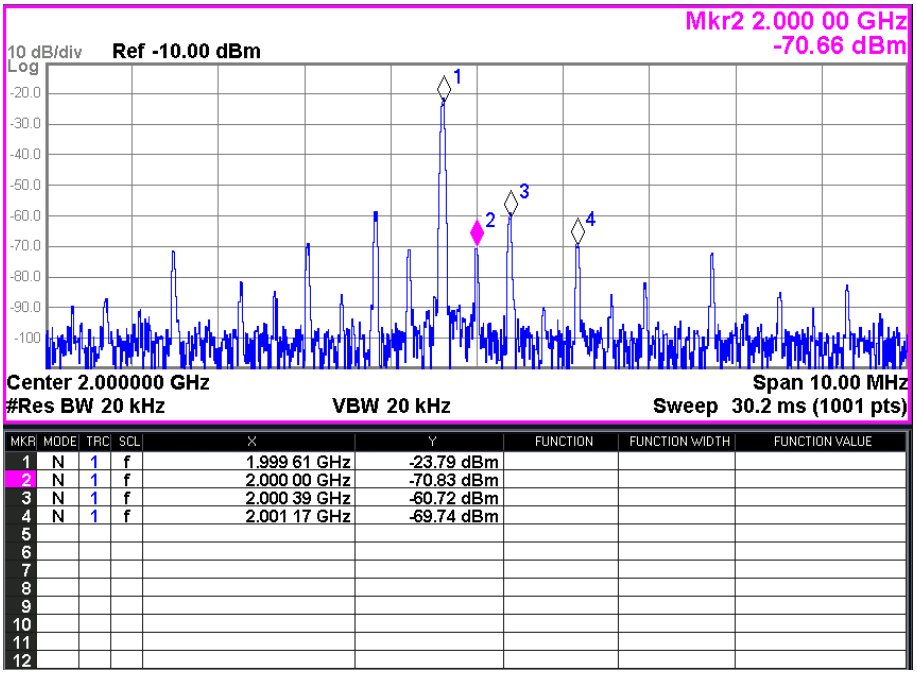


Fig. 7. 13 PM linearity measurement

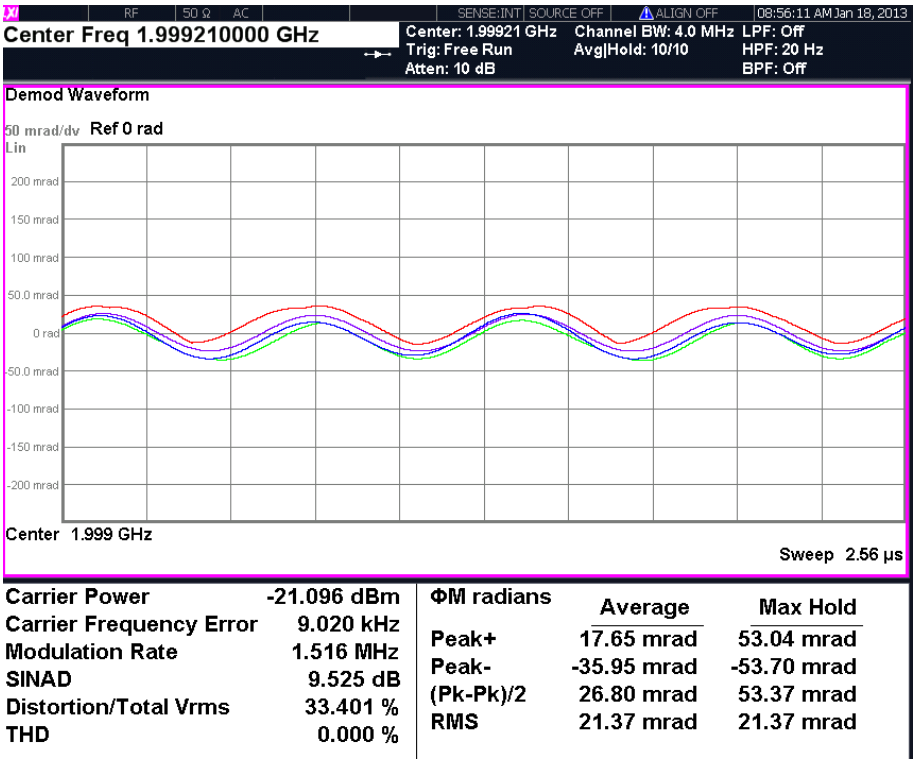


Fig. 7. 14 PM phase error measurement

7.2.6 Polar Power Amplifier

Fig. 7.15 and 7.16 shows the AM-AM and AM-PM conversion of the polar PA with/without linearization.

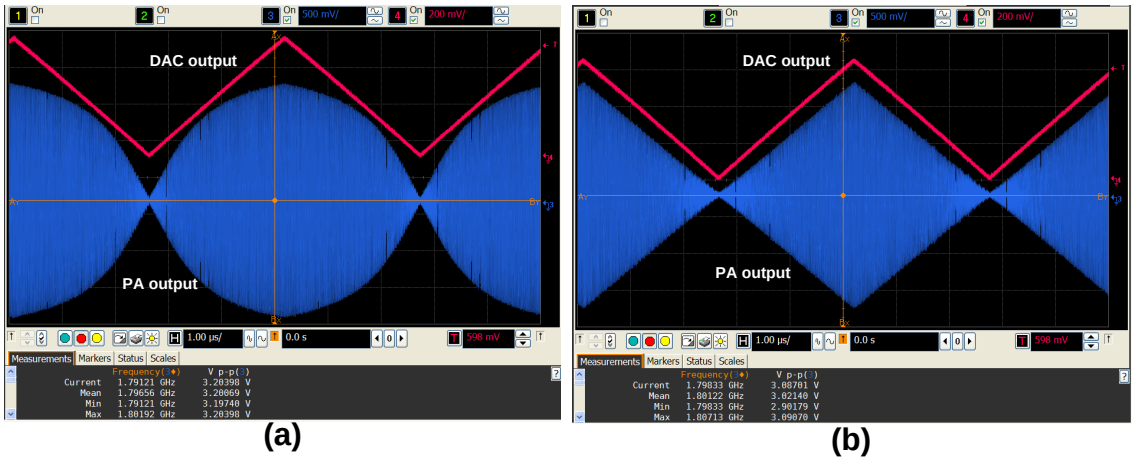


Fig. 7. 15 PA AM-AM (a) without linearization (b) with linearization

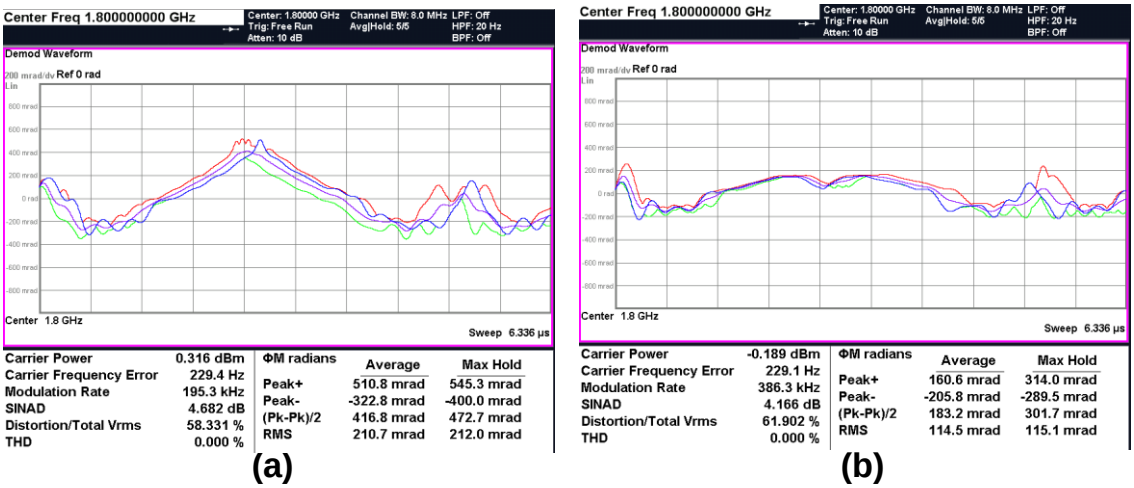


Fig. 7. 16 PA AM-PM (a) without linearization (b) with linearization

7.2.7 Transmitter System

Fig. 7.17 ~ 7.20 show the measured WCDMA and WLAN transient waveform and the EVM and spectrum mask.

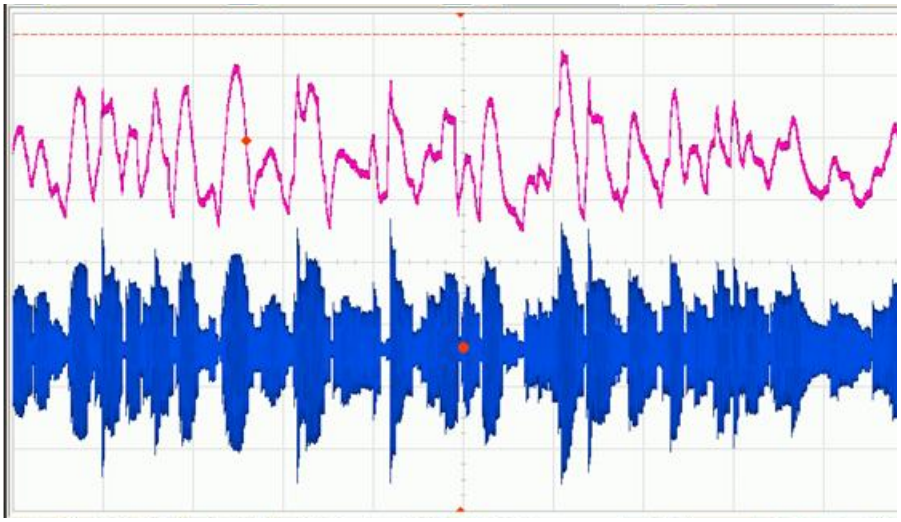


Fig. 7. 17 WCDMA transient waveform

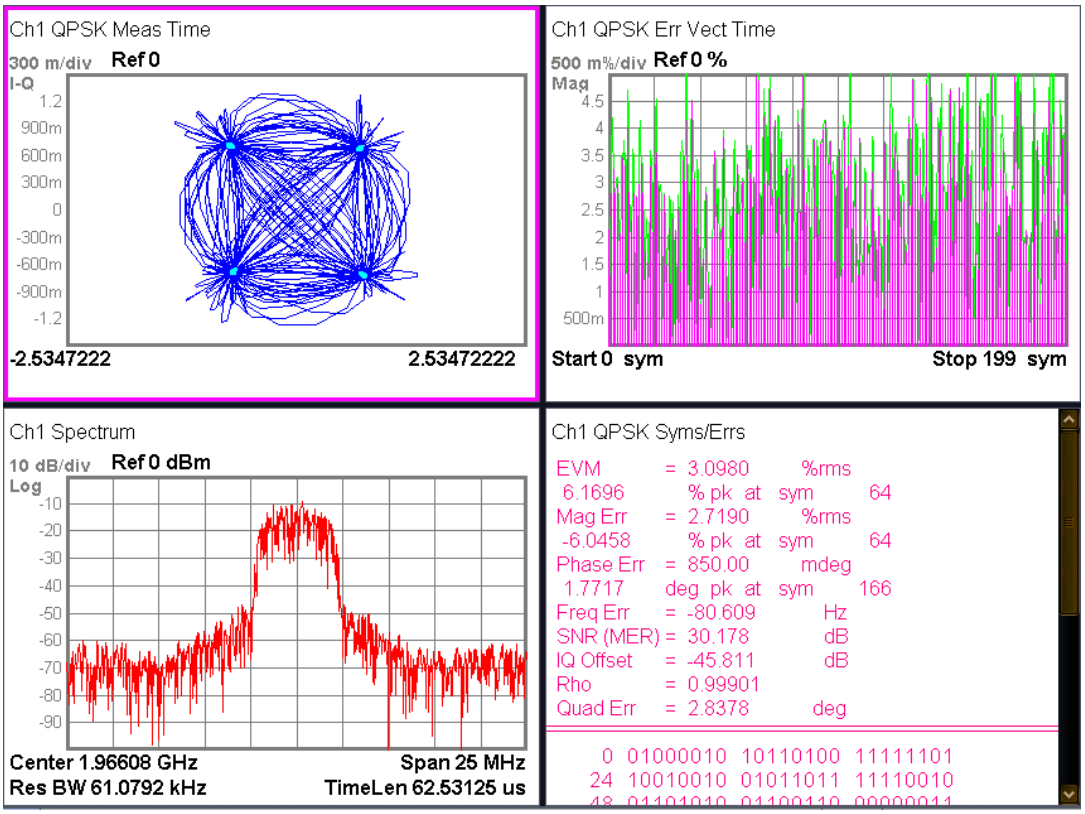


Fig. 7. 18 Measured WCDMA spectral mask and EVM

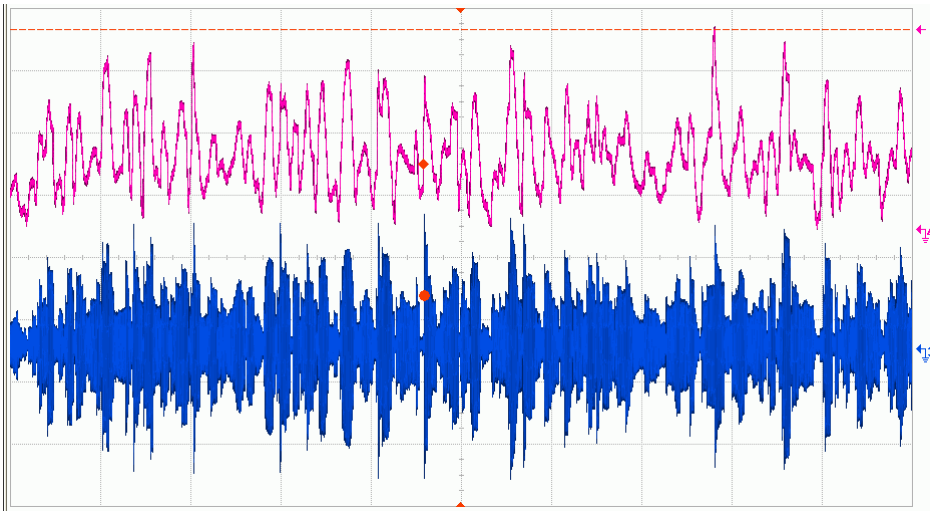


Fig. 7. 19 WLAN 54-Mb/s 64-QAM transient waveform

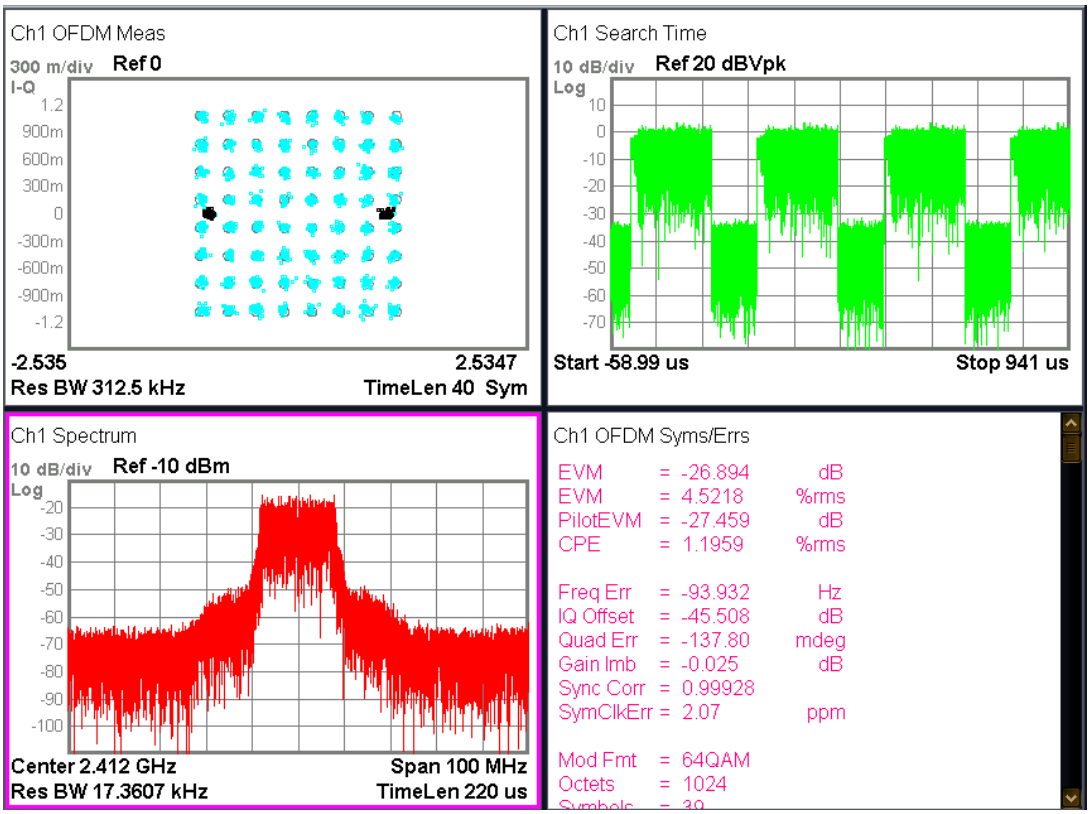


Fig. 7. 20 Measured spectral mask and EVM for WLAN 802.11g 54-Mb/s 64-QAM OFDM data

Table 7. 1 Tx Performance Summary and Comparison

Parameters	This work	JSSC 12 Chen [7.1]	JSSC 12 Ravi [7.2]	JSSC 11 Youssef [7.3]
Technology	65nm	90nm	32nm	65nm
Architecture	polar	polar	outphasing	polar
Mode/Modulation	WCDMA WLAN (20MHz)	π/4-QPSK * 16-QAM *	WLAN (20/40MHz)	GSM EDGE WCDMA
LO Generation	on-chip ADPLL	on-chip ADPLL	external	on-chip analog PLL
Frequency (GHz)	1.6~2.7	~1.68	~2.4	~0.9/~1.8
Phase noise @1MHz (dBc/Hz)	-123.5	-121.5	N/A	-125
EVM	3% (WCDMA) 4.5% (20M WLAN)	3.2% (π/4-QPSK) 7% (16-QAM)	2.6% (20M-WLAN) 5.6% (40M-WLAN)	2.4% (EDGE) 2.9% (WCDMA)
ACLR (dBc)	-41/-54 (5/10MHz)	N/A	-53 (30MHz)	-42/-58 (5/10MHz)
Maximum output Power (dBm)	22	6.8	26	0
PAE	19% **	8.3%	22% **	N/A
Supply Voltage (V)	1.2/2	1	1.05/2	1.2/1.8/2.5
Power Consumption (mW)	88	58	82	144

* Symbol rate: 250KHz ** For 20M WLAN with EVM < 5.6%

7.3 Contribution of the Dissertation

In this dissertation, we investigate the feasibility of an all-digital radio transmitter system with full-levels of integration in advance scale-down CMOS technology. The transmitter architecture and circuit implementation have been explored to achieve multi-standards operation with low-cost, low-noise, high-linearity, and high-efficiency

In particular, the following contributions are made:

1) Design of a low noise all-digital frequency synthesizer (ADFS) for LO carrier generation. To reduce the out-band phase noise, a quadrature phase digitally-

controlled oscillator (QDCO) with quantization noise suppression technique is proposed and measured 6.6dB improvement of the out-band phase noise. In addition, the proposed QDCO operates in Class-C mode with embedded phase shifter for better DC-to-RF efficiency and I-Q accuracy. The in-band phase noise of the ADFS is minimized by using a statistical TDC with ultra-fine time resolution and a proposed phase-interpolated ΣΔ programmable divider to reduce the TDC input range.

2) To reduce the VCO pulling effects, a quadrature output ÷1.5 divider is proposed for the LO frequency plan. The proposed ÷1.5 divider employs 8-phases harmonic rejection mixing and duty-cycle correction techniques to minimize the output I-Q mismatch. The residue phase errors are reduced further by a statistical TDC based high accurate all-digital phase calibration.
3) Wide-band and fine-resolution phase modulation is achieved with proposed phase-interpolated ΣΔ digital phase modulator. This phase modulator employs 2-segments architecture. For the coarse-tuning segment, a 6-bit phase interpolator together with a phase selection MUX provide a phase tuning range of 0~360° with a resolution of 5.625°. For the fine-tuning segment, a delay tuning buffer with 5-bit digitally-controlled loading capacitor achieves 0.2° phase resolution. The 2 segments are cascade to achieve wide-range and fine-resolution phase modulation. The gain mismatch between the 2 segments can be shaped by a digital ΣΔ modulator. In addition, wide-band modulation can be achieved due to its open-loop architecture.
4) Propose a digital polar PA with AM replica feedback linearization. It is composed of a digital interpolation filter for up-sampling of the input

amplitude-control word (ACW), a 9-bit switched-capacitor array for the digital polar modulation (DPM), and a 6-bit PA array to achieve the output power range for the target applications. A linearization technique is implemented by adaptively changing the PA bias voltage according to the RF envelope. To generate this bias voltage, the RF envelope of the PA input is extracted by a digital-to-analog converter (DAC) with the ACW signals as its input. A replica of the PA which only needs to operate at the AM frequency senses the RF envelope and regulates the output bias voltage with an analog feedback loop to minimize the distortion in the AM path.

7.4 Future work

The main focus and contribution of this work are phase noise reduction for the ADPLL, modulation bandwidth extension and linearity improvement of the polar PA. Nevertheless, there are also some potential topics worthy to be investigated in design of the digital transmitter.

1) Auto phase noise and power consumption optimization. In the ADPLL, the phase noise over the frequency spectrum can be estimated by analysis the output of the digital loop filter. For example, if the in-band phase noise is over design, then we can reconfigure the TDC with lower performance and lower power consumption. Then we can meet the standard requirement with minimum power consumption.

2) Fast channel switching for the PLL. The setting time of the open loop frequency synthesis can be controlled into nanosecond level. However, the setting time for the PLL is in the order of tens of microseconds even using a large loop bandwidth together

with quantization noise compensation or dynamic bandwidth control. Considering a wide range of spectrum scanning for the future cognitive radio, many tens of microseconds would still be too long. Therefore, novel techniques to further reduce the switching time are highly desirable.

3) Highly reconfigurable digital polar power amplifier. As we know, the digital polar amplifier modulates its output envelope by on/off subsets of the PA cells with a fixed voltage supply. If the bandwidth of the supply modulator is large enough, then the combination of supply modulator and DPA will has a much better efficiency. Also, the PA cells in the Polar PA are normally fixed at one type of operation mode, for example, Class-E. It is desirable to have multi-mode operation mode to optimize the linearity and efficiency.

Bibliography

[7.1] Ravi, A.; et al., “A 2.4-GHz 20–40-MHz Channel WLAN Digital Outphasing Transmitter Utilizing a Delay-Based Wideband Phase Modulator in 32-nm CMOS,” IEEE J. Solid-State Circuits, vol.47, no.12, pp. 3184 - 3196, Dec 2012

[7.2] Jian Chen, et al., “The Design of All-Digital Polar Transmitter Based on ADPLL and Phase Synchronized ΔΣ Modulator,” IEEE J. Solid-State Circuits, vol.47, no.5, pp. 1154 - 1164, May 2012

[7.3] Michael Youssef; et al., “A Low-Power GSM/EDGE/WCDMA Polar Transmitter in 65-nm CMOS,” IEEE J. Solid-State Circuits, vol.46, no.12, pp. 3061 - 3074, Dec 2011

Appendix-I

Design and Characterization of Inductive Components

The inductive passive components, such as inductor and transformer play an important role in the RFIC design. In this appendix, I will briefly discuss about the design flow of the inductive components by using the CAD tools: ASITIC [A-I.1] and ADS [A-I.2]. After that I will introduce an on-wafer characterization method to verify our design. The technical aspects of monolithic inductors and transformers, including the layout configurations, the physical analysis and the fitting models can be found in numerous literatures [A-I.3]-[A-I.7].

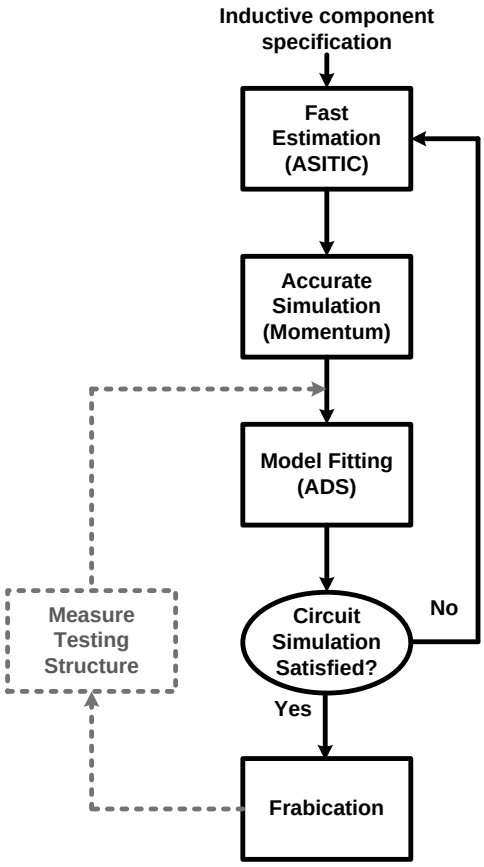


Fig. A-I. 1 Design flow of the inductive components

Fig. A-I.1 shows the design flow of the inductive components. At the beginning, the component parameters like the inductance, Q and coupling coefficient can be quickly estimated and optimized using the tool ASITIC, with simulating different layout configurations and adjusting the physical parameters such as the turn number, the diameter, the metal width, the line spacing and so on. It should be noticed that the estimated Q from ASITIC is typically higher than the actual Q, especially at the frequencies above 5GHz. So enough design margins should be left for the inductive Q before moving to the next step.

After obtaining the basic physical parameters, the inductor or the transformer is then simulated in a 2.5D EM simulator Momentum from Agilent. The simulation would take much longer time but has a more accurate result. Then, the simulated S-parameter data from Momentum are fitted into a discrete component model in ADS, so that the inductor or the transformer can be well simulated in the circuit simulators, such as Spice or SpectreRF. If the circuit performance with the designed inductor or transformer is satisfied, the design is done. If not, the flow needs to go back to the beginning and repeat all the steps.

When we have finished the design of the inductive components, then a set of testing structures would be built for characterization [A-I.8]. Here, we have 2 examples: one is for the inductor and the other one is for the transformer.

Fig A-I.2 shows the testing structures for a symmetrical centre tapped inductor, which include: one inductor testing structure, one “open” de-embedding testing structure and one “short” de-embedding testing structure.

A network analyzer with one balanced port (truly differential) is employed for the measurement. Before measuring the data, the whole test environment needs to be

calibrated through probing a calibration substrate for the associated probes. Then, the inductor is measured by replacing the calibration substrate with the device under test. Since the measured raw data contain both the parasitic capacitance of the pads and the parasitic inductance of the interconnecting lines between the device and the pads, the testing structures of the open pads and short pads are also measured.

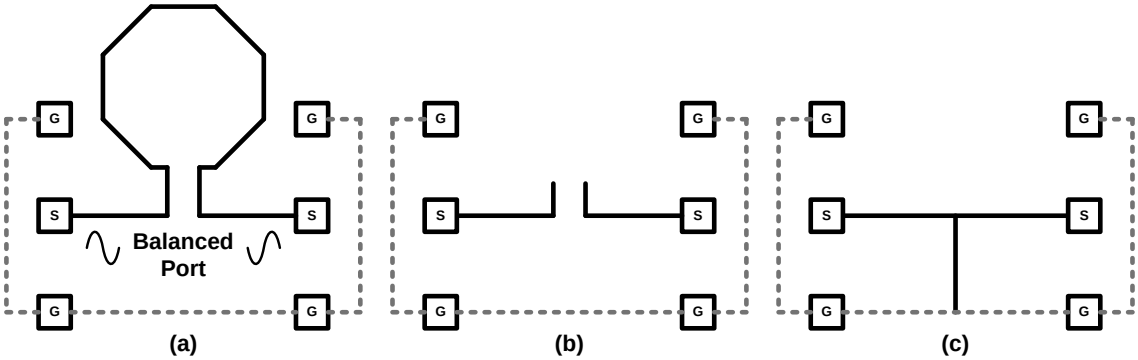


Fig. A-I.2 Testing structure for (a) inductor, (b) open de-embedding and (c) short de-embedding

Assume the measured mixed mode Y-parameters for the 3 testing structures are: Y_{ind}, Y_{open} and Y_{short}. Then we can do the de-embedding calculation for the inductor:

1) Open correction of short

$$Y_{short\_cor} = Y_{short} - Y_{open}$$

2) Open correction of the inductor

$$Y_{ind\_cor} = Y_{ind} - Y_{open}$$

3) Short correction of the device

$$Z = Z_{ind\_cor} - Z_{short\_cor}$$

Then the inductance and Q can be calculated by:

$$L = \mathrm{Im}(Z)/\omega \tag{A-I.1}$$

$$Q_p = \frac{\mathrm{Im}(Z)}{\mathrm{Re}(Z)} \tag{A-I.2}$$

A similar method can be employed for the transformer characterization and Fig. A-I.3 shows the testing structures for the transformer. As we seen, a network analyzer with two balanced ports is used so we need to do a 2-port calibration.

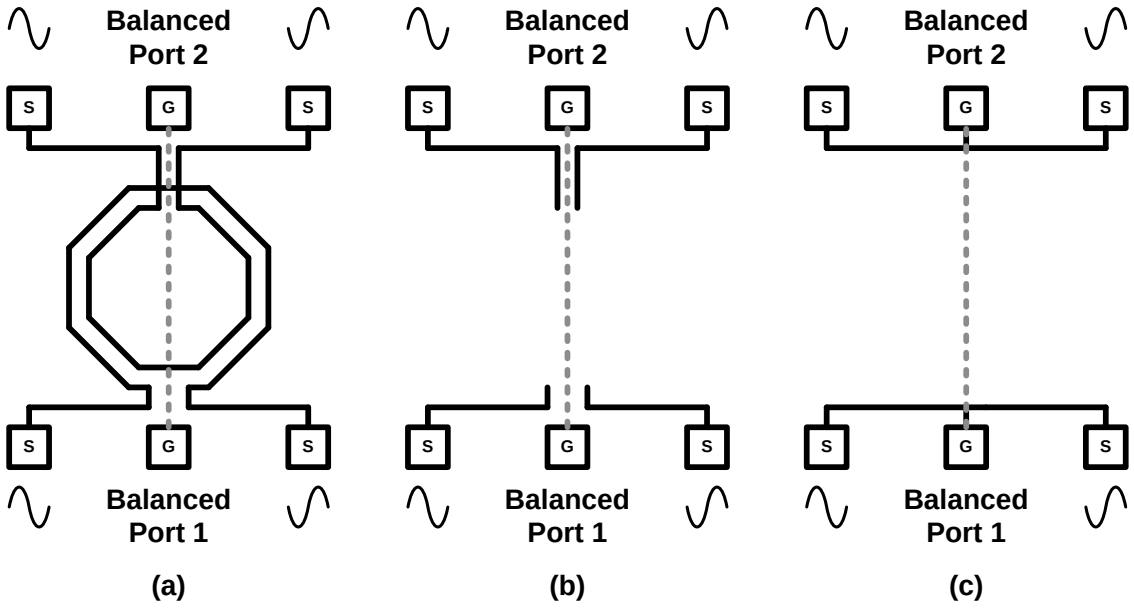


Fig. A-I.3 Testing structure for (a) Transformer, (b) open de-embedding and (c) short de-embedding

Assume the measured mixed mode Y-parameters for the 3 testing structures are: Y_{ind}, Y_{open} and Y_{short}. (All are 2 ports) Then we can do the de-embedding calculation for the inductor:

1) Open correction of short

$$Y_{short\_cor,11} = Y_{short,11} - Y_{open,11} \text{ and } Y_{short\_cor,22} = Y_{short,22} - Y_{open,22}$$

2) Open correction of the inductor

$$Y_{ind\_cor,11} = Y_{ind,11} - Y_{open,11} \text{ and } Y_{ind\_cor,22} = Y_{ind,22} - Y_{open,22}$$

3) Short correction of the device

$$Z_{11} = Z_{ind\_cor,11} - Z_{short\_cor,11} \text{ and } Z_{22} = Z_{ind\_cor,22} - Z_{short\_cor,22}$$

Then the parameters L_p, L_s, Q_p, Q_s and k can be calculated by:

$$L_p = \mathrm{Im}(Z_{11})/\omega \tag{A-I.3}$$

$$L_s = \mathrm{Im}(Z_{22})/\omega \tag{A-I.4}$$

$$Q_p = \frac{\mathrm{Im}(Z_{11})}{\mathrm{Re}(Z_{11})} \tag{A-I.5}$$

$$Q_s = \frac{\mathrm{Im}(Z_{22})}{\mathrm{Re}(Z_{22})} \tag{A-I.6}$$

$$k = \sqrt{\frac{(Y_{11}^{-1} - Z_{11})Z_{22}}{\mathrm{Im}(Z_{11})\,\mathrm{Im}(Z_{22})}} \tag{A-I.7}$$

After characterization, we will compare the measured data with the ADS simulation result. The measured data will be imported to ADS for model fitting. After that, the fitted model is verified again in the circuit level simulation, to find out the actual influence of the inductor or the transformer on the circuit performance, if necessary, the inductive component needs to be re-designed from the beginning.

Bibliography

[A-I.1] Available in http://rfic.eecs.berkeley.edu/~niknejad/asitic.html

[A-I.2] Available in http://www.home.agilent.com/en/pc-1297113/advanced-design-system-ads?&cc=HK&lc=eng

[A-I.3] J. R. Long, and M. A. Copeland, "The Modeling, Characterization, and Design of Monolithic Inductors for Silicon RF IC's," IEEE J. Solid-State Circuits, vol. 32, No. 3,pp. 357-369, Mar. 1997.

[A-I.4] A. M. Niknejad, and R. G. Meyer, "Analysis, Design, and Optimization of Spiral Inductors and Transformers for Si RF IC's," IEEE J. Solid-State Circuits, vol. 33, No.10, pp. 1470-1481, Oct. 1998

[A-I.5] Y. K. Koutsoyannopoulos, and Y. Papananos, "Systematic Analysis and Modeling of Integrated Inductors and Transformers in RF IC Design," IEEE Transactions on Circuit and Systems –II: Analog and Digital Signal Processing, Vol. 47, No. 8, Aug. 2000.

[A-I.6] J. R. Long, "Monolithic Transformers for Silicon RF IC Design," IEEE J. Solid-State Circuits, vol. 35, No. 9, pp. 1368-1382, Sept. 2000.

[A-I.7] A. M. Niknejad, and R. G. Meyer, "Analysis of Eddy-Current Losses Over Conductive Substrates with Applications to Monolithic Inductors and Transformers," IEEE Transactions on Microwave Theory and Techniques, Vol. 49, No. 1, Jan. 2001.

[A-I.8] Gianesello, F.; et al., "Characterization and Model Parameter Extraction ofSymmetrical Centre Tapped Inductor using Build in Mixed Mode and Pure Differential S-Parameters," IEEE Microelectronic Test Structures, 2009. ICMTS 2009.

Appendix-II

List of Publications

Conference papers:

1. **Shiyuan, Zheng** and H. C. Luong, "A WCDMA/WLAN Digital Polar Transmitter with AM Replica Feedback Linearization in 65nm CMOS" *IEEE European Solid-State Circuits Conference (ESSCIRC)*, Bordeaux, France, Sep 2012
2. **Shiyuan, Zheng** and H. C. Luong, "A 4.1-to-6.5GHz Transformer-Coupled CMOS Quadrature Digitally-Controlled Oscillator with Quantization Noise Suppression," *IEEE Radio Frequency Integrated Circuit Symposium (RFIC)*, Montreal, Canada, June 2012
3. Alan W.L. Ng, **Shiyuan, Zheng** and H. C. Luong, "A 4.1GHz-6.5GHz All-Digital Frequency Synthesizer with a 2nd-Order Noise-Shaping TDC and a Transformer-Coupled QVCO" *IEEE European Solid-State Circuits Conference (ESSCIRC)*, Bordeaux, France, Sep 2012

Journal Papers

1. **Shiyuan, Zheng** and H. C. Luong, "A CMOS WCDMA/WLAN Digital Polar Transmitter with AM Replica Feedback Linearization" *IEEE J. Solid-State Circuits*, submitted in November 2012
2. **Shiyuan, Zheng** and H. C. Luong, "Design of the Class-C mode QDCO with embedded phase shifter and quantization noise suppression" *IEEE J. Solid-State Circuits*, to be submitted in Feb 2013
3. **Shiyuan, Zheng** and H. C. Luong, "Design of the ALL-Digital Polar Transmitter"

IEEE J. Solid-State Circuits, to be submitted in Feb 2013

Patents

1. **Shiyuan, Zheng** and H. C. Luong, "Quantization noise suppression techniques for digitally-controlled oscillator," *US patent, to be filed.*
2. **Shiyuan, Zheng** and H. C. Luong, "Linearization techniques for digital polar transmitter," *US patent, to be filed.*