A 900-MHz CMOS Bandpass Amplifier for Wireless Receivers

A thesis submitted to

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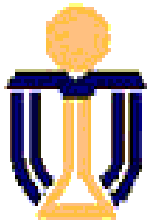

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Abstract

This dissertation describes the design of a CMOS 900-MHz bandpass amplifier that is suitable for RF transceivers. The work employs the state-of-art inductive degeneration techniques to minimize the noise figure and explores the use of lossy spiral inductors in high frequency circuit to realize input matching networks on-chip. A Q-compensation circuit is included to achieve a 25-MHz 3-dB bandwidth. Besides, a center frequency tuning circuit is also embedded to compensate for frequency deviations due to process variations.

In the first prototype, a second-order bandpass amplifier had been fabricated in standard 0.8 μm single-poly, triple-metal CMOS process (HP SCN26G) provided by MOSIS®. With a 3-V supply, at 950-MHz and a 3-dB bandwidth of 25-MHz, the measured voltage gain is 26 dB and the input S_{11} is -13 dB. Under the same baising condition, the input third-order intermodulation product (IIP_3) and input-referred 1-dB compression point ($P_{o,1\text{-}dB}$) are - 21.5 dBm and -31.5 dBm respectively. The image rejection at 140-MHz away from the desired signal is 20 dB. In addition, the Q of the amplifier can be tuned from around 2 to infinity and the center frequency can also be varied from 930 MHz to 1040 MHz. On the grounds that the measured on-chip spiral's quality factor is merely around 2 (compared to around 3 to 5 in recent literatures), the measured noise figure of the whole amplifier is around 10 dB. The power dissipation and the die area of the first prototype are 90 mW and 1.2 $mm \times 0.8\ mm$ respectively.

So as to enhance the image rejection ability and to reduce the power consumption, a sixth-

order bandpass amplifier had been implemented and fabricated in standard 0.5μm CMOS process using 2-V supply. In this second prototype, a bandpass amplifier was cascaded with two identical second-order bandpass filters to realize the sixth-order bandpass response.

For the bandpass amplifier in the second prototype, the measured voltage gain is 26 dB at 832 MHz and a S_{11} of -14 dB. With an overall 3-dB bandwidth of 25-MHz, the measured IIP_3 and the 1-dB compression point of the bandpass amplifier are -18.5 dBm and -29 dBm respectively. Besides, the center frequency can be varied between 760 MHz and 832 MHz. The measured noise figure is 9.6 dB, which is much higher than the simulation due to inadequate modeling of the thermal noise in short-channel MOSFETs and the use of low-quality inductors.

Meanwhile, the performance of the three-stage design in the second prototype was tested, the measured center frequency of the design is located at 830 MHz with a gain of 16 dB. The corresponding 3-dB bandwidth is 25 MHz and the image rejection at 140 MHz away from the desired signal is around 45 dB. In addition, the input third-order intermodulation product (IIP_3) and the input-referred 1-dB compression point are -15 dBm and -26 dBm respectively. The total current consumption of the three-stage design is 90 mA and the die area of the circuit is only $1.2\ \ mm \times 0.8\ \ mm$ as two-layer inductors were utilized in the design.

Acknowledgment

At this moment, I believe, is the most suitable time for me to express my heartfelt gratitude to the people who have helped me and supported me during this two-year of studies. Without their help, I can not complete this work on time.

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Chapter 1

Overview

1.1 Motivation

The recent upsurge in the demand for low-power portable wireless communication products creates a lot of research opportunities in both system design and hardware implementation. Some of the popular applications include mobile phones, pagers, wireless LANs (local area networks), RFIDs (radio frequency identification systems). In the past decades, radio-frequency (RF) circuits were dominated by GaAs and silicon bipolar technologies, which exhibit much higher unity-gain frequencies (f_t), higher device transconductance (gm) and better noise performance than complementary metal-oxide-semiconductor (CMOS) counterparts. Because the components implemented in these technologies were incompatible with the digital integrated circuits that were usually realized in CMOS domains, wireless systems often comprise several ICs and many discrete components. As a result, the size and the power dissipation of these applications are inevitably large.

Meanwhile, the advancement in digital sub-micron CMOS technology and the continuous

down scaling in CMOS device size have made low-cost and small-size implementation of CMOS RF integrated circuits (ICs) more and more feasible. As digital CMOS technology is known for its low-power dissipation and high density, it provides an attractive solution for integrating analog RF front-end with digital baseband back-ends in a single chip.

1.2 Technical Challenges

Even though CMOS technology has provided a lot of attractions, there are still many technical hurdles needed to be overcome before monolithic integration of a transceiver is possible. The realization of some RF circuits in CMOS technology, including low-noise amplifiers (LNAs) [2], image-reject mixers [6] and voltage-controlled oscillators (VCOs) [7] [8] have been demonstrated in recent literatures. These circuits have comparable performance in terms of linearity, power consumption and noise to those implemented in GaAs and bipolar technologies. Nevertheless, passive on-chip elements, such as inductors and resistors have poor quality and large process variations, and thus some of the key components in a wireless receiver, for example, image-reject filters and intermediate-frequency (IF) channel selection filters, are still usually found to be off-chip.

On-chip planar inductors emerge in CMOS substrate for more than a decade yet their quality factor Q is so low that they were not used in practical circuits, e.g. LNAs, LC-oscillators, until recent years. The low Q is resulted from the highly resistive lossy substrate, which increases high-frequency resistive losses through the lossy substrate [20]. Recently, improvement has been made in reducing the losses of spiral inductor's by etching away the lossy substrate [27], inserting ploy-Si shielding [11], or using highly-conductive copper interconnecting layers [10].

Nonetheless, these methods are not commercially compatible with mainstream digital CMOS technology. The maximum achievable Q of planar inductors in modern CMOS technology is usually less than ten and more commonly less than five.

1.3 Research Goals

The implementation of a single chip wireless transceiver [3] [27] [33] [34] [35] is still one of the hottest research topics in Radio Frequency Integrated Circuit (RFIC) design. Although many obstacles need to be circumvented, recent publications have demonstrated the possibility to implement the RF circuits and the RF front-ends in standard CMOS technology. As a result, it is worthwhile to devote effort to explore the area.

LNAs and especially RF image-reject filters are usually implemented either off-chip or with incompatible hybrid technologies. It is not until recently found that they can be constructed in CMOS technology with some reasonable performance [14] [16]. This thesis explores the design of a bandpass amplifier [5], which can be considered as a Q-enhanced low noise amplifier. It not only amplifies the received signal as a LNA but also helps in rejecting the blocking signals outside the 25-MHz receiver band. It is realized with a compensation circuit to improve the overall Q of the output resonant circuit. The details will be discussed in depth later. Because the Q is enhanced, the image rejection of the bandpass amplifier is also improved and it helps to share the burden of the image-reject filter. Accordingly, the implementation of the image-reject filter on CMOS technology becomes more feasible. As a part of the research work, a RF bandpass filter is designed and cascaded with the original bandpass amplifier in an attempt to provide enough image rejection at the image frequency so that the off-chip image-reject filter can be eliminated.

1.4 Thesis Outline

As an introduction, some important receiver specifications that are related to the design of the bandpass amplifier are reviewed in Chapter 2, and the RF fundamentals such as linearity, noise figure and sensitivity are defined as well.

Chapter 3 covers the basic LNA design and tuning circuits. Different types of input matching, the working principles of the resonant circuit, Q-compensation and frequency tuning circuit. Simulation results are also included to demonstrate the functionality.

To optimize the design in terms of noise, power and linearity, a detailed noise analysis of the bandpass amplifier including tuning circuits are presented in Chapter 4. The analysis provides some hints on optimizing the noise figure of the complete circuit.

The linearity of the bandpass amplifier is much lower than that of typical LNAs due to the Q-compensation circuitry. In Chapter 5, origins of the non-linearity of the circuit are explained. Different type of linearization methods are addressed in terms of their pros and cons. To improve the bandpass amplifier's poor linearity, a proposed linearized circuit is explained and simulation results are presented as well.

Chapter 6 first describes the design of a simple second-order LC filter. Then, the general design of a three-stage, sixth-order bandpass amplifier that is realized by cascading a bandpass amplifier and two second-order bandpass filters, is presented. Design issues such as the allocation of the gain, the center frequency and the quality factor among the three stages are also mentioned

Layout consideration regarding to the bandpass amplifier and bandpass filter are presented in Chapter 7. Furthermore, measurement results are discussed in Chapter 8. Finally, a conclusion is summarized in Chapter 9.

Chapter 2

RF Fundamentals

2.1 Introduction

This chapter provides some general background to facilitate the discussion of the bandpass amplifier. Firstly, important parameters for evaluating the performance of LNA will be described. Then, a brief review of the GSM receiver standard and how the specification of the standard affects the design of the amplifier will be addressed.

2.2 Basic RF Fundamentals

In this section, we will explore some of the useful parameters for RF receivers and individual RF circuit designs, namely, sensitivity, noise figure, linearity, IIP_3 and 1-dB compression point.

2.2.1 Sensitivity

To measure how well a RF circuit can pick up the weak signal from a noisy frequency spectrum, sensitivity is defined as the minimum signal level that a circuit can detect with certain

signal-to-noise ratio (SNR). Quantitatively, sensitivity is usually measured in terms of the minimum detectable signal (MDS) that a circuit or a system can detect and demodulate correctly. The minimum detectable signal ($P_{in,min}$) can be expressed as

$$P_{in,\,min} = P_{Rs} + NF + 10\log B_c + SNR_{min}, \tag{2.1}$$

where P_{Rs} is the source resistance noise power, NF is the noise figure of a system, SNR_{min} is the minimum acceptable signal-to-noise ratio and B is the bandwidth of the system. It should be noted that all the quantities are in dB scale.

For a 50-Ω source resistance, the source resistance noise power P_{Rs} is

$$\begin{aligned} P_{Rs} &= \frac{4kTR_s}{4}\frac{1}{R_s} \\ &= -174 \;\; dBm/Hz. \end{aligned} \tag{2.2}$$

Other than P_{Rs}, the other three quantities vary with different systems. For GSM standard, with a channel bandwidth (B_c) of 200 kHz, noise figure (NF) of 9 dB and SNR_{min} of 10 dB, MDS can be calculated as -102 dBm.

2.2.2 Noise Figure (NF)

The signals received at the antenna most likely are very weak and have to be amplified in order to drive the mixer. So as not to further deteriorate the SNR of the received signal, the circuits afterwards should be designed to add as small noise as possible especially at the front end of the receiver. Noise figure is a measure of the amount of noise added after the signal goes through a circuit and it is defined as the ratio of the available output noise power to available output noise due to the source (a 50-Ω impedance),

$$F = \frac{S_i/N_i}{S_o/N_o} = \frac{SNR_{in}}{SNR_{out}}. \quad (2.3)$$

$$F = \frac{S_i}{N_i}\frac{(N_iG + N_{c,o})}{S_iG} = 1 + \frac{N_{c,o}}{N_iG} = 1 + \frac{N_{c,i}}{N_i}, \quad (2.4)$$

where $N_{c,i}$ and $N_{c,o}$ are circuit's input-referred and output-referred noise, respectively. G is the gain of the circuit and N_i is the source noise power. Noise Figure (NF) is usually expressed in log scale (dB) and the noise factor is the corresponding value in linear scale. In this dissertation, the noise performance is evaluated in terms of noise figure. The relationship between noise figure (NF) and noise factor (F) are as follows:

$$NF(in\ \ dB) = 10 \bullet \log F\ . \quad (2.5)$$

2.2.3 Linearity

As the frequency spectrum is limited, an ISM frequency band usually assigns with more than one applications, it is likely that the received signal is close to a strong interferer. This situation is more severe if the received signal is already weak when it reaches at the antenna. Desensitization and blocking phenomenon occurs. This is due to the non-linear property of active devices.

Ideally, the input-output relationship of a linear, time-invariant system can be modeled as

$$y(t) = a_1x(t), \quad (2.6)$$

where x(t) and y(t) are the input and output of the non-linear system, But, due to non-linearity, the system input-output relationship si modified to be

$$y(t) = a_1x(t) + a_2x^2(t) + a_3x^3(t) + \ldots\ , \quad (2.7)$$

The coefficients a_2, a_3 provide information on the non-linearity of a device or a circuit. When a sinusoidal signal Acosωt is applied to the system in Eq. (2.7), the output y(t) would be

$$y(t) = \frac{a_2 A^2}{2} + \left(a_1 + \frac{3a_3 A^2}{4} \right) A\cos\omega t + \frac{a_2 A^2}{2}\cos 2\omega t + \frac{a_3 A^3}{4}\cos 3\omega t . \qquad (2.8)$$

From Eq. (2.8), the output contains not only the fundamental frequency term, but also many higher order harmonics caused by $x^2(t)$ and $x^3(t)$. Typically, high-order terms are negligible. However as the input amplitude becomes large enough, their effects become to affect the output significant. If the circuit is implemented in fully-differential architecture, the even-order harmonics can usually be neglected. Among the high-order harmonics, the most troublesome the third-order. Several important parameters that affect the performance of analog and RF circuits are now described.

2.2.3.1 1-dB compression point

1-dB compression point is defined as the input signal amplitude at which the output of the signal deviates from the ideal response by 1-dB, and it is depicted in Fig. 2.1. In Eq. (2.7), the first-order coefficient includes two terms, the desired gain a_1, and the undesired term $3a_3A^3/4$. For small input amplitude A, the first term dominates and the output is linearly dependent on the input. However, due to non-linearity, when the input signal amplitude is large, the gain of the fundamental frequency begins to diminish because a_1 and a_3 are usually of opposite sign; thus, the term $a_1 A$ and $3a_3A^3/4$ cancel each other. The typical 1-dB compression point of a MOSFET device occurs at around -20 to -25 dBm.

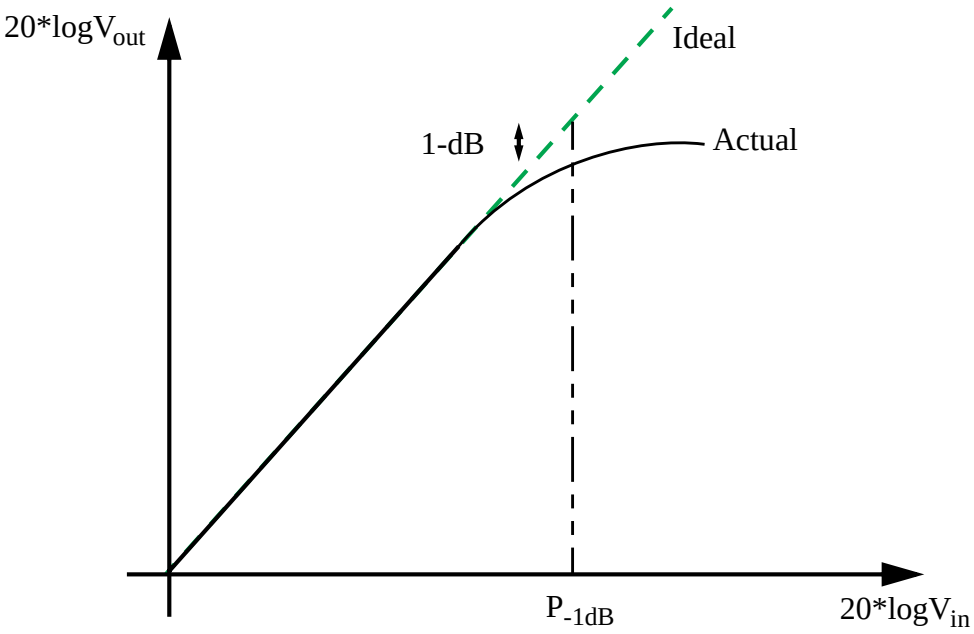


Fig. 2.1 The plot of 1-dB compression point

2.2.3.2 Third-order Intermodulation Distortion

Another key parameter to evaluate the linearity of a circuit is intermodulation distortion. When two closely spaced signals mix with each other, they produce signals with frequencies other than the high-order harmonics of the two signals. The most severe distortion is called third-order intermodulation due to the non-linear x^3 term. If the two signals are $A_1\cos\omega_1 t$ and $A_2\cos\omega_2 t$ are applied to a system like Eq. (2.7), the output will consist of frequency terms $\cos\omega_1 t$, $\cos\omega_2 t$, $\cos(2\omega_1+\omega_2)t$ and $\cos(2\omega_1-\omega_2)t$. Intermodulation causes trouble when a weak signal is closed to two strong interferer shown in Fig. 2.2. At the desired signal frequency, the amplitude of the intermodulation product sometimes is much larger than that of the signal. As a result, the desired signal is corrupted. The third order intermodulation (IM) can be measured by applying two tones $A\cos\omega_1 t$ and $A\cos\omega_2 t$ at the input of the circuit, the amplitude of the intermodulation product is measured at the output of the circuit. A plot of the output signal versus the input signal of both

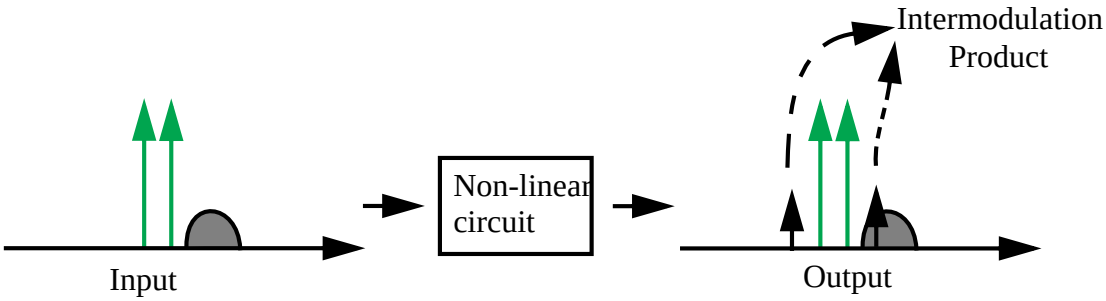


Fig. 2.2 Illustration of the intermodulation product

fundamental and intermodulation product frequency is in logarithmic scale is shown in Fig. 2.3.

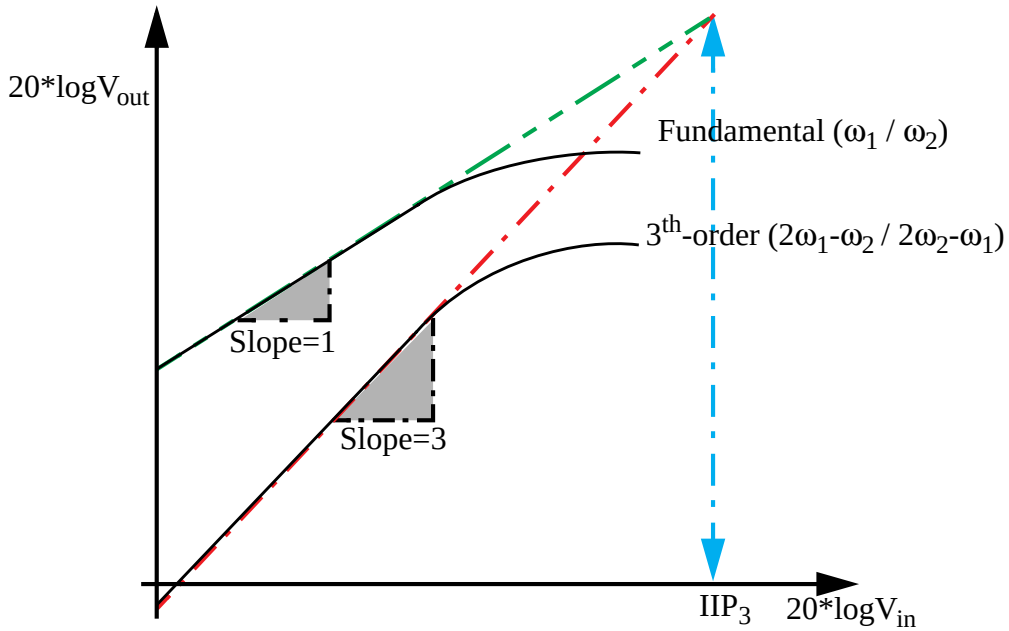


Fig. 2.3 The plot of IIP_3

The third-order IM product increases at a rate of 3 while the fundamental frequency increases at a rate of 1. Third-order intermodulation product (IP_3) is used to measure the distortion, which occurs when the third-order IM product equals the fundamental signal amplitude. Indeed, it does not occur in practical due to the compressive nature of the circuit. The

IP3 is calculated by extrapolating both components until they finally intercept with each other. The input-referred IP_3 is called IIP_3. The IIP_3 can be calculated as

$$IIP_3 = \frac{P_{out} - P_{out,IM3}}{2} + P_{in}, \tag{2.9}$$

where P_{out} is the fundamental output power, $P_{out,IM3}$ is the output IM_3 power and P_{in} is the input power.

2.2.3.3 Desensitization and Blocking

Blocking occurs when the weak signal is accompanied by a strong interferer that is closed to the received signal, from other wireless applications or other users. This interferer reduces the overall gain of the circuit. As a result, the weak signal received will experience a smaller gain, and this is termed as desensitization. When the interferer's signal amplitude is large enough to reduce the overall gain of the circuit to zero, the phenomena is known as blocking.

2.2.4 Quality Factor (Q-Factor)

Before discussing the quality factor, a simple parallel RLC circuit in Fig. 2.4 is considered. It can readily be proved that the impedance Z(s) is

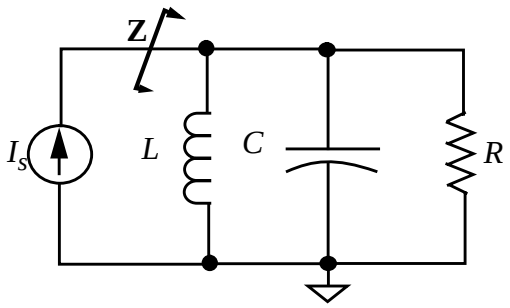


Fig. 2.4 A general second-order parallel resonant circuit

$$Z(s) = \frac{s/C}{s^2 + s/RC + 1/LC} = \frac{sk}{s^2 + s\omega_{-3dB} + \omega_o^2} = \frac{sk}{s^2 + s\frac{\omega_o}{Q} + \omega_o^2}, \quad (2.10)$$

where k is a constant, $\omega_o = 1/LC$ and $\omega_{-3dB} = 1/RC$. ω_o is the resonant frequency, which is defined as the frequency at which the imaginary part in Eq. (2.10) vanishes. ω_{-3dB} is the 3-dB bandwidth of the transfer function. The frequency response is given in Fig. 2.5.

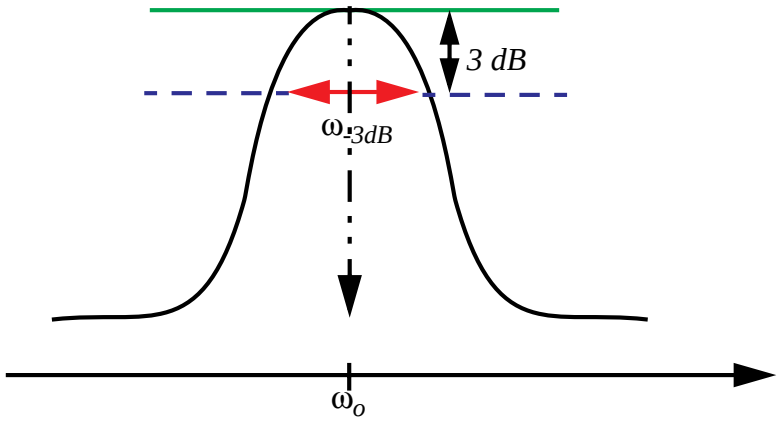


Fig. 2.5 The frequency response of a bandpass transfer function

The ability of a bandpass circuit to reject the out-of-band signals is termed as selectivity. It is usually expressed in terms of quality factor Q,

$$Q = \left(\frac{\omega_o}{\omega_{-3dB}}\right). \quad (2.11)$$

It is equal to the ratio of the resonant frequency to 3-dB bandwidth. The higher is the quality factor, the smaller is the 3-dB bandwidth and the better is the selectivity. Furthermore, the

roll-off of the second-order transfer function in Eq. (2.10) outside frequencies outside the band is 20 dB/decade, i.e. if the 3-dB bandwidth of the response is 25 MHz, the attenuation at 140 MHz away from the resonant frequency is around 18 dB.

2.3 GSM standards and System architecture

Global System for Mobile Communications, or GSM for short, is one of the most widely used wireless communications standard over the past decades. The standard also imposes one of the hardest specifications to be met by system and circuit designers. The frequency band assigned for GSM applications has been divided into two portions, namely the transmitter band (895 - 915 MHz) and the receiver band (935 -960 MHz). The blocking signal levels in the GSM standard are illustrated in Fig. 2.6. The input and output impedance of RF circuits is often 50-Ω matched to

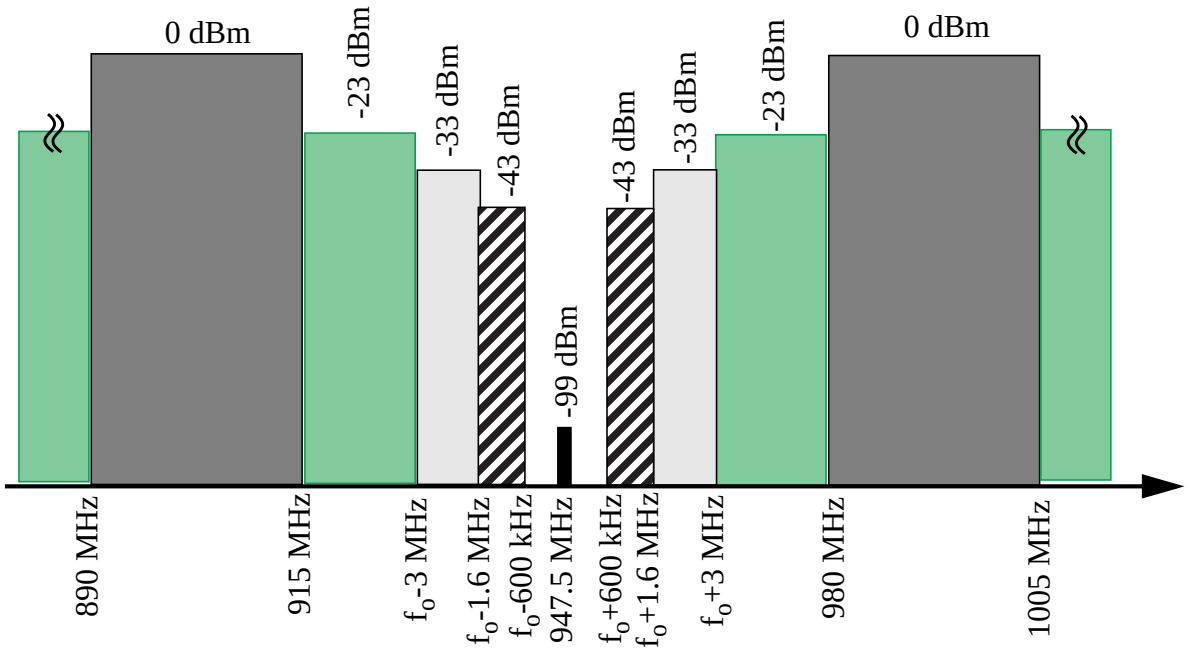


Fig. 2.6 Blocking signals levels of the GSM Standard

provide maximum power transfer and RF signals are usually expressed in terms of dBm or dBV.

The definitions of these two units are presented here as

$$dBm = 10\log\frac{(Power\ \ in\ \ W)}{1mW} \tag{2.12}$$

and

$$dBV = 20\log\left(\frac{V_{rms}}{1V_{rms}}\right). \tag{2.13}$$

1 dBm is 13 dB larger than 1 dBV.

Different receiver architectures have their own strength and weaknesses. Direct conversion is the simplest architecture, however, it suffers from many problems e.g. dc offset and even-order harmonics. Super-heterodyne structure is better than direct conversion in these aspects. On the other hand, the implementation requires a lot of highly selective passive components like image-reject filters and channel-selection filters that make monolithic integration of the receiver very difficult. To fulfill the ultimate goal of a single-chip receiver or even a transceiver, several key components such as LNAs, mixers and frequency synthesizers are designed as part of a GSM receiver with single-IF (70 MHz) superheterodyne architecture. The system is shown in Fig. 2.7.

The discussion here is focused on the design of LNA or bandpass amplifier.

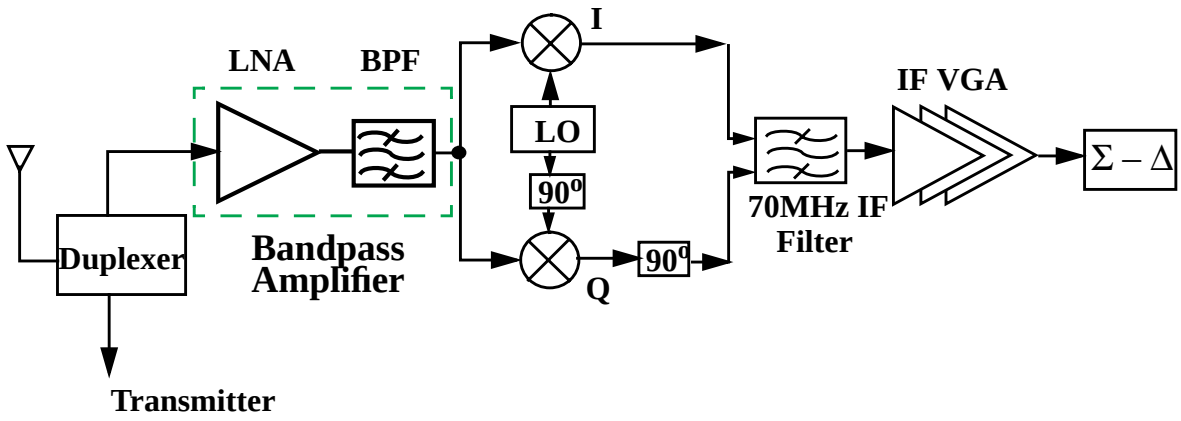


Fig. 2.7 A superheterodyne receiver architecture with single IF and I & Q channel

2.3.1 Minimum and Maximum Tolerable Signals

Minimum detectable signal (MDS) specified as -102 dBm within the 25 MHz GSM receiver band. For maximum signal level, 0 dBm blocking signals at frequency below 915 MHz and above 980 MHz pose stringent requirements on the linearity of the LNA. Even though a duplexer is often inserted in front of a LNA in a transceiver, the blocking signals can at most be attenuated by about 25 dB. It implies that the LNA's 1-dB compression point needs to be much larger than -25 dBm.

2.3.2 Noise Figure

As mentioned in 2.3.1, the MDS of the GSM standard is -102 dBm. The signal-to-noise ratio (SNR) is at least 9 dB to achieve a bit error rate (BER) < 10^{-4}. Meanwhile, the noise spectral density of the antenna (50-Ω matched) or a 50-Ω source resistor at 290K is -174 dBm ($4kT(50)$) and the channel bandwidth (B_c) is 200 kHz. Thus, the minimum noise floor is -121 dBm. The

noise figure is related to the minimum input signal by

$$P_{in,min} = -174\ dBm/Hz + NF + 10\log B_c + SNR \qquad (2.14)$$

The maximum system noise figure (NF) can be calculated from Eq. (2.14) as 9 dB. The noise contribution of all the stages after the LNA is usually large in our design, but due to the large gain of the LNA, the equivalent input-referred noise is small compared to the LNA noise. As a consequence, the noise figure of the LNA is set to be around 6 dB to leave 3 dB margin for later stages.

2.3.3 Image Rejection

Due to the limited frequency spectrum that can be used in wireless communications, radio receivers must be able to select the weak signal from the strong interfering signals which lie close to the receiver band. As a result, image rejection is a very important parameter to evaluate the performance of a radio receiver. Without loss of generality, let us assume that a low-sideband conversion is employed, i.e. the local oscillator (LO) frequency is 70 MHz (IF frequency) lower than the desired signal (ω_{RF}). As illustrated in Fig. 2.8, there usually exists undesired signals located at 70 MHz below the LO frequency referred to as image frequency (ω_{LO}). Due to the

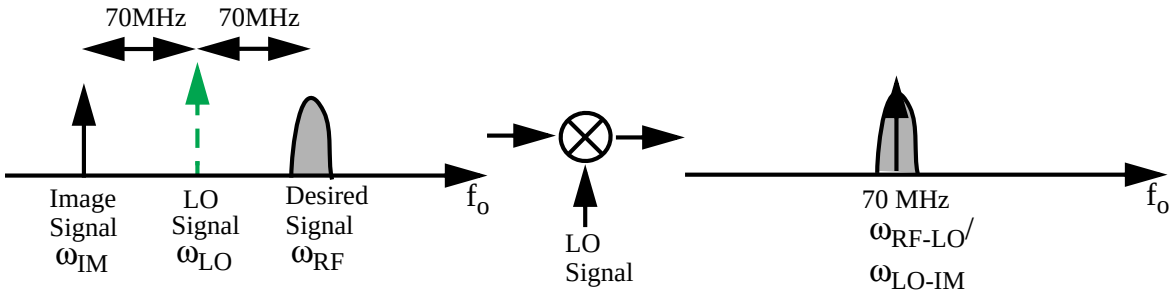


Fig. 2.8 Illustration of the effect of image signal

mixing, both the desired and image signals shown in Fig. 2.8 modulate with the LO ($\sin\omega_{LO}t$) signal and produce frequency components including $\sin(\omega_{RF}+\omega_{LO})t$, $\sin(\omega_{RF}-\omega_{LO})t$, $\sin(\omega_{LO}+\omega_{IM})t$ and $\sin(\omega_{LO}+\omega_{IM})t$. In this case, the frequency components $\sin(\omega_{RF}-\omega_{LO})t$ and $\sin(\omega_{LO}+\omega_{IM})t$ coincide and cannot be separated after mixing. If the image signal is large enough, the modulated image signal corrupts the desired signal and degrades the SNR. Therefore, the image signal needs to be attenuated before entering the mixer.

As an example, the image rejection (IR) of a GSM receiver with single IF being at 70MHz is calculated. The blocking signal level (Fig. 2.6) at 140 MHz away from the receiver band is -23 dBm and the MDS of the GSM standard is -102 dBm. To achieve a 9 dB SNR ratio of the whole system, the blocking signals need to be smaller than the MDS by at least 9 dB. Therefore, the attenuation of the image signal at 140 MHz away from the desired signal should be equal to $IR = -23-(-99)+9 = 85dB$. This value of image rejection is very difficult to be achieved with today's receiver architecture, not to mention a single-chip implementation.

In the GSM receiver architecture shown in Fig. 2.7, in-phase (I) & quadrature-phase (Q) channels have been employed to provide some image rejection for the whole system. Owing to the amplitude and phase mismatches of the I and Q channels, typically within 1 dB and 1^{o} respectively, the image rejection achieved is at most 35 to 40 dB. To maintain 80 dB image rejection, the combination of LNA and RF image rejection filter must be able to provide the remaining 40 dB attenuation at the image frequency.

Chapter 3

Design of Low-Noise Amplifier (LNA) and Bandpass Amplifier

3.1 Introduction

Low-noise amplifier (LNA) is the first component in a wireless receiver; it not merely provides enough gain to amplify weak signals received from the antenna but also needs to contribute minimum noise to the received signal so that the signal-to-noise ratio will not be severely degraded by the circuit. Another feature of a LNA is the ability to sustain large signals without distortion. Because the preceding stage of a LNA is either an antenna or a RF bandpass filter, the input needs to be well matched to 50-Ω so that maximum power transfer can be achieved. The general requirement [13] of a LNA is summarized in Table 3.1.

Parameter(s)	**Specification(s)**
Noise Figure	~ 3 dB
IIP_3	-10 dBm
Gain	15 - 20 dB
Input impedance	50–Ω

Table 3.1 General specifications of a LNA in super-heterodyne systems

Based on the GSM specifications described in Chapter 2, the LNA requirements in Table 3.1 are modified and tabulated in Table 3.2.1. In conventional LNA design, inductors are realized using bond-wire to minimize the noise figure, nonetheless, it is the best if they can also be integrated on the same chip. As a consequence, inductors in both the matching network and the resonant circuit are on-chip. These on-chip spirals are lossy and generate a lot of noise, therefore, a large gain is required to mitigate the total noise figure. At the same time, they needs to be compensated so that a better Q can be achieved. Therefore, the total noise figure has to be increased to around 6 dB to account for the lossy inductors and the compensation circuits. Meanwhile, as the amplifier gain is high to reduce the noise figure, the linearity of a bandpass amplifier is degraded and is usually much lower than conventional LNAs. The linearity requirement is adjusted so that the amplifier can meet the minimum GSM standard, yet this value is still very tough to be achieved. The 3-dB bandwidth of the amplifier is set to be 25-MHz to filter out the blocking and image signals.

Parameters	**Requirement**
Gain	20 - 30 dB
IIP_3	- 18 dBm
Image Rejection	~ 20 dB
3-dB Bandwidth	25 MHz
Center frequency	940 ~ 950 MHz
Noise Figure	~ 5 - 6 dB

Table 3.2: Modified Requirement for the bandpass amplifier

3.2 Basic LNA Design

In this section, important design parameters of a LNA will be presented including the input matching, LNA topology and the output resonant tank.

3.2.1 Input Matching

As discussed before, the input of a LNA needs to be matched to 50-Ω to ensure maximum power transfer. There are several types of input matching that can be employed in the design.

The first one is to insert a real 50-Ω resistor in parallel with the input of device shown in Fig. 3.1 so that 50-Ω matching can be guaranteed at any frequencies. It is the simplest way, but

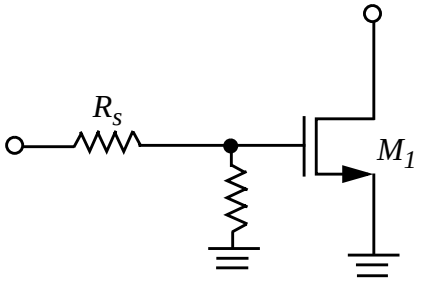


Fig. 3.1 Input matching using 50-Ω resistor

not an effective way to be utilized for LNA design. The major drawback is poor noise performance because the noise contributed from the 50-Ω resistor is exactly the same as that of a 50-Ω source resistor. As a consequence, the noise figure of this configuration would exceed 3 dB.

Common-gate configuration is another method to realize the input matching as illustrated in Fig. 3.2. It is known that the impedance looking from the source of a device is $\frac{1}{gm}$, and an input impedance of 50-Ω can be achieved by properly biased the input device M_1. The

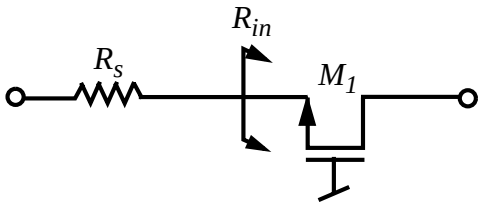


Fig. 3.2 Input matching using common-gate configuration

disadvantage of this approach is that the transconductance of the input device is fixed, the noise after the input device M_1 cannot be reduced by simply increasing the transconductance of the input device.

The noise factor (F) of the configuration is

$$NF = \left(\frac{4kTR_S + 4kT\gamma gm}{4kTR_S}\right)$$
$$= (1 + \gamma) \quad . \tag{3.1}$$

As stated in Chapter 2, there is actually no difference between noise factor and noise figure, the former will be used in the following discussion

For long-channel devices, $\gamma = \frac{2}{3}$, and the minimum NF would be around 2.2 dB. However, for short-channel device, γ can be as large as 2 to 3, and NF would approach to 6 dB. Therefore, the configuration is not commonly used as well.

Another method is inductive source degeneration, which is given in Fig. 3.3. The input impedance Z_{in} is equal to

$$Z_{in}(s) = sL_g + sL_s + \frac{1}{sC_{gs}} + \frac{gm}{C_{gs}}L_s = sL_g + sL_s + \frac{1}{sC_{gs}} + \omega_T L_s \ , \tag{3.2}$$

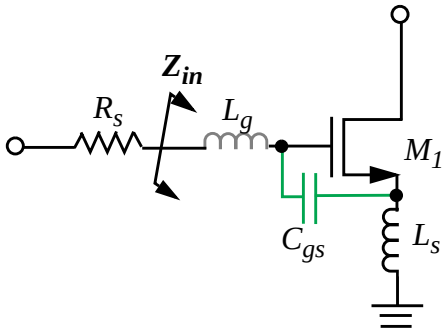


Fig. 3.3 Input matching using inductive source degeneration

where L_g, L_s and C_{gs} are the gate inductance, the source inductance and the gate-to-source capacitance of M_1 respectively. ω_T is defined as g_m/C_{gs}, unity-gain frequency. The imaginary part vanishes at ω_o, where $\omega_o = \frac{1}{\sqrt{(L_g + L_s)C_{gs}}}$. At resonance, the impedance Z_{in} is purely resistive and equal to

$$Z_{in}(\omega_o) = \omega_T L_s, \tag{3.3}$$

The advantage of this configuration is that the resistive term in Eq. (3.2) is not realized using a physical resistor or its equivalents, and it is therefore theoretically noiseless. However, if on-chip spiral inductors are used, their noise contribution due to the resistive losses cannot be neglected. To take the resistive losses into account, the modified output impedance Z_{in} is

$$Z_{in}(s) = sL_g + sL_s + \frac{1}{sC_{gs}} + \frac{g_m}{C_{gs}}L_s + R_g + R_l = sL_g + sL_s + \frac{1}{sC_{gs}} + \omega_T L_s + R_g + R_l, \tag{3.4}$$

where R_g and R_l represent the series loss of the inductor L_g and L_s respectively. The real part of Z_{in} becomes

$$Z_{in}(\omega_o) = \omega_T L_s + R_g + R_l. \tag{3.5}$$

If inductors are realized using bond-wire, the quality factor can be as high as 50 and the noise degradation due to lossy inductors are very small. Nonetheless, if inductors are achieved using on-chip spirals, the quality factor is usually limited to around 5. This degrades the noise performance of the whole circuit. The detailed noise analysis is going to be discussed in depth in Chapter 4. To investigate how the resistive component in spiral inductors affects the input matching, a plot of the input matching of the LNA employing the inductive degeneration near resonance under different inductor's quality factor are displayed in Fig. 3.4. It should be noted that the resistive losses of the spirals contributes a large portion in the 50-Ω matching. When Q is set to 5, the input impedance drops to around 30-Ω. As mentioned above, no noisy resistive component in the inductive degeneration is the key advantage of this configuration. However, the planar inductor's loss reduces the advantage and limits the noise performance of the design. Actually, more than 20 Ω of the matching originates from the resistive loss and it inevitably produces noise at the input which cannot be reduced by the gain of the amplifier. As an example, if 20-Ω of the matching is contributed from the inductor's resistive losses, the low limit of NF is around 2.2 dB already. As a result, the LNA has poor noise figure and the condition would be more severe if Q is lower than 2.5.

The noise figure of the configuration can be proved to be

$$F = 1 + \frac{R_g + R_l}{R_s} + \frac{\gamma (R_s \omega_o C_{gs})^2}{R_s gm} = 1 + \frac{R_g + R_l}{R_s} + \frac{\gamma R_s (\omega_o C_{gs})^2}{gm} . \quad (3.6)$$

From the expression, the term $1 + \frac{R_g + R_l}{R_s}$ is governed by the intrinsic Q of the inductor,

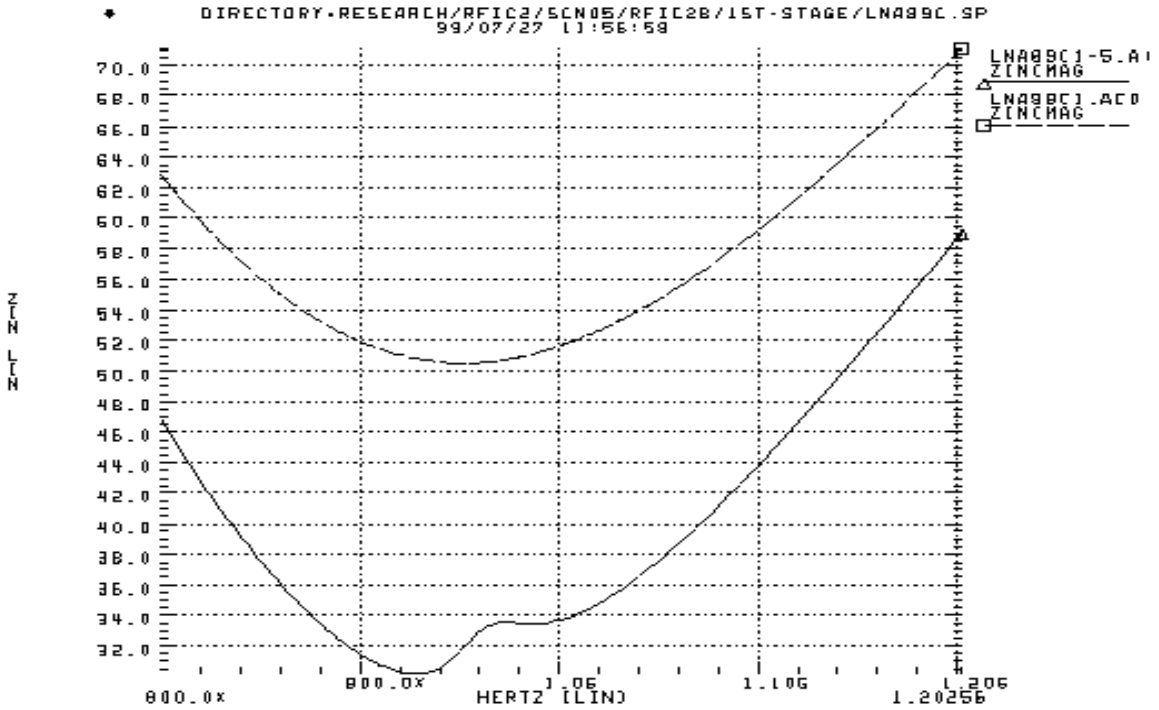


Fig. 3.4 The magnitude of the input matching under different inductor's Q

it cannot be altered unless the spiral's Q can be improved. The last term depends on two design constraints, gm and C_{gs}. The noise figure can be reduced by increasing the transconductance, but, it dissipates more power. Another method is to reduce C_{gs} by using minimum channel length (L), nonetheless, the reduction degrades the linearity as the Q of input matching network which is defined as

$$Q_{in} = \frac{1}{\omega C_{gs}(R_s + R_g + R_l + \omega_T L_s)} = \frac{1}{2\omega R_s C_{gs}} \tag{3.7}$$

increases when C_{gs} decreases. Accordingly, there are trade-offs between linearity and noise figure. In this design, the use of on-chip inductors poses additional constraints on the size of C_{gs}. It should be pointed out that a small C_{gs} is accompanied with a large L_g so that the series input resonant circuit resonants at the desired frequency. Therefore, L_g cannot be arbitrarily selected as

it also governs the input matching and the noise performance of the whole circuit. Balance should be made so that an optimum noise figure can be obtained.

3.2.2 LNA Topology

Even though the inductive source degeneration is not noiseless as deduced from the formula, its noise performance would be acceptable unless the inductor's Q is very low. The configuration has been chosen as the input matching of the LNA. In Eq. (3.5), the input matching is $\omega_T L_s$ if the resistive loss is omitted and it is clear that only L_s is involved. Indeed, the gate inductance L_g in the matching network is to combine with L_s and C_{gs} to provide narrowband response at the input. At resonance ω_o, the series resonant circuit impedance is at a minimum (R_s).

Another advantage of the configuration is that it provides current gain (G_i) at resonance, which is given by

$$G_i = \frac{gm_1}{sL_g + sL_s + \frac{1}{sC_{gs}} + \omega_T L_s + R_g + R_l + R_s}. \quad (3.8)$$

This current gain also reduces the noise from the following stages. The simulated input matching of the LNA design is depicted in Fig. 3.5. The input impedance at the frequency of interest is 101 Ω. The resonant frequency of the series RLC circuit is at 940 MHz and the S_{11} is -45 dB.

The basic architecture of a narrowband LNA is illustrated in Fig. 3.6.
It consists of a common-cascoded structure with the input matching described to reduce the noise from the output of the LNA and the subsequent stages. The cascode device M_2 was chosen to

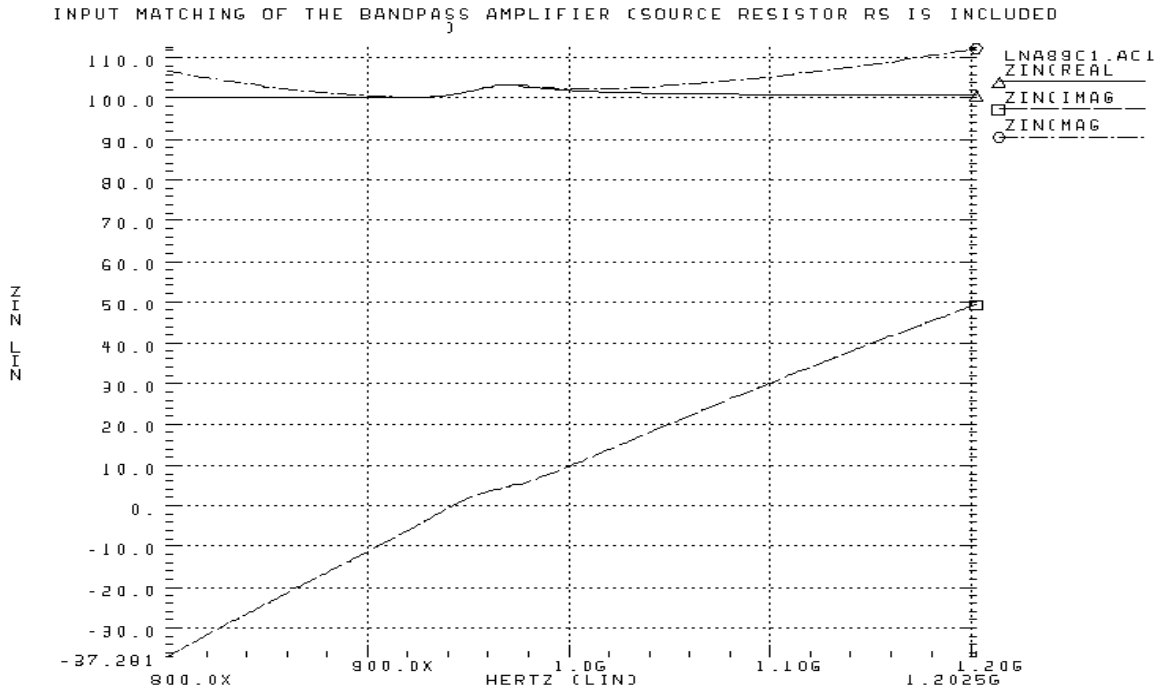


Fig. 3.5 The simulated input matching of the amplifier

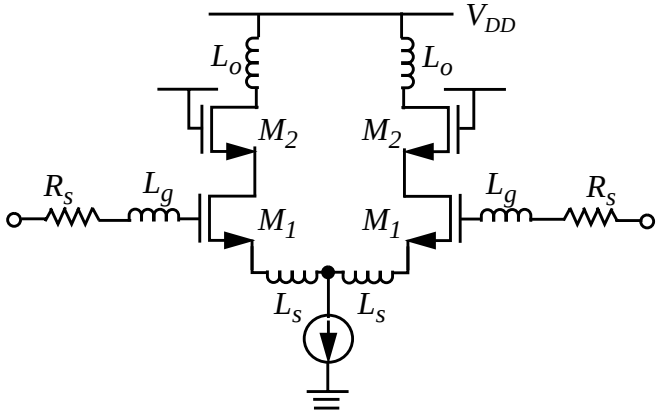


Fig. 3.6 The basic architecture of a common-cascoded LNA

improve the reverse isolation between the input and the output and alleviate the Miller effect of M_1 on the input matching. The LNA is implemented in differential manner to minimize even-order harmonics and improve the linearity. It also helps to reject the common-mode substrate noise and parasitics due to packaging. To provide the highest level of integration, all components are realized on-chip. The output of the LNA is a parallel LC resonant tank, which resonates at the

GSM's receiver band, 935 MHz to 960 MHz.

The transconductance of the amplifier is

$$Gm_{in}(s) = \frac{gm_1\left(\frac{1}{sC_{gs}}\right)}{sL_g + sL_s + \frac{1}{sC_{gs}} + \omega_T L_s + R_g + R_l + R_s}. \quad (3.9)$$

The imaginary part of the input impedance vanishes at resonance and merely the real part ($R_g + R_l + \omega_T L_s$) is left, which is designed to be equal to R_s. The transconductance at resonance is

$$Gm_{in}(\omega_o) = \frac{gm_1}{2\omega_o C_{gs} R_s} = \frac{\omega_T}{2\omega_o R_s} \quad (3.10)$$

From the expression in Eq. (3.10), the transconductance only depends on the ratio of gm/sC_{gs}. Since a smaller C_{gs} is accompanied with larger inductance values ($L_g + L_s$) for a given resonant frequency, it increases the size and the noise of the circuit.

3.2.3 Parallel RLC resonant circuit

After discussing the input matching circuit and the transconductance of the narrowband LNA, the output resonant circuit is now addressed. A lossy LC resonant tank is illustrated in Fig. 3.7. The circuit in Fig. 3.7a can be transformed into a parallel RLC circuit in Fig. 3.7b. The transformed L_p and R_p are

$$L_p = \frac{(Q^2 + 1)L_s}{Q^2} \quad (3.11)$$

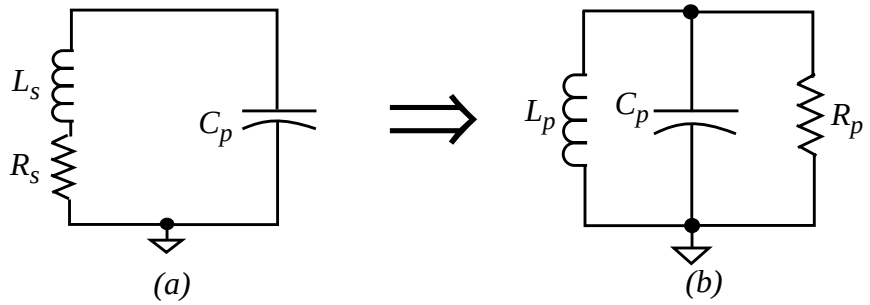


Fig. 3.7 A parallel lossy LC circuit

$$R_p = (Q^2 + 1)R_s \tag{3.12}$$

respectively, where Q is the quality factor of the inductor.

$$Q = \frac{\omega L_s}{R_s} . \tag{3.13}$$

The transfer function of this parallel RLC circuit is

$$Z(s) = \frac{\frac{s}{C_p}}{s^2 + \frac{s}{R_p C_p} + \frac{1}{L_p C_p}}. \tag{3.14}$$

The corresponding natural frequency and the 3-dB bandwidth are given by

$$\omega_o = \frac{1}{\sqrt{L_p C_p}} \tag{3.15}$$

and

$$\omega_{-3\ dB} = \frac{1}{R_p C_p} . \tag{3.16}$$

So as to filter out the out-of-band blocking and image signals, the 3-dB bandwidth of this narrowband bandpass amplifier is 25 MHz, which is the bandwidth of the GSM receiver band

(935 -960 MHz). The Q of an LNA is usually dominated by the intrinsic Q of the output inductor (<5). Nonetheless, to attain a the specified bandwidth, the circuit's quality factor needs to be around 35 to 40. As a result, compensation methods have been proposed to cancel out the resistive losses of the spiral inductors and it is going to be discussed in Section 3.4.1.

3.2.4 Noise Considerations

Since low-noise figure is the one of the most important specification of a LNA, the noise considerations will be analyzed in depth in Chapter 4.

3.3 Monolithic Spirals [15] [32] [31]

3.3.1 Limitations of on-chip spirals

One of the critical limitations on integrating high performance LNAs and bandpass filters on chip are spiral inductors. Unlike resistors and capacitors, whose their values are well estimated except for variations due to the process (around 10%), on-chip spirals are still not well optimized in terms of shape, metal width, metal spacing, quality factor and value. Modern CMOS process usually consists of an heavily doped epi layer which is highly conductive, eddy current induced by the magnetic field of the inductor onto the substrate directly degrades the inductor performance.

3.3.2 General Spiral Inductor Model

A widely used inductor model [20] is depicted in Fig. 3.8, where R_s is the series resistance of the inductor L_s. C_s represents the capacitance between the spiral and the center-tap underpass.

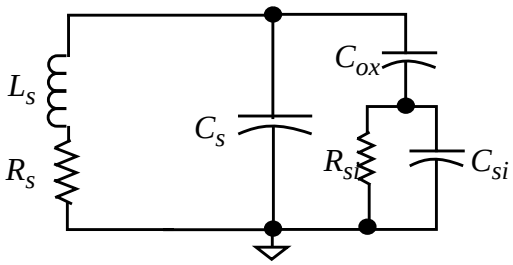


Fig. 3.8 A complete inductor model

C_{ox} is the capacitance between the spiral and the substrate. R_{si} and C_{si} models the lossy silicon substrate.

The losses of on-chip spirals is usually not limited only by the metal winding losses but also by the lossy silicon substrate. At low frequencies, the impedance of C_{ox} is very large, and the spiral is isolated from the lossy substrate. Thus, the loss is only contributed from the metal layer. As frequency increases, the impedance of C_{ox} decreases, and the resistive loss due to the substrate begins to increase. At high frequency, C_{ox} is virtually shorted and the substrate losses dominates. Thus, the resistive losses increases with the frequency instead of remaining constant. Some of the process information for 0.8 μm single-poly, triple metal CMOS is duplicated graphically in Fig. 3.9.

The inductance value (single-layer metal) is well estimated by the Greenhouse's formula [19]. A simple estimate of a spiral inductance can also be found to be [13]

$$L = \mu_o n^2 r, \tag{3.17}$$

where μ_o is the permeability of free space, n is the number of turns, and r is the radius of the inductor. To have a more accurate estimate of the inductance value, the inductor structure can be analyzed in 3-D electromagnetic simulator like SONNET EM [26]. Nonetheless, it is usually

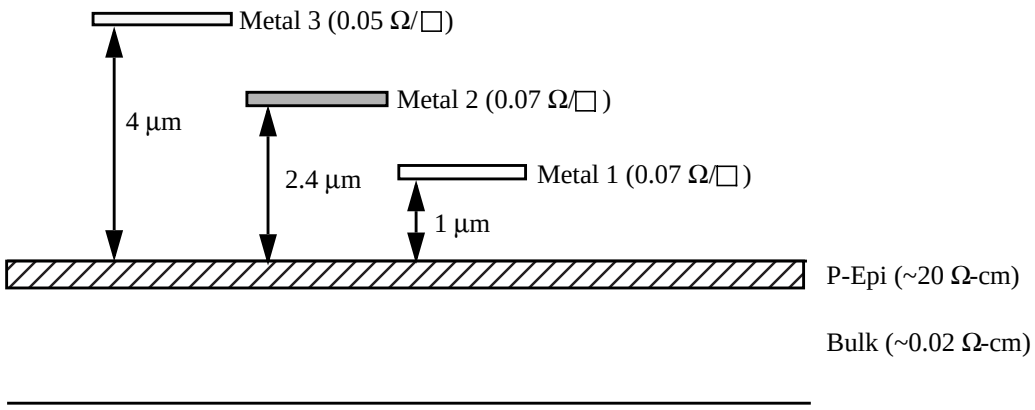


Fig. 3.9 General process information of a typical 0.8 μm CMOS (HP SCN26G)

time-consuming especially when the structure needs to be optimized using the simulator in terms of spacing, metal width and total area. As a compromise, another program ASITIC [21], which has been reported to have a good agreement between the modeling and the measurement result of the inductors on BiCMOS technology, is employed in the design to optimize the design. An attractive advantage of using the program is that it is much faster than E-M SONNET and circular inductor can also be analyzed. One of the drawbacks of the tool is that the simulator does not include the effect of eddy current in the substrate, which is not serious in a less-conductive BiCMOS substrate but quite important in lossy CMOS substrate. This accounts for the fact that the simulated high-frequency inductor's Q is much better than the measured one.

Monolithic spirals are usually put on the topmost metal (Metal 3 in our case) as the sheet resistance is the smallest (50 mΩ/□) and the separation between the spiral and the lossy substrate is the largest (4 μm). Besides, circular spirals are known to have higher Q than the square inductor with the same metal width, spacing. They are utilized in the design in an attempt to optimize the quality factor. Other design consideration such as metal spacing, number of turns, inner hole size will be discussed in Chapter 7.

3.4 Design of a bandpass amplifier

As discussed earlier in Chapter 2, the image-reject filter will be finally integrated together with other components in a single-chip transceiver. To realize the goal, the LNA in a receiver has to share the image rejection burden together with the on-chip RF bandpass filter so that the image rejection provided by the front-end is enough to meet the minimum requirement of the GSM standard and the off-chip image-reject filter can be eliminated. However, as stated in Section 3.3.1, the spiral inductor's Q is so low that the LNA utilizing them cannot provide much image rejection (~ 10 dB) and thus Q-compensation circuit is required to enhance or to compensate the loss in the spiral. After compensation, both the 3-dB bandwidth and the image rejection of a LNA can be greatly improved at the expense of larger noise figure and poorer linearity, which will be discussed later. The LNA with Q-compensation described below is termed as bandpass amplifier as it can provide not only signal amplification as conventional LNA but also filtering function as bandpass filters.

3.4.1 Q Compensation Technique

To compensate the losses due to low-quality spiral inductors, a negative conductance G_n is introduced in parallel to the resonant tank depicted in Fig. 3.10, where R_{eq} is the resultant parallel resistance. For ideal LC resonant tank, the energy is stored in the magnetic field of the inductor or in the electric field of the capacitor, and no energy is lost in the circuit. In practice, energy is dissipated in the non-ideal inductors and capacitors. This loss is represented as R_p in Fig. 3.10. So as to reduce the losses in the LC tank, the current flowing through the resistor R_p is partially provided by the negative conductance G_n rather than the LC resonant circuit. Accordingly, the LC

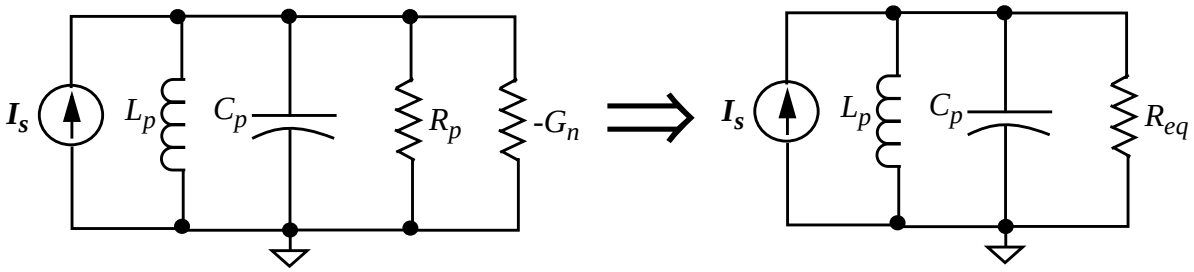


Fig. 3.10 A parallel LC resonant tank compensated with negative conductance

resonant circuit looks like to be lossless when all the current flowing through R_p is supplied by G_n. Nonetheless, it is unstable when the circuit is over-compensated, i.e. $G_n > R_p$.

To understand the role of the negative conductance in the circuit, the transfer function of the circuit in Fig. 3.10 is presented as

$$\begin{aligned} Z(s) &= (R_s + sL_s) \parallel \frac{1}{sC_p} \parallel \frac{1}{-G_n} \\ &= \frac{R_s + sL_s}{1 - G_n R_s + s^2 L_s C_p + s(R_s C_p - G_n L_s)}. \end{aligned} \tag{3.18}$$

The center frequency and the impedance at resonance can be proved as

$$\omega_c = \sqrt{\frac{1}{L_s C_p}\left(\sqrt{1 - 2G_n R_s + \frac{2R_s C_p}{L_s}} - \frac{R_s^2 C_p}{L_s}\right)} \tag{3.19}$$

and

$$R_{eq} \approx \frac{1}{R_s\left(1 + Q_o^2\right) - G_n}. \tag{3.20}$$

From Eq. (3.19), it is clearly that the center frequency ω_c depends not only on the choice of L_s and C_p but also varies when G_n is changed.

The quality factor Q_c of an output resonant circuit is

$$Q_c = R_{eq}\sqrt{\frac{C_p}{L_p}}, \tag{3.21}$$

where R_{eq} is the compensated parallel resistance at resonance. Q_c is defined in order to distinguish the Q between a resonant tank and the Q of an inductor.

Firstly, from eqs. (3.12) and (3.13), it is obvious that R_p is directly proportional to L_p. An increase in L_p results in a larger parallel equivalent R_p. As a result, a smaller negative conductance is required to compensate the parallel resonant circuit to achieve the same Q_c and it reduces the power consumption of the Q-compensation circuit. From Eq. (3.21), the output resistance R_{eq} in Fig. 3.10 is governed by the choice of L_p and C_p. To keep the product L_pC_p unchanged, an increase in inductor value L_p is accompanied with a reduction of C_p. This in turns increases both R_{eq} (for the same Q_c) and the overall gain at the same time. Because the linearity of an amplifier will be degraded with a high amplifier's gain, there exists a constraint on the maximum input transconductance that can be used in the design. As a compromise, the inductor used in the design is 4.3 nH, which corresponds to a R_{eq} of around 1100 Ω, so that the linearity will not be severely degraded so much by the gain (28 dB) of the amplifier. Meanwhile, the input transconductance Gm (~20 mS) is enough to provide an acceptable noise figure.

The simplest way to achieve a negative conductance cell is using a simple differential pair given in Fig. 3.11. Fig. 3.11a shows the Q-compensation circuit and Fig. 3.11b gives the equivalent small signal representation of the circuit in Fig. 3.11a. The negative conductance provided by the simple differential can be found readily as

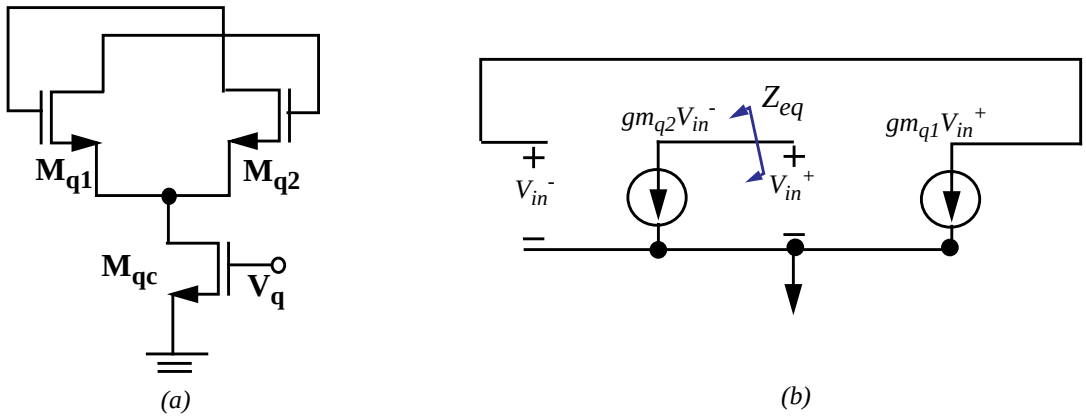


Fig. 3.11 Q-compensation circuit

$$Z_{eq} = \frac{V_{in}^{+}}{gm_{q2}V_{in}^{-}} = \frac{\frac{V_{in}}{2}}{gm_{q2}\left(-\frac{V_{in}}{2}\right)} = -gm_{q2} = -gm_{q1}. \tag{3.22}$$

When compared with the negative conductance generated by a single-ended version Q-compensation circuit [5], the negative conductance provided by the circuit in Fig. 3.11 is double with the same dc biasing condition. To generate the same conductance, the current needed is halved and the power consumption is 4 times smaller than a single-ended Q-compensation circuit. As a result, it is more attractive to implement a differential LNA instead of a single-ended version.

3.4.2 Center-frequency tuning circuit

Due to process variations in fabrication, it is difficult to control the absolute value of both active devices and the passive elements. The variation is typical much larger than the discrete components in the market. Passive on-chip components are subjected to variations of 10 to 20 percent. Meanwhile, the modeling of the planar inductors is still not accurate, and the estimation

merely depends on the time consuming 3-D simulation tools such as E-M SONNET [26] or modeling tools like ASITIC [21]. So as to alleviate the unpredictable process variations and inaccurate inductor's modeling, a frequency tuning circuit is incorporated in the design to allow certain degrees of frequency variation. The resonant frequency, is governed by both the inductor and the capacitor, can be controlled by varying the capacitance C_p of the resonant tank.

There are several methods to provide a tunable capacitor. Firstly, the capacitor can be implemented by a varactor diode, which is the simplest and the least power-consuming way as it actually does not consume any power. Yet, the varactor diode is not very linear and varies also with the small-signal applied at the input of the varactor. It is undesirable as the frequency of the resonant tank will vary with the input signal amplitude and hurts the linearity of the LNA. Details on how the linearity of the capacitor affects the linearity of the whole circuit are going to be discussed in Chapter 5.

Another method that can generate a tunable capacitor is called impedance multiplication [14] depicted in Fig. 3.12. In Fig. 3.12a, the total current drawn is $(1+G_mR)I_z$ and the voltage drop

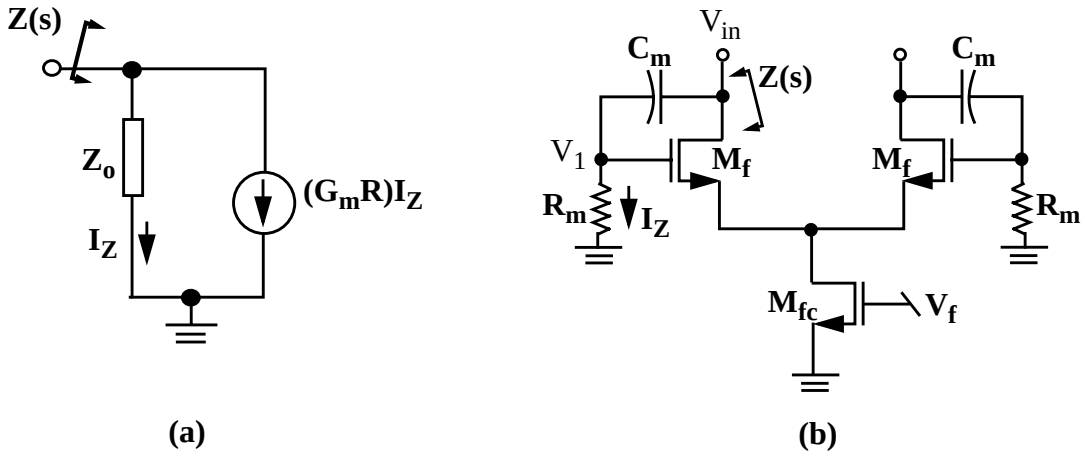


Fig. 3.12 Circuit diagram of impedance multiplication

is $I_z(Z_o)$, accordingly, the impedance is equal to

$$Z(s) = \frac{V_{in}(s)}{I_{in}(s)} = \frac{I_z Z_o}{(1 + G_m R) I_z} = \frac{Z_o}{(1 + G_m R)}, \tag{3.23}$$

where G_mR is the multiplication factor.

If $Z_o = \frac{1}{sC}$, the equivalent impedance of (3.23) is

$$Z(s) = \frac{1}{(1 + G_m R) sC} \tag{3.24}$$

and the effective capacitance C_{eff} is

$$C_{eff} = (1 + G_m R) C \quad . \tag{3.25}$$

By varying G_mR, C_{eff} is tuned.

In practice, the impedance multiplication can be implemented as the circuit in Fig. 3.12b. The small signal current passing through the capacitance C_m is sensed by the resistor R_m. The current drawn by the device M_f is directly proportional to the voltage V_1 sensed by R_m. Thus, the total current drawn from the input and the overall impedance Z(s) looking at the input are,

$$I_{total} = (1 + g_{mf} R_m) I_z \tag{3.26}$$

and

$$Z(s) = \frac{V_{in}}{I_{total}} = \frac{(sC_m + R_m) I_z}{(1 + g_{mf} R_m) I_z} = \frac{sC_m}{1 + g_{mf} R_m} + \frac{R_m}{1 + g_{mf} R_m} \quad . \tag{3.27}$$

In Eq. (3.27), it comprises two terms, the first one is the desired tunable capacitance, and the second term can be treated as the extra losses to the resonant tank and needs to be compensated by the Q-tuning circuit.

Another well-known techniques to implement a variable capacitor is called Miller method illustrated in Fig. 3.13. The effective capacitor is

$$C_{eq} = (1 + A_o)C_o \,, \tag{3.28}$$

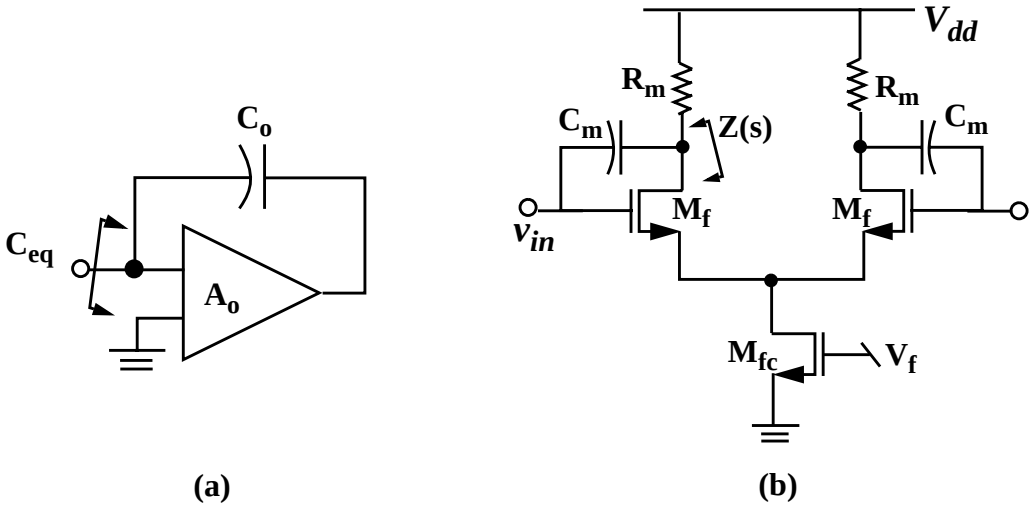


Fig. 3.13 Circuit diagram of Miller capacitance

where A_o is the amplifier gain and C_o is the physical capacitor utilized in the Miller capacitance method. By tuning the amplifier gain A, a variable capacitor can be realized. In Eq. (3.28), the impedance is purely capacitance. It is true only when the amplifier is ideal, i.e. the amplifier has an infinite bandwidth. Indeed, the finite bandwidth of the miller amplifier not only reduces its high frequency gain, but also creates a real part, which can be treated as the extra losses from the center frequency tuning circuit. To be more comprehensive, the admittance (Y_m) of the Miller amplifier is modified to be (For simplicity, the admittance instead of the impedance is analyzed but the result will be the same),

$$Y_m = \frac{1}{Z_m} = sC_{gs,m} + \frac{sC_m(1+g_{mf}R_m)}{1+(\omega C_m R_m)^2} + \frac{(\omega C_m)^2 R_m(1+g_{mf})}{1+(\omega C_m R_m)^2}, \quad (3.29)$$

where $C_{gs,m}$ is the gate-to-source capacitance of the Miller amplifier.

Similar to the impedance multiplication, the Miller amplifier's admittance also exists a real term, that contributes losses to the resonant circuit. Ideally, a larger R_m or C_m can provide a larger tuning range, nonetheless, the product R_m C_m also reduces the bandwidth of the amplifier and contributes a larger losses to the circuit. As a consequence, R_m and C_m are chosen so as to provide enough tuning range, around 10 percent, to account for the process variations.

Both the impedance multiplication and the Miller capacitance method can provide a tunable capacitor, nonetheless, the noise performance of these two methods also needs to be taken into consideration. As the output impedance of the bandpass amplifier is large, it is reasonable that the current noise will be dominant and only the noise current of the two configuration are compared. The noise current of the impedance multiplication (i_{im}) and the Miller capacitance (i_{mc}) are

$$i_{im} = \left(\frac{2}{3}g_{mf} + R_m g_{mf}^2\right) \qquad i_{mc} = \left(\frac{1}{R_m} + \frac{2}{3}g_{mf}\right)\left(\frac{\omega C_{gs}}{g_{mf}}\right)^2 = \left(\frac{1}{R_m} + \frac{2}{3}g_{mf}\right)\left(\frac{\omega}{\omega_{T,f}}\right)^2,$$

where ω_T is the unity-gain frequency. The noise of the Miller amplifier is reduced by the ratio (ω/ω_T), which is smaller than 1. For the impedance multiplication, the resistor noise is actually amplified by the transconductance of the amplifier g_{mf}. Therefore, the Miller capacitance is superior than that of the impedance multiplication in terms of noise performance.

3.4.3 50-Ω Output Buffer Design

So as to isolate the output resonant tank from the measurement equipment and to facilitate the noise figure measurement of the circuit, a 50-Ω buffer is added at the output of the amplifier. The schematic of the buffer is given in Fig. 3.14.

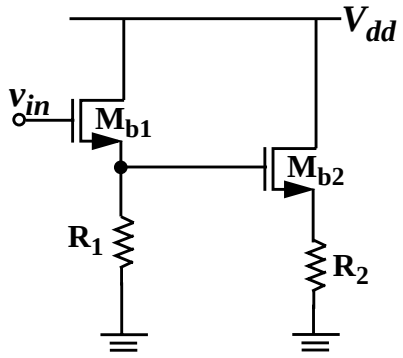


Fig. 3.14 The 50-Ω output buffer

In conventional buffer design, active load is usually preferred as it is small in size and has a high output impedance. But it is not suitable in this 50-Ω buffer design since a large transconductance is required (20 mS) to achieve 50–Ω. For a single-stage voltage follower, the gain ($G_{buf,sing}$) and the output impedance ($R_{out,sing}$) are

$$G_{buf,\,\mathrm{sing}} = \frac{gm_{b1}R_1}{1+gm_{b1}R_1} \tag{3.30}$$

and

$$R_{out,\,\mathrm{sing}} = R_1 \parallel \frac{1}{gm_{b1}}, \tag{3.31}$$

where gm_{b1} is the transconductance of M_{b1}. A small R_1 should be selected so that the biasing condition will not be changed much when the 50-Ω load is attached at the output node. For

example, if R_1 is chosen to be 100-Ω, gm_b would be 10 mS so that 50–Ω is achieved. However, because the V_{gs} of M_{b1} is large (the input dc of M_{b1} is close to the supply voltage while the source is connected to a small R_1), the current needed to provide the required conductance (10 mS) would be very large. Therefore, a single-stage voltage follower is not employed. Indeed, a two-stage voltage follower was chosen such that the first stage acts as a level shifter for the second stage and the second follower is biased to maintain a 50-Ω matching at the output. The gain of a two-stage voltage-follower ($G_{buf,two}$) is

$$G_{buf,\,two} = \left(\frac{gm_{b1}R_1}{1+gm_{b1}R_1}\right)\left(\frac{gm_{b2}R_2}{1+gm_{b2}R_2}\right), \tag{3.32}$$

where gm_{b2} is the transconductance of M_{b2}. The parameters of the output buffer are summarized in Table 3.3.

Parameters	**Values**
M_{b1}	60 μ/0.6 μ
M_{b2}	100 μ/0.6 μ
R_1	2-kΩ
R_2	100-Ω

Table 3.3: The parameters in the 50–Ω output buffer

The buffer is simulated and the results are given in Fig. 3.15. The loss of the buffer is 16 dB when a 50-Ω load is inserted at its output. The corresponding noise figure of the buffer is 19 dB.

The complete schematic of the designed bandpass amplifier is depicted in Fig. 3.16.

In Fig. 3.17, the frequency response of the amplifier is depicted. At a center frequency of

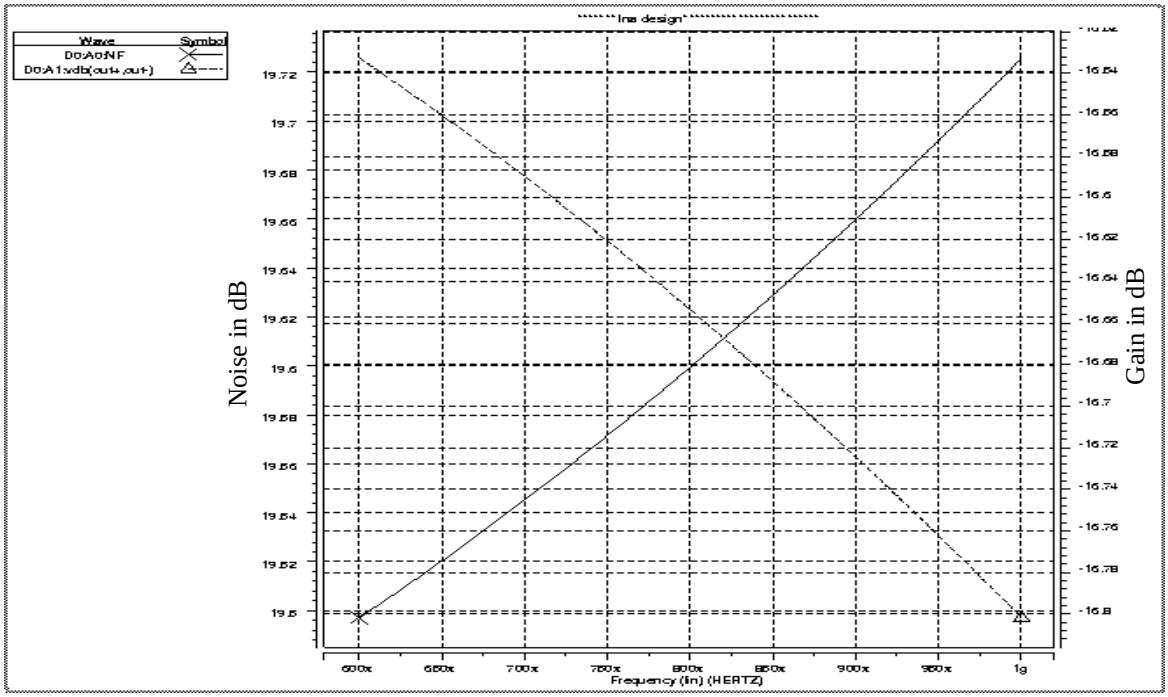


Fig. 3.15 The gain and the noise figure of the output buffer

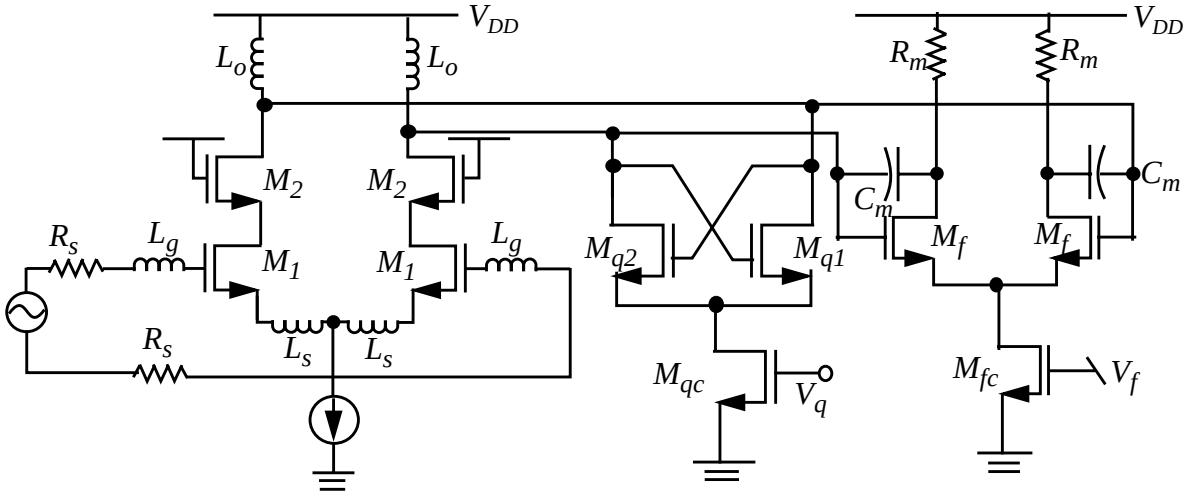


Fig. 3.16 The complete schematic of the bandpass amplifier

940 MHz and a 3-dB bandwidth of 25-MHz. The simulated gain of design is 28 dB and the image rejection at 800 MHz is 18 dB.

The Q-tuning and frequency tuning range of the amplifier is demonstrated in Fig. 3.18 and Fig. 3.19.

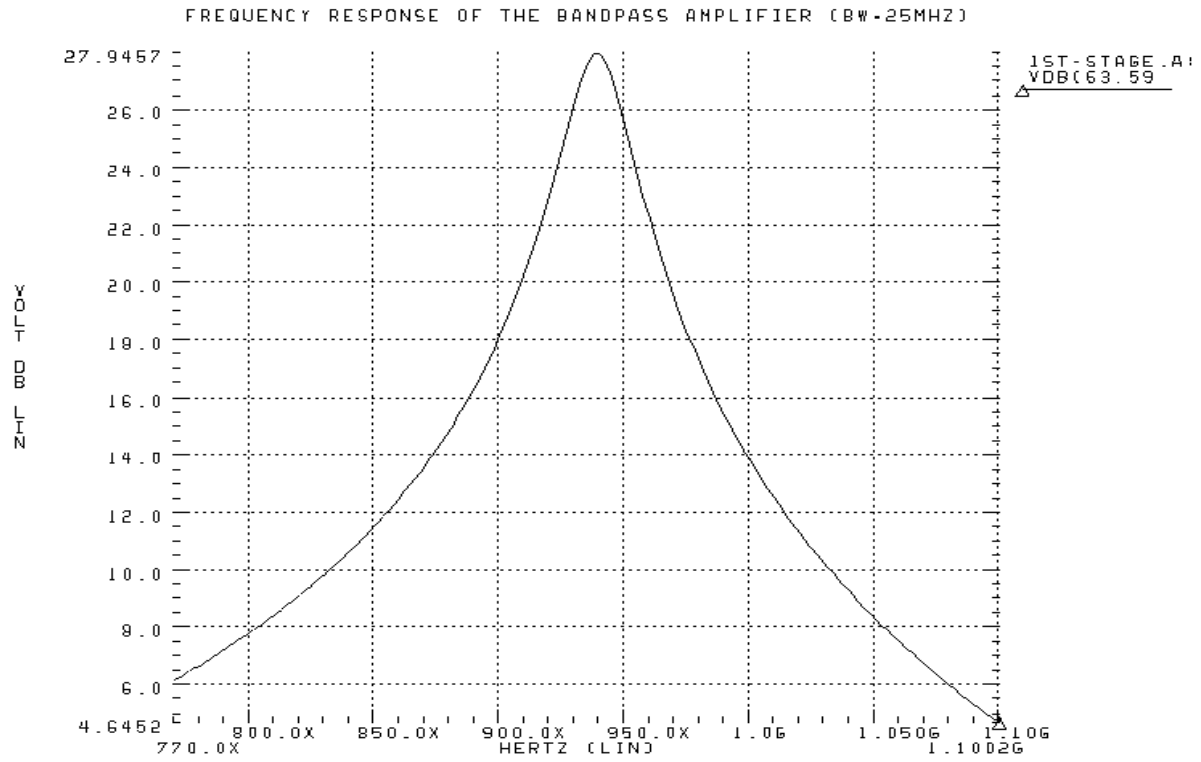


Fig. 3.17 The simulated frequency response of the amplifier

In Fig. 3.18, the Q-tuning voltage (V_q) is swept from 0.9 V to 0.99 V and the frequency tuning voltage (V_f) is fixed to be 0.8 V. The Q is increased from 7 up to 56. At the same time, the center frequency is shifted from 956 MHz to 938 MHz. This inevitable interaction between the Q-tuning and the center frequency tuning circuit affects the linearity of the complete circuit.

In Fig. 3.19, the Q-tuning voltage is fixed while the frequency tuning voltage is varied from 0 V to 1.2 V. The center frequency is shifted from the 1 GHz down to 927 MHz. Meanwhile, the Q of the circuit is degraded from 12 at 1 GHz to 6 at 927 MHz. It is obvious that the effect of frequency tuning on Q is much larger than the reverse. Once the Q-tuning voltage is varied, the frequency tuning voltage also needs to be adjusted at the same time to restore the same center frequency as shown in Fig. 3.20 and vice versa.

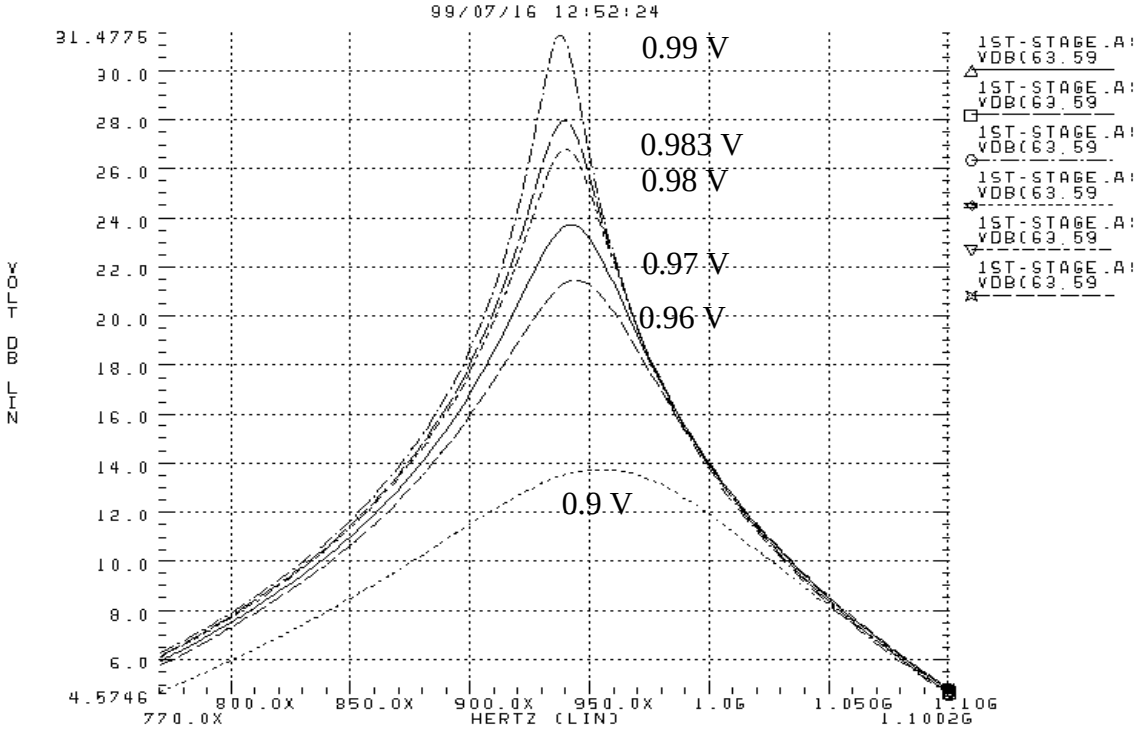


Fig. 3.18 The Q-tuning ability of the circuit

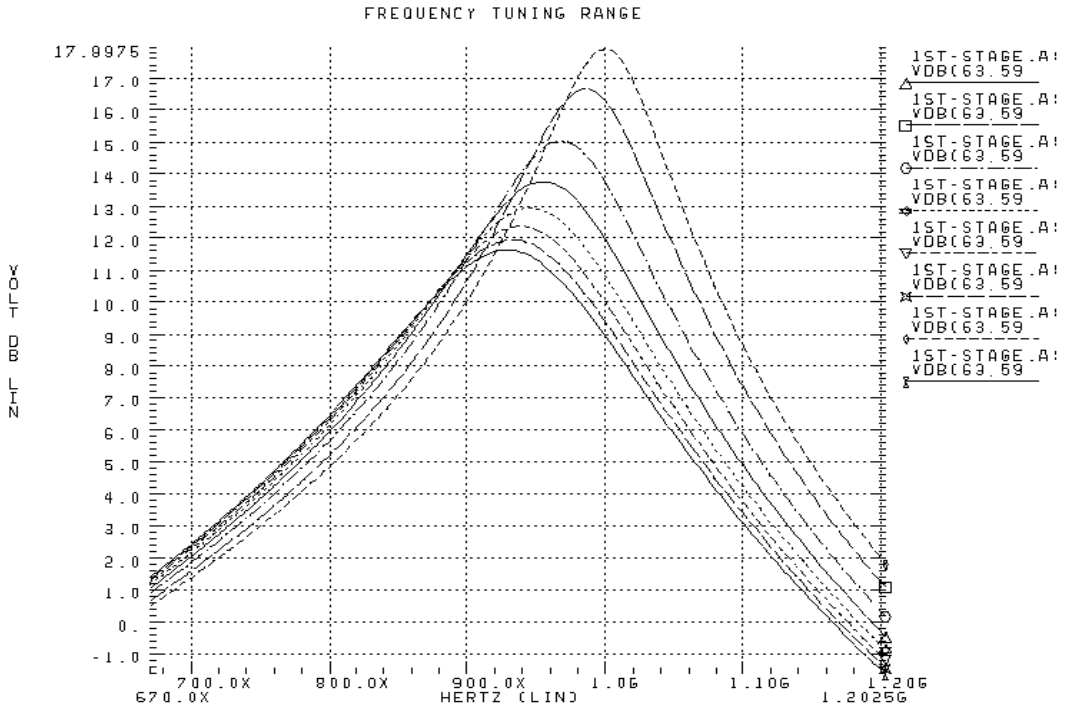


Fig. 3.19 The frequency tuning ability of the circuit

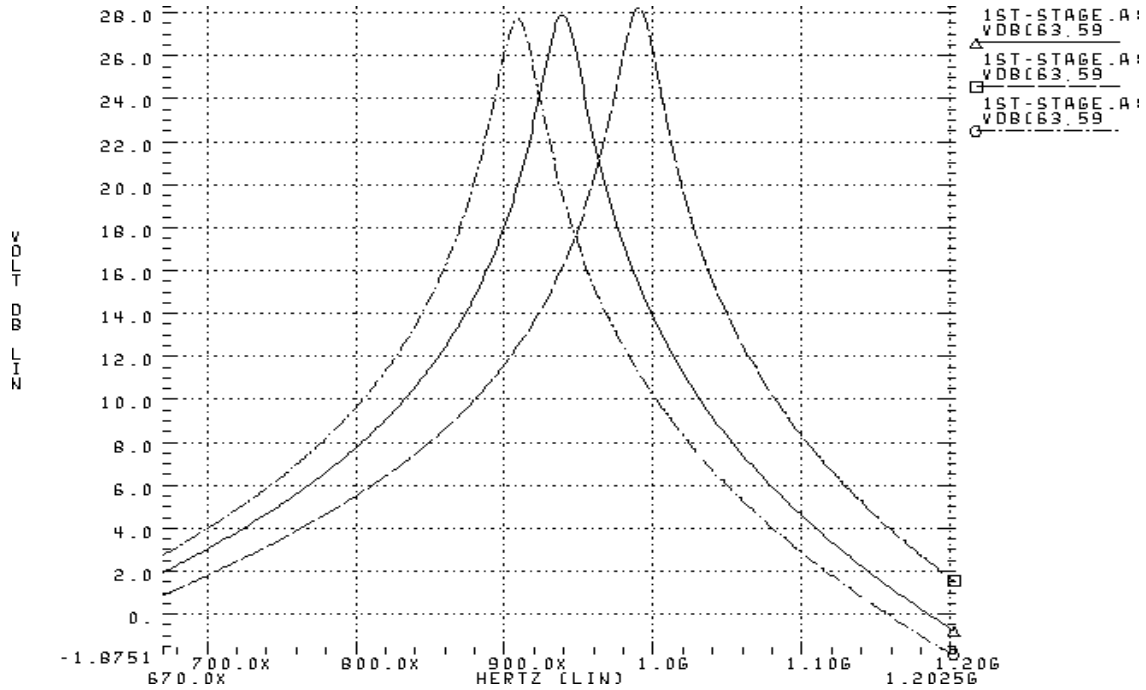


Fig. 3.20 The frequency response the circuit with both Q and frequency varied at the same time

Chapter 4

Noise Analysis and Measurement of a bandpass amplifier

4.1 Introduction

As discussed in Chapter 2, noise figure is one of the key parameters in the bandpass amplifier design. To mitigate the noise figure of a LNA, inductive source degeneration and a large input transconductance are employed in the design. In this chapter, detailed analysis of the noise contributions from each source in a bandpass amplifier are described. Because spiral inductors utilized in the design have a low quality factor, the noise contributed by their resistive losses cannot be neglected and thus will be included in this analysis. As the frequency of interest is around 1 GHz, thermal noise is the most important and will be considered as the only noise source.

4.2 Noise Analysis

Before analyzing the noise performance of the bandpass amplifier, a brief review of the noise contribution from passive elements and active devices are presented.

4.2.1 Noise contribution from a resistor

Resistors are one of the most commonly used components in the circuit design. The mean square noise voltage spectral density of a physical resistor R due to thermal noise [12] as shown in Fig. 4.1 is

$$\frac{\overline{V_R^2}}{\Delta f} = 4kTR \text{ or } \frac{\overline{I_R^2}}{\Delta f} = 4kT\frac{1}{R}. \tag{4.1}$$

Fig. 4.1 Resistor thermal noise model

It is worthwhile to point out that noise voltage and noise current components do not have any particular polarity and that they are usually referred to its root-mean-square (r.m.s) value.

4.2.2 Thermal Noise in MOSFETs [23]

For a MOSFET device, the complete noise model of a sub-micron MOSFET transistor is depicted in Fig. 4.2 [29]. The mean-square noise current due to thermal noise is

$$\frac{\overline{I_d^2}}{\Delta f} = 4kT\gamma g_{do}. \tag{4.2}$$

γ is equal to $\frac{2}{3}$ and 2 to 3 for long-channel and sub-micron devices respectively. The dramatic increase in γ for sub-micron devices is caused by a strong electric field in short-channel devices. g_{do} is the drain-source conductance at zero V_{DS}, which is close to the transconductance g_m for

long-channel devices and is assumed to be g_m in the analysis.

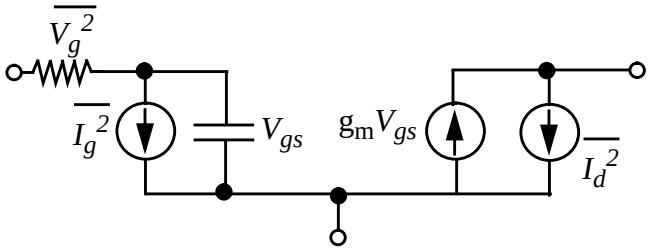


Fig. 4.2 Complete transistor noise model

4.3 Noise Analysis of the basic LNA

To facilitate the noise analysis, part of the circuit diagram of the bandpass amplifier is redrawn in Fig. 4.3. Without loss of generality, all the noise components are referred to the output of the circuit.

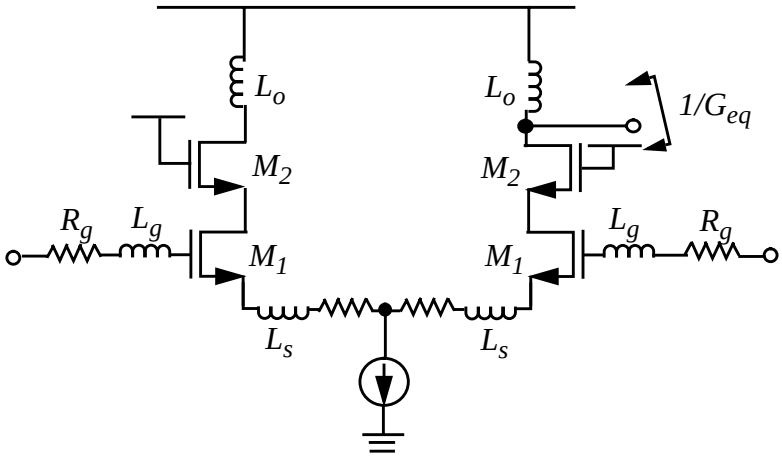


Fig. 4.3 The LNA including the resistive losses

As a reference, the transconductance gain of the amplifier is repeated as

$$Gm(\omega_o) = \left(\frac{gm}{(R_s + R_g + R_l + \omega_T L_s)sC_{gs}}\right) = \left(\frac{\omega_T}{2\omega_o R_s}\right). \qquad (4.3)$$

The noise power spectral density due to the source resistance R_s at the output of the amplifier is

$$\frac{S_{01}}{\Delta f} = 4kTR_s\left(\frac{\omega_T}{2\omega_o R_s}\right)^2\left(\frac{1}{G_{eq}}\right)^2 \quad , \tag{4.4}$$

where G_{eq} is the equivalent output conductance of the resonant tank after compensated by the Q-compensation circuit.

The output noise power spectral density due to the series resistance R_g and R_l of inductor L_g and L_s is

$$\frac{S_{02}}{\Delta f} = 4kT(R_g + R_l)\left(\frac{\omega_T}{2\omega_o R_s}\right)^2\left(\frac{1}{G_{eq}}\right)^2 . \tag{4.5}$$

Also, the output noise power spectral density due to input device M_1 is

$$\frac{S_{03}}{\Delta f} = 4kT\left(\frac{2}{3}g_{m1}\right)\left(\frac{\left[(R_s + R_g + R_l)^2 + \omega^2\left((L_s + L_g) - \frac{1}{\omega^2 C_{gs}}\right)^2\right]}{(2R_s)^2}\right)\left(\frac{1}{G_{eq}}\right)^2 . \tag{4.6}$$

The noise due to M_2 in Fig. 4.3 is not taken into account as the impedance looking from the source of M_2 is relatively low, the noise contribution is less than the other counterparts. The next item needs to be considered is the output resonant tank illustrated in Fig. 4.4.

The output power spectral density due to the resistive losses (R_o) of the output inductor L_o is

$$\frac{S_{R_o}}{\Delta f} = 4kT\left(\frac{1}{Q_o^2+1}\right)\left(\frac{1}{R_o}\right)\left(\frac{1}{G_{eq}}\right)^2 \quad . \tag{4.7}$$

which strongly depends on the intrinsic Q_o of the inductor.

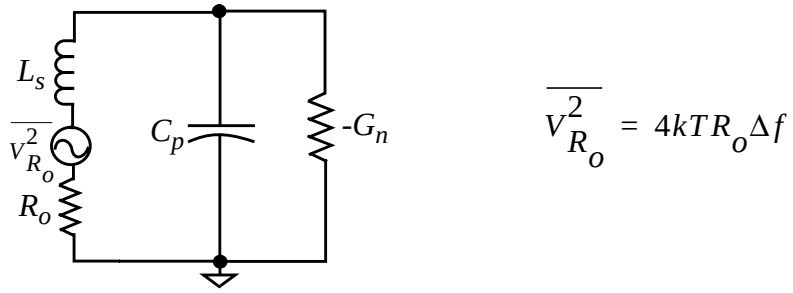


Fig. 4.4 The output resonant tank

The total output noise spectral density of the basic LNA configuration is therefore equal to

$$\frac{S_{total}}{\Delta f} = 4kT(R_s+R_g+R_l)\left(\frac{\omega_T}{2\omega_o R_s}\right)^2\left(\frac{1}{G_{eq}}\right)^2 + 4kT\left(\frac{2}{3}g_{m1}\right)(C_1)\left(\frac{1}{G_{eq}}\right)^2 \quad , \tag{4.8}$$

where

$$C_1 = \frac{\left[(R_s+R_g+R_l)^2+\omega^2\left((L_s+L_g)-\frac{1}{\omega^2 C_{gs}}\right)^2\right]}{(2R_s)^2} \quad . \tag{4.9}$$

The noise figure (NF) is defined as

$$NF = \frac{Total\ \ Noise\ \ Power\ \ Spectral\ \ Density}{Noise\ \ Power\ \ Spectral\ \ Density\ \ due\ \ to\ \ R_s}. \tag{4.10}$$

Thus, the LNA noise factor (F_{LNA}) is equal to

$$F_{LNA} = 1 + \frac{R_g + R_l}{R_s} + \frac{2}{3} gm_1 \left(\frac{2\omega_o R_s}{\omega_T} \right)^2 \frac{C_1}{R_s} + \left(\frac{1}{\left(Q_o^2 + 1 \right) R_o} \right) \left(\frac{2\omega_o R_s}{\omega_T} \right)^2 \left(\frac{1}{R_s} \right) \qquad (4.11)$$

4.3.1 Noise Analysis of the Q-compensation Circuit

The equivalent model for analyzing the noise of the Q-compensation circuit is depicted in Fig. 4.5. The output noise spectral density of the Q-compensation circuit is

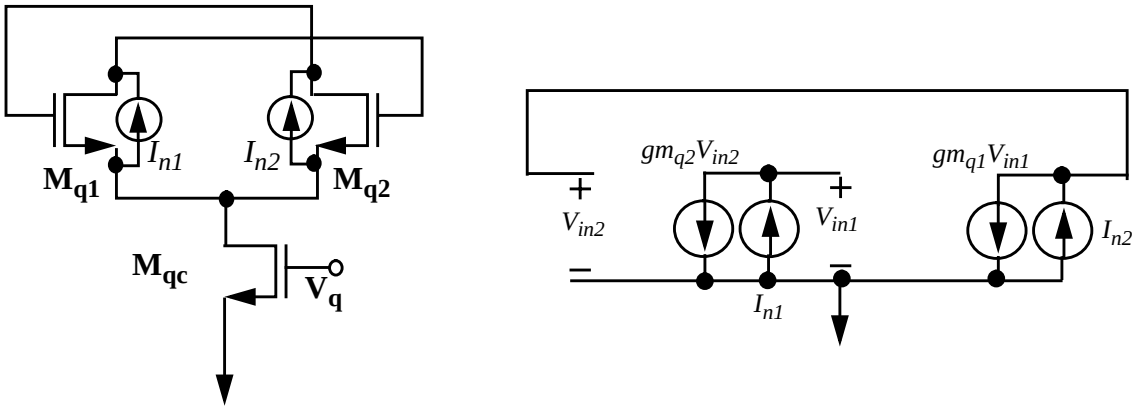


Fig. 4.5 The small-signal analysis of the Q-compensation circuit

$$\frac{S_{oQ}}{\Delta f} = 4kT \left(\frac{4}{3} gm_{q1} \right) \left(\frac{1}{G_{eq}} \right)^2 \qquad (4.12)$$

4.3.2 Noise Analysis of the Frequency tuning circuit

The major noise contribution of the frequency tuning circuit illustrated in Fig. 4.6 is the loading resistor R_m and the input device M_f of the Miller amplifier circuit. The calculated output noise spectral density of the frequency tuning circuit is

$$\frac{S_f}{\Delta f} = \frac{(4kT(1/R_m) + 4kT\gamma gm_f)(sC_{gs,f})^2}{(gm_f)^2}\left(\frac{1}{G_{eq}}\right)^2$$

$$= \left(\frac{4kT}{(gm_f)^2 R_m} + \frac{4kT\gamma(sC_{gs,f})^2}{gm_f}\right)\frac{1}{G_{eq}^2} \quad , \qquad (4.13)$$

where gm_f is the input transconductance of the miller amplifier and R_m is the corresponding loading resistor.

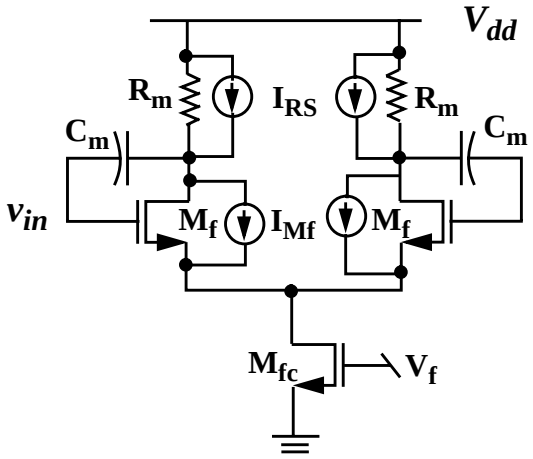


Fig. 4.6 The frequency tuning circuit

4.3.3 Noise Analysis of the Output Buffer

A output buffer shown in Fig. 4.7 is designed to isolate the output resonant tank and the instrument so that the frequency would not be altered by the loading of the equipments. The output noise spectral density of the output buffer is

$$\frac{S_{ob}}{\Delta f} = \frac{4kT\left(\frac{2}{3}gm_{b2}R_2 + R_2 + \left(\frac{gm_{b2}R_2}{1+gm_{b2}R_2}\right)^2\left(\frac{2}{3}gm_{b1}R_1 + R_1\right)\right)}{\left(\frac{gm_{b2}R_2}{1+gm_{b2}R_2}\right)^2\left(\frac{gm_{b1}R_1}{1+gm_{b1}R_1}\right)^2}, \qquad (4.14)$$

where gm_{bi} and R_i are the transconductance and the loading resistor of the buffer stage respectively.

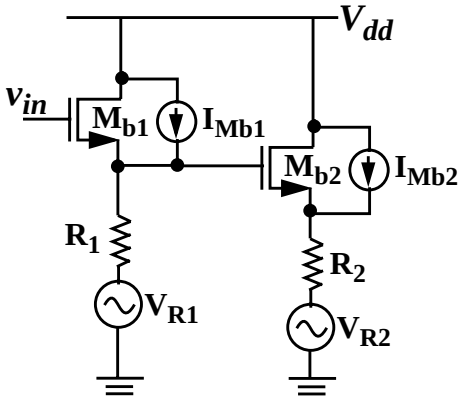


Fig. 4.7 Noise Analysis of the output buffer

The noise factor (F_{tun}) of the tuning circuits is

$$F_{tun} = \frac{\left(\frac{4}{3}gm_{q1}\right)}{R_s\left(\frac{\omega_T}{2\omega_o R_s}\right)^2} + \frac{\left(\frac{1}{R_m} + \frac{2}{3}gm_f\right)\left(\frac{\omega}{\omega_{T,f}}\right)^2}{R_s\left(\frac{\omega_T}{2\omega_o R_s}\right)^2}. \qquad (4.15)$$

As shown in Eq. (4.15), the noise contribution from the frequency tuning circuit is already reduced by $(\omega_T/\omega_o)^2$, which is much smaller than 1, before being further reduced by the gain of the amplifier. Thus, its contribution will be much smaller than the other noise components. For the output buffer, the current noise component is much smaller than the voltage noise counterpart, yet these voltage noise will be smaller as long as the output impedance of the amplifier is large.

Consequently, the buffer noise contribution is negligible in the analysis. Most of the noise is contributed from the inductors and the Q-compensation circuit. In the following analysis, we will omit the noise originated from the frequency tuning and the output buffer.

As a whole, the noise factor of the complete circuit is

$$F = 1 + \frac{R_g + R_l}{R_s} + \frac{2}{3} gm_1 \left(\frac{2\omega_o R_s}{\omega_T} \right)^2 \frac{C_1}{R_s} + \left(\frac{1}{\left(Q_o^2 + 1 \right) R_o} \right) \left(\frac{2\omega_o R_s}{\omega_T} \right)^2 \left(\frac{1}{R_s} \right) + \frac{\left(\frac{4}{3} gm_{q1} \right)}{R_s \left(\frac{\omega_T}{2\omega_o R_s} \right)^2} + \frac{\left(\frac{1}{R_m} + \frac{2}{3} gm_f \right) \left(\frac{\omega}{\omega_{T,\,f}} \right)^2}{R_s \left(\frac{\omega_T}{2\omega_o R_s} \right)^2} \quad . \qquad (4.16)$$

4.3.4 Noise Figure Simulation and Calculation

The noise distribution between the input matching, the LNA, and the tuning circuits are decomposed and tabulated in Table 4.1.

Building Block(s)	**Noise contribution**	**Normalized w.r.t R_s**
Source Resistor R_s	1.13×10^{-16}	1
Input Matching	9.2×10^{-17}	0.81
LNA	5.3×10^{-17}	0.47
Output inductor	4.9×10^{-17}	0.44
Q-tuning circuit	7.7×10^{-17}	0.7
Frequency tuning circuit	5.0×10^{-17}	0.045
Output buffer	2×10^{-18}	0.02

Table 4.1 The distribution of the noise of each building block

The spot noise figure at 940 MHz is 5.7 dB and the noise figure versus frequency is also plotted in Fig. 4.8. From Table 4.1, it is obvious that the major noise sources are the input

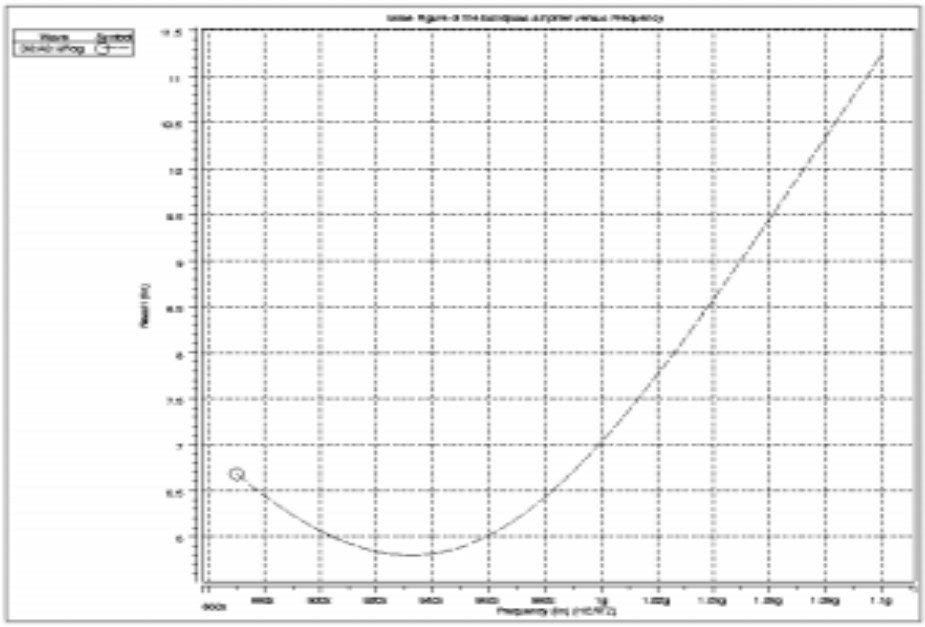


Fig. 4.8 The noise figure of the bandpass amplifier versus frequency

matching, LNA and the Q-tuning circuits. Since the input matching is in front of the LNA's gain stage, it cannot be reduced by increasing the gain of the amplifier. The noise is mainly originated from the low-Q inductors in the matching. Another sources of noise is the output inductors. Even though the noise is already reduced by the gain stage, the output inductor noise contribution is still large. The low-quality inductors also increase both the power and the noise in the Q-tuning circuit as a larger negative conductance is required to compensate the losses of the inductor.

With the designed parameters as shown in Table 4.2, the noise figure is calculated using

Parameters	Value	Parameters	Value	Parameters	Value
gm_1	25 mS	R_g	40	R_l	1.13

Table 4.2: The major designed parameters for the bandpass amplifier

Parameters	Value	Parameters	Value	Parameters	Value
C_{gs}	1.74 pF	R_m	50	R_o	10.7
Q_o	2.5	f_o	950 MHz	gm_q	12.27 mS

Table 4.2: The major designed parameters for the bandpass amplifier

Eq. (4.16). The calculated and the simulated noise figure of the bandpass amplifier are 5 dB and 5.7 dB respectively. The decomposition of the noise contributed from each part are tabulated in Table 4.3. The calculated noise contribution from the Q-tuning is much smaller than the simulated

Building Block(s)	**Calculated**	**Simulated**
Source Resistor R_s	1	1
Input Matching	0.81	0.81
LNA	0.46	0.47
Output inductor	0.48	0.44
Q-tuning circuit	0.408	0.7
Frequency tuning circuit	0.02	0.045
Total	3.2	3.5

Table 4.3: The decomposition of the calculated and simulated noise figure of the amplifier

because only the noise from the unbalanced differential pair is not considered in the calculation due to difficulties in analyzing them in the balanced circuits. But, as the unbalanced gm-cells in the modified Q-tuning circuit are not symmetrical, and their noise has to be taken into account during the simulation. From simulation, the noise from the unbalanced gm-cell accounts for about half of the noise contributed from the unbalanced gm-pair's current source. As a result, for the whole amplifier, the simulated noise figure is larger than the calculated one.

4.4 Noise Figure Measurement

Instruments utilized in RF circuit measurement are mainly single-ended. In recent years, more and more RF integrated circuits are implemented in differential topologies due to the abilities to reject parasitics and common-mode noise. Nevertheless, there are still not many equipments available in the market tailored for differential circuits. Differential signals can be generated by a low-loss hybrid transformer/ balun (M/A-Com H-183-4) and the output is then combined by another identical balun. Since a balun loss is much less than a power splitter (Mini-Circuits ZFSC-2-4), it reduces the inaccuracy due to the losses of the measurement setup. The connection is the same as the one shown in Fig. 4.9. The noise generated from the source HP 346C is splitted by a 2-way 180^{o} balun and the dc bias is added to the noise signal before fed into the differential circuit through a pair of high-speed SG-GS dual probe (40-A-SG-150-DUAL) from GCB. Furthermore, the output differential signal is picked up by a SG-GS dual probe. It is then combined by another balun and fed back to the noise-figure meter HP 8970B. Because the configuration consists of a lot of lossy components, it is inaccurate for measuring circuits with low-noise figure. Even though the noise-figure meter HP8970B can be calibrated in advance before the measurement, the accuracy is still not acceptable. Accordingly, noise figure estimation

based on Friis's system noise-figure equation in [23] is employed in the noise figure calculation.

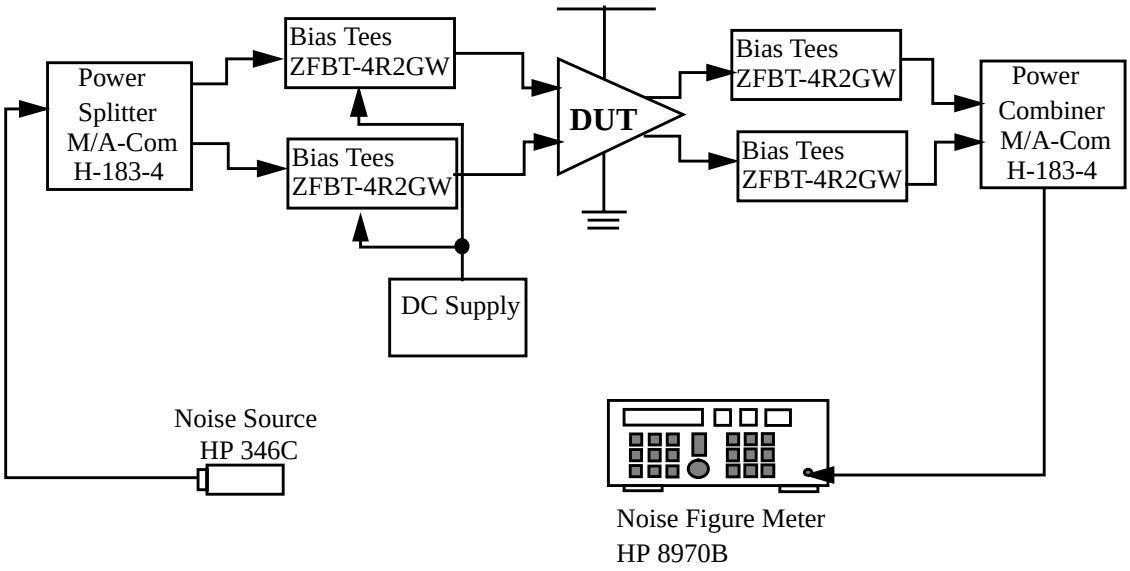


Fig. 4.9 Noise Figure Measurement Setup

For a cascaded system, the Friis's equation for noise figure calculation is given by

$$F_{sys} = 1 + (F_1 - 1) + \frac{(F_2 - 1)}{A_{p1}} + \ldots + \frac{(F_m - 1)}{A_{p1} \cdots A_{p(m-1)}} \tag{4.17}$$

where F_i and A_{pi} are the noise factor and the available gain of the i-th stage. F_i is calculated with respect to the source impedance R_s of the preceding stage. The output impedance of the preceding stage, the (i-1)th stage, is conjugate-matched with the input impedance of the next stage, the i-th stage. The noise due to the component under test (N_i) alone can be expressed in terms of the noise factor (F_i) measured and the noise power spectral density due to R_s,

$$\begin{aligned} F_i &= \frac{N_{Rs} + N_i}{N_{Rs}} = 1 + \frac{N_i}{N_{Rs}}, \\ N_i &= (F - 1) N_{Rs} \end{aligned} \tag{4.18}$$

The noise factor (F_i) measured includes the source resistance, thus it needs to be calibrated out in Eq. (4.18).

In Fig. 4.9, the components used in the setup can be treated as several cascaded stages in a system and the noise figure can then be evaluated using Eq. (4.17). The noise figure of each component is first measured using the noise figure meter HP8970B. To improve the accuracy of the measurement, the setup is calibrated in advance to cancel out any inaccuracy owing to the calibration fixture in Fig. 4.10. It should be pointed out that the input of the components need to

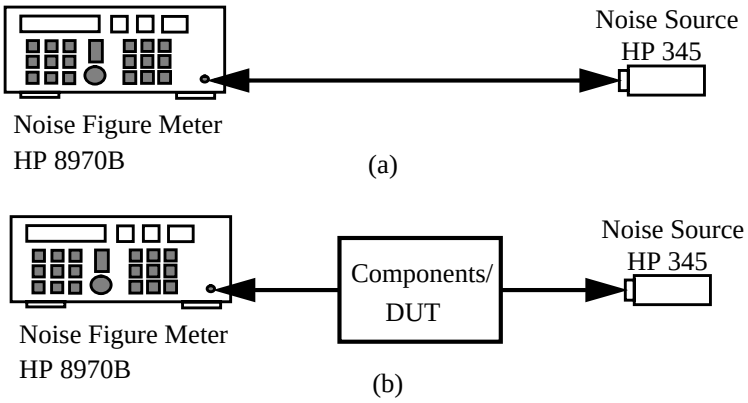


Fig. 4.10 (a). Calibration Setup; (b). Actual Measurement of the components

be conjugate-matched with the output of the preceding stage so that the simplified Friis's equation is valid. As the discrete components, like baluns and bias-tees, are matched to 50-Ω, it is easy to figure out the noise figure using the noise figure meter. The amplifier under test is also matched to 50-Ω for the noise measurement.

4.4.1 Noise Figure and Gain Measurement of a Hybrid Transformer / Balun

The balun shown in Fig. 4.11 is a three-port device which splits the incident signal power at port 1 equally into two anti-phase signals (each 3 dB lower than the input) appearing at the output ports (Port2 & Port3). Even though the term power splitter and power combiner is used

throughout the dissertation, they are actually the same as the balun is a bi-directional device and the name is just to distinguish different uses of a balun. As the balun is a three port device, the noise measurement is different from the conventional two-port network. The noise figure (NF)

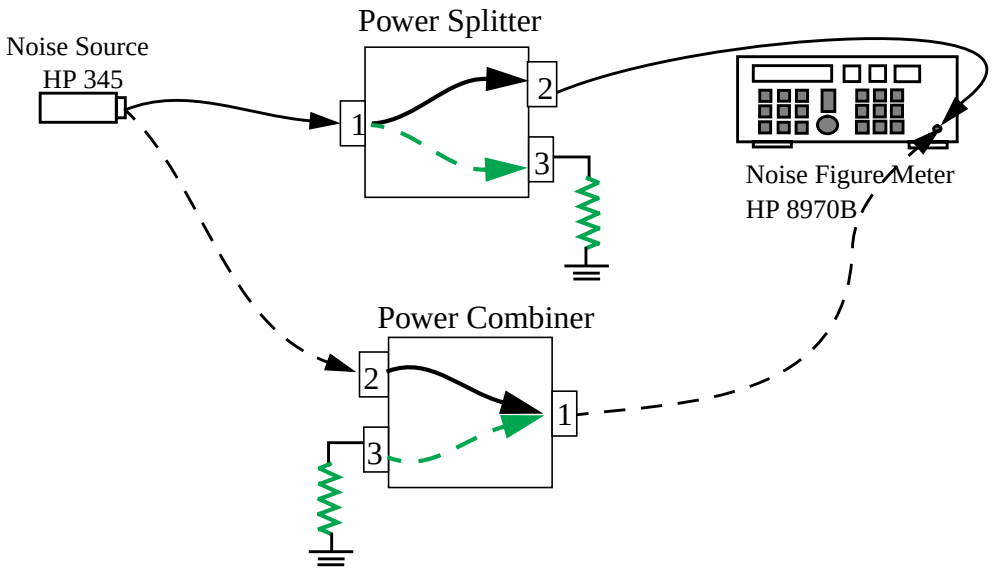


Fig. 4.11 (a). Measurement Setup for the power splitter / power combiner

and gain of a power splitter/ balun are measured as shown in Fig. 4.11. When the noise figure of Port 2 is measured, Port 3 needs to be terminated with a 50-Ω so that its noise power will not be reflected back to Port 1 or Port 2 and not to affect the measurement result. This is also true for measuring the noise figure at Port 3. Similarly, when measuring the noise figure and the gain of the power combiner, the noise power is introduced at either Port 2 or Port 3 with the other port terminated with a 50-Ω. As two independent 50-Ω source resistance generate noise at the inputs (Port 2 and Port 3) of the balun, the noise due to the balun alone is $N_{Rs} \times F_{PC} \times G_{PC} - 2N_{Rs} \times G_{PC} = N_{Rs} \times (F_{PC} - 2) \times G_{PC}$, where G_{PC} and F_{PC} are the gain and the noise factor of a power combiner.

To demonstrate the basic idea, consider the setup with only one power splitter, one

differential DUT (device under test), and one power combiner. Yet, the formula can be extended according to the actual setup once the idea is clear. The noise factor and the gain of the power splitter, the power combiner, and the differential DUT are F_{PS}, G_{PS}; F_{PC}, G_{PC} and F_{test}, G_{test} respectively. The total output noise power is

$$\begin{aligned} &Total\ output\ noise\ power \\ &= 2F_{PS}\times G_{PS}\times G_{test}\times G_{PC}\times N_{Rs} + 2(F_{PS}-1)\times G_{test}\times G_{PC}\times N_{Rs} \\ &\quad + (F_{PC}-2)\times G_{PC}\times N_{Rs} \end{aligned} . \qquad (4.19)$$

Meanwhile, the output noise power due to source resistor is

$$\begin{aligned} &Total\ output\ noise\ power\ due\ to\ source\ resistor \\ &= G_{PS}\times G_{test}\times G_{PC}\times N_{Rs} \end{aligned} . \qquad (4.20)$$

The cascaded noise factor (F_{casc}) is thus

$$F_{casc} = \frac{1}{2}F_{PS} + \frac{1}{2}(F_{test}-1)/G_{PS} + \frac{1}{4}(F_{PC}-2)/(G_{PS}\times G_{test}) . \qquad (4.21)$$

The corresponding cascaded gain of the system (G_{casc}) is

$$G_{casc} = 4\times G_{PS}\times G_{test}\times G_{PC} . \qquad (4.22)$$

Both F_{casc} and G_{casc} can be measured by the noise figure meter, and the quantities other than the device under test are known before the measurement, thus, the gain and the noise figure of DUT can be calculated accordingly. Nevertheless, the accuracy of the noise figure based on Eq. (4.17) decreases when the number of stages in the measurement setup increases. It is illustrated in the following two examples.

The first one is the simplest one, with one power splitter and one power combiner

connected together as shown in Fig. 4.12. The measurement result is compared with the result

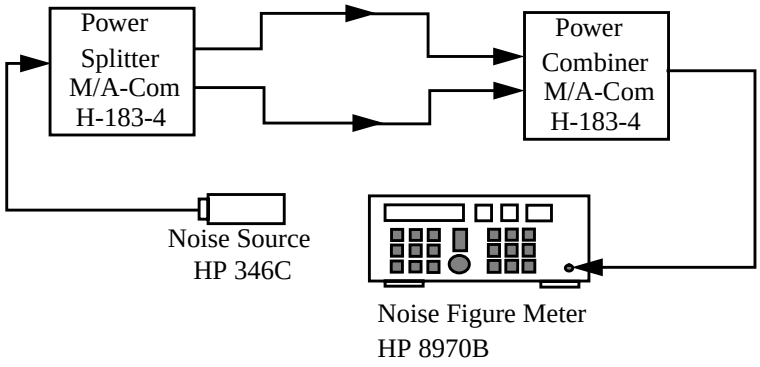
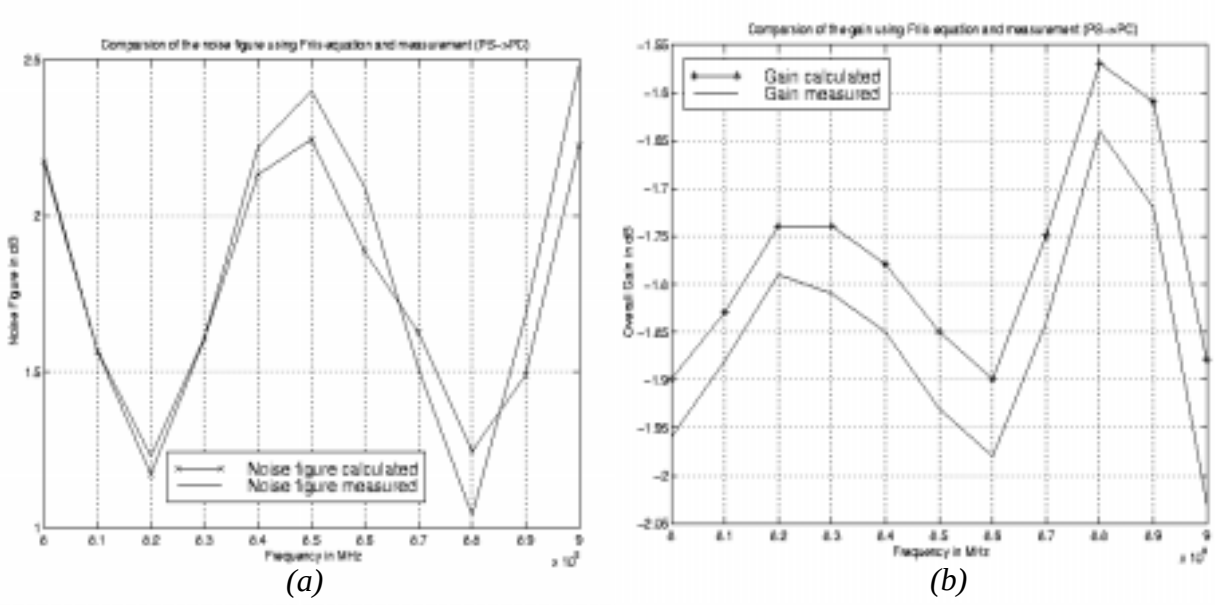


Fig. 4.12 Noise Figure Measurement Setup (Configuration 1)

based on Eq. (4.17) and is illustrated in Fig. 4.13. In Fig. 4.13a, the noise figure of the



(a) *(b)*

Fig. 4.13 Comparison of (a), the noise figure and (b), the gain between the measurement result and the result based on Friis's equation (Configuration 1)

measurement and the calculation based on Friis's equation is very close and the discrepancy is usually smaller than 0.1 dB. The agreement of the calculated and measured gain in Fig. 4.13b is

very good and within 0.05 dB in the frequency of interest.

The second configuration is the same as the setup shown in Fig. 4.9 with the DUT omitted. The measured and calculated noise figure and gain are given in Fig. 4.14a and Fig. 4.14b respectively. As there are more components (bias tees, SMA cables) added in between the power

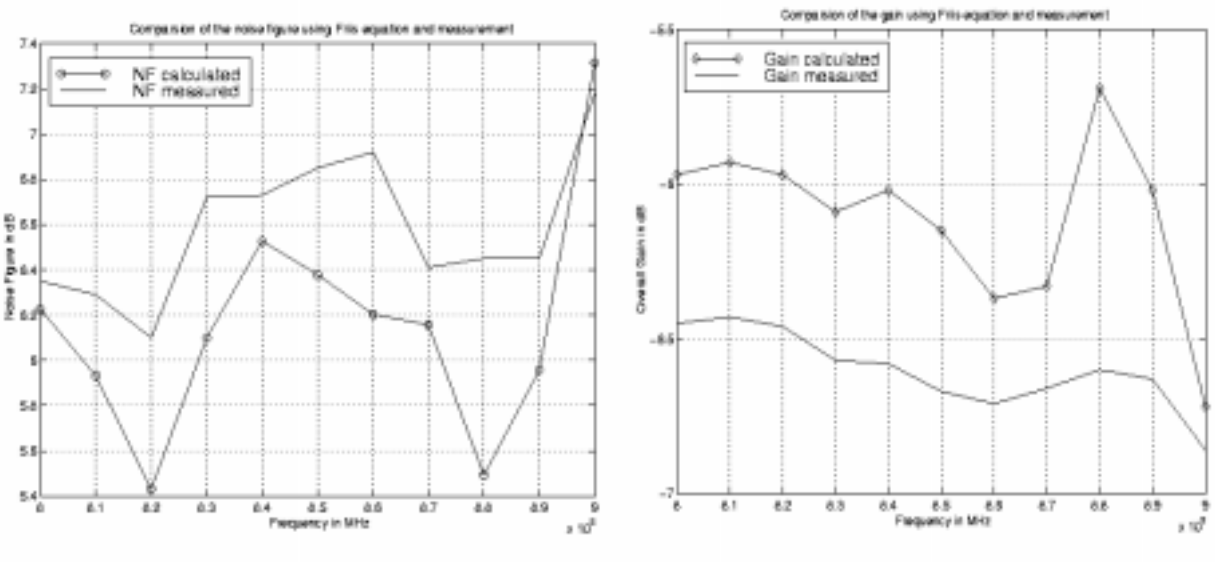


Fig. 4.14 Comparison of the noise figure and the gain between the measurement result and the result based on Friis's equation (Configuration 2)

splitter and the power combiner, the precision is degraded as the components are not perfectly matched in each channel. It can be observed from Fig. 4.14a, the noise figure variation between calculation and measurement is much larger (0.3 to 0.4 dB). Also, the discrepancies between measured and calculated gain is increased to around 0.5 dB. As a consequence, it is important to keep the number of lossy components in front of the DUT as small as possible.

Chapter 5

Linearity Considerations

5.1 Introduction

In RF circuit design, trade-offs exists between noise, linearity and power. Noise performance can be improved by increasing the gain of the circuit, but at the same time, the linearity has inevitably to be sacrificed. Therefore, compromise has to be made between the noise and the linearity of the design so as to meet the designed requirements. As discussed in Chapter 4, the noise performance of the bandpass amplifier can be improved by increasing the input effective transconductance (Gm) of the amplifier, however, this reduction is accompanied by an increase in the gain of the circuit and would cause a degradation of the linearity of the system. In this chapter, origins of the non-linearity in bandpass amplifiers are going to be addressed, and solutions are given to alleviate the non-linearity issues.

5.2 Current Situation

As discussed in Chapter 3, a simple differential pair shown in Fig. 3.11 is employed as the

Q-compensation circuit. The simulation result indicates that the linearity is much lower than the conventional LNAs. The simulated IIP_3 of the bandpass amplifier is depicted in Fig. 5.1. The extrapolated IIP_3 and the input 1-dB compression point (P_{-1dB}) are -32.5 dBm and -44 dBm.

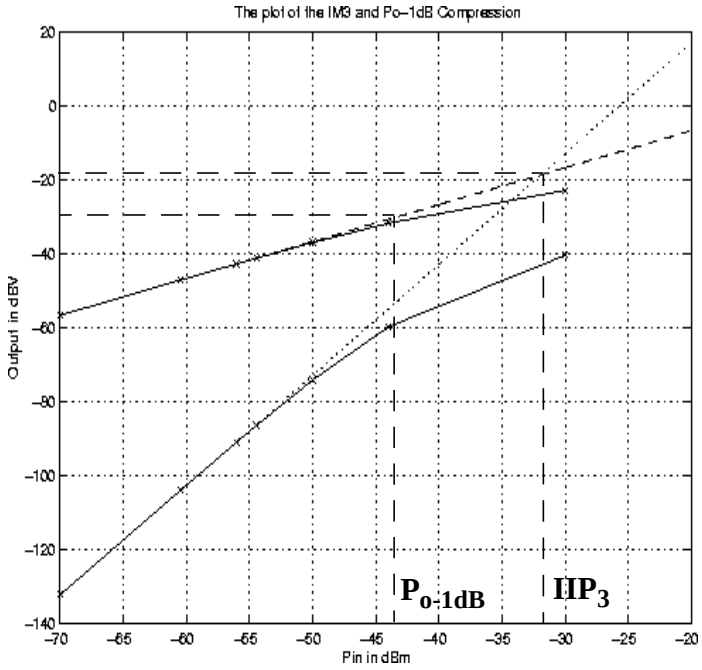


Fig. 5.1 The simulated IIP_3 of the bandpass amplifier using simple differential pair as the Q-compensation circuit

5.3 Origins of non-linearity in bandpass amplifiers

5.3.1 Non-linear characteristic of a MOS device

It is well known that a MOS transistor exhibits square law characteristics, the drain current I_d of a MOS device is modeled as

$$I_{ds} = \frac{1}{2}\mu C_{ox}\frac{W}{L}(V_{gs} - V_t)^2(1 + \lambda V_{ds}), \tag{4.23}$$

where μ is the mobility of the majority carrier, C_{ox} is the gate oxide thickness, W/L is the width-

length ratio of the device, V_{gs} is the gate-to-source bias voltage, V_{ds} is the drain to source bias voltage. V_t is the threshold voltage and λ is the channel length modulation factor.

For the simple differential pair shown in Fig. 3.11, the current I_{ds1} is

$$I_{ds1} = \frac{1}{2}\mu C_{ox}\frac{W}{L}\left(\frac{v_{in}}{2} + V_{gs} - V_t\right)^2\left(1 + \lambda\left(\frac{-v_{in}}{2} + V_{gs}\right)\right)$$

$$= \frac{1}{2}\mu C_{ox}\frac{W}{L}\left(\frac{v_{in}^2}{4} + v_{in}(V_{gs} - V_t) + (V_{gs} - V_t)^2\right)\left(1 + \lambda\left(\frac{-v_{in}}{2} + V_{gs}\right)\right) \qquad (4.24)$$

From Eq. (4.24), the small signal transconductance gm is thus equal to

$$gm = \frac{1}{2}\left(\mu C_{ox}\frac{W}{L}\right)\left(-\frac{\lambda v_{in}^2}{2} + \frac{v_{in}}{2}(1 + 2\lambda V_t - \lambda V_{gs}) + (V_{gs} - V_t)(1 + \lambda V_t)\right) \qquad (4.25)$$

The small signal conductance has a square term proportional to λ, the channel-length modulation factor, and it contributes to the non-linearity of the device. Besides, when the small signal V_{in} is large, the total current needed to be supplied by the current source is

$$I_{d1} + I_{d2} = \mu C_{ox}\frac{W}{L}\left[(V_{GS} - V_t)^2 + \frac{V_{in}^2}{4}\right], \qquad (4.26)$$

and the current actually provided by the current source (I_{dc}) is

$$I_{dc} = \mu C_{ox}\frac{W}{L}(V_{GS} - V_t)^2 = I_{d1} + I_{d2} - \frac{V_{in}^2}{4}. \qquad (4.27)$$

The current generated from the current source is not enough for M_1 and M_2 when the small signal becomes large, thus, both the current and the transconductance degrades when the signal begins to increase.

In an amplifier, the gain is equal to

$$Gain = G_m Z_o, \tag{5.1}$$

where Gm is the input transconductance and Z_o is the output impedance. The linearity of an amplifier is governed by both the compressive voltage-to-current transconductance stage and the voltage-dependent output impedance variation. In normal LNAs, the output impedance is passive (either inductive, capacitive or resistive) and usually more linear than the input transconductance stage, thus, the linearity is basically limited by the input gm-cell. Small signal gm with respect to the small signal *v* can be modeled by a polynomial equation:

$$i(v) = av + bv^2 + cv^3 \quad . \tag{5.2}$$

The linearity of the gm-cell is mainly governed by the coefficients *a*, *b* and *c*. The maximum input signal amplitude that gm-cells can tolerate before 1-dB compression from occurring is on the order of 20-30 mV, which is equivalent to around -15 to -20 dBm. This can be achieved with most LNAs. Nonetheless, in a Q-compensated bandpass amplifier, the 1-dB compression is well below this value (between -30 to -50 dBm depending on the equivalent Q of the circuit). To account for the low linearity, let's consider a simplified lossy parallel LC resonant tank with Q-compensation at the output of the amplifier shown in Fig. 5.2, where R_p is the parallel resistance of the LC tank and gm_q is the conductance provided by the negative gm cell.

The output impedance is compensated for high Q (~38) by an active circuit, say a simple cross-coupled differential pair. The equivalent output impedance (Z_{out}) near the resonant frequency (Fig. 5.2) is

$$Z_{out} = \frac{1}{\left(\frac{1}{R_p} - gm_q\right)} \tag{5.3}$$

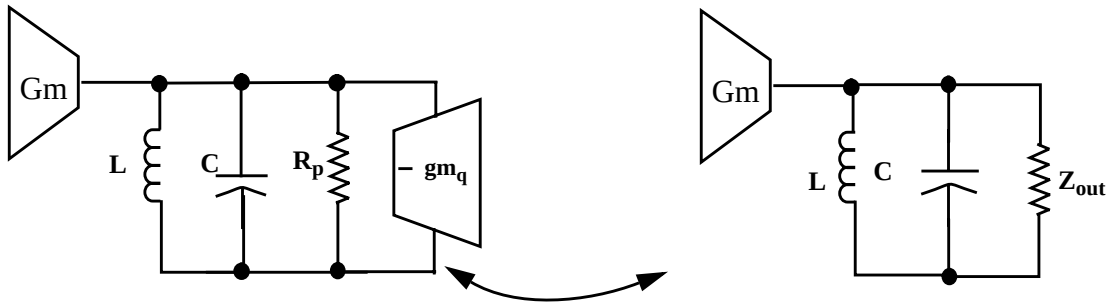


Fig. 5.2 The simplified Q-compensated bandpass amplifier

Because of the active circuit's non-linearity, the negative conductance generated for compensation degrades when the signal amplitude is large. As a result, the impedance is no longer constant but depends on negative conductance of the active circuit. At the same time, in order to suppress the noise at the output of the LNA, the input transconductance gain Gm cannot be small (>10 mS in our case) so as to reduce the noise figure of the output resonant tank and the tuning circuit. Also, the compensated output impedance needs to be larger than 2500-Ω so as to have a 25-MHz 3-dB bandwidth at 950 MHz. As a result, the resultant gain is larger than 25 dB. With such a large signal at the input of the gm-cell, the gm value provided for the compensation is diminished and this reduces the output impedance Z_{out} in Eq. (5.3). Accordingly, the overall gain of the bandpass amplifier is compressed and the linearity is significantly degraded by the variations of the output impedance depending on the signal amplitude. With a voltage gain of 20-30, the linearity of the whole amplifier is mainly dominated by the negative gm cells in the Q-tuning circuitry. This explains why bandpass amplifiers usually have poorer linearity compared to conventional low-Q LNAs.

To verify the hypothesis, the transconductance cell in the Q-tuning and center frequency

tuning circuits are replaced by gm-cell model shown in Fig. 5.3. To closely model the actual gm-value, an ideal gm is modeled as a polynomial function of small signal input V_{in}. To prove that the non-linearity is not contributed from the input transconductance stage, a simulation was conducted with all the circuits to be ideal except for the input transconductance stage Gm, i.e. the transconductance-cells in the Q-tuning and the center frequency tuning circuits are replaced by the gm-cell model in Fig. 5.3, with coefficients b and c set to zero, to model the constant gm in an ideal gm-cell. The simulation result can confirm whether the linearity is degraded from the input transconductance stage. The center frequency, and the gain of the circuit are kept to be the same

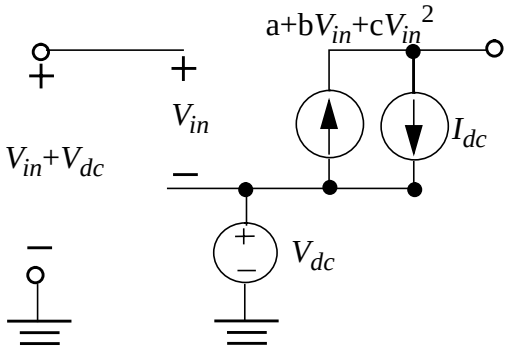


Fig. 5.3 The model of a gm-cell

so that comparisons can be made on the simulation results. The plot of the relationship between the fundamental power (P_{fund}) and the third-order intermodulation product (P_{IM}) and the input power (P_{in}) is illustrated in Fig. 5.4. The extrapolated IIP_3 is around -2 dBm, which is much better than -32.5 dBm obtained from the bandpass amplifier with real Q-tuning circuit. Therefore, it is reasonable to assume that the non-linearity is due to the input transconductance stage is negligible and that of the tuning circuit (Q-compensation circuitry) is the most dominant.

Besides, the non-linear gm-cell in the tuning circuits is modeled by the circuit in Fig. 5.3. The modeled gm is compared with the gm-value obtained from the actual Q-tuning circuit in Fig.

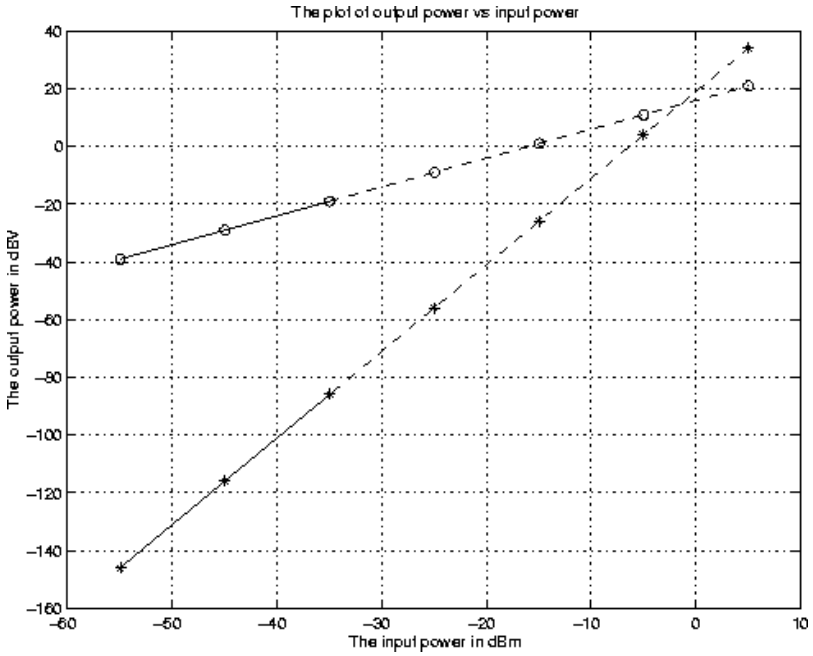


Fig. 5.4 The relationship between P_{fund}, P_{IM} and P_{in}

5.5. It is obvious that there is a good agreement between the model and the actual circuit in the range between ± 250 mV. Thus, the model in Fig. 5.3 is used to investigate how the non-linearity of the tuning circuits degrades the complete circuit.

As mentioned earlier, the non-linearity of a differential gm-cell is mainly governed by the coefficient *c* in Eq. (5.2). Thus, the non-linearity can be investigated by varying the gm-cell in the tuning circuit with several values of *c*, and the simulation result is plotted in Fig. 5.6. A smaller *c* implies that the non-linearity of the circuit is less severe and the simulated IIP3 is expected to be better. When the coefficient *c* is reduced by two times, the linearity can be improved by 3 dB. The simulation results shown in Fig. 5.6 confirm that the non-linearity of the Q-tuning circuit degrades the performance of the complete circuit.

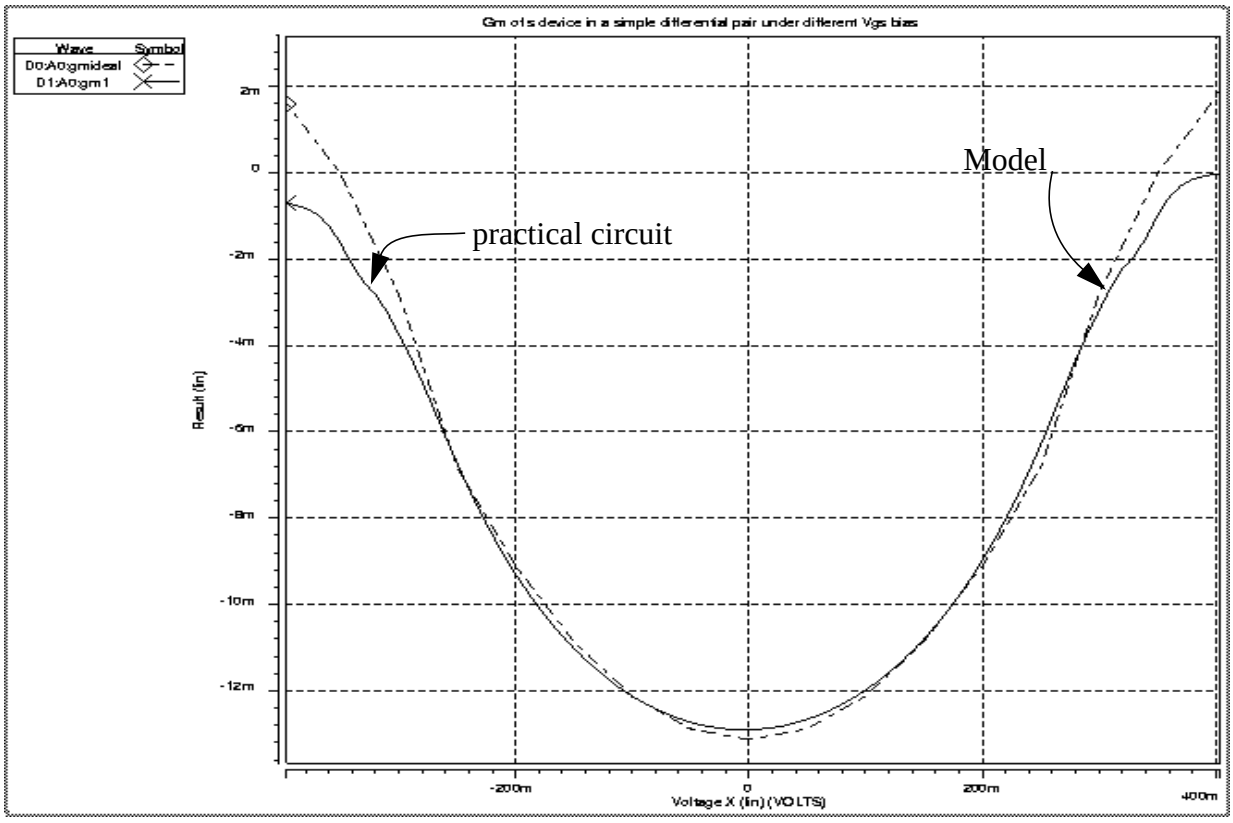
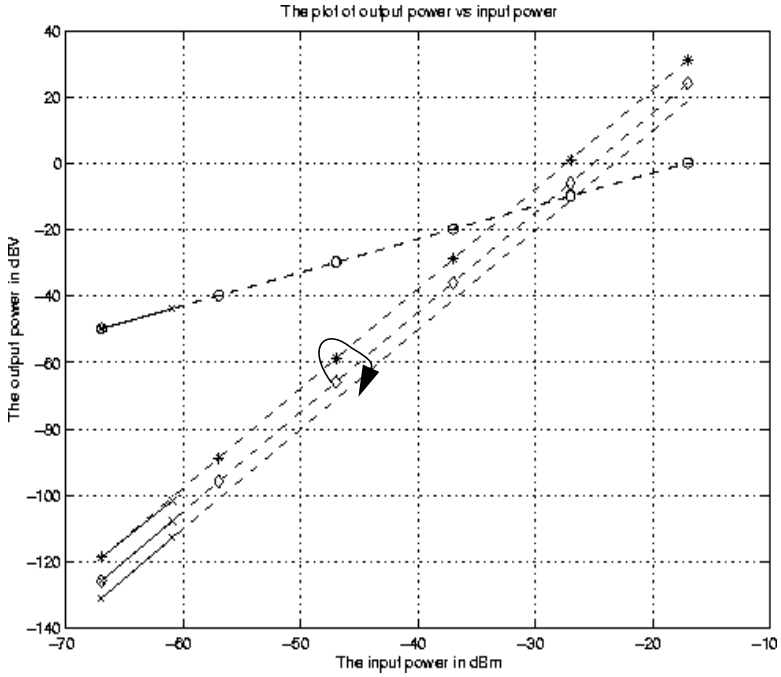


Fig. 5.5 The comparison of the modeled and actual gm value

5.4 Requirements on the linearity

Before designing suitable circuit for the application, it is important to identify the limitations of the existing solutions and the requirement we need so as to achieve the target.

As discussed in last section, the non-linearity is increased due to the voltage-dependent output impedance variation. The first one is the variation of the center frequency at large signal amplitude. The output impedance not only depends on the compensated transconductance value but also depends on both the inductance and the capacitance of the resonant circuit. The output impedance is repeated as



* c = 26.6 e-3 ⇨ IIP_3 = -32 dBm

◇ c = 13.3 e-3 ⇨ IIP_3 = -29 dBm

-- c = 6.65 e-3 ⇨ IIP_3 = -26 dBm

Fig. 5.6 The simulated IIP_3 of the bandpass amplifier with different degrees of non-linearity

$$Z(\omega_o) \approx \frac{L}{G_n L - R_s C_p}. \tag{5.4}$$

When the total capacitance is varied with the input signal, the output impedance is also changed and this affects the gain and the linearity of the whole circuit. Eventually, it is clear that the center frequency has to be less susceptible to changes of the output amplitude. Even though the frequency is quite constant, the linearity of the amplifier will be degraded due to the degradation of the reduction of the negative transconductance (G_n) when the signal level v_{in} is large. It is well known that a gm-cell is non-linear, that is, the gm value is inevitably not only independent to the signal amplitude but also degrades when the signal is large. A plot of gm versus input signal amplitude is given in Fig. 5.7. As the compensated transconductance is smaller, the output impedance of the resonant tank is also changed, the gain is compressed, and the linearity is degraded. It is worthwhile to point out that the negative conductance discussed in

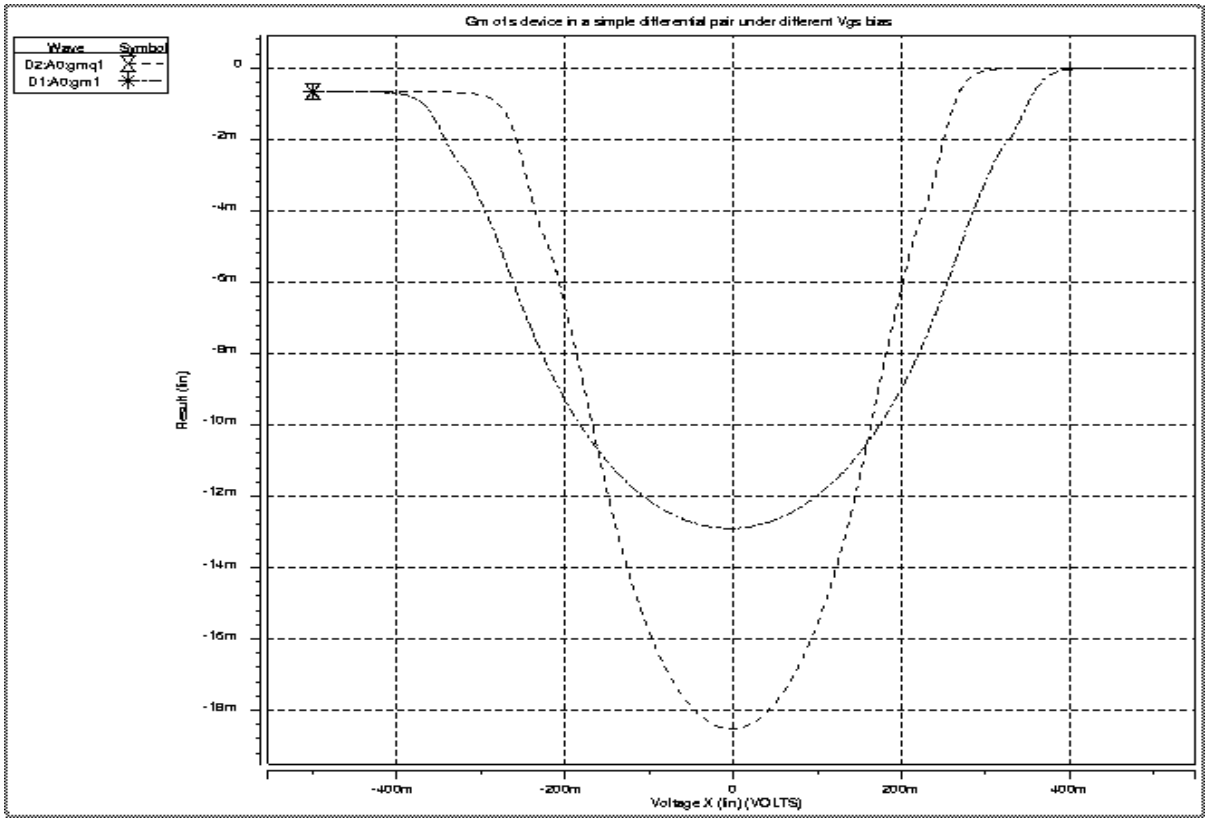


Fig. 5.7 A plot of the gm value versus input V_{in} with different gate bias

this chapter is referred to a single-ended transconductance rather than differential transconductance.

The differential output impedance can be proved to be

$$\begin{aligned} Z_{out,\,d} &= Z_{out,\,p} - Z_{out,\,n} \\ &= \frac{L}{G_{n,\,p}L - R_s C_p} + \frac{L}{G_{n,\,n}L - R_s C_p} \quad , \\ &= L\frac{(G_{n,\,p}L + G_{n,\,n}L - 2R_s C_p)}{(G_{n,\,p}L - R_s C_p)(G_{n,\,n}L - R_s C_p)} \end{aligned} \tag{5.5}$$

where the subscripts p and n denotes the positive and negative ended of the differential circuit respectively.

There are a lot of linearization techniques reported to provide relatively constant

differential transconductance over a broad input range. Yet, it is not applicable in this application. Beside the term ($G_{n,p}$+$G_{n,n}$), there exists a product term ($G_{n,p}G_{n,n}$) in the denominator in Eq. (5.5). Because the product term changes when the signal increases the overall output impedance and the linearity are directly affected.

In Eq. (5.5), when the positive-ended transconductance ($G_{m,p}$) is reduced, the negative ended transconductance ($G_{m,n}$) is increased correspondingly so that the overall differential transconductance is constant. However, this creates a potential instability for the Q-compensation circuit as either the positive or the negative-ended parallel resonant tank would be over-compensated by the large negative single-ended transconductance. As a result, the linearization techniques can only be used to provide constant differential transconductance but not constant single-ended transconductance. To sum up, there are two factors we need to take into account in the negative transconductance cell design. The first one is “constant” center frequency, and the second one is a “constant” negative transconductance not only for differential but even more important for single-ended.

5.5 Different types of linearization techniques

In this section, we will go over several types of linearization that are commonly employed in improving the linearity of the gm-cells including source degeneration and unbalanced-gm pairs. The working principles and the limitations are going to be discussed. Finally, a modified tuning circuit will be described and some simulation will be included as well.

5.5.1 Source-Degeneration

One of the commonly used techniques for improving the linearity of a gm-cell is source-degeneration depicted in Fig. 5.8.

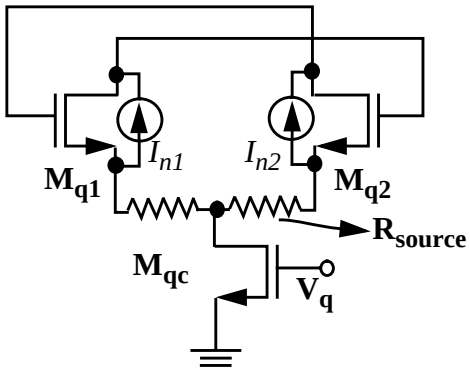


Fig. 5.8 Q-compensation with source degeneration

The effective Gm of Fig. 5.8 is

$$Gm = \frac{gm}{1 + gmR_{source}} \tag{5.6}$$

The linearity is related to the choice of R_{source}. If a large source resistor is employed, the linear range can be improved at the expense of an reduction of Gm. To achieve a specified Gm, this method needs to consume a lot more power. Another consideration is the noise degradation. It is clear that the noise performance will be worsen as the inclusion of the lossy resistor in the circuit. It is undesirable especially in the design of low noise circuits, therefore, it was not selected.

5.5.2 Unbalanced Transconductance pair/ Multi-tanh Approach

Another linearization technique, which is usually applied in the mixer design [13] to enhance the linearity, is the unbalanced gm-pair. The circuit diagram of this configuration is

depicted in Fig. 5.9. The two devices (M_1 & M_2) are scaled in a ratio of 1:M in a differential pair.

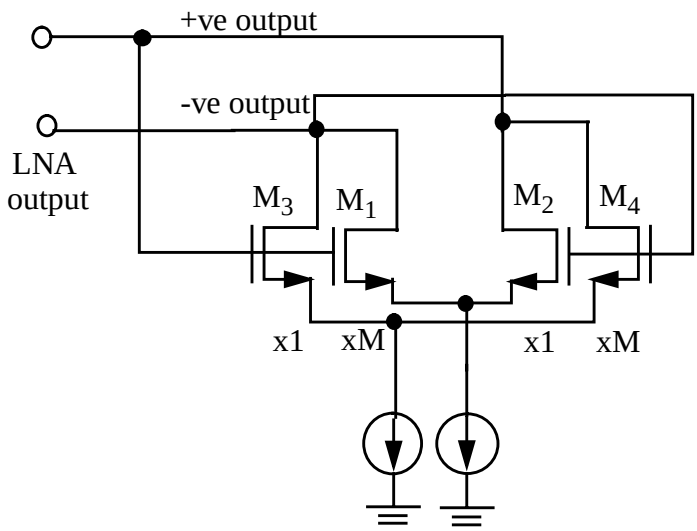


Fig. 5.9 The circuit diagram of an unbalanced gm-pair

The gm of transistors M_1 and M_2 in a simple differential pair and that of an unbalanced gm pair are drawn in Fig. 5.10. In a simple differential pair (M_1 and M_2 are of the same size), the

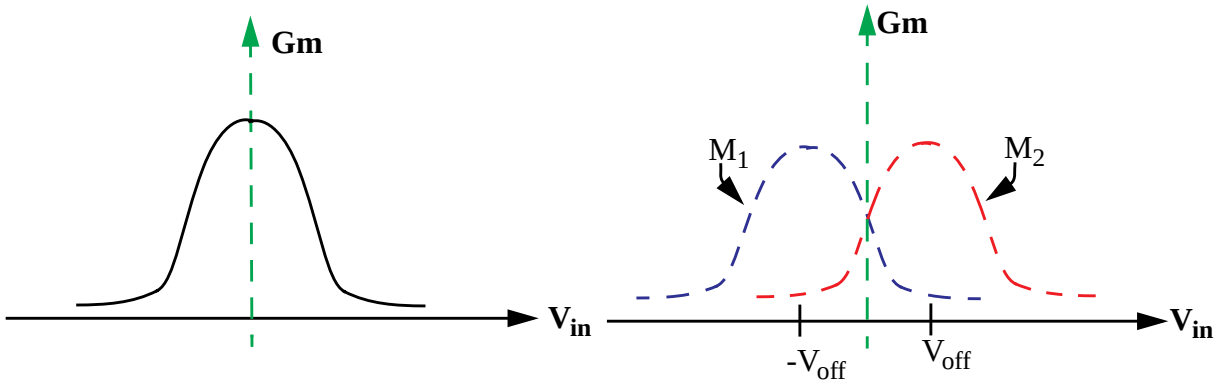


Fig. 5.10 The gm of the unbalanced gm-pair

gm for both transistors are the same. On the other hand, in an unbalanced gm pair, the gm of M_1 and M_2 are different as shown in Fig. 5.10 and depend on the ratio of the device size. The voltage offset V_{off}, where gm of M_1 or M_2 shifted, can be calculated by considering that when $I_{d1} = I_{d2}$ or

$I_{d3} = I_{d4}$,

$$\frac{1}{2}\mu C_{ox}\frac{W_1}{L_1}(V_{GS1} - V_t)^2 = \frac{1}{2}\mu C_{ox}\frac{W_2}{L_2}(V_{GS2} - V_t)^2$$

$$\frac{1}{2}\mu C_{ox}\left(\frac{MW_2}{L_2}(V_{GS} + V_{off} - V_t)^2 - \frac{W_2}{L_2}(V_{GS} - V_{off} - V_t)^2\right) = 0$$

$$\boldsymbol{V_{off} = -(V_{GS} - V_t)\frac{(\sqrt{M} - 1)}{(\sqrt{M} + 1)}} \quad , \qquad (5.7)$$

where V_{GSi} is the gate-to-source voltage of the device M_i. V_t is the threshold voltage of a device.

Without loss of generality, we have assume that all the parameters except W/L are the same. Clearly, the V_{off} is as a function of M. The gm of M_1 and M_2 are the same as that of the simple gm pair but merely shifted by $\pm V_{off}$ in x-axis respectively. Thus, the overall differential transconductance would be much flatter than that of a simple gm-cell. This is an attractive way to improve the linear range of a gm-cell.

Despite the fact that an unbalanced gm cell can provide a wider linear range, the parasitic capacitance associated with the unbalanced gm cell varies with the input small signal amplitude. When the input signal is positive and large, most of the resultant gm is resulted from M_1 and device M_2 is almost off or in sub-threshold region. The junction capacitances (C_{gd}, C_{gs}, C_{sb}, and C_{db}) of transistor M_2 change during the transition from one region to another. The effect is not so obvious for low frequency applications but becomes significant at high frequencies.

In addition, the effect would be more pronounced if a large portion of the parallel capacitance (C_p) of the resonant circuit is contributed from the Q-tuning circuit. The capacitance variation alters the center frequency of the resonant tank and in turn changes the output impedance and the gain of the amplifier. Even though the effect seems to be minor, it affects the

linearity of the amplifier significantly.

5.5.3 Modified unbalanced gm-pair [18]

The capacitance variation makes unbalanced gm pairs unsuitable as the Q-tuning circuit while the drawback of the simple differential pair is the degradation of the gm value at large input signal. Consequently, a simple differential pair combined with two pairs of unbalanced gm-cell is proposed in an attempt to provide a relatively constant gm over a larger input range. The circuit diagram of the Q-compensation circuit is illustrated in Fig. 5.11.

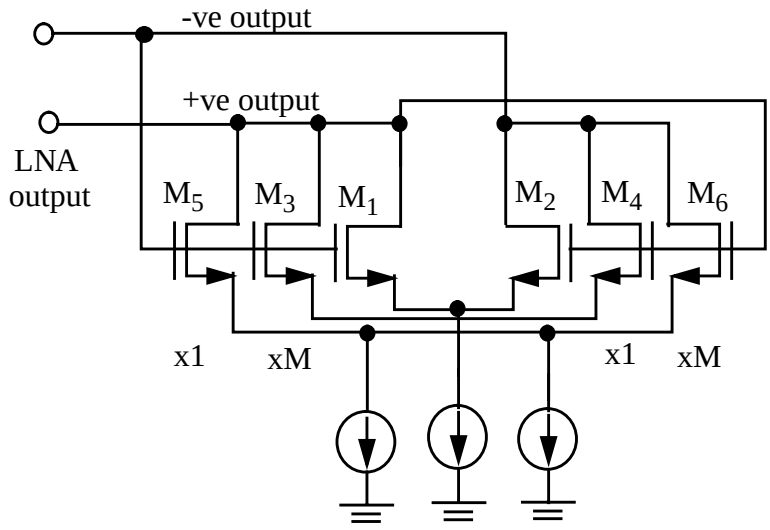


Fig. 5.11 The Q-compensation circuit with 2 pairs of unbalanced gm cells

M_1 and M_2 in Fig. 5.11 form the original simple negative gm-cell. M_3-M_4 and M_5-M_6 form two pairs of unbalanced gm-cell with a ratio of M to 1. In a simple transconductance cell, the small signal current is limited by the current source and will no longer proportional to input signal when the signal amplitude is large. The two pairs of unbalanced gm cells (M_3-M_4, M_5-M_6) provide extra current to maintain a constant gm.

Qualitative speaking, when the differential output signal is small, the current in the

unbalanced gm cell is drawn by M_3 and M_6, and almost no current flows in M_4 and M_5. When the output signal is positively large, the signal at the negative node goes down and V_{gs}-V_t of M_3 decreases. Meanwhile, as V_{gs}-V_t of M_4 increases, more current will be drawn by M_4. The current drawn by M_4 is small initially. Accordingly, the rate of current drop is slower than the rate of the voltage drop, the gm of M_3 increases. Similarly, when the signal is negatively large, the negative output node increases and V_{gs}-V_t of M_5 increases. More current flows into M_5, therefore, gm of M_5 increases. Since the gm of either M_3 or M_5 increases depending on the signal, they can provide the required gm at both positive and negative input signal to compensate the losses of M_1 and M_2 when the signals become large. Even though the same unbalanced gm cell is utilized, the function is not the same as the one described in Section 5.5.2. The gm is intentionally pulled much far away from the usual unbalanced gm cell does. The equivalent gm provided by the Q-compensation circuit is shown in Fig. 5.12. The resultant gm remains constant within a larger input range than the original design.

Quantitatively, the gm degradation of the simple gm-cell within 5% is less than $\pm$ 65 mV input voltage while that of the modified design is improved to $\pm$ 100 mV. Another consideration is about the capacitive variation. Because most of the negative gm is provided by the simple differential pair and the unbalanced gm-cell is only designed for gm compensation at large signal level, the width-length ratio of the unbalanced gm-pair is relatively small. As a result, the capacitive variation is much smaller than using unbalanced gm-pair alone. The sizes of the

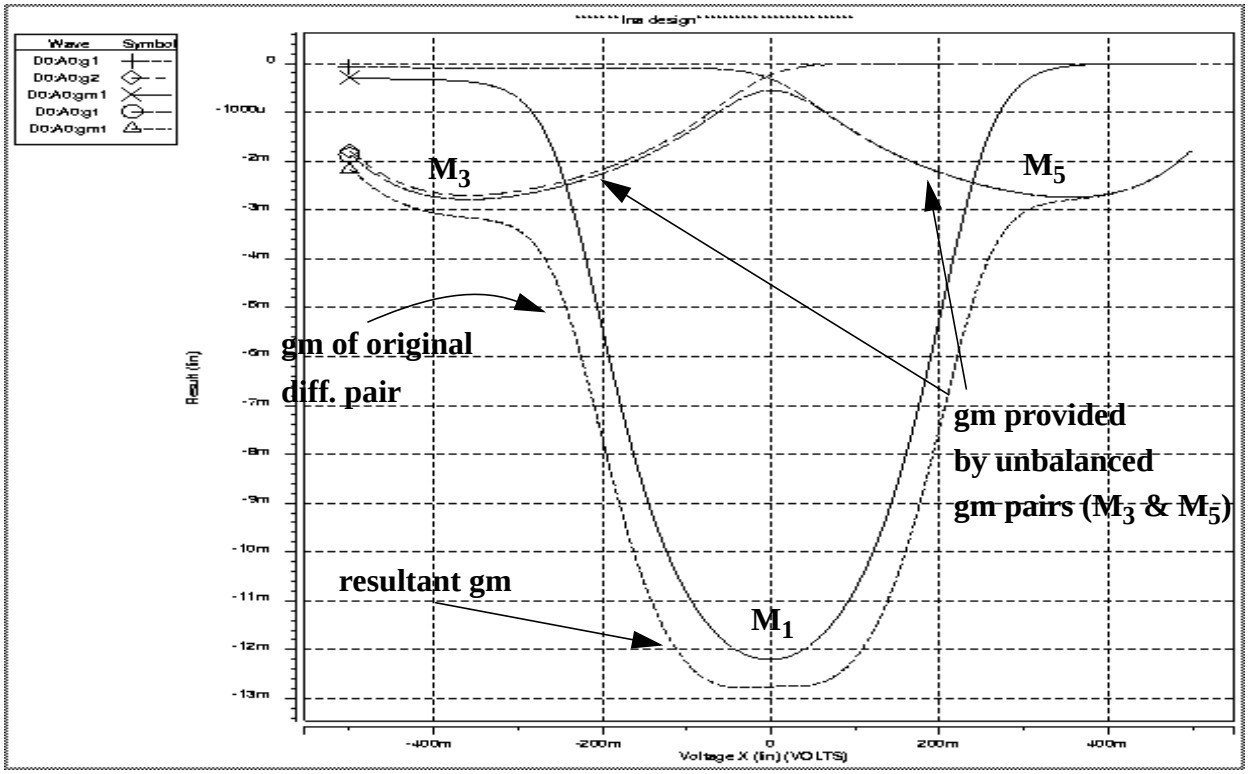


Fig. 5.12 Gm curves with and without unbalanced coupled pairs

designed gm-cells are tabulated in Table 5.1. A comparison of the linear range, the power and the

Transistor(s)	**Size** (μm/μm)
M_1, M_2	57/1.65
M_3, M_6	19.95/0.6
M_4, M_5	19.95/1.2

Table 5.1: The size of the modified Q-tuning circuit

capacitance variation are given in Table 5.2.

Parameters	**Simple-Gm pairs (V_{gs}-V_t=0.5-V)**	**Unbalanced Gm-Pair**	**Our design**
Gm variation (~ 5%)	± 90 mV	± 100 mV	± 100 mV

Table 5.2: The comparison of three different linearization techniques

Parameters	Simple-Gm pairs (V_{gs}-V_t=0.5-V)	Unbalanced Gm-Pair	Our design
Capacitive variation	0.01 pF	0.08 pF	0.01pF
Power Con-sumption	9 mA	8 mA	7 mA

Table 5.2: The comparison of three different linearization techniques

5.5.4 Linearity

To demonstrate the improvement in the linearity of the bandpass amplifier, two-tones, located at 947 MHz and 947.8 MHz with the same power are applied at the input of the circuit. In addition to the fundamental output power at 947 and 947.8 MHz, the output third-order intermodulation products at 948.6 MHz are also measured and plotted against the input power in Fig. 5.13. The simulated IIP_3 is -15 dBm and the 1-dB compression point is around -30 dBm. As

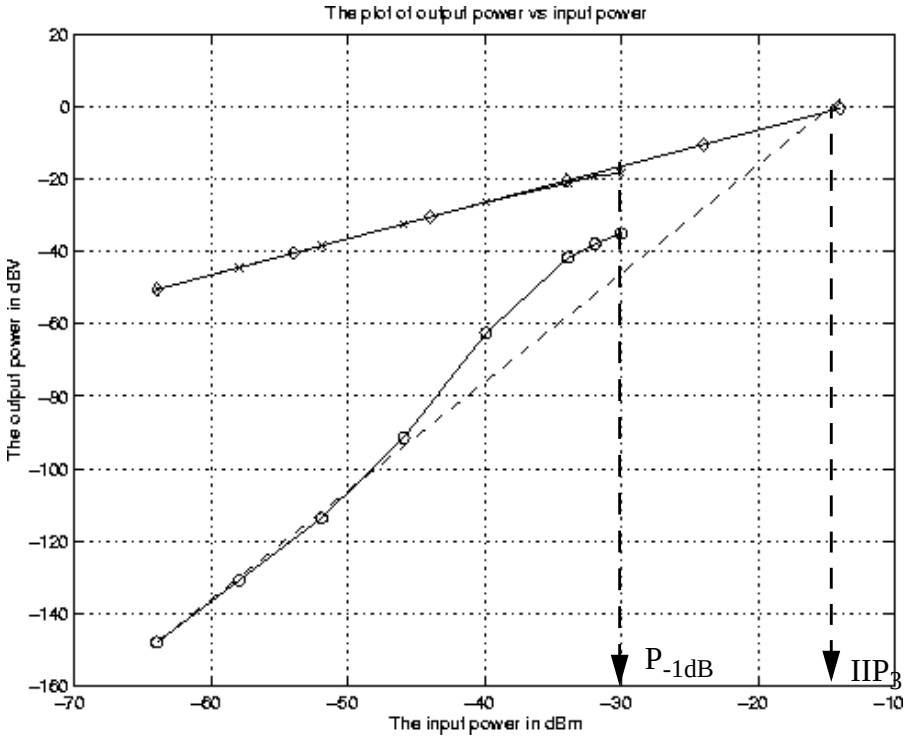


Fig. 5.13 The relationship between fundamental output power, third-order intermodulation and input power

compared to the linearity of the bandpass amplifier employing simple differential pair as Q-compensation circuit, the improvement is quite obvious.

Chapter 6

High-Order Bandpass Amplifier Design

6.1 Introduction

As discussed in Section 2.3.3, the combined image rejection of a LNA and an image-reject filter has to be at least 40 dB. Typical LNAs definitely cannot provide enough attenuation at the image frequency. Even for the bandpass amplifier in Chapter 3, the image rejection at 140 MHz away from the desired signal is merely 18 to 20 dB. As a result, an off-chip image-reject filter is needed between a LNA and a mixer in conventional receiver architecture to filter out strong interferers and image signals. Nevertheless, this filter is usually bulky in size and requires matching networks at both its input and its output, and thus it would need to be eliminated ultimately in a monolithic receiver. To provide enough image rejection on-chip, a second-order RF bandpass filter that will be used as part of sixth-order design is described first. Afterwards, the design of a sixth-order bandpass amplifier is discussed. To demonstrate the functionality, some simulation results are also included.

6.2 Bandpass Filter Design

The implementation of the bandpass filter is now addressed. Basically, the bandpass filter design is very similar to the bandpass amplifier in Chapter 3. It also comprises an input transconductance stage and a parallel LC resonant circuit. A simplified schematic of the bandpass filter is shown in Fig. 6.1. As presented in Chapter 4, inductive source degeneration utilized in the

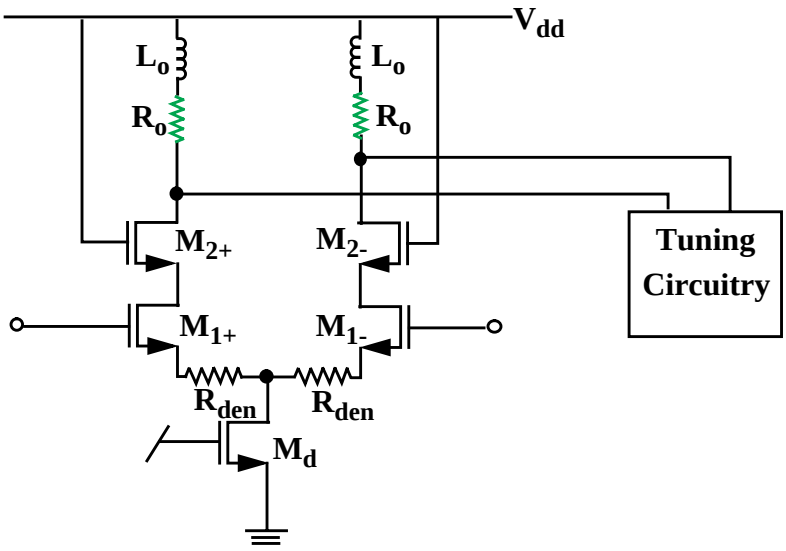


Fig. 6.1 The schematic of a bandpass filter

bandpass amplifier design can help reduce the noise of a circuit but its large area consumption makes it less attractive especially when the noise of the filter can be attenuated by the high amplifier gain. As a result, resistive source degeneration (R_{den}) was employed to improve the linearity of the input devices as the signal have already been amplified by 20-30 times by the bandpass amplifier in front. The tuning circuits in the bandpass filter are chosen the same as the one discussed in the amplifier design.

6.2.1 Biasing Circuit

A single 2-V supply voltage is utilized in the three-stage design to reduce the power

consumption. Since there is almost no voltage drop across the inductor, the bandpass amplifier dc output voltage is close the supply voltage and it is too high to drive the input of bandpass filter directly. On the other hand, the dc common-mode voltage after a voltage follower is too low (1.2-V) to bias the filter input transconductance stage. Therefore, the filter input needs to be self-biased. Even though an off-chip bias-tees can generate the required dc bias, it is convenient to synthesize the dc bias on-chip. The circuit diagram of the dc bias is depicted in Fig. 6.2.

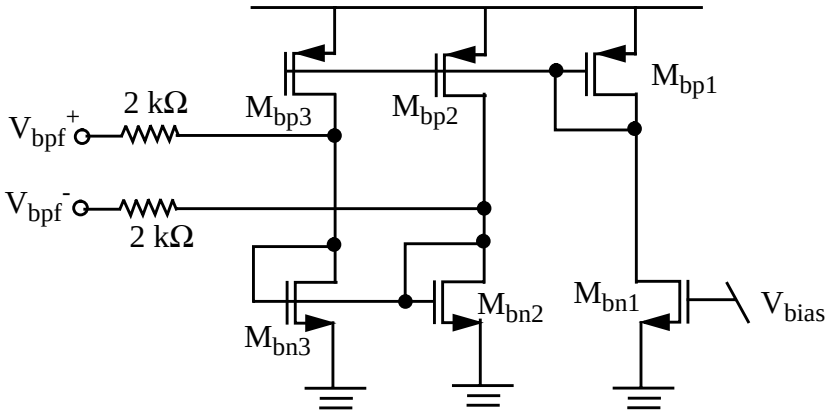


Fig. 6.2 The dc biasing circuit

The working principle is as follows. The voltage V_{bias} at the gate of M_{bn1} controls the current flowing through M_{bp2} and M_{bp3} through the current mirror M_{bp3}. This current change in turn can alter the dc biases V_{bpf}^{+} and V_{bpf}^{-} by varying the gate voltage of the diode-connected nMOS M_{bn2} and M_{bn3}. A 2 kΩ resistor is added to isolate the low impedance diode-connected nMOS device from the input of the bandpass filter.

The ac signal from the amplifier is ac-coupled through an ac-coupling capacitor to the input of the filter as depicted in Fig. 6.4. The capacitance of an on-chip ac-coupling capacitor is usually large so that its impedance at the frequency of interest is small enough to minimize the

signal losses. As an example, when an ac-coupling capacitor is connected to the gate of a transistor (~ 0.2 pF), the capacitance of the ac-coupling capacitor is at least 2 pF in order to restore 90 percent of the signal at the gate of the device at 1 GHz.

However, since the gain of the bandpass amplifier (1st-stage) is high, the signal attenuation at the ac-coupling capacitor actually helps reduce the amplified signal before entering the first bandpass filter. At the same time, the transconductance of the bandpass filter can be increased to reduce the noise of itself and of subsequent stages.

6.2.2 Simulation Result of the bandpass filter

The frequency response and the noise figure of the bandpass filter are illustrated in Fig. 6.3. The center frequency is at around 925 MHz with a maximum gain of 5 dB. The frequency tuning range of the design is similar to that of the bandpass amplifier, which is around 80 MHz. Its power consumption is 26 mW. The minimum noise figure with respect to a 50-Ω source resistor is 24.3 dB which occurs at the center frequency of the filter.

6.3 Three-stage, sixth-order Bandpass Amplifier Design

The sixth-order bandpass amplifier is realized by cascading one bandpass amplifier and two bandpass filters (three-stage) as illustrated in Fig. 6.4. They are connected together through ac-coupling capacitors as shown in Fig. 6.4 in order to be able to operate at supply voltage as low as 2-V. The most important considerations of the design are the distribution of the gain, of the quality factor and of the center frequency among the three stages. In choosing these parameters, linearity and noise performance of the whole circuit also have to be taken into consideration. As

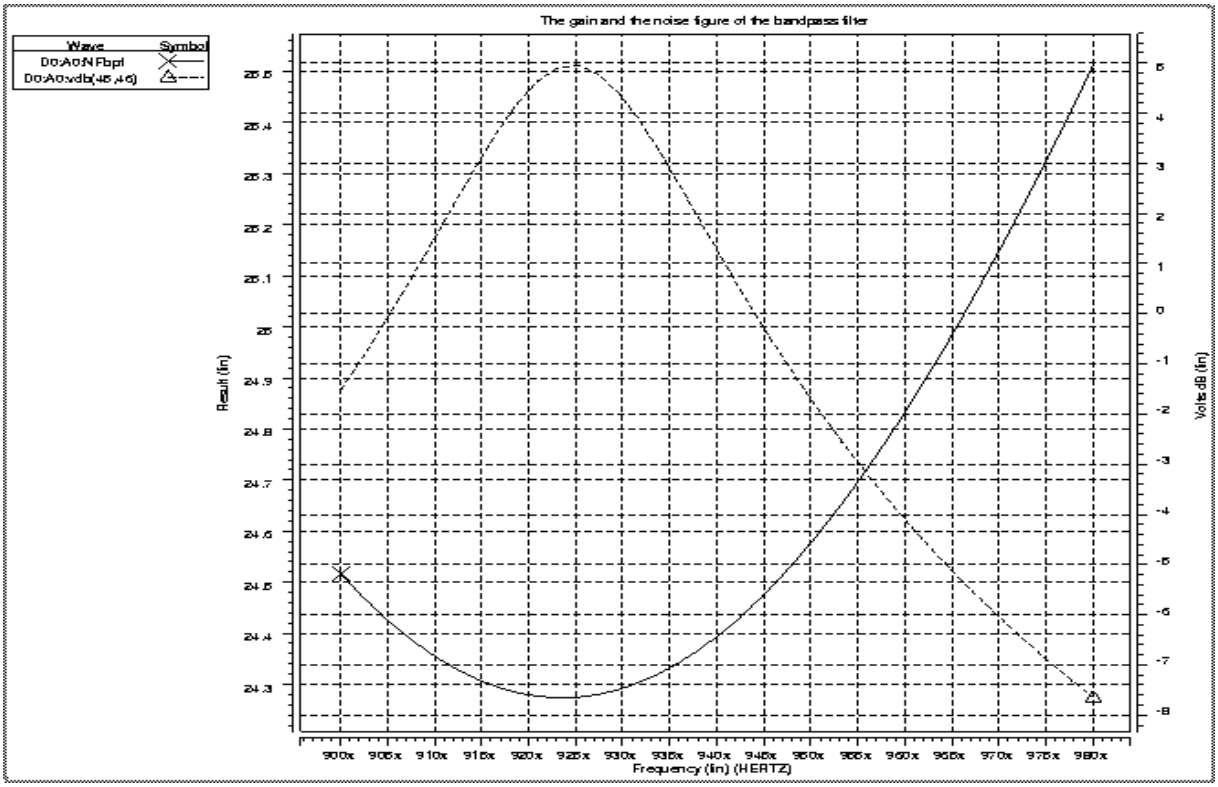


Fig. 6.3 The frequency response and the noise of the bandpass filter

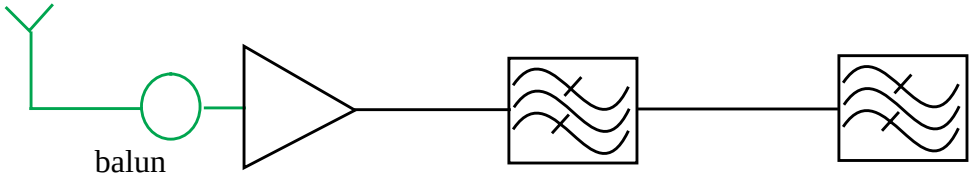
discussed earlier, the required linearity of the tuning circuits limits the overall gain to be around 28 dB at maximum so as to satisfy GSM's linearity requirement.

6.3.1 Gain Consideration

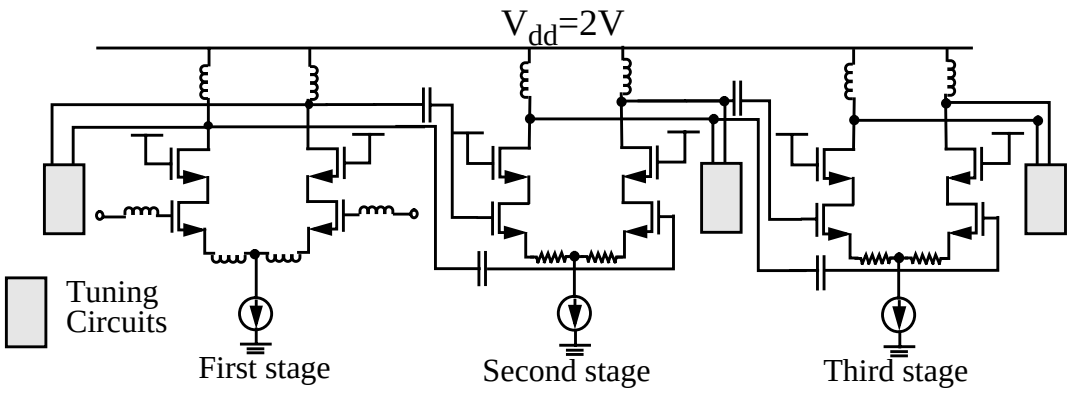
It should be noted that the gain distribution in each stage affects the total noise figure of the whole receiver. As stated earlier in Chapter 4, the noise figure of the receiver can be calculated using the Friis's equation on system noise factor (F_{sys}) [23] and it is repeated below for reference,

$$F_{sys} = 1 + (F_1 - 1) + \frac{(F_2 - 1)}{A_{p1}} + \ldots + \frac{(F_m - 1)}{A_{p1} \cdots A_{p(m-1)}} . \qquad (6.6)$$

where the F of each stage is calculated with respect to the source impedance of the preceding stage and F_i and A_{pi} are the noise factor and the available gain of the i-th stage. As illustrated Eq.



(a)



(b)

Fig. 6.4 Block diagram and schematic of the sixth order Bandpass Amplifier

(6.6), the noise of the i-th stage will be attenuated by the available gain of the preceding stages, $A_{p1} \cdots A_{p(m-1)}$. Therefore, it is prudent to keep the gain of the first few stage large enough so that the noise power at the subsequent stages can be reduced provided that the gain will not saturate any stage in the system. As a result, the gain of the bandpass amplifier is set to be around 25 dB, which provides most of the gain in the three-stage design. The high amplifier gain helps reduce the noise from the two noisy bandpass filters and the later stages in the receiver. With the amplifier's gain fixed, the filter's gain can also be determined easily. The designed filter gain is around a few dB (< 5) and it is chosen so that the noise of the filter can still be reduced by a small gain of the filter.

6.3.2 Distribution of the Quality Factor

The overall image rejection depends mainly on the quality factors of all three stages Q_1, Q_2 and Q_3. It is well known that a high Q can provide better image rejection but a smaller 3-dB bandwidth. To satisfy an overall 25 MHz 3-dB bandwidth and better image rejection at the same time, the relationship of the image rejection and the quality factors is studied. Without loss of generality, the discussion below is focused on the design of the two-stage design, yet, the general idea can also be extend to the three-stage design.

6.3.2.1 Equal Center frequencies

The most straight forward configuration is that the center frequencies of the first stage and the second stage are the same. In this case, the bandwidth of either one must be larger than 25-MHz, else, the overall attenuation at 25-MHz would be 6 dB instead of 3 dB. In other words, the quality factor of either stage or both needs to be reduced. As stated earlier, the image rejection greatly depends on the quality factor, and a reduction of the quality factor inevitably degrades the image rejection. To study what are the optimal value for the Q-factor of the bandpass amplifier, Q_1, and the Q-factor of the bandpass filter, Q_2, to achieve maximum image rejection, a plot of Q_1 and Q_2 that can provide an overall 25-MHz 3-dB bandwidth is depicted in Fig. 6.5. As expected, when Q_1 is large, Q_2 has to be reduced so as to maintain the same 3-dB bandwidth, and vice versa. For all possible combination of Q_1 and Q_2, the maximum image rejection at 140 MHz away from the desired signal is 34 dB when Q of both stages are the same and equal to 24. The condition is similar for the three-stage design, however, the quality factor of Q_1, Q_2 and Q_3 will be even smaller (~ 20) than the Q in two-stage design. Nonetheless, the increment in the image

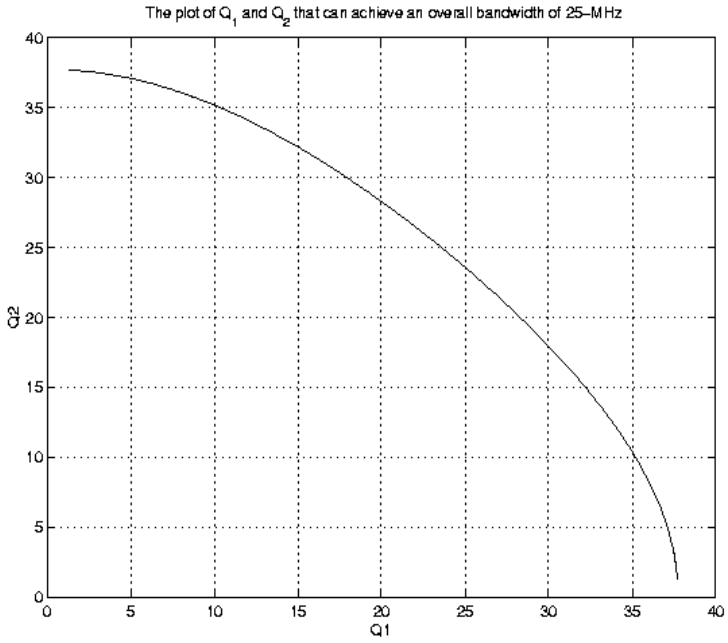


Fig. 6.5 A plot of the possible Q_1 and Q_2 that can achieve 25-MHz 3-dB BW

rejection will be diminished as the number of stages continue to increase so as to maintain a 25-MHz bandwidth.

6.3.2.2 Unequal Center Frequencies

Another possible scenario is that when the center frequencies of the first and the second stage are designed to be separated slightly in frequency (within 25 MHz), the 3-dB bandwidth of the overall response is no longer merely governed by the quality factors Q_1 and Q_2, but depends on the frequency separation of the two bandpass response as well. If the two bandpass responses are separated too far, a trough will occur in the passband and it affects the gain and the image rejection of the overall circuit. On the other hand, if the two response separation is less than 25 MHz, the 3-dB bandwidth of the overall response is extended above 25-MHz. In order to maintain the designed bandwidth, both Q_1 and Q_2 have to be increased to attenuate the signal enough at 25-

MHz bandwidth. This increase in Q_1 and Q_2 improves the image rejection ability. For this reason, the center frequencies of both stages are intentionally separated slightly. The frequency response of a two-stage design with different center frequencies is given in Fig. 6.6.

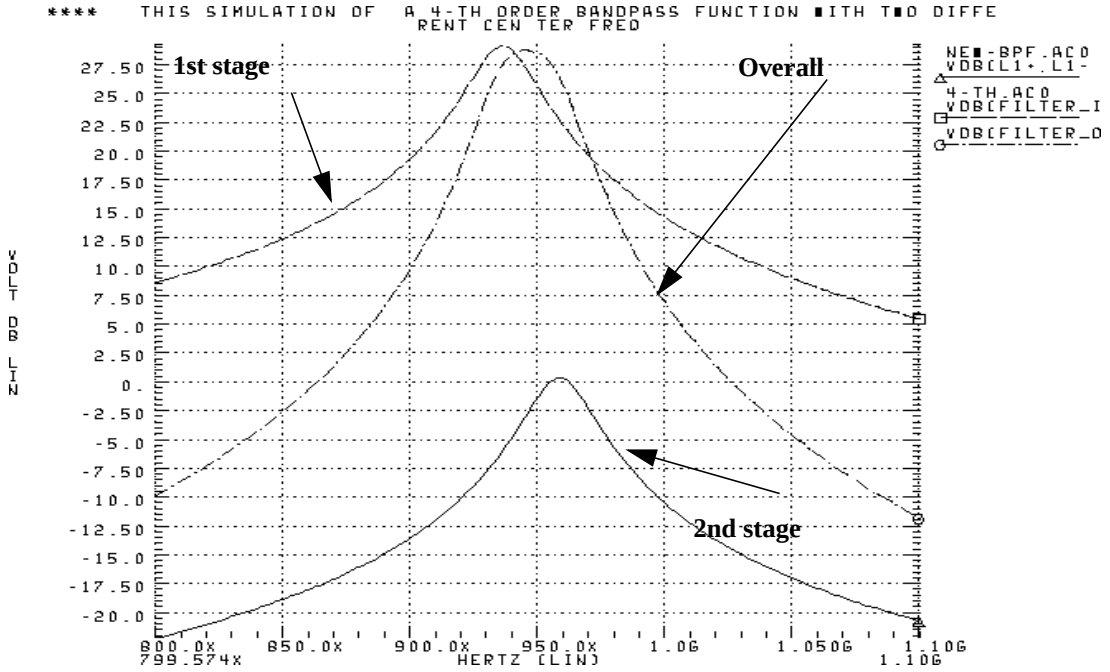


Fig. 6.6 The frequency response of the first stage, the second stage and the overall circuit

Nevertheless, high Q is accompanied with higher gain and degrades the overall linearity. Fortunately, when the center frequencies are slightly different, the maximum gain of the overall response occurs at frequency between that of the first stage and the second stage. Furthermore, the overall gain will be smaller than the combined gain of both stages when the center frequencies are the same. As shown in Fig. 6.6, signals at the center frequency of the first stage is attenuated by the response of the second stage. Likewise, signals at the center frequency of the second stage is already reduced by the first stage. Because the gain of the overall response is smaller, it can be increased until the linearity limit of the tuning circuit is reached. As shown in Fig. 6.6, most of the gain is concentrated on the first stage, the amplifier, and the gain of the bandpass filter is around 5

dB to reduce the noise at the filter output. The overall image rejection of the two-stage design is around 37 dB. There is a 3-dB improvement in image rejection when compared to the rejection achieved with the center frequencies of both stages being the same.

6.4 Simulation Results of the three-stage design

6.4.1 Design with Three Stages Having Same Center Frequencies

As a comparison, the three-stage design with equal center frequencies is described first. The designed parameters of each of the three stage are depicted in Fig. 6.7 and summarized in Table 6.1.

As discussed earlier in the chapter, if the center frequencies are the same (946.5 MHz in this case), the quality factor of each of the three stages needs to be reduced to achieve the same 3-dB bandwidth, 25 MHz. The designed Q_1, Q_2 and Q_3 are 20, 20 and 18 respectively when compared to 38 in a single-stage design. The overall 3-stage gain is reduced to 17 dB. The frequency response at the output of each stage is illustrated in Fig. 6.8.

Parameters	First stage	Second stage	Third stage
Center frequency	946.5 MHz	946.5 MHz	946.5 MHz
Gain	23 dB	1.5 dB	-1 dB
Q	20	20	18

Table 6.1 The gain, center frequency and the Q distribution among the three stages

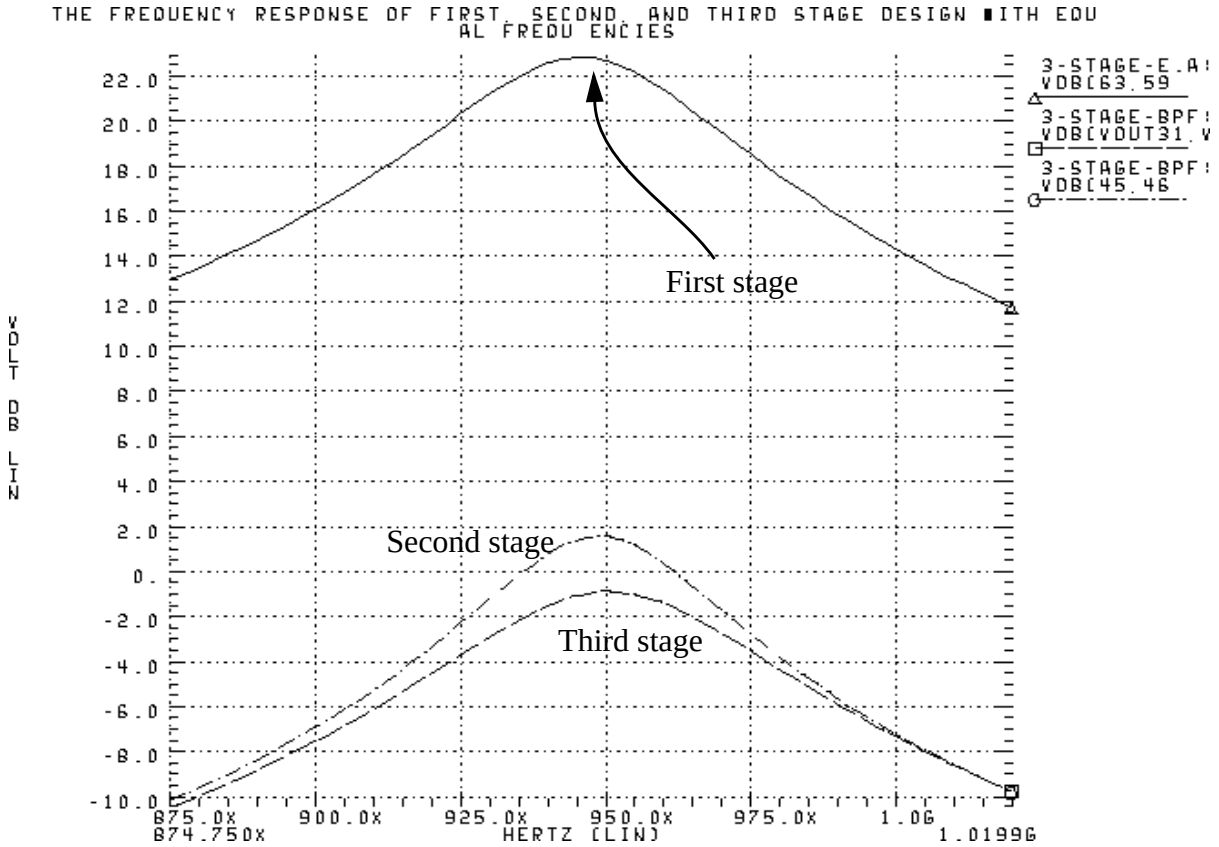


Fig. 6.7 The frequency response of the sixth-order bandpass amplifier

The information about the three-stage design is tabulated in Table 6.2. The overall image

Parameters	At the amplifier output	At the first filter output	At the second filter output
Center frequency	946.5 MHz	946.5 MHz	946.5 MHz
Gain	23 dB	21 dB	17 dB
Image Rejection	15 dB	32 dB	47 dB

Table 6.2: Information at the output of the first, second and the third stage with equal center frequencies

rejection achieved by the three-stage design at 140 MHz away from the desired signal is only 47 dB.

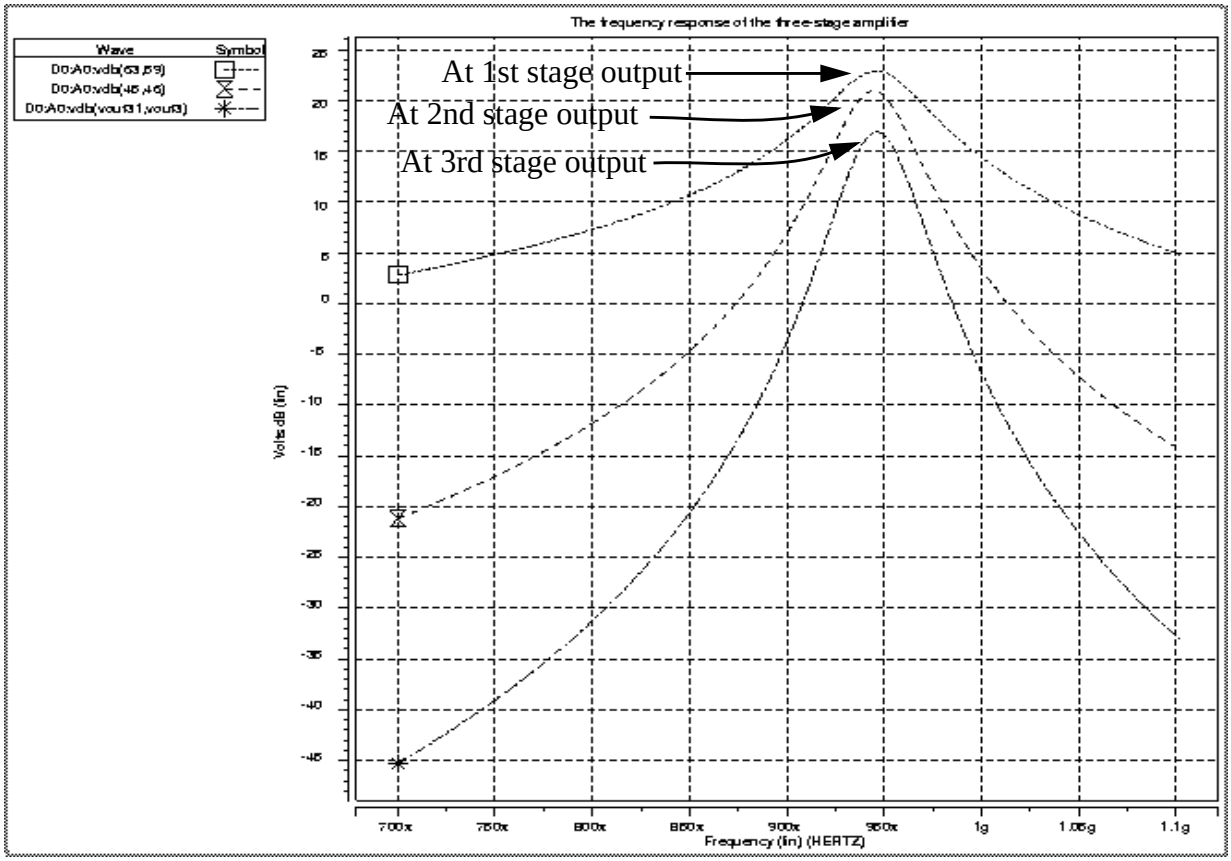


Fig. 6.8 The frequency response of the sixth-order bandpass amplifier (with equal center frequencies

6.4.2 Design with Three Stages Having Unequal Center Frequencies

The simulation results of the design with the center frequencies of the three stages to be slightly different is now addressed. The frequency response of the first stage, the second stage and the third stage are given in Fig. 6.9. The details of these three stages are also tabulated in

Parameters	First stage	Second stage	Third stage
Center frequency	941 MHz	925 MHz	953 MHz
Gain	28 dB	5 dB	5.7 dB
Q	38	34	38

Table 6.3: The gain, center frequency and the Q distribution among the three stages

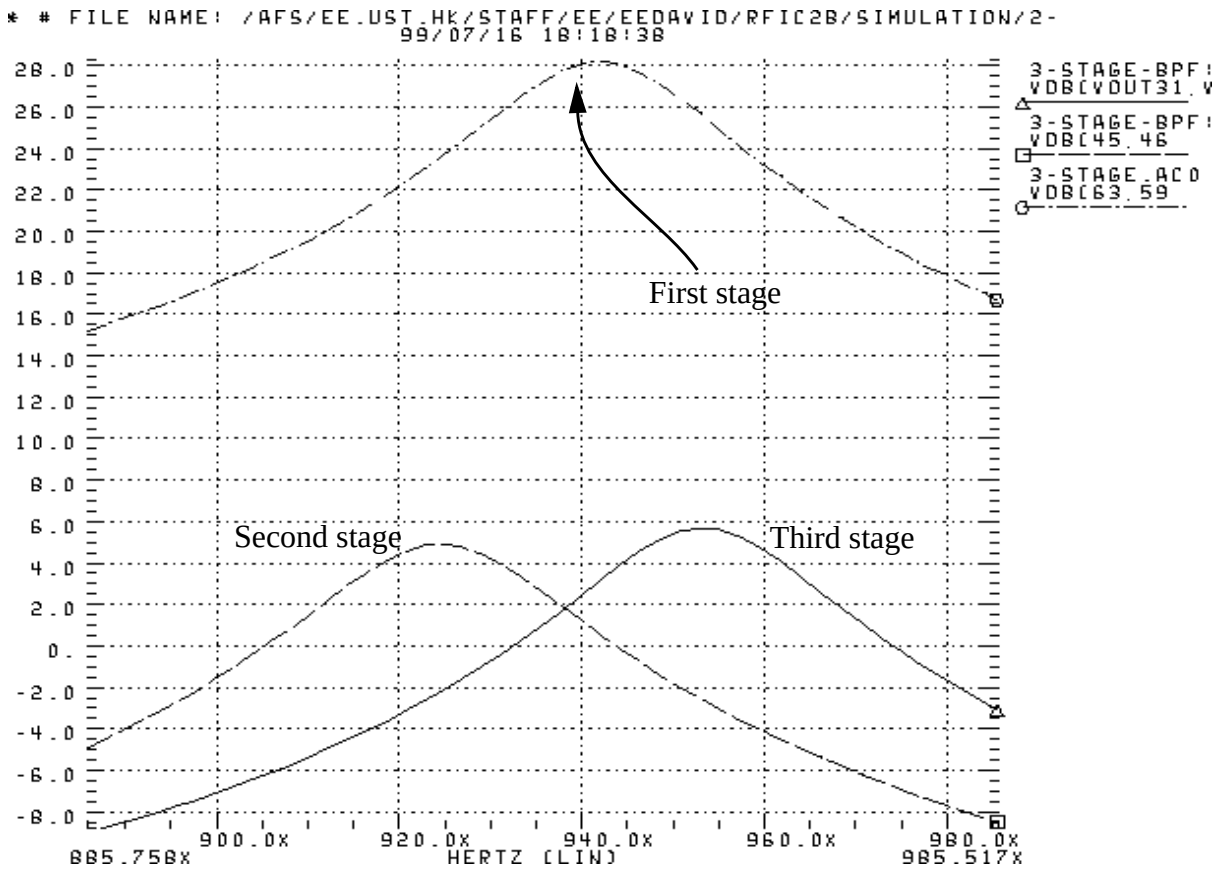


Fig. 6.9 The frequency response of the sixth-order bandpass amplifier (with center frequencies of the three stages to be slightly different)

Table 6.3. The center frequency of the first stage is selected close to the center frequency of the overall response so that the noise contributed by the subsequent stages can be reduced by the maximum gain of the first stage. As the second and the third stage are identical, their center frequencies are interchangeable without affecting the performance of the whole circuit and they are chosen so that an overall 25 MHz bandwidth can be achieved and the gain is also within 28 dB.

The frequency responses at the output of each of the three stages are depicted in Fig. 6.10.

The corresponding gain, center frequency and image rejection are tabulated in Table 6.4.

Parameters	At the output of the first stage	At the output of the second stage	At the output of the third stage
Center frequency	941 MHz	932 MHz	943 MHz
Gain	28 dB	27 dB	26 dB
Image Rejection	20 dB	37 dB	54 dB

Table 6.4: The gain, the center frequency and the image rejection of using single, two and three stage design

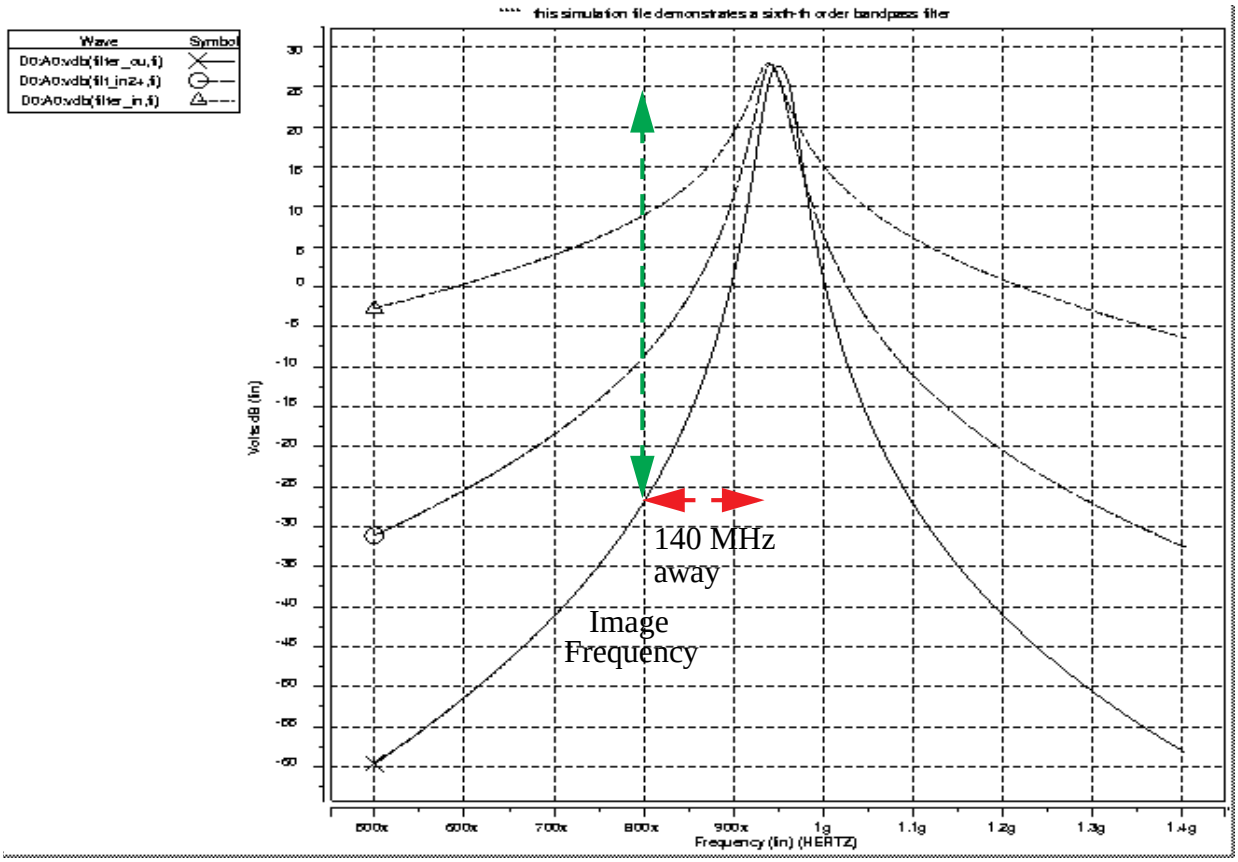


Fig. 6.10 The frequency response of the sixth-order bandpass amplifier with unequal center frequencies

For the fourth-order bandpass amplifier, the simulated image rejection at 140 MHz away from the desired signal is 37 dB. For the sixth-order response, the simulated signal attenuation at the same image frequency is 54 dB. When compared to a 47 dB image rejection achieved by the

design with same center frequencies in each stages, the improvement is quite impressive.

The noise figures of the single-stage, the two-stage and the three-stage amplifier design are simulated and plotted in Fig. 6.11. Their corresponding noise figures near the resonance are

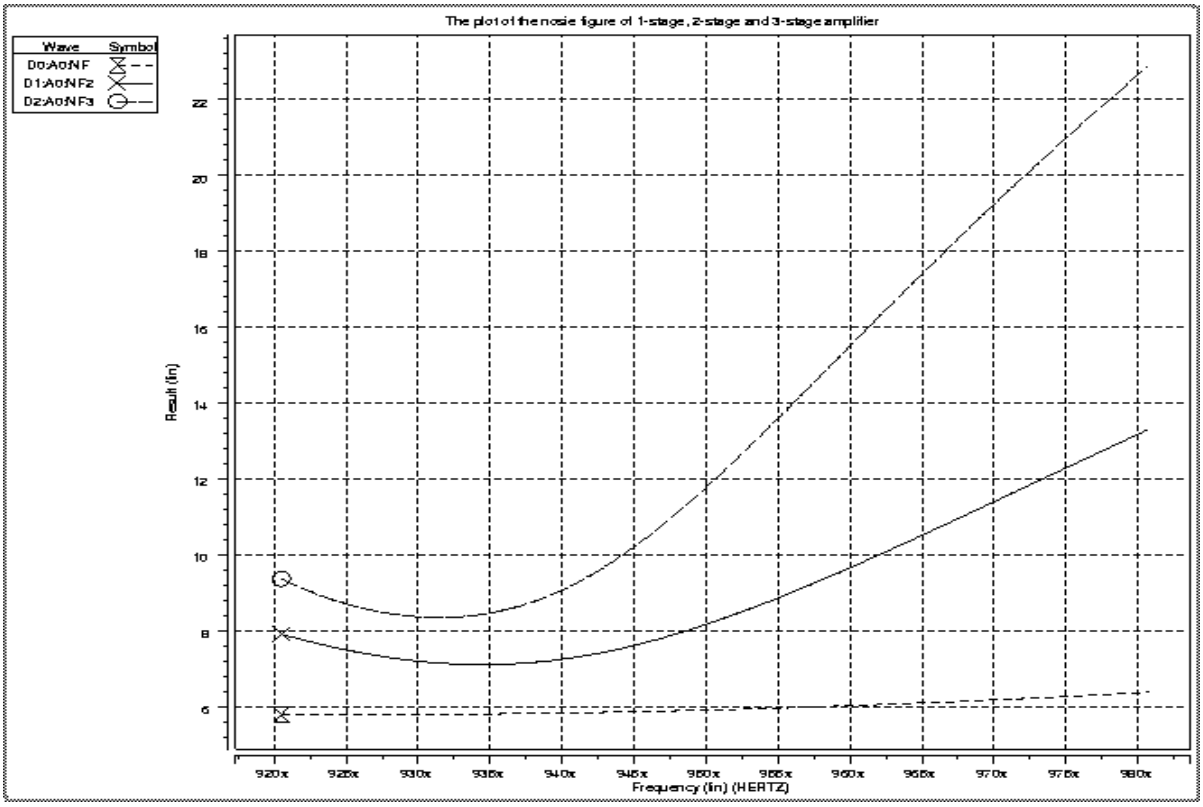


Fig. 6.11 The plot of the noise figure of 1-stage, 2-stage and 3-stage bandpass amplifier versus frequency

summarized in Table 6.5.

For the three-stage design, the minimum noise figure occurs near its center frequency, the noise figure of the first stage is around 5.8 dB while the noise figure at the output of the second stage is around 7.2 - 7.6 dB. At the output of the third stage, the noise figure has increased to 9 dB. The noise figure is increased by around 1.5 dB after going through each filter stage. Because the gain of the filter is close to unity, the noise at the output of the second and the third stage are almost un-attenuated when they are referred to the output of the first stage. Therefore, the noise

contribution of the first and the second filter is about the same. The noise figure begins to rise

Frequency	Single-stage (NF)	Two-stage (NF)	Three-stage (NF)
940 MHz	5.8 dB	7.2 dB	9 dB
945 MHz	5.85 dB	7.6 dB	10 dB
950 MHz	5.9 dB	8.1 dB	12 dB

Table 6.5: The corresponding noise figure of the single, two and three stage design

when it deviates from the center frequency of the design as the overall gain becomes smaller. Also, the noise contribution from the second and the third stage is actually amplified by the filter's loss instead of being reduced by the filter gain when it is referred to the input of the three-stage design. As a result, the total noise figure increases.

The linearity of the three-stage design is verified by the two-tone test. Two closely spaced input signals at 942.2 and 941.4 MHz with the same power are applied at the input of the amplifier, and both the fundamental (P_{fund}) and the third-order intermodulation power ($P_{o,3rd}$) at the output of the filter are measured. The relationship between P_{fund}, $P_{o,3rd}$ and the input power are plotted in Fig. 6.12.

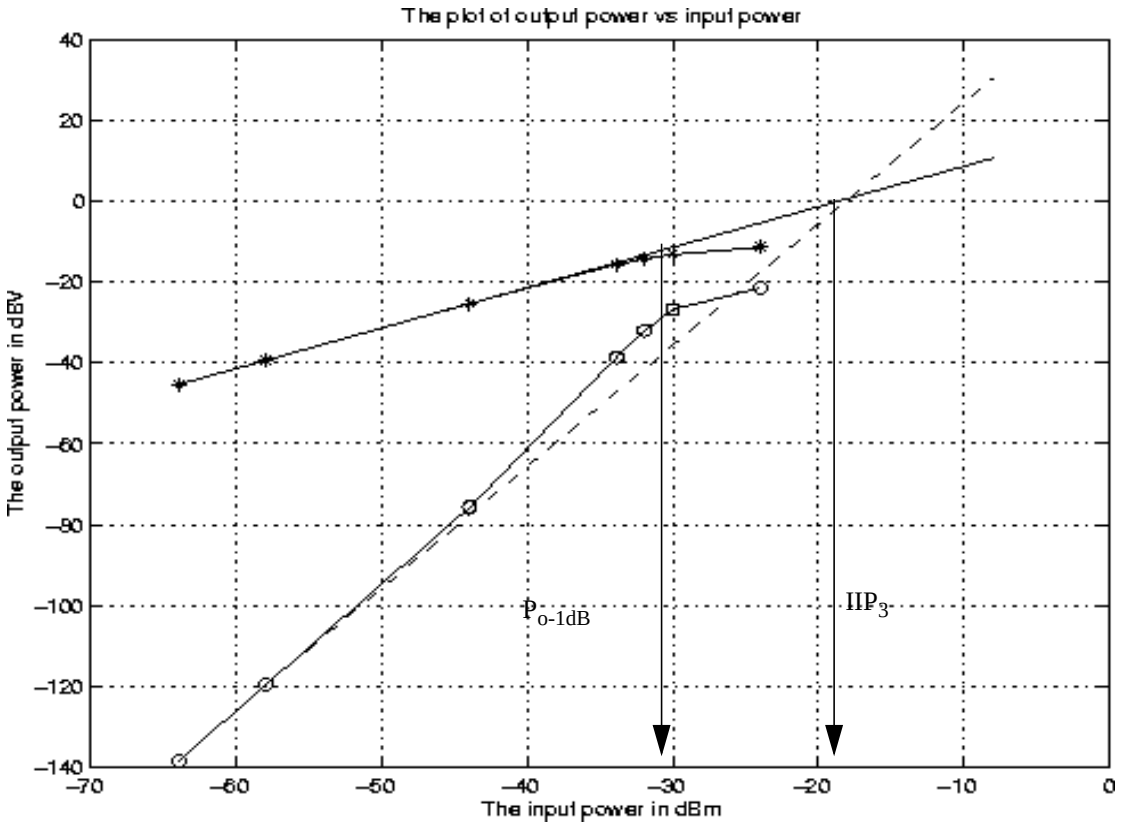


Fig. 6.12 The IIP_3 and $P_{o\text{-}1dB}$ plot for the sixth-order bandpass amplifier

Chapter 7

Layout Considerations

7.1 Introduction

Layout is the final design step where the circuit is transformed to its physical representation. Since a lot of processing steps are involved in the fabrication, process variations are difficult to be predicted very accurately during the design phase. No matter how well is the circuit design, a poor layout can lead to performance degradation and even circuit failures. So, careful floor plan and layout considerations are important, particularly to high frequency circuits which are sensitive to parasitics. This chapter describes the layout techniques of some basic elements that are utilized in the bandpass amplifier and filter design, including that of spiral inductors.

7.2 Inductor Layout

7.2.1 General Design Overview

Low quality factor of on-chip inductors usually limits their performance. As stated in Section 3.3.2, the topmost layer of metal is used in an inductor layout to separate the inductor from the lossy silicon substrate. In addition, its sheet resistance is the smallest. A wide metal width can help to reduce the series resistance of a metal inductor, but, at high frequencies, current actually does not flow near the center of the metal due to the well-known skin effect. The skin depth δ_s of a conductor can be calculated as

$$\delta_s = \sqrt{\frac{2}{\omega\mu_o\sigma}} = \sqrt{\frac{1}{\pi f\mu_o\sigma}} \ , \qquad (7.1)$$

where f is the frequency of interest, μ_o and σ are the permeability of space and the conductivity of the metal respectively. For pure aluminum, the skin depth can be estimated to be around 2.7 μm at 900 MHz. Due to the skin effect, the metal width that is larger than 10 μm can be considered to be a good conductor at frequency around 1 GHz. At the same time, the metal width should not be too large as the parasitic capacitance associated with the inductor is proportional to the inductor's size. The larger is the inductor size, the lower is the self-resonant frequency.

Hollow inductors usually have a better quality factor than solid one. The reason is that the innermost turns of an inductor do not provide much of the inductance while they suffer from serious resistance loss owing to the eddy current on the substrate. Therefore, it is prudent to use a hollow inductor though the area is a bit larger. To improve the magnetic coupling between each segment of an inductor, the spacing between metal segment (sp) of an inductor is often kept to be

minimum.

Besides, there are still two parameters, the radius (r) and the number of turns (n) need to be considered in the design of an inductor. In optimizing an inductor, the metal width (w) is limited to within 20 μm as this value is already much larger than the skin depth of the metal at the frequency of interest.

Two-layer inductors are used in an attempt to minimize the area and to improve the inductor quality factor. The two metal layers are connected together through the via contacts. Due to the magnetic coupling between the upper and the lower layer of a two-layer inductor, the inductance will be larger than the sum of the two independent single-layer inductance. As the inductor is implemented in series in the vertical direction, the size of a two-layer inductor will be smaller than a single-layer inductor with the same inductance and similar Q. In addition, the substrate losses is reduced when the size of the inductor is shrink. Nonetheless, the series losses of the metal 2 (70 mΩ) is much larger than that of the metal 3 (50 mΩ) and this would hurt the overall quality factor. Fortunately, thanks to the coupling of the inductor, metal resistive losses is not very serious as the physical inductor is smaller. Another drawback of two-layer inductors is that the capacitance between the inductor and the substrate is larger owing to a reduction in the separation between the inductor and the substrate. A comparison of the performance of two single-layer inductors and one two-layer inductor simulated with Asitic is summarized in Table 7.1.

Parameters	**Single-layer (fixed area)**	**Single-layer (fixed metal width)**	**Two-layer**
Inductance (nH)	4.293	4.288	4.249
Capacitance (pF)	0.133	0.233	0.26

Table 7.1 Comparison between single-layer and two-layer inductors

Parameters	Single-layer (fixed area)	Single-layer (fixed metal width)	Two-layer
Radius (μm)	105	150	105
Inner hole size (μmxμm)	30x25	60x50	105x100
Metal Width (μm)	11	18	18
Spacing (μm)	1.2	1.2	1.2
Resistive losses (Ω)	10.406	7.3	6.8
Q	3.3	2.3	3.6

Table 7.1 Comparison between single-layer and two-layer inductors

Two single-layer inductors with different design constraints are generated so that comparisons can be made with the two-layer design. The radius of the first and the metal width of the second single-layer inductors are kept to be the same as the two-layer inductor. As illustrated in Table 7.1, so as to generate an 4.3 nH inductor with a radius constraint of 105 μm, the maximum metal width is 11 μm and the Q at 950 MHz is 2.3, which is much lower than the two-layer inductor in the third column. On the other hand, if the metal width is fixed to be 18 μm, the radius of the inductor needs to be around 150 μm in order to provide a similar Q as the two-layer inductor. As a result, the area of the inductor is two times as the two-layer design. Therefore, two-layer inductors have been employed in the circuit.

The two-layer output inductor is depicted in Fig. 7.1. All inductors are surrounded by guard rings to minimize the interaction between the inductors and other circuits. A broken n-well guard ring is placed in between two ground substrate guard rings to provide maximum isolation between the inductors and the other circuits.

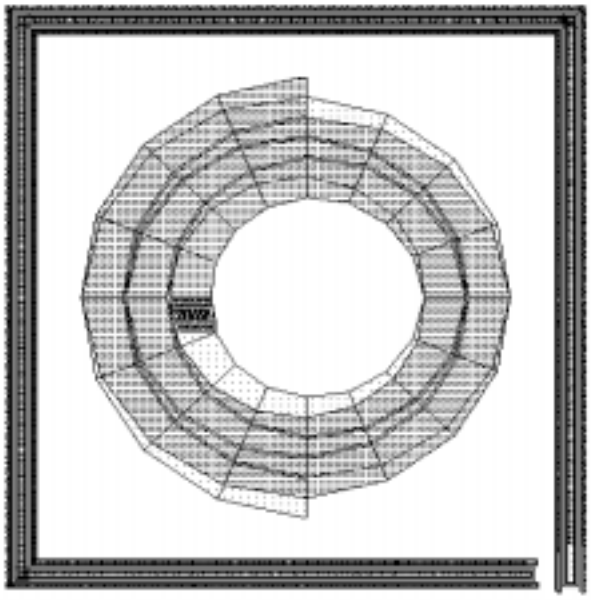


Fig. 7.1 A two-layer output inductor

7.3 Capacitor

Two different capacitors have been utilized in the design, namely the metal-to-metal capacitor and the linear capacitor. Metal-to-metal capacitor is used as the Miller capacitor in the frequency tuning circuit as the accuracy should be more accurate than the linear capacitor which is formed by the poly layer and the n-well. On the other hand, ac-coupling capacitors are formed by the linear capacitor as it is much smaller in size than the metal-to-metal capacitor. A summary of the capacitance per unit area for these two types of capacitor are tabulated in Table 7.2.

Parameters	Metal-to-metal capacitor	Linear capacitor
Capacitor value per unit area ($fF/\mu m^2$)	0.123	2.274
Parasitic capacitance associated ($fF/\mu m^2$)	0.086	--

Table 7.2: The capacitance per unit area for two types of capacitor

7.3.1 Metal-to-Metal Capacitor

Metal-to-metal capacitors are formed by the parallel plate capacitance between metal layers. A metal-to-metal capacitor is illustrated in Fig. 7.2. The capacitance of the structure in Fig.

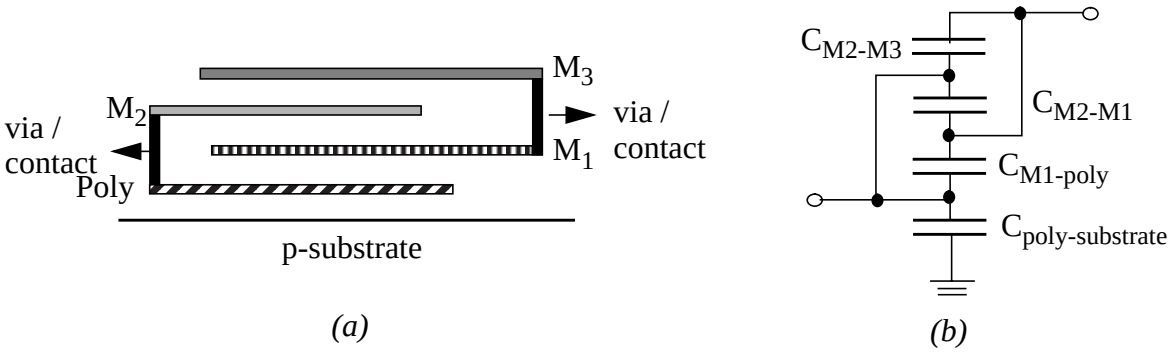


Fig. 7.2 (a). The structure and (b) the schematic of a metal-to-metal capacitor

7.2 is formed by three dielectric capacitor in parallel, $C_{M3\text{-}M2}$, $C_{M2\text{-}M1}$ and $C_{M1\text{-}poly}$,

$$C_{total} = C_{poly-M1} + C_{M1-M2} + C_{M2-M3}, \tag{7.8}$$

where $C_{M3\text{-}M2}$, $C_{M2\text{-}M1}$, $C_{M1\text{-}poly}$ are the parallel plate capacitance between Metal3 and Metal2, Metal 2 and Metal 1, and Metal 1 and poly layer respectively. $C_{poly\text{-}substrate}$ represents the parasitic capacitance between the poly layer and the substrate. The parasitic capacitance associated with the poly and the substrate affects the total capacitance of the circuit if it is not taken into consideration. The ratio of the total metal-to-metal capacitance (C_{total}) and the parasitic capacitance ($C_{poly\text{-}substrate}$) is around 0.7.

To reduce the parasitic capacitance effect, two unit capacitors are connected as shown in Fig. 7.3. In this way, the parasitic capacitance is only halved.

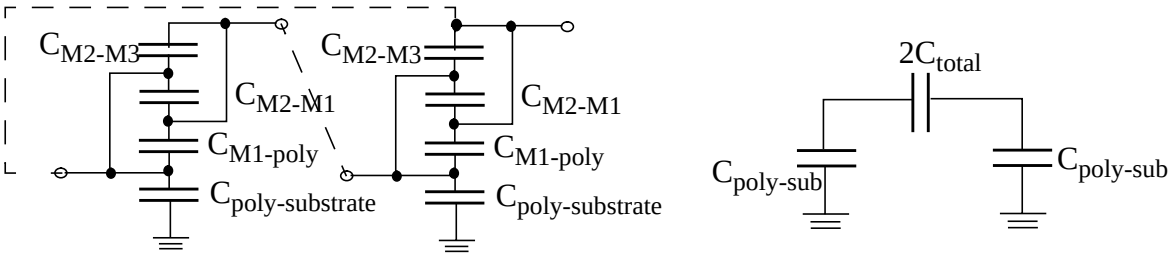


Fig. 7.3 The optimal connection of 2 identical metal-to-metal capacitors

7.3.2 Linear capacitor

A linear capacitor is a parallel plate capacitor between the poly layer and the substrate. The structure is illustrated in Fig. 7.4. Parasitic capacitor also exists in a linear capacitor but is not

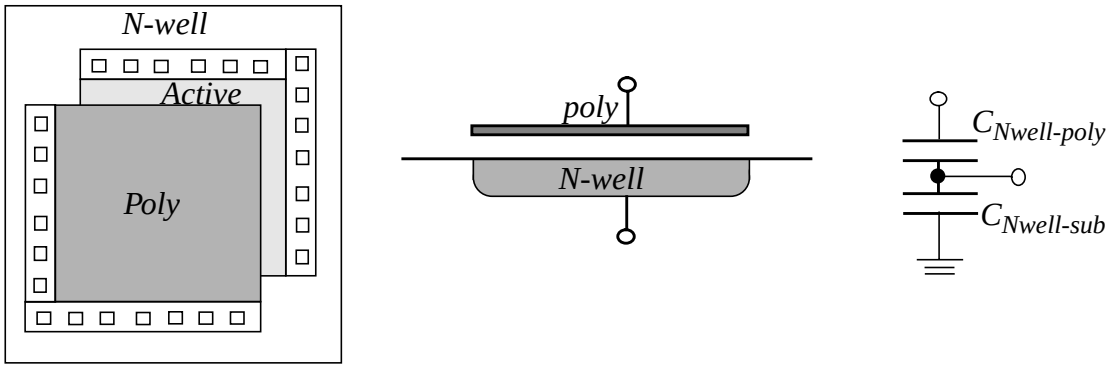


Fig. 7.4 The structure of a linear capacitor

very well modeled as the process parameters are not provided by the vendor.

7.4 Transistor Layout

The layout of a transistor has important influence on the overall performance of the design including symmetry and noise issues, especially for low noise circuit design. As stated earlier, the

major drawback of the modern sub-micron CMOS technology is the heavily-doped silicon substrate. It not only degrades the quality factor of an inductor, but affects the total noise figure of low-noise circuits as well. Thermal noise from the substrate resistance degrades the noise figure through the body transconductance g_{mb} [25]. The transistor is placed in parallel to reduce the parasitic capacitance and the gate resistance, whose noise is added to the total noise figure. To mitigate the substrate noise coupling, the transistors are surrounded by many substrate contacts.

Symmetry needs to be carefully planned if differential topology is employed in the design. Inter-digitized and common-centroid are some method that can achieve symmetry in differential architecture.

7.5 Pad Layout

Even though a pad looks really simple, it influences the measured noise figure a lot if the pad is not laid out properly. The substrate resistance on the heavily doped CMOS substrate is the major sources of noise that can couple to the pad if the substrate is not isolated from the pad. Consider a 70 μm x 70 μm pad on Metal-3 layer, the spreading resistance

$$R = \frac{\rho l}{A}, \tag{7.9}$$

in an 8–μm thick epi layer is equal to 80 Ω. The noise generated from this spreading resistance is at the input of the circuit and cannot be reduced by the gain of the circuit. The noise figure can be offset by as much as 3 dB easily if the spreading resistance is neglected when laying out the pad. The modified pad is given in Fig. 7.5 [27]. The p-diffusion and Metal 1 are connected to ground so that the pad is isolated from the substrate. Now, only capacitance is present between the pad

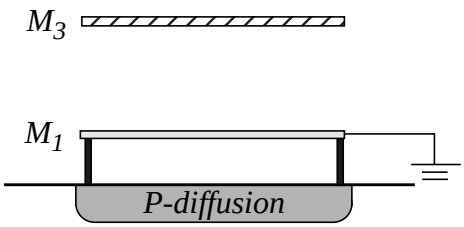


Fig. 7.5 The pad structure for minimum noise

and the substrate. The major disadvantage of inserting metal-1 in between the pad layer and the substrate is that the capacitance of is much larger (from 50 fF to 60 fF), yet, the noise figure would be better.

7.6 Layout of the actual circuits

7.6.1 Layout of the bandpass amplifier

For differential circuit, the layout of the circuit needs to be symmetrical so that the design is balanced. Since the inductors are the largest elements in the design, they governs the placement of the circuit. The floor plan and the layout of the bandpass amplifier is depicted in Fig. 7.6.

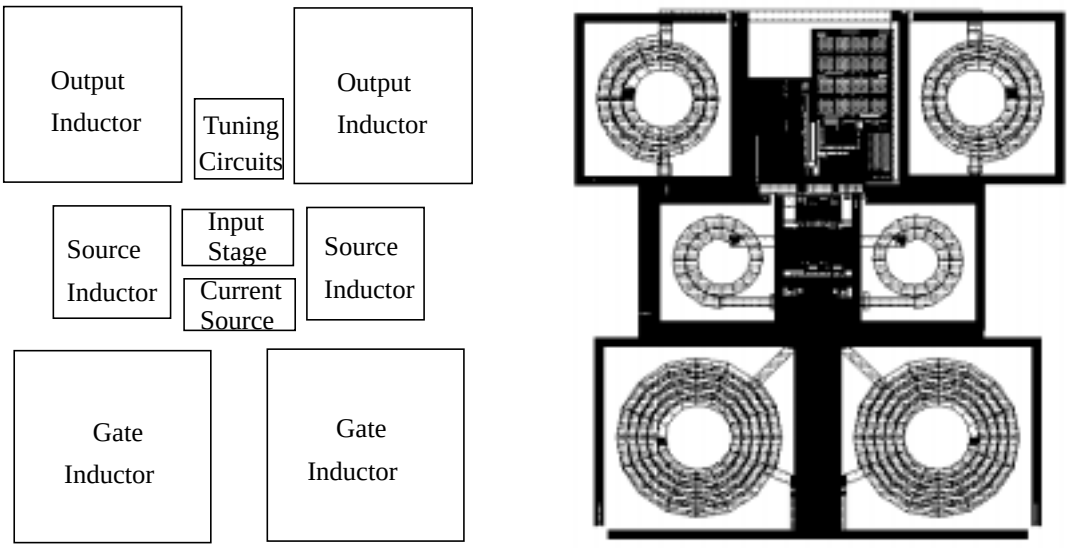


Fig. 7.6 The floorplan of the bandpass amplifier

7.6.2 Layout of the bandpass filter

In the second prototype, two bandpass filter are cascaded with the bandpass amplifier to improve the image rejection ability. Because there are merely two output inductors in the bandpass filter design, the flexibility of the placement of the circuits is increased. The floor plan and the layout of the bandpass filter are shown in Fig. 7.7 and Fig. 7.8.

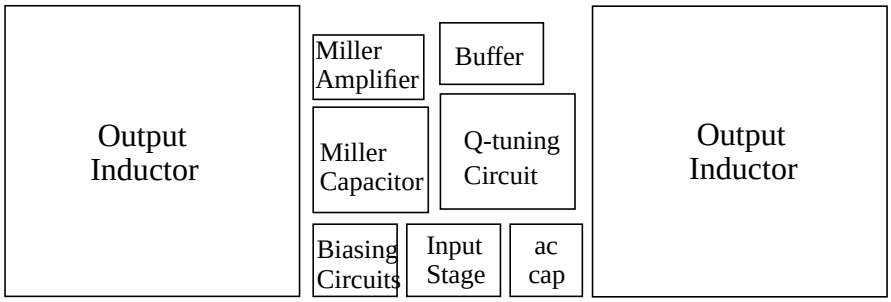


Fig. 7.7 The floorplan of the bandpass filter

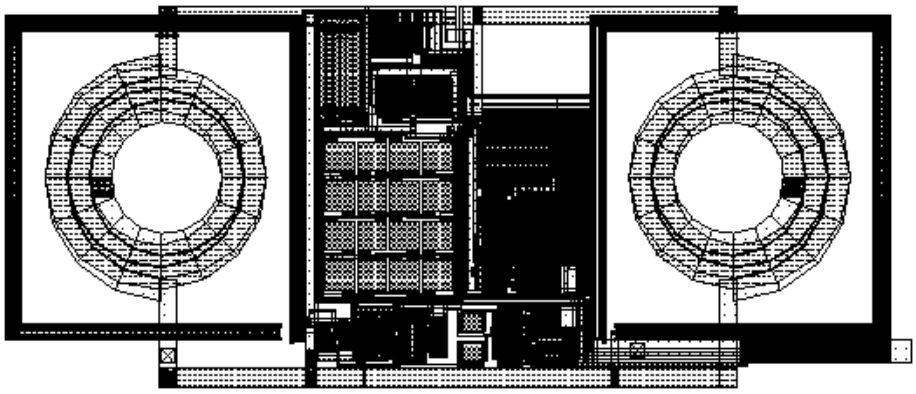
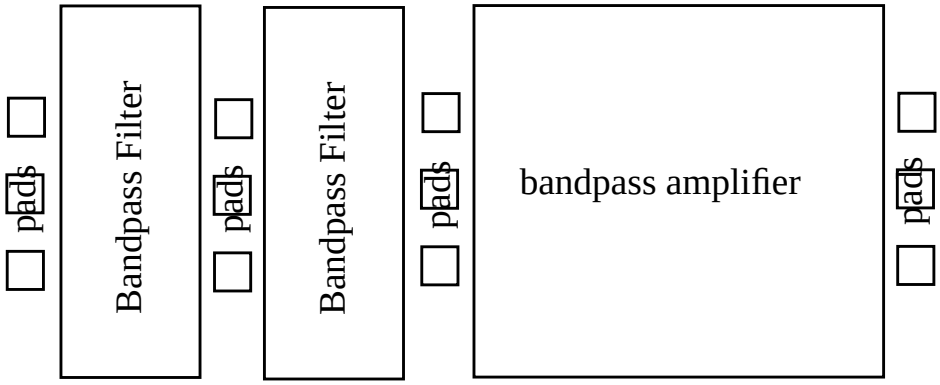


Fig. 7.8 The layout of the bandpass filter

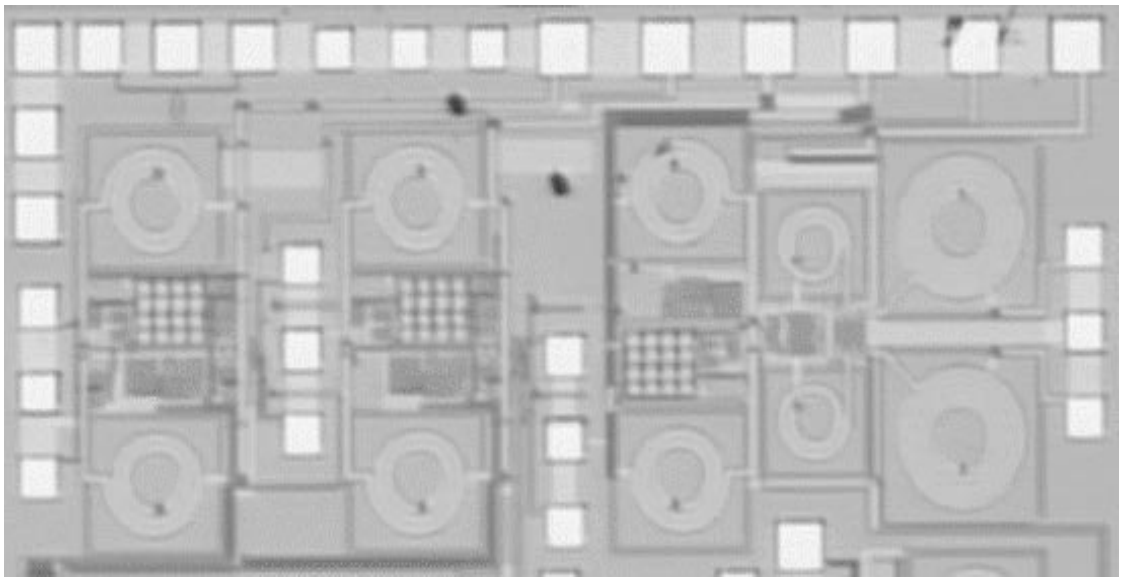
7.6.3 Complete Layout of the design

Internal high-speed probing pads are inserted in each stage so that the characteristic of the bandpass amplifier and the filter can be evaluated individually. The complete floor plan and the

layout of the circuit is given in Fig. 7.9.



(a)



(b)

Fig. 7.9 (a). Floor plan, and (b). Die-photo of the whole amplifier

Chapter 8

Measurement Results

8.1 Introduction

In this chapter, the measurement results of the first and the second prototypes will be presented including

(i). Input matching,

(ii). Frequency response and Gain of the amplifier,

(iii). Q-tuning ability,

(iv). Frequency tuning ability,

(v). Input 1-dB compression point,

(vi). Input third-order intermodulation intercept (IIP_3),

(vii). Noise Figure,

(viii). Image Rejection.

8.2 Bandpass Amplifier (First prototype)

This prototype was fabricated in 0.8 μm single-poly, triple-metal CMOS technology provided through MOSIS®.

8.2.1 Frequency Response Test Setup

The measurement setup shown in Fig. 8.1 is used to evaluate circuit parameters including center frequency, maximum gain, Q-tuning and frequency-tuning abilities and image rejection.

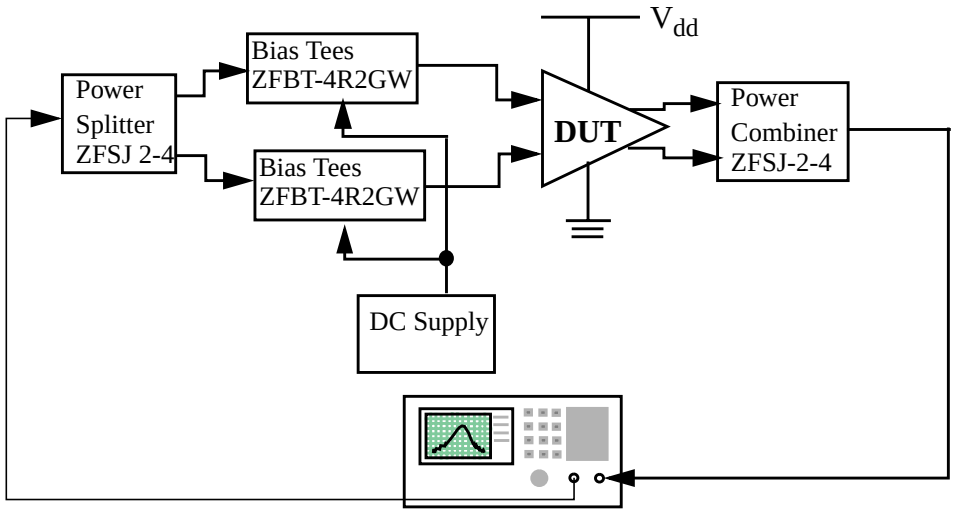


Fig. 8.1 The test setup for high-frequency measurement

To identify the center frequency of the circuit, a wideband signal from Port-1 of the network analyzer HP8510C is first splitted by a 2-way 180^{o} power splitter (ZFSJ-2-4). Then, it is superimposed with the common-mode dc bias through the bias-tees (ZFBT-4R2GW). A signal-ground-signal (SGGS) dual pico-probe (40A-GS-150-DUAL) from GCB passes the differential signals to the input of the circuit. At the same time, the output signal is picked up by a SG-GS dual probe and combined by another 2-way 180^{o} power combiner before returning back to Port-2

of the network analyzer.

8.2.1.1 Center frequency, Gain and Image Rejection

To prevent the amplifier gain from being compressed, the test power of the network analyzer is set to be -50dBm. Using the test setup in Fig. 8.1, the power gain of (S_{21}) of the amplifier is measured and plotted in Fig. 8.2. The quality factor of the circuit is adjusted to

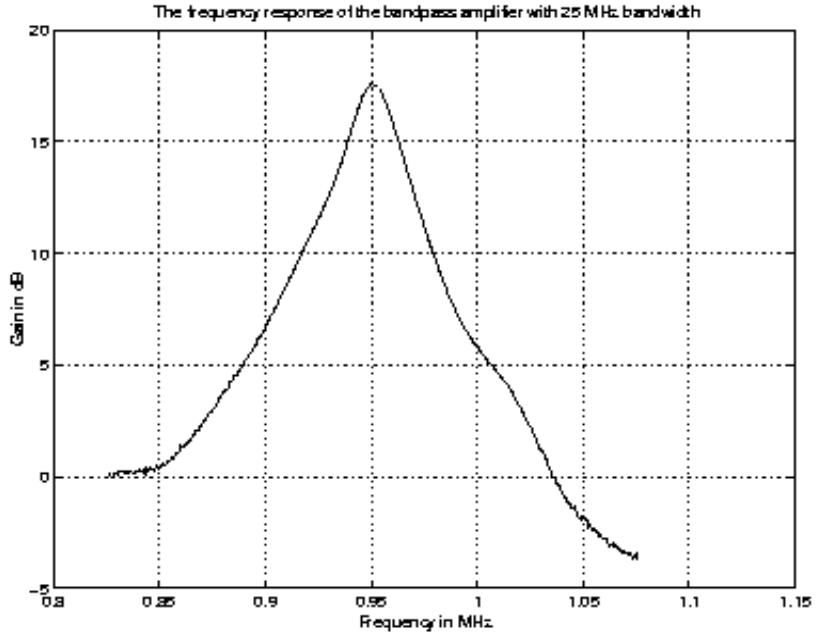


Fig. 8.2 The measured frequency response of the amplifier

provide a 25-MHz 3-dB bandwidth (ω_{-3dB}). The center frequency of the amplifier is located at 950 MHz and the maximum gain at the output of the buffer is 18 dB.

With an intermediate frequency (IF) at 70 MHz, the signal attenuation at 140 MHz away from the desired frequency is 18 dB as shown in Fig. 8.2.

8.2.1.2 Tuning ability

As presented in Chapter 3, the circuit's quality factor and the center frequency can be

varied by the corresponding tuning circuits. To demonstrate the features, the frequency responses of the amplifier under different Q-tuning voltage are plotted in Fig. 8.3. The Q can be tuned between 2 and infinity. Meanwhile, the center frequency can be varied between 930 to 1040 MHz.

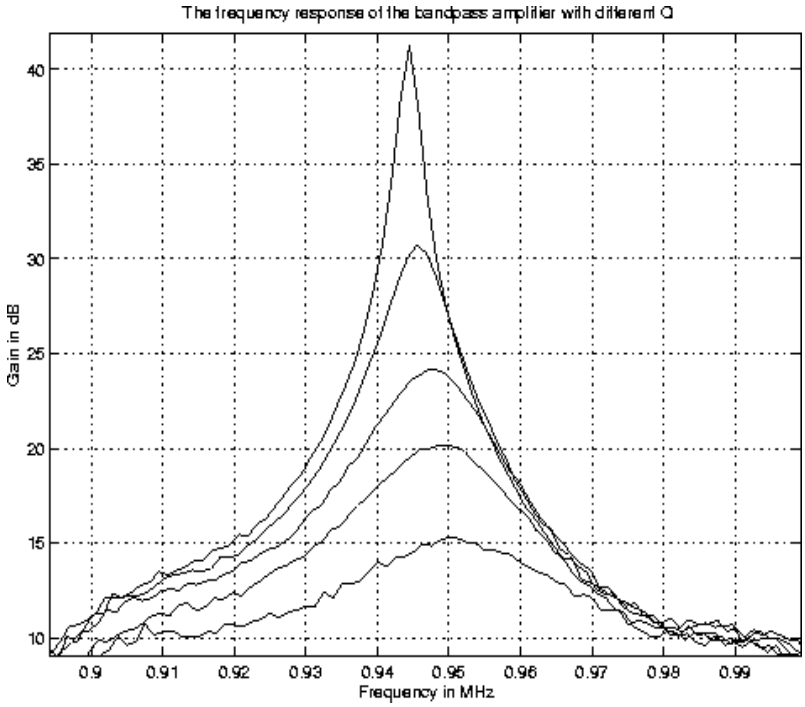


Fig. 8.3 The measured frequency response of the circuit under different Q

8.2.2 Input Matching

On the grounds that no differential calibration kit is available, only single-ended input matching is measured by the setup shown in Fig. 8.4. The setup is first calibrated with the substrate CS-5 for GSG pico-probes (40A-SG-150) to ensure that the measured parameters are accurate and valid.

The measured input reflection coefficient S_{11} is shown in Fig. 8.5. The S_{11} minimum appears at 1.13 GHz while the designed should occur at 950 MHz. Nonetheless, the measured S_{11} at 950 MHz is -13.2 dB, which can still be considered as good input matching.

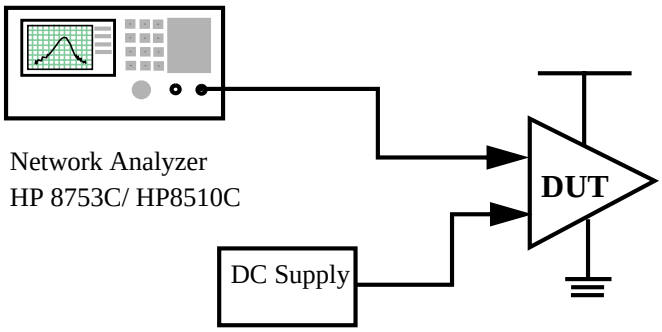


Fig. 8.4 The measurement setup for the input matching

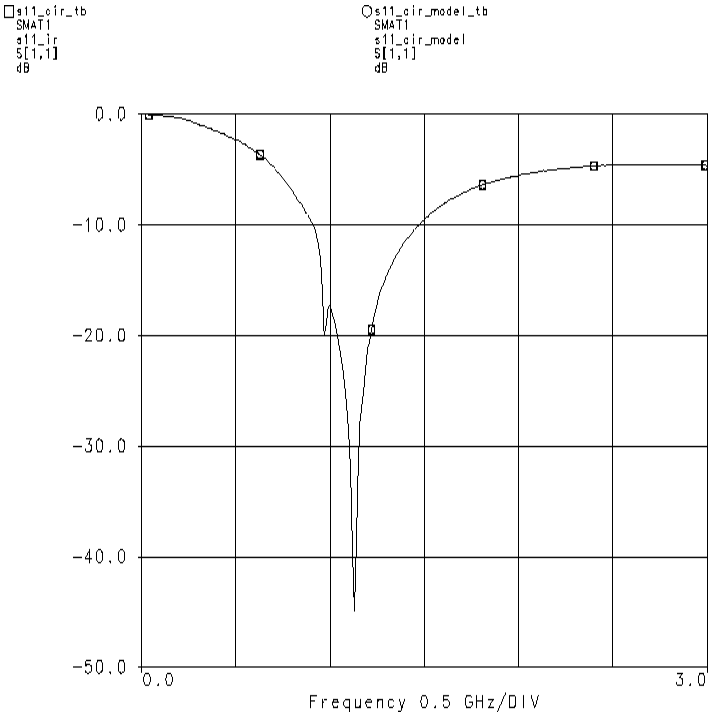


Fig. 8.5 The measured input S_{11} (log magnitude)

8.2.3 Linearity Measurement

The linearity is measured by a two-tone test and its basic principle of the two tone test is already discussed in Chapter 2. The setup is illustrated in Fig. 8.6. Two closely spaced signals (f_o-1.6 MHz, f_o-0.8 MHz) with equal amplitude are first combined by a 2-way 0^o power combiner

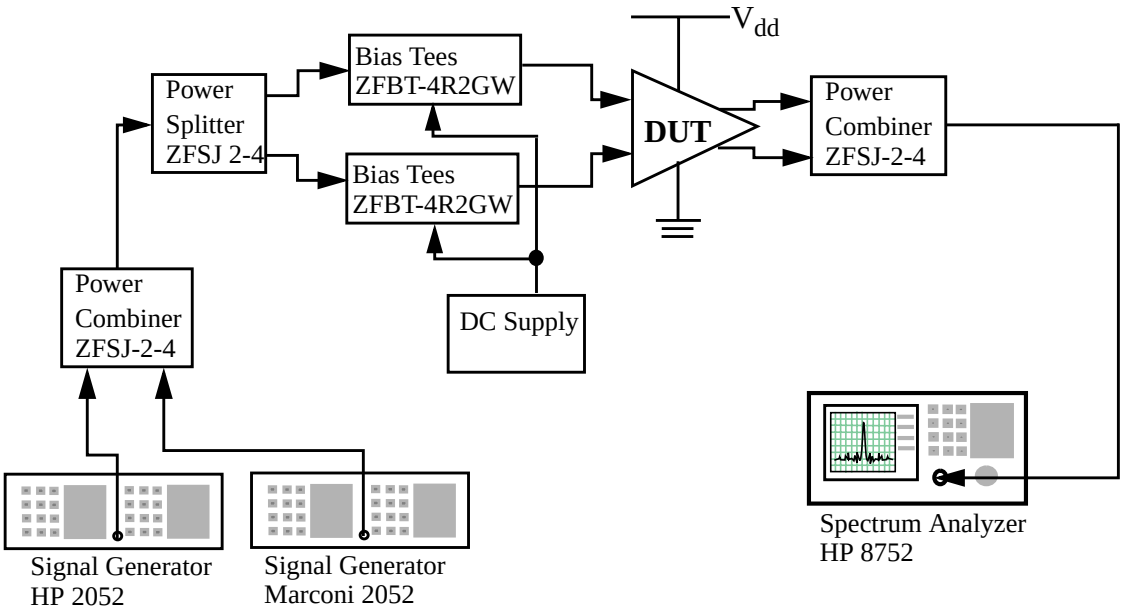


Fig. 8.6 Two-tone test setup

before being splitted by the power splitter. Then, the signals are fed into the circuit and the output response at the fundamental frequencies (f_o-1.6 MHz, f_o-0.8 MHz) and the third-order intermodulation frequency (f_o) are measured from the spectrum analyzer. The two-tones with different signal amplitude are applied, both fundamental ($P_{o,fund}$) and intermodulation product output power ($P_{o,\ IM}$) are obtained. The signal amplitude of the two-tone is increased until the gain of the amplifier is compressed by 1-dB. Both $P_{o,fund}$ and $P_{o,IM}$ versus the input power (P_{in}) are plotted in Fig. 8.7. The measured results are extrapolated to obtain the input third-order intermodulation product (IIP_3). The measured IIP_3 and the $P_{o\text{-}1dB}$ are -21.5 and -31.5 dBm respectively.

8.2.4 Noise Figure Measurement

Techniques and testing procedures related to the noise figure measurement have already been addressed in Chapter 4. The noise figure of all the components in the setup shown in Fig. 4.9

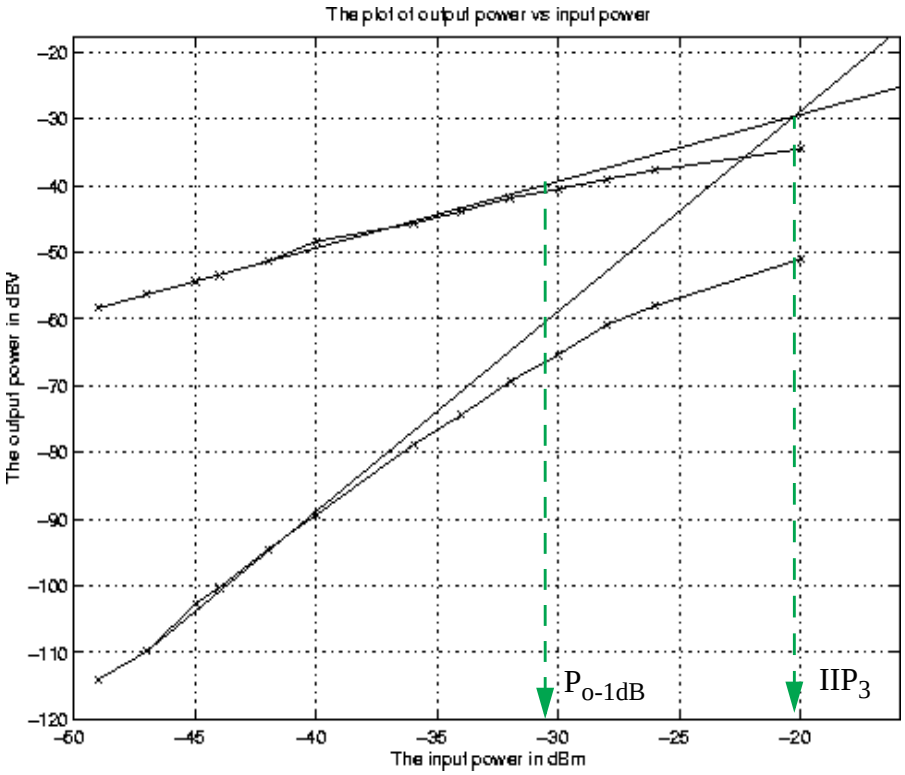


Fig. 8.7 Measured result of the two-tone test

are measured in advance so that their noise contribution can be eliminated during the noise figure calculation. The measured noise figure of the bandpass amplifier is 10 dB, which is much larger when compared to the simulated value of 6 dB. The high noise figure is partly due to an improper layout of the pads and the input stage such that the substrate noise can couple to the input of the circuits. In addition, inadequate modeling of short-channel MOSFET channel noise in the circuit causes the discrepancy.

To sum up, the measured and the simulated results of the first prototype are tabulated in Table 8.1.

Parameters	**Specifications**	**Simulation**	**Measurement**
Supply Voltage	3V	3V	3V

Table 8.1 The comparison between simulation and measurement results

Parameters	Specifications	Simulation	Measurement
Center frequency	~950 MHz	947 MHz	950 MHz
Gain	~20 dB	28 dB	25-26 dB
S_{11} @ 950 MHz	< 0 dB	-50 dB	-13.2 dB
Q	38	38	38
Noise Figure	N. A	5-6 dB	10 dB
Frequency tuning range	N. A	930-1050 MHz	930-1040 MHz
IIP_3	> -18 dBm	-21 dBm	-21.5 dBm
$P_{o\text{-}1dB}$	N. A	-31 dBm	-31.5 dBm
M. D. S	-102 dBm	--	-100 dBm
Image Rejection @140 MHz away	20-40 dB	20 dB	20 dB
Power dissipation (current)	N. A	20 mA	24 mA

Table 8.1 The comparison between simulation and measurement results

8.3 Bandpass Amplifier (Second Prototype)

To improve the performance of the amplifier in terms of power, noise performance, linearity and image rejection, the circuit was modified with a lower power supply (2-V) fabricated in 0.5 μm CMOS technology process. Two-layer inductors were also employed in the design in an attempt to reduce the die area of the bandpass amplifier and the bandpass filters in the design. The measurement results of the second prototype and testing structures are addressed now.

8.3.1 Inductor Measurement

A two-layer output inductor had been fabricated on the same die to investigate its performance in terms of inductance value, Q and self-resonant frequency. The inductor is measured using GSG pico-probe (40A-GSG-150), that had been calibrated in advance utilizing

CS-1 calibration substrate. To eliminate the open probing-pad capacitance, its one-port s-parameter is measured and substrate from the s-parameter of the inductor. S_{11} is related to the input impedance Z_{in} in a 1-port network as

$$S_{11} = \frac{V_i^-}{V_i^+} = \frac{Z_{in} - Z_o}{Z_{in} + Z_o}, \tag{10.1}$$

where Z_o is the characteristic impedance which is equal to 50-Ω in this case. From Z_{in}, the quality factor and the inductance value can be obtained.

The one-port measurement result of the inductor is given in Fig. 8.8. The inductor's model

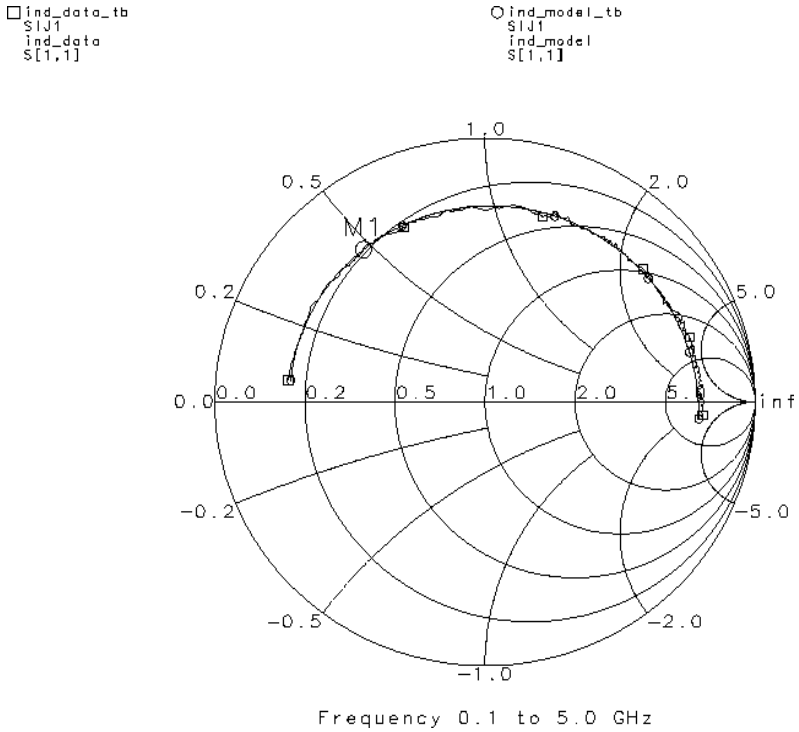


Fig. 8.8 The measured S_{11} of the two-layer output inductor

is repeated in Fig. 8.9 for reference. Compared the simulated result obtained from the Asitic

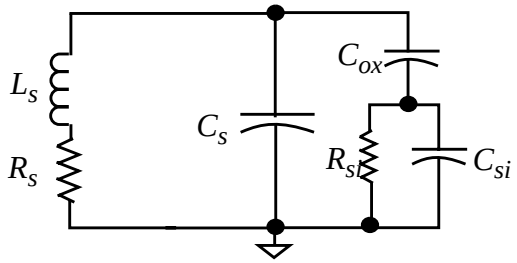


Fig. 8.9 The extracted model from the two-layer output inductor

program with the measured inductor parameters shown in Table 8.2, the measured inductance measured is around 10% larger than expected while the series resistance of the inductor is also increased from 7 Ω to 8.3 Ω. Besides, the parasitic capacitance C_{ox} between the inductor and the substrate is much larger in the measurement.

Parameters	Simulated Value	Measured Value
L_s	4.3 nH	4.7 nH
R_s	7 Ω	8.3 Ω
C_{ox}	0.26 pF	0.8 pF
R_{si}	22.3 Ω	250 Ω
Q	3.6	2.7

Table 8.2: A comparison of the parameters of the two-layer inductor obtained from simulation and measurement

8.3.2 Frequency Response of the bandpass amplifier

The measured frequency response of the bandpass amplifier is depicted in Fig. 8.10. The gain has a maximum of 12.3 dB at 832 MHz. Meanwhile, the image rejection of the amplifier is around 20 dB at frequency 140 MHz away from the desired signal. The measured maximum center frequency of the bandpass amplifier (832 MHz) is much lower than the designed value,

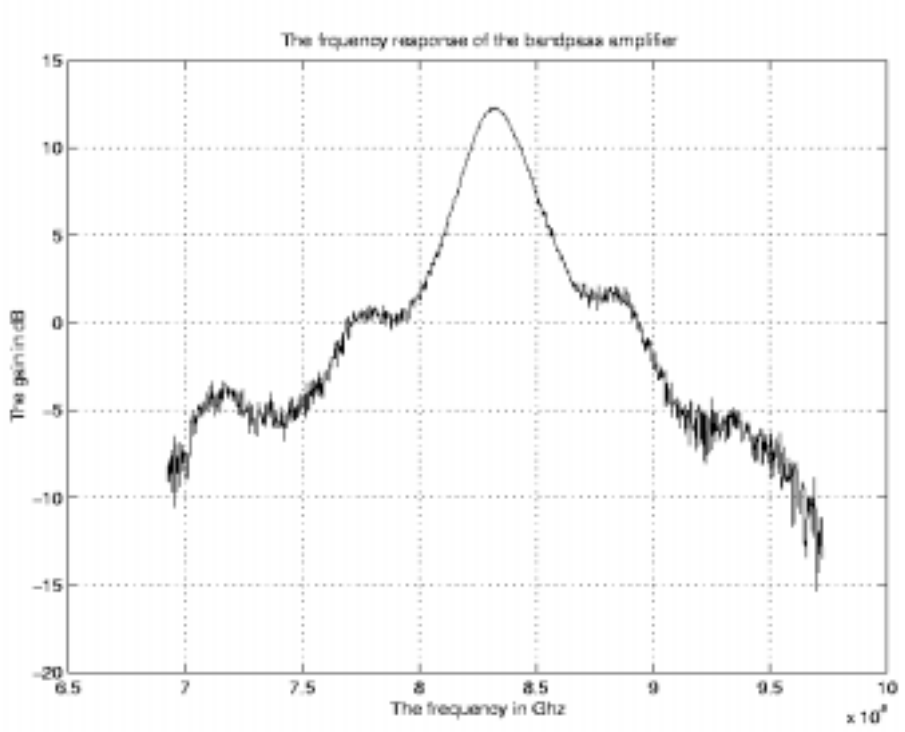


Fig. 8.10 The measured frequency response of the bandpass amplifier

which is around 960 MHz. This frequency deviation is due to the inaccurate modeling of the inductance and the parasitic capacitance in the design.

The designed and measured inductance and capacitance in the amplifier output resonant circuit are given in Table 8.3. As stated in Section 8.3.1, the measured inductance and the

Parameters	Designed	Measured	Percentage Increment
Inductance	**4.3 nH**	**4.7 nH**	**9%**
Capacitance (total)	**5.3 pF**	**5.93 pF**	**11%**
Parasitic capacitance (inductor)	0.26 pF	0.8 pF	220%
Miller capacitor	0.7 pF	0.8 pF	10%

Table 8.3: the designed and measured inductance and capacitance value

capacitance of the output inductor is larger than expected, it causes part of the frequency deviation

in the design. Furthermore, the power supply line connection causes mismatches in the output inductor layout and it is modeled as the extra inductance and losses as depicted in Fig. 8.11. Including the extra capacitance and inductance in the design, the circuit is re-simulated and the

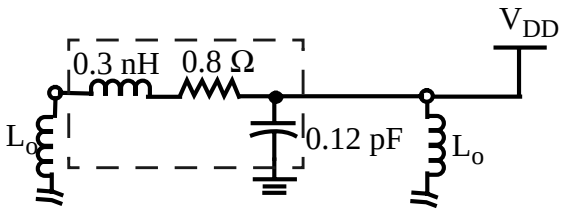


Fig. 8.11 The measured frequency response of the bandpass amplifier

result is illustrated in Fig. 8.12. The center frequency of the modified circuit is 840 MHz, which is

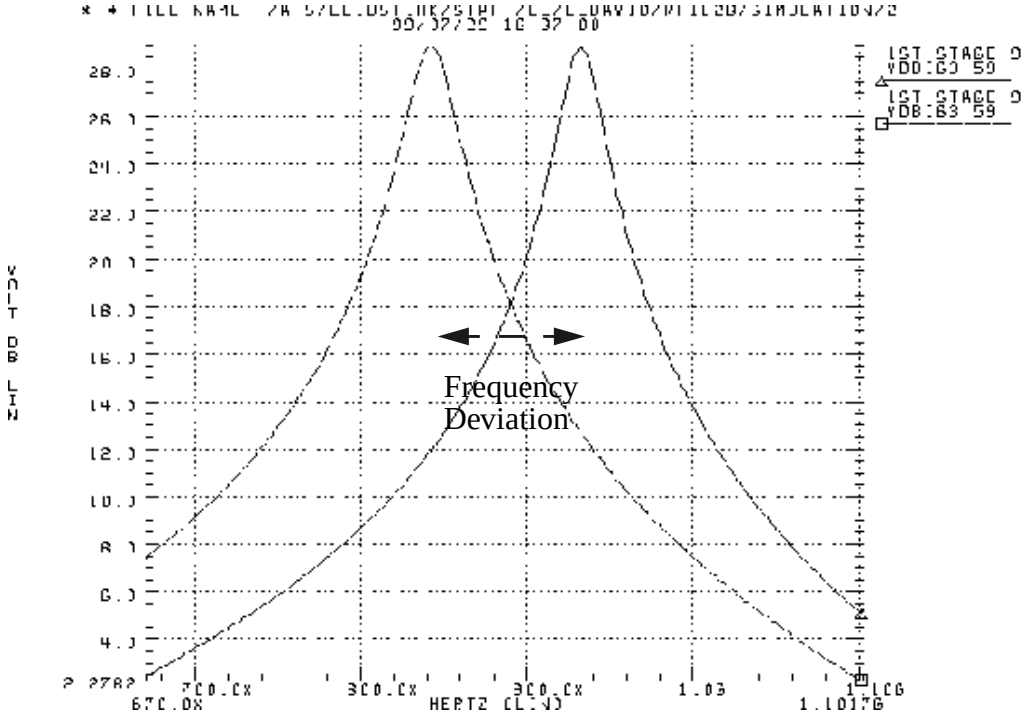


Fig. 8.12 The re-simulated frequency response of the bandpass amplifier

much closer to the measurement result.

8.3.2.1 Tuning range

The frequency response of the amplifier under different Q-tuning voltage are depicted in

Fig. 8.13.

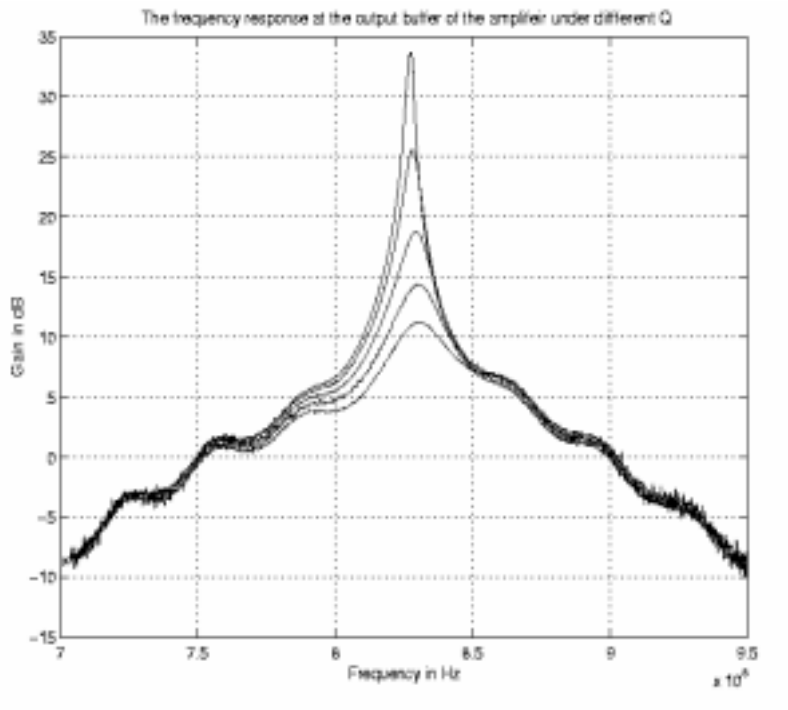


Fig. 8.13 The measured frequency response of the bandpass amplifier with different 3-dB bandwidth

With a frequency tuning voltage varied from 0.86 V to 1.1 V, the frequency responses are plotted in Fig. 8.14. The frequency tuning range of the amplifier can be varied between 760 MHz and 832 MHz.

8.3.2.2 Input Matching

The measured input reflection coefficient S_{11} of the amplifier input matching is illustrated in Fig. 8.15. The minimum S_{11} is located at 950 MHz which is as designed, yet the magnitude (-14 dB) is much larger than the simulation result (- 45 dB). Actually, the measured real part of the input matching is around 60-Ω instead of 50-Ω as designed. As derived in Chapter 3, the input impedance as resonant should be equal to

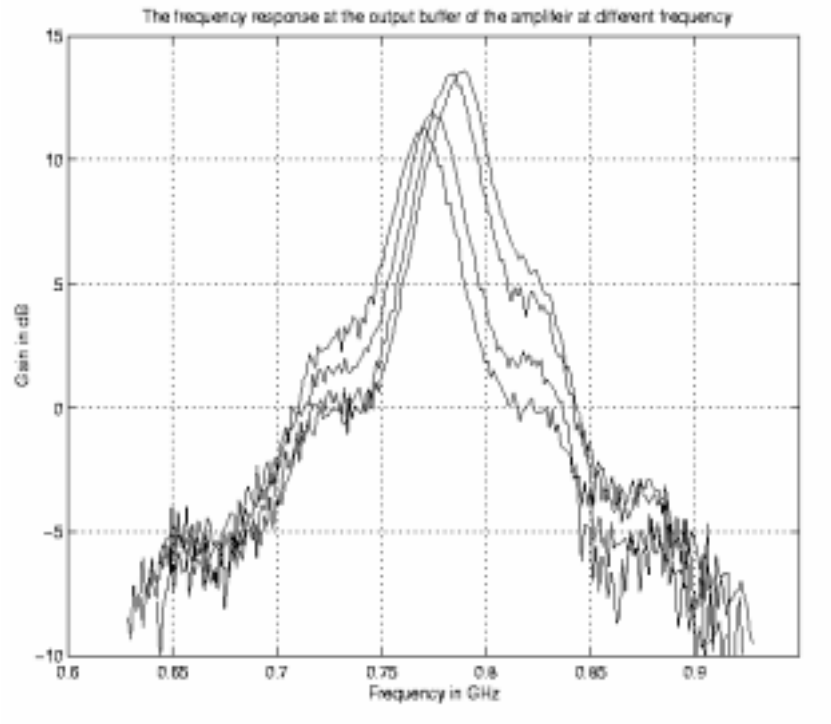


Fig. 8.14 The measured frequency response of the bandpass amplifier with different frequency tuning voltage

$$Z_{in}(\omega_o) = \omega_T L_s + R_g + R_l. \tag{10.2}$$

The 10-Ω mismatch between the simulation and the measurement is contributed from the increase in the inductor resistive losses. Besides, an increase in the source inductance L_s also increases the input impedance.

8.3.3 Noise Figure Measurement

As presented in Chapter 4, the noise figure measurement setup is calibrated in advance to eliminate out the noise contributed from the components in the setup. Then the gain and the noise figure of the amplifier are measured. Afterwards, the data are processed to get rid of the noise originated from the setup. The calibrated gain and the noise figure are 17.5 dB and 9.6 dB respectively as plotted in Fig. 8.16. The measured noise figure of the bandpass amplifier is much

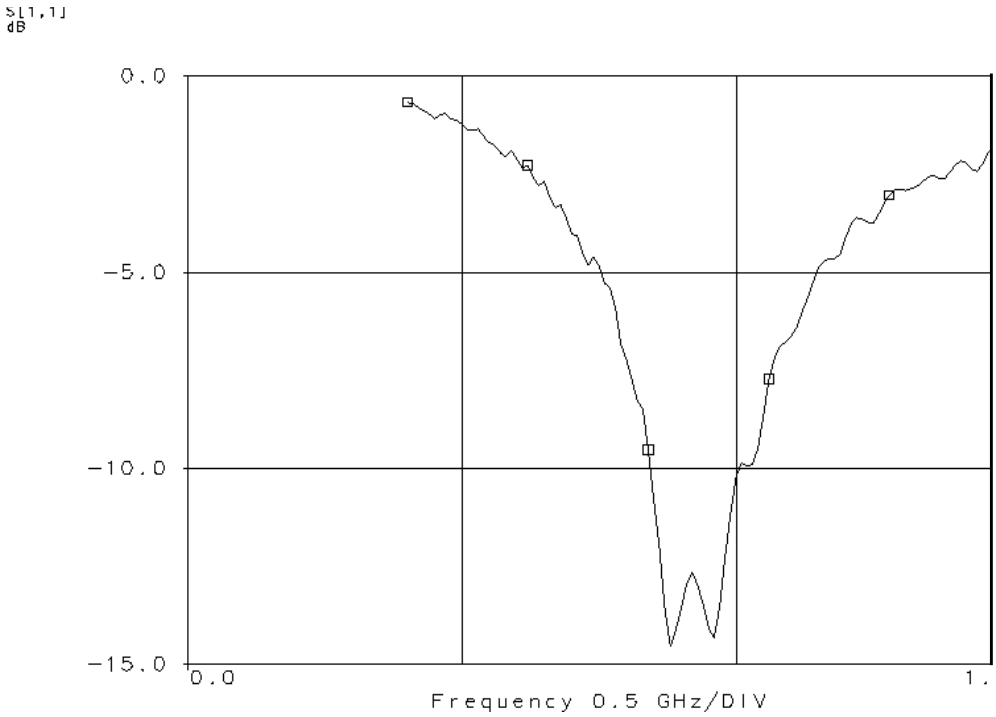


Fig. 8.15 The S_{11} plot of the amplifier input matching

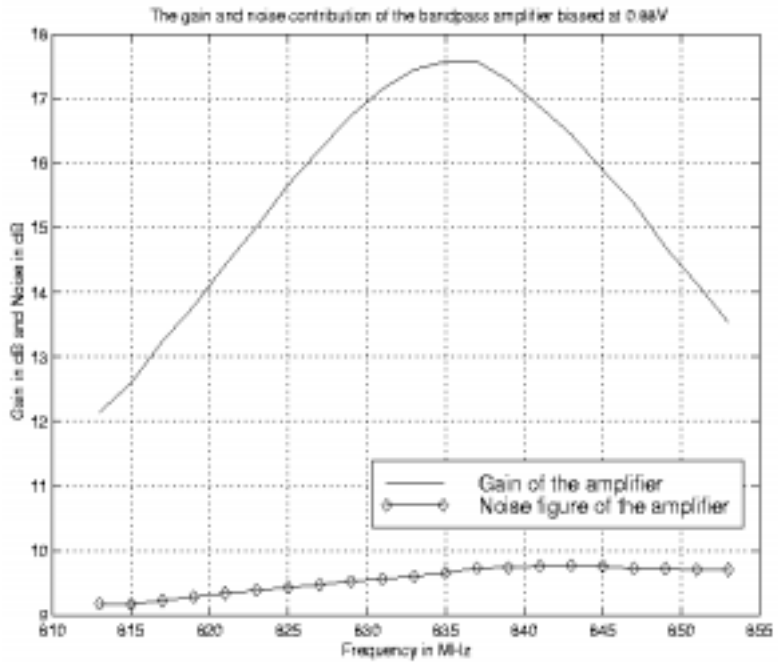


Fig. 8.16 The noise figure of the amplifier with BW = 25 MHz

higher than the simulated result (5.7 dB). The difference is contributed from two reasons.

Firstly, the measured input matching's resistive part is larger than the designed. It not only contributes more noise at the input, but also reduces the transconductance gain of the amplifier. The reduction degrades the ability of the amplifier in reducing the noise at the output of the amplifier and of the subsequent stages. As a result. a high noise figure is anticipated. To illustrate the effect, the noise figure of the amplifier under different current biases are shown in Fig. 8.17. As discussed in Chapter 4, the noise contribution from the output inductor and the tuning circuits

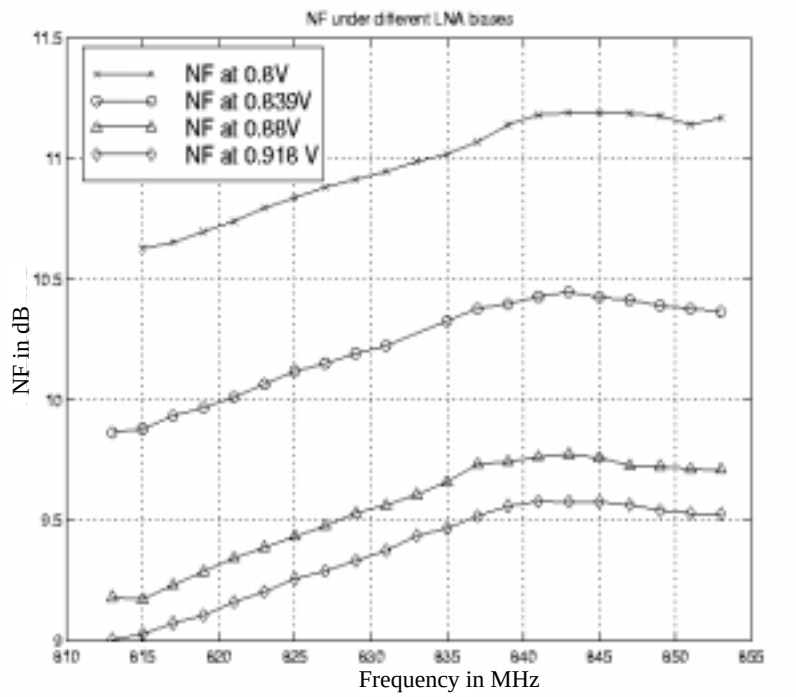


Fig. 8.17 The noise figure of the amplifier under different biases

can be reduced by increasing the transconductance gain (Gm) of the amplifier. Therefore, the total noise figure is reduced when the overall gain of the amplifier is increased.

Besides, the MOSFET noise model employed in both Hspice® simulation and calculation has only taken into consideration the noise of long-channel devices. The drain current noise of a MOSFET device is repeated below for reference,

$$\frac{\overline{I_d^{\,2}}}{\Delta f} = 4kT\gamma g_{do}. \tag{10.3}$$

The γ in long-channel devices is around 2/3, however, it is between 2 and 3 in short-channel devices. This difference in γ is quite significant if it is not properly considered during the simulation and the calculation. Since γ cannot be changed in the Hspice® simulation, the noise figure equation derived in Chapter 4, which has already been demonstrated that it is quite accurate in modeling the noise figure of amplifier, is utilized to illustrate the effect of γ.

In the first example, the measured noise figure of the low noise amplifier is compared with the simulation results obtained from the noise figure equation with γ = 2/3 and 2 as depicted in Fig. 8.18. The simulated noise figure with γ = 2/3 is only 5.3 dB, but with γ = 2, the noise figure is

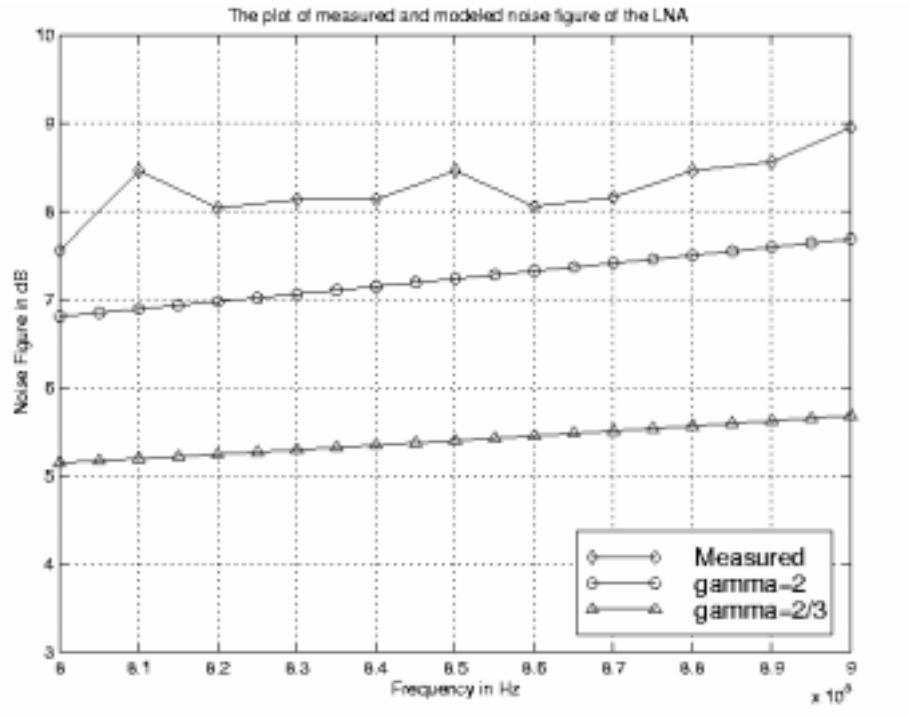


Fig. 8.18 A comparison of the measured and modeled noise figure of the low-noise amplifier

increased up to 7.1 dB. Clearly, the result using γ = 2 is much closer (within 1 dB) to the

measurement result. From the comparison, it shows that the value γ significantly affects the total noise figure of the amplifier.

To demonstrate the effect of γ in the noise figure of the bandpass amplifier, the comparison of the measured noise figure and the modeled noise figure with γ = 2/3 and 2 are shown in Fig. 8.19. The modeled noise figure with γ = 2/3 is 7.1 dB. For γ = 2, the noise figure is 8.7 dB and it is

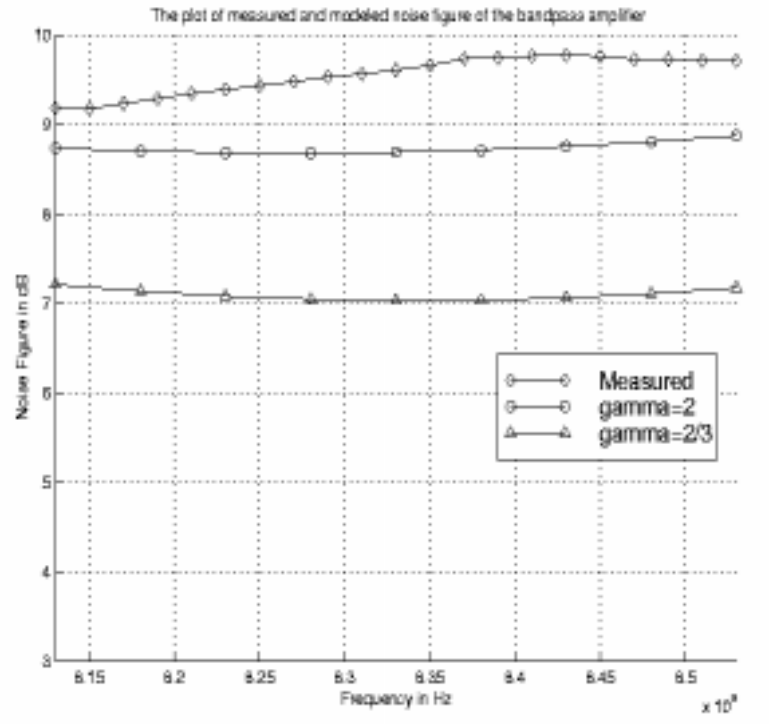


Fig. 8.19 A comparison of the measured and modeled noise figure of the bandpass amplifier

much closer to the measurement result.

8.3.4 Linearity

Two tones at 830 MHz and 831.8 MHz are applied at the input of the bandpass amplifier, which is adjusted for a 25-MHz 3-dB bandwidth, the fundamental power and the intermodulation product are measured as shown in Fig. 8.20 and the plot of the relationship between the input and output powers are depicted in Fig. 8.21. The IIP_3 and the $P_{o\text{-}1dB}$ are -18.5 dBm and -29 dBm

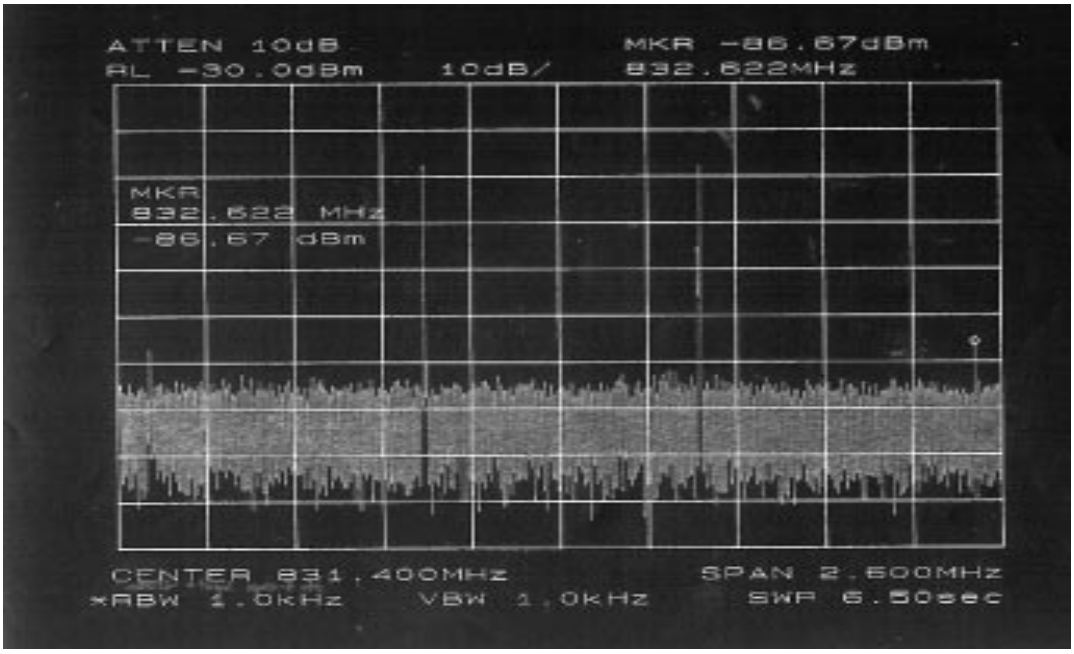


Fig. 8.20 Two tone test result

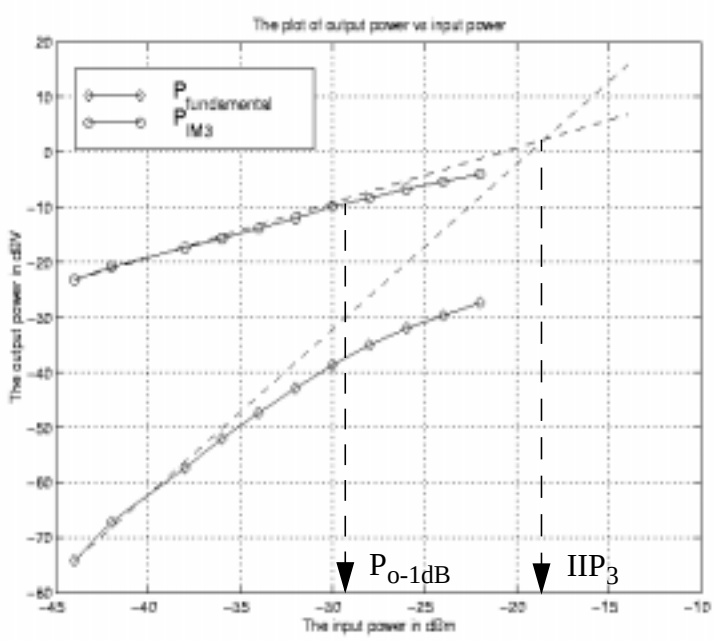


Fig. 8.21 The plot of $P_{o,fund}$ and $P_{o,\,IM}$ versus P_{in}

respectively.

8.4 Bandpass Filters

8.4.1 First bandpass filter

8.4.1.1 Frequency Response

The measured maximum center frequency of the first bandpass filter is 827 MHz and the corresponding gain is 0.5 dB with a 3-dB bandwidth of 25-MHz. The response is plotted in Fig. 8.22. The image rejection of the filter at 140 MHz away from the receiver band is 20 dB. The

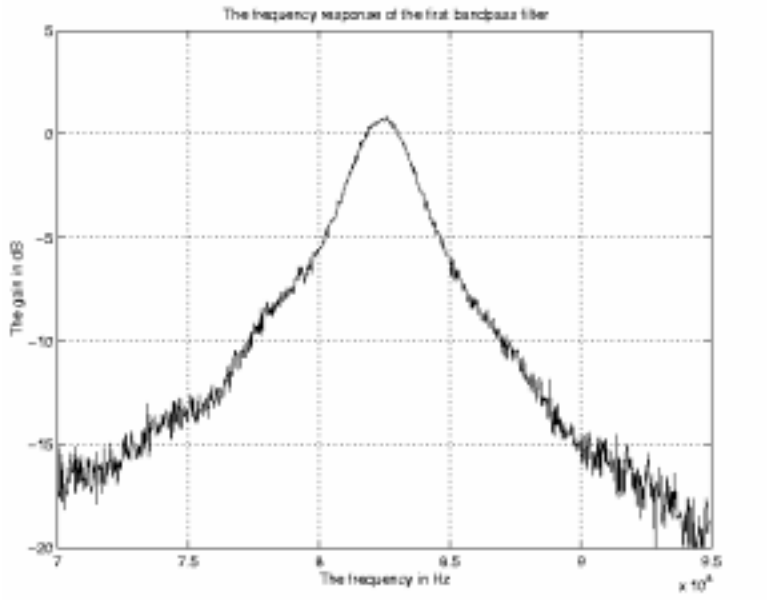


Fig. 8.22 The frequency response of the first bandpass filter (2nd-stage)

tuning range of the filter is the same as that of the bandpass amplifier in the second prototype.

8.4.1.2 Noise Performance of the first bandpass filter

The noise figure of the first bandpass filter is depicted in Fig. 8.23. At the center frequency 827 MHz, the noise figure is equal to 26 dB.

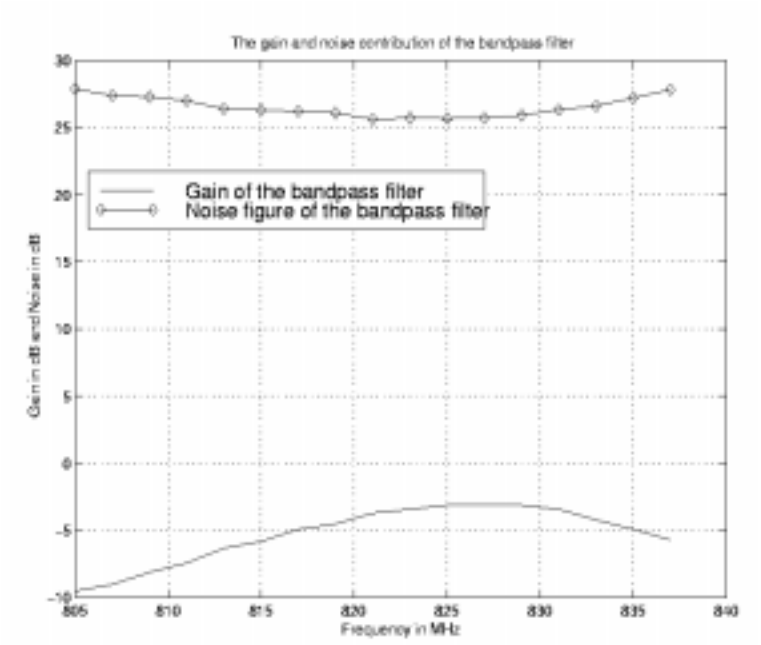


Fig. 8.23 Measured noise figure versus frequency of the first filter

8.4.2 Measurement Results of the second filter

The second bandpass filter is also measured and the response is shown in Fig. 8.24. The maximum center frequency of the second filter is 857 MHz and the corresponding gain at the output buffer is -1 dB.

8.4.2.1 Noise Measurement of the second filter

The noise figure of the second filter is given in Fig. 8.25. As shown in Fig. 8.25, the noise figure of the filter is 23 dB.

The performance of the two filters are summarized in Table 8.4. The center frequency of

Parameters	First filter	Second filter
Gain after the output buffer	0.5 dB	-1 dB
Center frequency	825 MHz	850 MHz

Table 8.4: The performance of the bandpass amplifier and the two filters

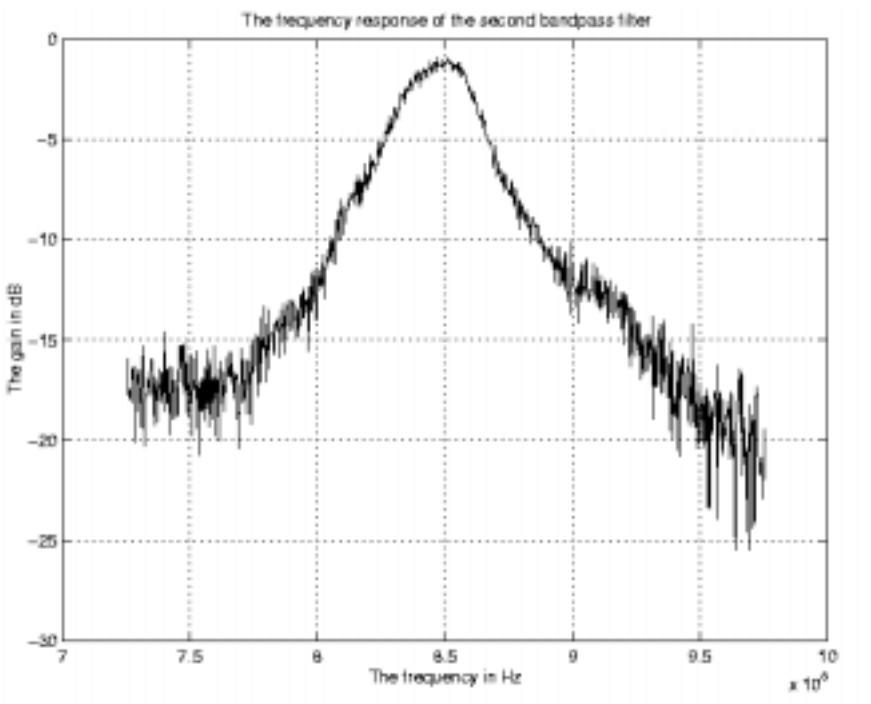


Fig. 8.24 The frequency response of the second bandpass filter (3rd-stage)

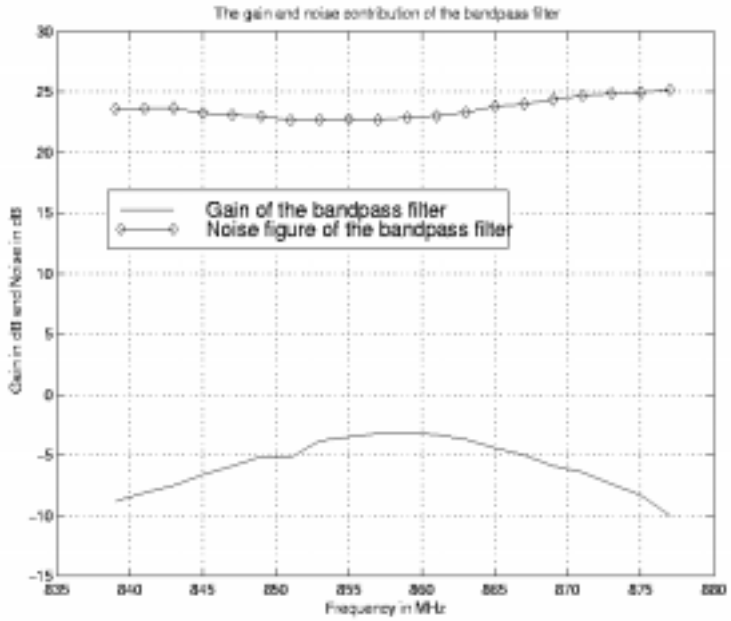


Fig. 8.25 Measured noise figure versus frequency of the second filter

Parameters	First filter	Second filter
Noise Figure w.r.t 50-Ω source resistor	26 dB	23 dB

Table 8.4: The performance of the bandpass amplifier and the two filters

the first filter is lower because the output of the first filter is also connected to an ac-coupling capacitor and an output buffer while the second filter is only connected to an output buffer. The extra capacitance at the output of the first filter reduces the center frequency of the first filter.

8.4.3 Measurement Result of the buffer

The noise figure of the buffer is measured and is depicted in Fig. 8.26. The gain of the buffer is -15 dB and the noise figure is around 18 dB. The measured result is close to the simulation.

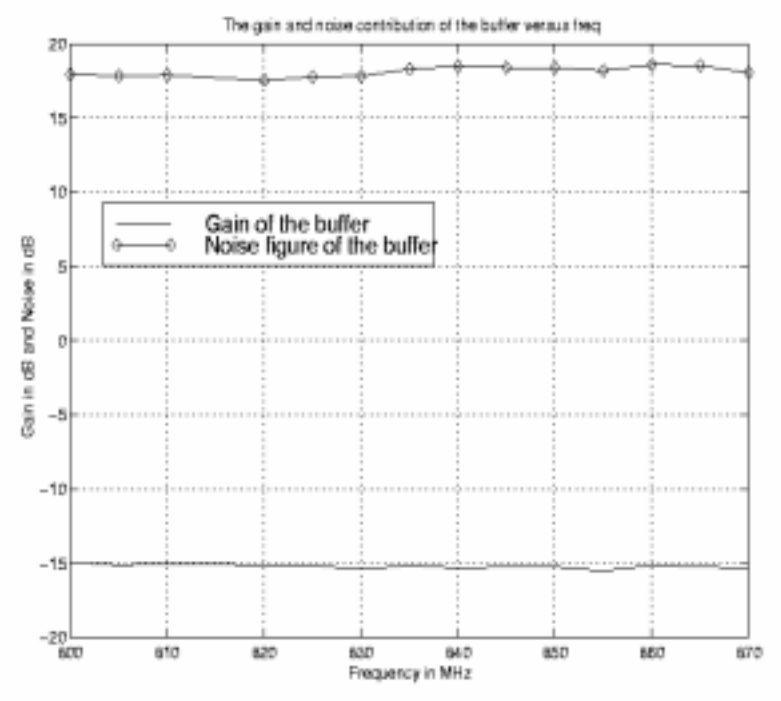


Fig. 8.26 The noise figure and the gain of the output buffer

8.5 Measurement Results of the two-stage and three-stage design

8.5.1 Two-stage measurement Results

The center frequency and the gain of the two-stage amplifier circuit are 820 MHz and 8.5 dB respectively as depicted in Fig. 8.27. The distribution of the gain, the quality factor and the

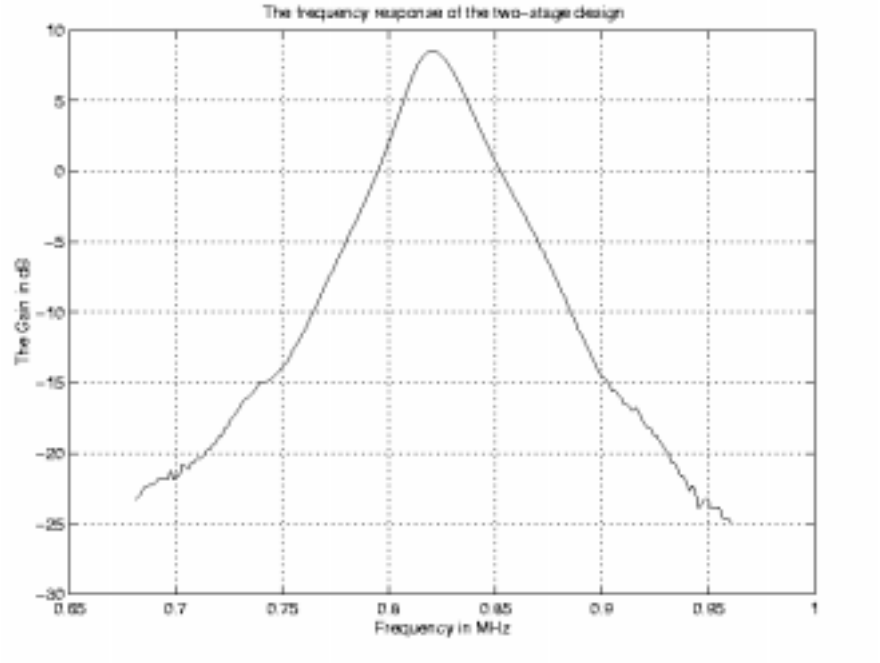


Fig. 8.27 The frequency response of the two-stage amplifier

center frequencies of the first and the second stage are tabulated in Table 8.5.

Parameters	First stage	Second stage
Gain	23 dB	3 dB
Center frequency	815 MHz	827 MHz
Q	38	34

Table 8.5: The distribution of the design parameters in the first and the second stage

The image rejection of the two-stage design at 140 MHz away from the desired signal is

32 dB. The noise figure of the design is 11.7 dB, which is shown in Fig. 8.28. For the linearity, the

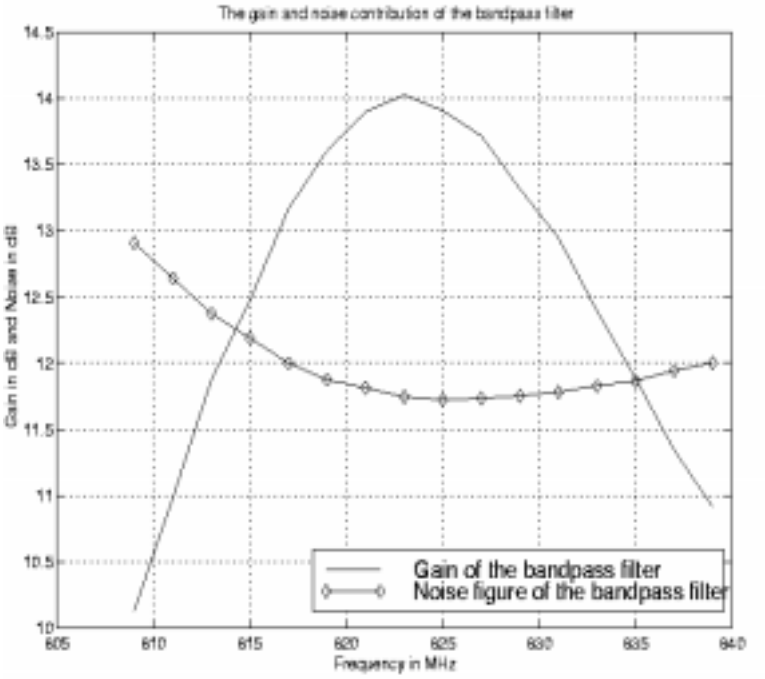


Fig. 8.28 The noise figure of the two-stage amplifier

measured IIP_3 and the $P_{o\text{-}1dB}$ are -15 and -29 dBm respectively. The plot of the fundamental output power and the third-order intermodulation versus input power is given in Fig. 8.29.

8.5.2 Three-stage amplifier measurement results

The center frequency and the gain of the three-stage amplifier circuit are 830 MHz and -4.5 dB respectively as depicted in Fig. 8.30. The distribution of the design parameters in each of the three-stage design are summed up in Table 8.6.

Parameters	First-stage	Second-stage	Third-stage
Center frequency	832 MHz	820 MHz	836 MHz
Gain	23 dB	0 dB	-3 dB
Q	34	34	30

Table 8.6: The distribution of the design parameters in each of the three-stage design

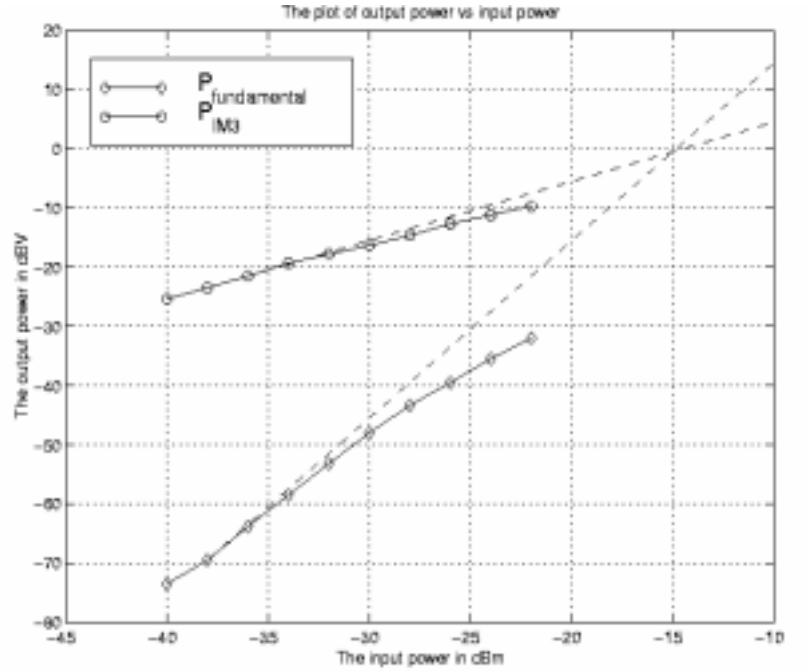


Fig. 8.29 The plot of $P_{o,\,fund}$ and $P_{o,\,IM}$ versus P_{in} (Two-stage)

The image rejection of the three-stage design at 140 MHz away from the desired signal is

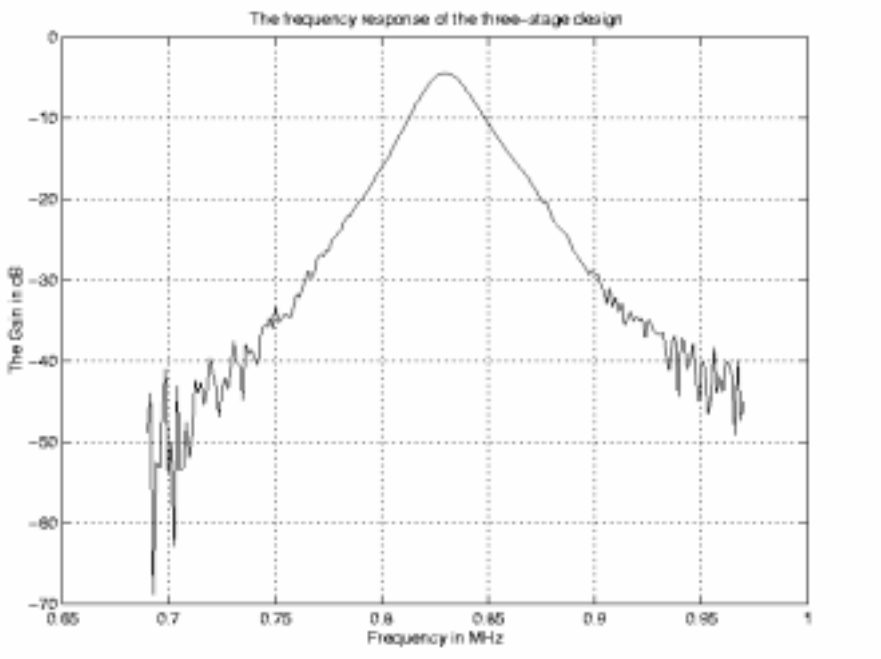


Fig. 8.30 The frequency response of the three-stage amplifier

45 dB. The noise figure of the complete circuit is 15 dB. In addition, the linearity is also measured

by a two-tone test. The IIP_3 and the $P_{o\text{-}1dB}$ are -15 dBm and -26 dBm respectively. The plot of the fundamental output power and the third-order intermodulation versus input power is given in Fig. 8.31.

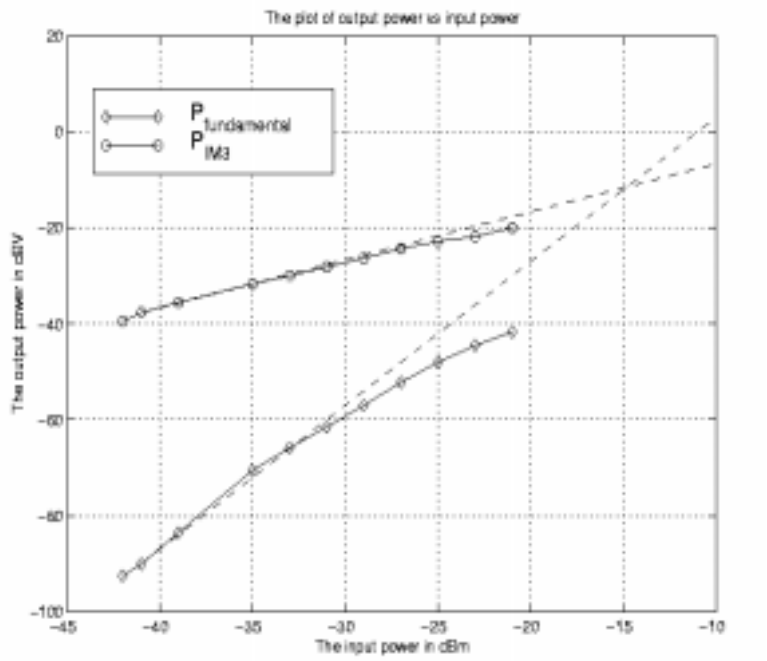


Fig. 8.31 The plot of $P_{IM,3}$ and P_{fund} versus P_{in} (Three-stage)

The measured results of the single, the two and the three-stage design are summarized in Table 8.7.

Parameters	**Single-stage**	**Two-stage**	**Three-stage**
Gain at the output	25 dB	20 dB	16 dB
Center frequency	832 MHz	820 MHz	830 MHz
IIP_3	-18.5 dBm	-15 dBm	-15 dBm
$P_{o\text{-}1dB}$	-29 dBm	-29 dB	-26 dB
Noise Figure	9.6 dB	11.7 dB	15 dB
Image Rejection	18 dB	32 dB	45 dB

Table 8.7: The measured results of the single, the two and the three-stage design

Chapter 9

Conclusion

A CMOS 900-MHz bandpass amplifier that is suitable for RF transceivers was presented. The design employs the state-of-art inductive degeneration techniques to minimize the noise figure and explores the use of lossy spiral inductors in high-frequency circuit to realize on-chip input matching network. To filter out the out-of-band blocking signals, a Q-compensation circuit is embedded to fulfill a 25-MHz 3-dB bandwidth. Besides, a center frequency tuning circuit is also included to compensate frequency deviation due to process variations. Origins of poor circuit linearity was investigated and a modified linearized circuit was designed.

In the first prototype, a second-order bandpass amplifier had been fabricated in standard 0.8 μm single-poly, triple-metal CMOS process. With a 3-V supply, the test-chip achieves a voltage gain of 25 dB with a 25-MHz 3-dB bandwidth. The measured input matching is -13 dB. At a quality factor of 40, the measured input third-order intermodulation product (IIP_3) and the input 1-dB compression point are -21.5 dBm and -32 dBm respectively. Because the measured on-chip spiral's quality factor is smaller than 2 (compared to around 3 to 5 in recent literatures), the noise figure of the whole amplifier is around 10 dB. With the frequency tuning circuit, it allows a

110 MHz (930 to 1040 MHz) tuning range. The power dissipation and the die area are 90 mW and $1.2\ \ mm \times 0.8\ \ mm$ respectively.

So as to enhance the image rejection ability of the design, a three-stage, sixth-order bandpass amplifier had also been implemented. The first stage is a bandpass amplifier, and cascaded with two bandpass filters to realize the sixth-order amplifier. As a whole, the simulated image rejection can be as high as 57 dB.

In an attempt to reduce the total area of the design, two-layer inductors was employed in the design and the design had also been fabricated using 0.5 μm CMOS technology. With a 2-V supply, the bandpass amplifier exhibits a 26 dB voltage gain and a S_{11} of -14 dB. The corresponding IIP_3 and the 1-dB compression point are -18.5 dBm and -29 dBm respectively. Besides, the center frequency can be varied between 760 MHz and 832 MHz. The measured noise figure is 9.6 dB, which is higher than the simulation due to an increase in the thermal noise of the short-channel MOSFET and low-quality inductors.

For the three-stage design, the maximum center frequency is located at 830 MHz with a gain of 16 dB. The corresponding 3-dB bandwidth is 25 MHz and the image rejection at 140 MHz away from the desired signal is around 45 dB. In addition, the input third-order intermodulation product (IIP_3) and the input-referred 1-dB compression point are -15 dBm and -26 dBm respectively. The total current consumption of 90 mA for 3-stage circuit. The die area of the circuit is only $1.2mm \times 0.8\ \ mm$ as two-layers inductors were utilized in the design. The frequency deviation in the second prototype is mainly due to an inadequate modeling of the inductors and the parasitic capacitance.

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