# A 70MHz CMOS $G_m$-C Bandpass Filter with Automatic Tuning

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The Hong Kong University of Science and Technology
In partial fulfillment of the requirements for
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Electrical and Electronic Engineering

by

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B. Eng. (Hons), Electronic Engineering

Submitted in August 1999

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*Devoted to my parents*

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**Choi Yu Wing**
for the Degree of
Master of Philosophy in Electrical and Electronic Engineering
at The Hong Kong University of Science and Technology
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# ABSTRACT

In this thesis, the relationship among power consumption, linearity and noise performance of a CMOS transconductance ($G_m$)-C bandpass filter are studied and optimized. Two 70 MHz bandpass filters are fabricated and measured. Both filters are 6th-order bandpass filters constructed by cascading 3 stages of biquads. The center frequency is 70MHz with a 3-dB bandwidth of 180KHz for the GSM standard.

The first design of the filter uses unbalanced $g_m$ cell design for the gyrators and cross-coupled $g_m$ cell design for the input $g_m$ cells. Only the last 2 stages function properly with a shifted center frequency at 92.5 MHz. The measured $IIP_3$ is –4 dBm with an equivalent input noise of 653 nV/√Hz and a gain of 8 dB. The power consumption is 82 mW with a single 3 V supply. The filter is fabricated in 0.8 μm HP process. The chip area is 1.2 mm by 1 mm. The use of MOS capacitors causes the center frequency to deviate by 36 % and a lowering of the Q value.

The second design of the filter employs actively biased $g_m$ cells for both the gyrators and the input $g_m$ cells. Automatic tunings of both center frequency and Q are included. The actively biased $g_m$ cells have been modified for better linearity. Linear capacitors are employed as the loading capacitance. The series resistance of the capacitors causes a lowering of Q value to about 14 for the whole filter. The corresponding gain is –51.5 dB at 70 MHz.

On the other hand, the automatic frequency tuning loop works from 35 MHz to 68 MHz. While the automatic Q tuning loop operates from 25 MHz to 72MHz and can operate with a deviation of center frequency of ± 8 MHz. The master biquads in the automatic tuning loops can function properly with a Q of 200 or above. The $IIP_3$ of the master biquad is -14 dBm with an equivalent input noise of 1.41 μV/√Hz and a gain of 0 dB. The power consumption of the automatic tuning loop is 28 mW while that of the filter is 88 mW with a single 2.5 V supply. The whole filter is fabricated in 0.5 μm HP process. The chip area is 0.8 mm by 1.2 mm.

# Acknowledgments

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# Chapter 1 Introduction

## 1.1 The role of IF filters in wireless receivers

Nowadays, wireless receivers for mobile phones mainly utilize the super-heterodyne structure to achieve good selectivity and to avoid the problem of DC offset in homodyne (direct-down) receivers. IF bandpass filters are then needed for the channel selection and filtering. A simple block diagram of a wireless receiver is shown in Fig. 1-1.

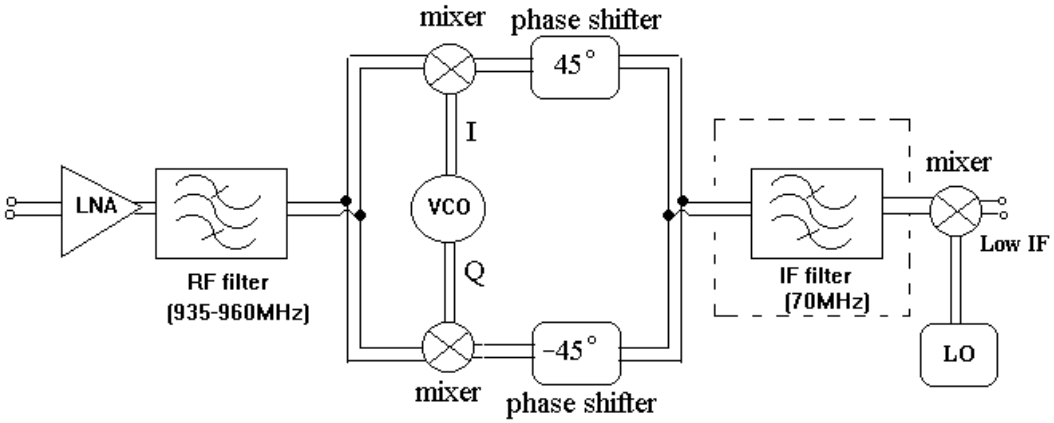


Fig. 1-1 The structure of a super-heterodyne receiver

Most transceivers still use external filters such as surface acoustic wave (SAW) filters for IF filtering. The advantages of using external filters, especially SAW filters, are their high Q, stable center frequencies and no extra power is needed for operation. But in order to drive the 50 Ω input impedance of these off-chip filters, much power (hundreds of mW) has to be supplied for the drivers. More noise is coupled into the external connections too. This motivates the design of monolithic receivers with on-chip filters to avoid the extra power consumption for driving the 50 Ω load and also to minimize noise coupling.

## 1.2 Why $G_m$-C is needed

There are various designs of on-chip bandpass filters including MEMS resonators, simple RC filters, switched-capacitor (SC) filters, spiral inductor-capacitor tanks and $G_m$-C filters. The MEMS resonators can provide a Q of about 100 [1] but requires special MEMS process to fabricate and also requires several tens of volts to operate. On the other hand, the simple RC filters suffer from variation of resistors and capacitors. Each resistor has to be tuned after fabrication. SC filters solve the mismatch problem of the RC filters because the filter parameters depend on capacitor ratios which can be controlled accurately in CMOS processes. However, SC filters are not suitable for frequencies above 10 MHz due to the strict requirement of the unity-gain frequency of Opamp for fast settling. Spiral inductors are only suitable for high frequencies of GHz range. For operation in the IF band, which is from 10 MHz to 100 MHz, however, the Q of these inductors are too low (smaller than 1) to be compensated. The resistance of the inductors dominates the reactance of the inductance. Moreover, a lot of chip area is required for the large inductors and the large capacitors.

$G_m$-C filters can operate in a wide range of frequencies from several hundred of KHz to more than 100 MHz. The limit of the operation frequency of these filters is the amount of excess phase which depends on the speed of response of the filters. Unlike the spiral inductors, the Q of $G_m$-C filters can be adjusted by controlling the output impedance even at lower frequencies. Therefore for the IF band $G_m$-C filters is a good choice of on-chip filtering.

## 1.3 The requirement of the IF filter in GSM receivers and the challenges

The filter is intended to act as a channel filter for the GSM receivers. The filter specifications for –90 dBm sensitivity of the receiver are listed in Table 1-1.

| | |
|---|---|
| Center frequency ($f_o$) | 70 MHz |
| 3 dB bandwidth | 180 KHz |
| Adjacent channel attenuation | 10 dB |
| 600 KHz-1.6 MHz offset attenuation | 53 dB |
| Input equivalent noise | 30 μV |
| Input $IIP_3$ (interferers at 800 KHz & 1.6 MHz offset) | 0 dBm |

Table 1-1 The requirement of the IF filter for –90 dBm sensitivity of a GSM receiver

This requires the filter to have a Q of about 390 while the $IIP_3$ to noise ratio has to be about 80 dB. For the filter to have an attenuation of 53 dB, at least 6 orders are required. This is a rather tough challenge to the $G_m$-C filters. Approximations of filter functions such as Butterworth, Chebyshev and Elliptic functions cannot be applied for such high Q purpose. For a 3-stage filter, the Q of each component for Butterworth filters is 3x390 = 1170. Such high Q easily causes oscillation of the filter and severe degradation of the linearity and the noise performance. Therefore, a simple bandpass filter function is implemented with 3 stages of biquads instead. The Q required for each stage is only 200. Another challenge of $G_m$-C filter is the wide variation of $f_o$ and Q due to process variation. Therefore automatic tuning has to be implemented to restore the nominal $f_o$ and Q. The power allowed for the filter is limited to 120 mW. The chip area is limited to $2mm^2$. Most $G_m$-C filter designs published are for video-band frequencies (<20 MHz) or low Q (<20)

even for high frequencies. Several filter designs and the requirement of this filter are compared in Table 1-2.

| | Wang's[2] | Chang's[3] | Martinez's[4] | Stevenson's[5] | This filter |
|---|---|---|---|---|---|
| $F_o$ | 13 MHz | 300 KHz | 10.7 MHz | 10.7 MHz | 70 MHz |
| Q | 52 | 25 | 20 | 20 | 390 |
| No. of orders | 4 | 4 | 4 | 4 | 6 |
| Auto-tune? | Q and $f_o$ | Q and $f_o$ | Q and $f_o$ | Q and $f_o$ | Q and $f_o$ |
| Gain | N/A | N/A | -3 dB | N/A | N/A |
| Noise | 6 μV/√Hz | 280 nV/√Hz | 822 nV/√Hz | 305 nV/√Hz | 70 nV/√Hz |
| Linearity | 1% @ 211 mV | -72 dB @ 1.4 V | -40 dB @ 1.2 V | 1% @ 50 mV | $IIP_3$ 0 dBm |
| Dynamic Range | 37 dB | 75 dB | 68 dB | 47 dB | 80 dB |
| Power consumption | 350 mW | 70 mW | 220 mW | 108 mW | <120 mW |
| Voltage | ± 5-6 V | 5 V single | ±2.5 V | ±1.5 V | 3 V single |
| Process | 3 μm | 0.7 μm | 1.5 μm | 1.2 μm | 0.8 / 0.5 μm |
| Chip area | 2.3x3.4 $mm^2$ | 4.8 $mm^2$ | 6 $mm^2$ | 1.8x1.8 $mm^2$ | 2 $mm^2$ |

Table 1-2 Comparisons of 4 designs of $G_m$-C filters and the specification of this filter

## 1.4 The focus of the research and the thesis

The research focuses on the optimization of the linearity and the noise performance of a $G_m$-C filter with limited power consumption. In Chapter 2, the linearity and the noise problems of a $g_m$ cell are investigated. Several linearization techniques are compared and discussed as well. In Chapter 3, various design aspects of a biquad including the frequency and Q control, the effect of the noise and the linearity of $g_m$ cells to a biquad and the effects of process variation are investigated. The relationship among noise, linearity and power is discussed as well. In Chapter 4, automatic tuning strategies of both $f_o$ and Q are introduced and discussed.

Two filters are fabricated and tested consequently. The first one is designed with cross-coupled $g_m$ cells as the input $g_m$ cells and unbalanced $g_m$ cells as the $g_m$ cells for the gyrator. MOS capacitors are used as the loading. The filter is fabricated in 0.8 μm HP process. The design procedure and the simulated and measured results are presented in Chapter 5.

The second filter employs actively biased $g_m$ cells for all the $g_m$ cells of the filter. Linear capacitors are used as the loading instead of MOS capacitors. Automatic tuning circuitry is also implemented. The filter is fabricated in 0.5 μm HP process. The design procedure and the simulated results are presented in Chapter 6. The measurement results and discussions are presented in Chapter 7.

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# Chapter 2 Transconductance ($g_m$) Cells

## 2.1 Background

A transconductance ($g_m$) cell is a voltage to current (V-I) converter which converts input AC voltage to output current variation. It can be modeled with a voltage dependent current source. Since an ideal $g_m$ cell is a current source, infinite output impedance is expected. When the output is connected to a pure capacitance load, it is an integrator with one dominant pole at s=0 as shown in Fig. 2-1.

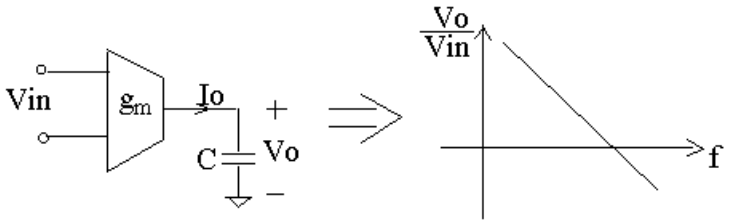


Fig. 2-1 $G_m$-C integrator and its frequency response

The relation of $V_o$ and $V_{in}$ is given by:

$$\frac{V_o}{V_{in}} = \frac{g_m}{sC} \tag{2-1}$$

An infinite DC gain is also expected for the integrator. In fact, this is not realistic. The output impedance of a real $g_m$ cell is always finite. A real $g_m$ cell is then a 2-pole system, with the dominant pole no longer equal to zero. Other non-idealities of real $g_m$ cells include also linearity and noise. The MOS device has a square-law I-V characteristic, therefore there exists intermodulation of interferes into the signal band.

In this chapter, the linearity and noise of a differential pair, which is the core unit of a $g_m$ cell, will be discussed. Then several linearization techniques to achieve better linearity of $g_m$ cells will be investigated and the corresponding noise will be compared. Finally, the calculation of the noise of a simple differential pair will also be delivered.

## 2.2 Discussion of linearity problem of simple differential pairs

### *2.1.1 Square-law I-V relation*

A long-channel MOS device has a square-law first order relation between the drain current $I_d$ and the gate voltage $V_{gs}$ :

$$I_d = K(V_{gs} - V_t)^2(1+\lambda |V_{ds}|) \qquad (2\text{-}2)$$

Where $K = \frac{1}{2}\mu C_{ox}\frac{W}{L}$.

But for the later expressions, the channel length modulation term $(1+\lambda|V_{ds}|)$ will be ignored. Equivalently, the output impedance $r_o$ of the transistor will be discussed.

Although a single-ended transistor can be a $g_m$ cell, the common-mode rejection ratio (CMRR) is 0dB which will cause common-mode instability when the transistor is applied in bandpass filters. Therefore our concern will focus on source-coupled differential pairs.

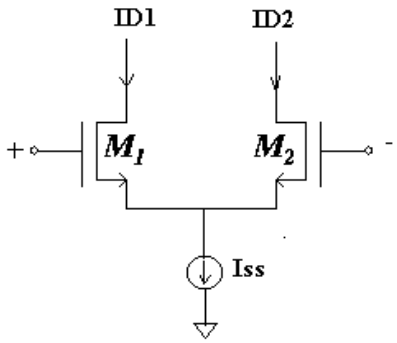


Fig. 2-2 A simple source coupled differential pair.

Fig. 2-2 shows a simple source-coupled differential pair. The current source $I_{ss}$ provides a high impedance current bias which suppresses the common-mode gain. When both transistors $M_1$ and $M_2$ are matched, the output current $I_{out}$ is given by:

$$I_{out} = \frac{1}{2}(I_{D1} - I_{D2}) = K(V_{gs} - V_t)V_{id} \quad (2\text{-}3)$$

where $V_{id}$ is the differential input voltage.

Apparently, $I_{out}$ is perfectly linear with respect to $V_{id}$, but actually $V_{gs}$, the gate-to-source bias voltage, of both $M_1$ and $M_2$ vary with the signal due to the fact that the source node of both transistors is not a perfect virtual ground. When $V_{id}$ is large, a square term, $V_{id}^2$ becomes significant in $I_{D1}+I_{D2}$:

$$I_{D1} + I_{D2} = K[2(V_{gs} - V_t)^2 + \frac{V_{id}^2}{2}] = I_{ss} \quad (2\text{-}4)$$

Since the DC bias current $I_{ss}$ is fixed, $V_{gs}$ of both transistors vary with $V_{id}$. The complete expression of $I_{out}$ is obtained below [1]:

$$I_{out} = \begin{cases} \frac{1}{2}V_{id}\sqrt{2I_{ss}K}\sqrt{1-\frac{V_{id}^2 K}{2I_{ss}}} & \text{when } |V_{id}| \le \sqrt{\frac{I_{ss}}{K}} \\ I_{ss}\,\mathrm{sgn}(V_{id}) & \text{when } |V_{id}| \ge \sqrt{\frac{I_{ss}}{K}} \end{cases} \quad (2\text{-}5)$$

The corresponding $g_m$ is then:

$$g_m = \frac{\partial I_{out}}{\partial V_{id}} = \frac{\frac{1}{2}\sqrt{2I_{ss}K}(1-\frac{V_{id}^2 K}{I_{ss}})}{\sqrt{1-\frac{V_{id}^2 K}{2I_{ss}}}} = \frac{1}{2}(\sqrt{2I_{ss}K} - \frac{3}{2\sqrt{2}}\frac{K^{\frac{3}{2}}}{\sqrt{I_{ss}}}V_{id}^2 - ...) \quad (2\text{-}6)$$

A reduction of $g_m$ will be resulted with an increase of $V_{id}$. Note that when $V_{id}$ tends to 0, the $g_m$ will become $\frac{1}{2}\sqrt{2I_{ss}K}$ and this is the approximation of the $g_m$ for small signals.

### *2.2.2 Body effect*

For an N-Well process, the sources of $M_1$ and $M_2$ of the differential pair have a voltage difference $V_{SB}$ with respect to the substrate. As a result, the $V_t$ of each transistor has to be modified as:

$$V_t = V_{FB} + \phi_B + \gamma\sqrt{\phi_B + V_{SB}} = V_{TO} + \gamma(\sqrt{\phi_B + V_{SB}} - \sqrt{\phi_B}) \tag{2-7}$$

$$\gamma = \frac{\sqrt{2qN_A\varepsilon_s}}{C_{ox}} \tag{2-8}$$

where $N_A$ is the doping concentration, $\varepsilon_s$ is the silicon dielectric constant, q is electron charge, $V_{FB}$ is the flat-band voltage, $\psi_B$ is the difference between the Fermi level and the intrinsic level and $V_{TO}$ is the original threshold voltage without body effect.

The subsequent drain current of the transistor can be approximated as:

$$I_D = \frac{K}{1+\delta}(V_{gs} - V_t)^2 \tag{2-9}$$

$$\delta = \frac{\gamma}{2\sqrt{1+\phi_B + V_{SB}}} \tag{2-10}$$

where the $V_t$ is given by Eq. (2-7).

From the I-V relationship of Eq. (2-4), we have that $V_{SB}$ varies with $V_{id}$. As a result, the non-linear characteristic of a differential pair is no longer a simple square-law relationship. This affects the linearization techniques such as active biasing or unbalanced $g_m$ cell that will be introduced later. For small signal amplitudes smaller than 100 mV,

$\Delta V_{SB} << V_{SB}$, the simple I-V relationship can still hold. This is one of the reasons that linearization techniques involving compensation of non-linearity can work for a limited range only.

### *2.2.3 Mobility degradation due to vertical gate field.*

The mobility degradation of transistors worsens the complexity of the non-linearity problem. The vertical electric field of the gate enhances collisions of channel electrons to the gate oxide and thus slows down the electrons. With the effect of mobility degradation, the new drain current is given as follows:

$$I_d = \frac{1}{2}\mu_{eff} C_{ox} \frac{W}{L}(V_{gs} - V_t)^2 = \frac{1}{2}\left(\frac{\mu_0}{1+\theta(V_{gs} - V_t)}\right) C_{ox} \frac{W}{L}(V_{gs} - V_t)^2 \qquad (2\text{-}11)$$

where $\theta$ is the mobility degradation constant which is about 0.181 for 0.5 μm HP process and 0.158 for 0.8 μm HP process.

This is especially significant for short channel devices because the gate oxide is very thin. For example, the $t_{ox}$ of 0.8 μm HP process is about 17 nm while that of 0.5 μm HP process is only 9.6 nm. Thinner gate oxide means a stronger vertical field. Moreover, in order to keep the same $V_t$, higher doping of the substrate is required. This reduces the channel "thickness" and therefore also increases the vertical field.

For a signal with an amplitude of 200 mV the mobility can cause a drop of $g_m$ by 5.2% and 4.5% respectively for the above 2 processes. This already affects the linearity severely where only <1% variation of $g_m$ is allowed for such signal amplitude. Eq. (2-4) is now modified as:

$$I_{D1} + I_{D2} = K \frac{(V_{gs} - V_t)^2 + (V_{id}/2)^2 + 2\theta(V_{gs} - V_t)[(V_{gs} - V_t)^2 - (V_{id}/2)^2]}{[1+\theta(V_{gs} - V_t)]^2 - (V_{id}/2)^2} = I_{ss} \quad (2\text{-}12)$$

Up to this point, the $V_{gs}$ is too complicated to be expressed as a function of $V_{id}$. But the fact that the mobility between $M_1$ and $M_2$ in the differential pair differs more with larger $V_{id.}$is significant when taking mobility degradation into consideration. This causes an error in the prediction of linearity by the simple square law.

The effect of mobility degradation can be alleviated by choosing processes with longer minimum length. The gate oxide is thicker and therefore with smaller vertical field. Another remedy is to bias the transistor to a higher $V_{gs}$-$V_t$ such that the percentage variation of its mobility will be smaller.

### *2.2.4 Short Channel effects*

For short channel devices, the lateral electric field (the E-field between source and drain) can reach the field strength $E_{sat}$ at which the velocity of the channel carriers saturates. As a result, the pinch-off phenomenon as predicted by the first order Eq. (2-2) is invalid. The modified expression of $I_d$ is given as:

$$I_d = wC_{ox}(V_{gs} - V_t - V_{dsat})v_{sat} \quad (2\text{-}13)$$

Here $V_{dsat}$ is the $V_{ds}$ when the channel carriers achieve saturation velocity $V_{sat}$ and is given by [2]:

$$V_{dsat} = \frac{(V_{gs} - V_t)E_{sat}L}{V_{gs} - V_t + E_{sat}L} \tag{2-14}$$

$$v_{sat} = \mu_{eff} E_{sat} / 2 \tag{2-15}$$

where $\mu_{eff}$ is the effective mobility.

Note that when the channel length L is long, Eq. (2-13) will be simplified as Eq. (2-2). When L is small, $I_d$ tends to have a linear relationship instead of the squared one with $V_{gs}$-$V_t$. It does not mean that the device is more linear now. The perfect linear relationship occurs only when L=0 which is impossible. For most sub-micron processes, the velocity saturation of channel carriers just causes the I-V relationship to be non-quadratic. Linearization techniques such as active biasing may not match the non-linearity function. Furthermore, the $V_{dsat}$ varies with $V_{gs}$-$V_t$. This makes accurate linearization very complicated or even impossible.

Short-channel effects include also the drain-induced barrier lowering (DIBL) and hot electron effects. Detailed analysis will be out of the scope of this thesis and thus not provided here.

## 2.3 Noise analysis of a differential pair

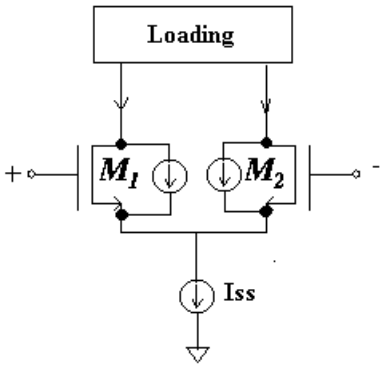


Fig. 2-3 The noise sources of a differential pair

In the calculation, the $R_{out}$, $C_{out}$ and $g_m$ all refer to the one of each transistor of the differential pair.

For long channel devices, the output noise $V_n^2$ of each $g_m$ cell can be readily expressed [3]:

$$V_n^2 = 2\gamma \times [\frac{8}{3} KTBg_m R_{out}^2] \qquad (2\text{-}16)$$

The noise power is doubled because there are 2 branches.

Note that the constant $\gamma$ is 1 for long channel devices and with noiseless loading. However, the output loading has its own noise, and if short channel effects, like hot electron effect, are taken into account, the value of $\gamma$ can be 1 to 4 times larger than the original value.

## 2.4 Linearization Techniques of gm cells

There are many techniques implemented to reduce the variation of $g_m$ of differential pairs towards the variation of $V_{id.}$ The techniques of the following categories will be discussed:

1. Source degeneration [4][5]
2. Cross-coupling [6]
3. Compensation using unbalanced differential pairs [7]
4. Active biasing. [8][9]

### *2.4.1 Source degeneration*

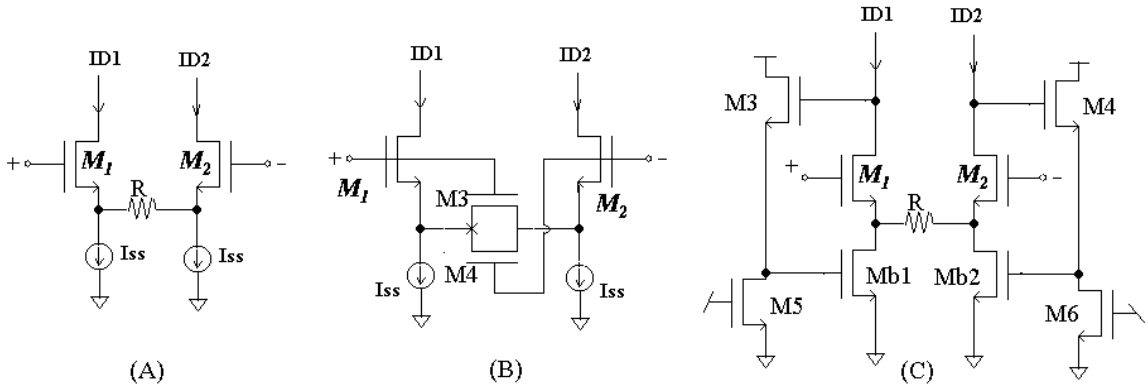


Fig. 2-4 Methods of applying source degeneration with (A) simple degeneration, (B) dynamic source degeneration and (C) degeneration with common-mode feedback.

Fig. 2-4(A) shows the simplest way to apply source degeneration.

Linearization is achieved because now the $I_{out}$ becomes:

$$I_{out} = \frac{1}{2}(V_{id} - I_{out}R)\sqrt{2I_{ss}K}\sqrt{1-\frac{(V_{id} - I_{out}R)^2 K}{2I_{ss}}} \tag{2-17}$$

The resultant transconductance $G_m$ is the familiar expression:

$$G_m \approx \frac{g_m}{1+g_m R} \tag{2-18}$$

Notice that the non-linear term now depends on ($V_{id}$-$I_{out}$R) rather than $V_{id.}$ When R>>1/$g_{m,}$ the non-linear term tends to be zero. That is, a very linear $g_m$ is obtained. However, this is traded-off with the power consumption which provides the $g_m$. Suppose the $G_m$ is allowed to vary only by 1% with a drop of 10% of the $g_{m,}$ then the R required is about 9/$g_{m.}$ That means $G_m$ = 0.1$g_m$. Ten times more power is required to achieve the same transconductance! The noise power is also increased by the same amount. Its advantage is

its simplicity and its fast response since local feedback is applied. Fig. 2-5 shows the simulated $g_m$ variation to the input signal. Differential pairs with $g_mR$ = 1 and without source degeneration are compared. Note that the power consumption for the degenerated pair has to be doubled for the same $g_m$ as well.

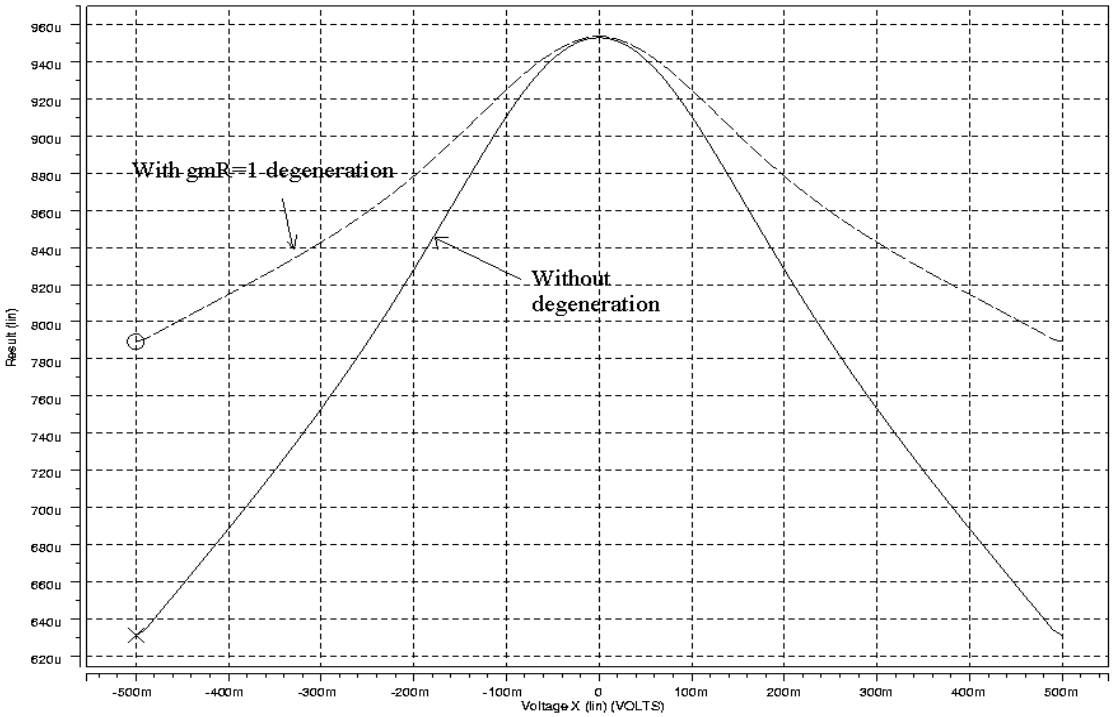


Fig. 2-5. Comparison between differential pairs with $g_mR$=1 degeneration and without degeneration

An improved version is shown in Fig. 2-4(B) [2]. The degeneration resistance can now be changed dynamically with the input signal amplitude. Qualitatively, when the amplitude of the input signal rises, the triode-mode degeneration MOS resistors will be more biased such that the synthesized resistance is reduced. This allows less degeneration and results in more $g_m$ of the differential pair to compensate for the drop of $g_m$.

The quantitative relationship is expressed as follows:

$$g_m \approx \frac{4K_1K_3(V_{gs1}-V_t)}{K_1+4K_3} \tag{2-19}$$

The rise of $g_m$ then compensates for the drop of $g_m$ expressed in Eq. (2-6). However, the compensation is not adaptive. Therefore it is suitable when the range of tolerance of $g_m$ is relatively large.

Fig. 2-6 shows the simulated variation of the plot of the $g_m$ of the differential pair employing the degeneration of Fig. 2-4(B) and is compared with the one of Fig. 2-4(A) for the linear range. Note that there is a boost-up of $g_m$ for signal amplitude of about 400 mV with the same power consumption. However the ripple of the $g_m$ value over the range is still too large for many applications.

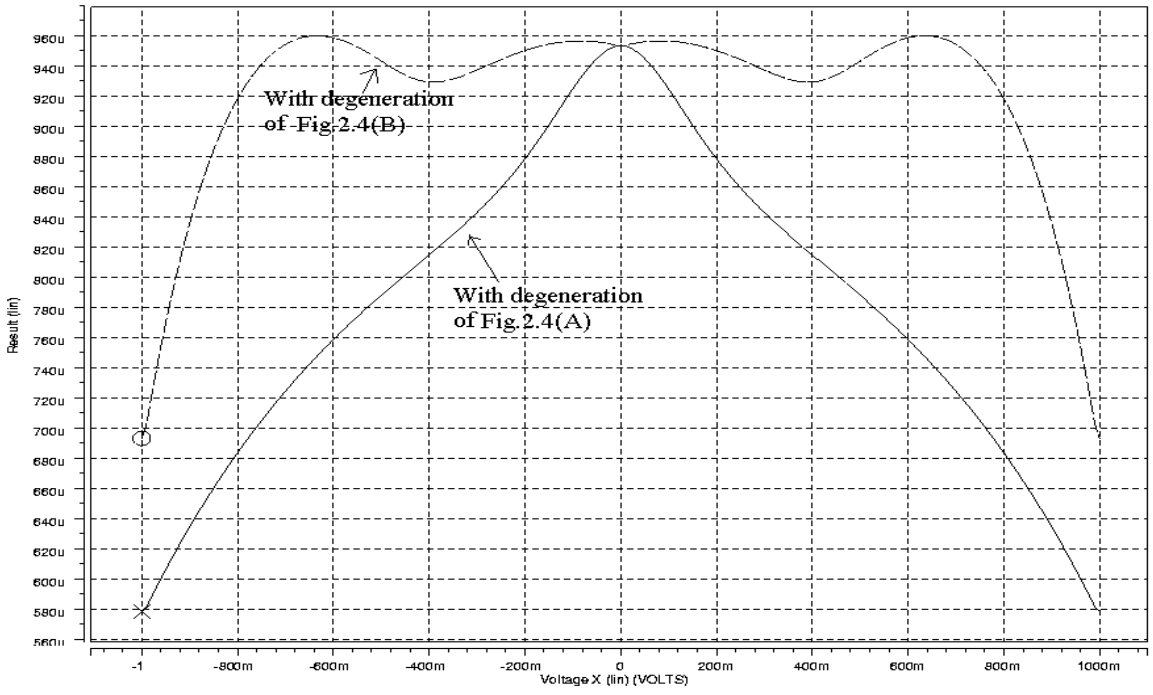


Fig. 2-6. Comparison of $g_m$ variation to input voltage between differential pairs with degeneration in Fig. 2-4(A) and Fig. 2-4(B)

To improve the problem of the ripple, Fig. 2-4(C) shows another design of source degeneration [3]. It modifies Fig. 2-4(A) in the way that an extra feedback circuitry is inserted to keep the voltage across the degeneration resistor to be constant for a range of the input signal. $M_3$-$M_6$ provide the level-shift. The $g_m$ is simply 1/R.

Fig. 2-7 shows the simulated $g_m$ variation of this design. The $g_m$ remains fairly constant within a range of ± 400 mV with the same power consumption as in previous designs. However, its effective $g_m$ reduces by half while the noise problem is not improved. So the design is not useful if effective use of power is essential.

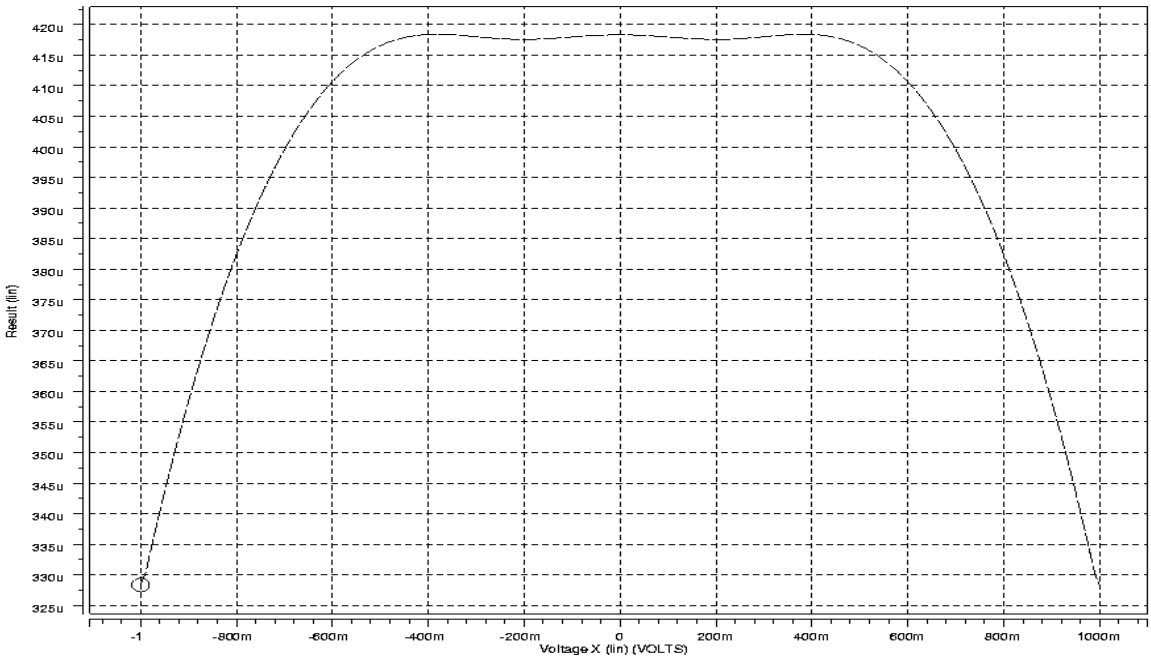


Fig. 2-7 Simulated $g_m$ variation with input signal voltage of the design of Fig. 2-4(c)

### *2.4.2 Cross-coupling*

A simple differential pair can cancel out the even order harmonics of distortion of $I_o$. The remaining odd order harmonics can be cancelled out by cross coupling 2 differential pairs with the same distortion but with different $g_m$ values. The circuit is shown in Fig. 2-8 [6].

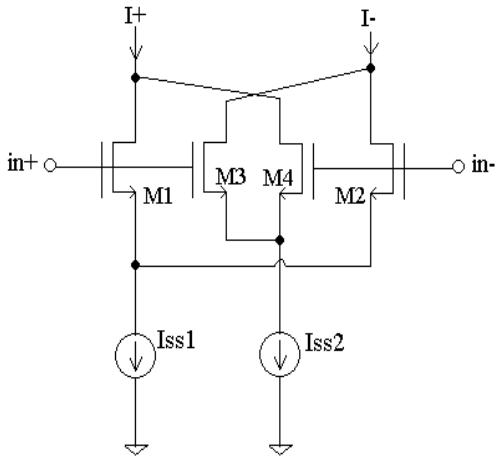

Fig. 2-8 A cross-coupled $g_m$ cell.

The 3rd order harmonic is the main concern since it is now the most significant distortion. From Eq. (2-6), the 3rd order harmonic distortion ($HD_3$) of $I_o$ can be obtained as:

$$HD_3 = \frac{K^{\frac{3}{2}}}{2\sqrt{2I_{ss}}}V_{id}^3 \qquad (2\text{-}20)$$

Since $HD_3$ depends on the ratio of $K^{3/2}$ and $I_{ss}^{1/2}$ only, the distortion can be cancelled by connecting 2 differential pairs in parallel with different $g_m$ but with the same distortion. $K_{3,4}$ and $K_{1,2}$ are related to $I_{ss2}$ and $I_{ss1}$ as follows:

$$(\frac{K_{3,4}}{K_{1,2}})^3 = \frac{I_{ss2}}{I_{ss1}} \qquad (2\text{-}21)$$

The corresponding effective $g_m$ is then given by:

$$g_{meff} = g_{m1,2}[1-(\frac{K_{3,4}}{K_{1,2}})^2] = g_{m1,2}[1-(\frac{I_{ss2}}{I_{ss1}})^{\frac{2}{3}}] \qquad (2\text{-}22)$$

But the non-linearity cancellation is not complete due to the difference in second order parameters such as the mobility between the 2 differential pairs. The incomplete cancellation is more significant when $I_{ss2} << I_{ss1}$ though more extra power consumption due to $I_{ss2}$ is saved. The perfect cancellation happens when $I_{ss2}$ approaches $I_{ss1}$. Yet the

resultant $g_m$ also tends to zero. There is also a problem of the smaller CMRR. The reason is that the differential gain is reduced by $M_3$ and $M_4$ whereas the common-mode gain is enhanced. This can be a serious problem for the common-mode stability if the $g_m$ cell is used to construct gyrators for $G_m$-C bandpass filters. Another disadvantage is the additional noise of $M_3$ and $M_4$. The factor of the noise to a simple differential pair is $1+(\frac{I_{ss2}}{I_{ss1}})^{\frac{2}{3}}$. But it is suitable when a very small and linear $g_m$ is required because the $g_m$ is obtained from the cancellation of 2 relatively large $g_m$'s.

Fig. 2-9 shows the simulated variation of the $g_m$ to the input voltage. $I_{ss2}$ : $I_{ss1}$ = 1:4. A flat response can be obtained over a range of about ± 420 mV.

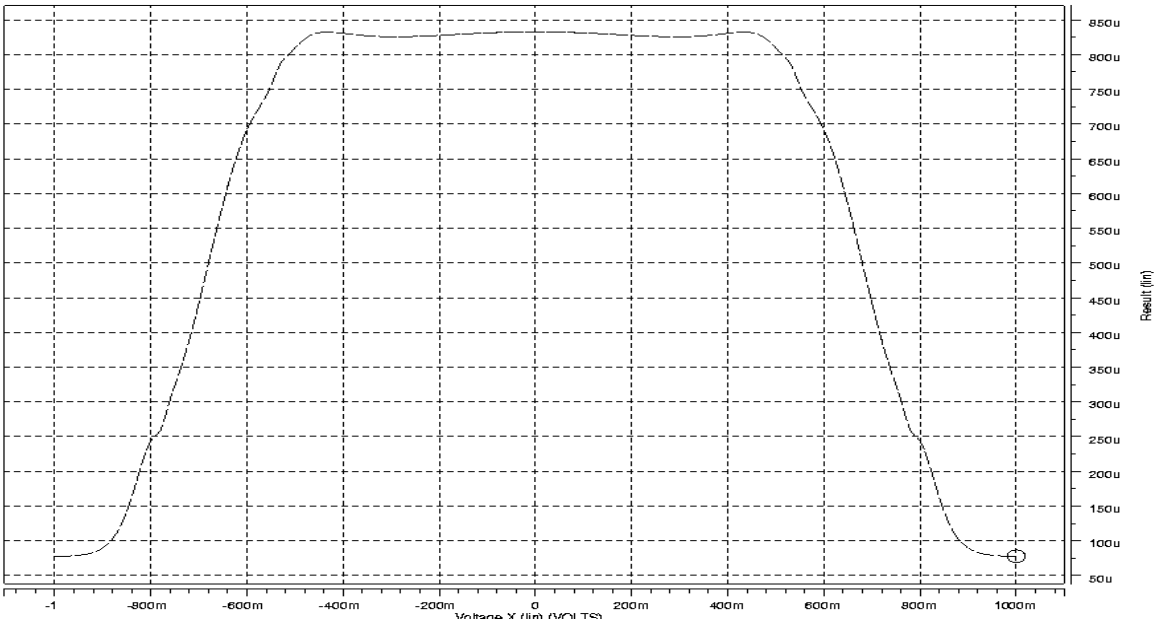


Fig. 2-9 Simulated $g_m$ variation with input signal voltage of the design of Fig. 2-8

### *2.4.3 Compensation using unbalanced differential pairs.*

From Fig. 2-5, the dome-shaped variation of $g_m$ to the input voltage of a simple differential pair is noticed. Two differential pairs with a symmetrical but opposite-signed input offset voltage can compensate for the drop of the $g_m$ of each other so that a flat $g_m$ can be obtained at a certain offset. The schematic and the basic operation principle are shown respectively in Fig. 2-10 [7] and Fig. 2-11.

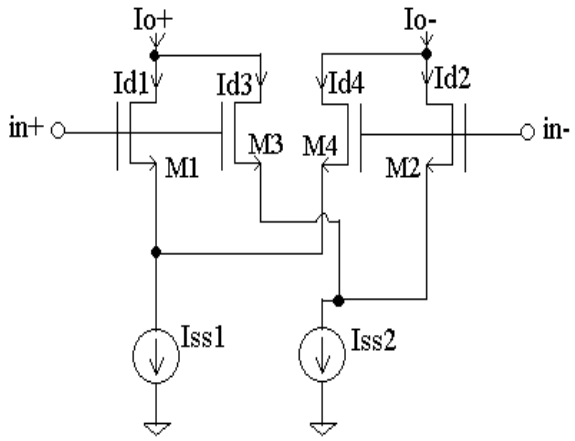


Fig. 2-10 A symmetrically unbalanced $g_m$ cell

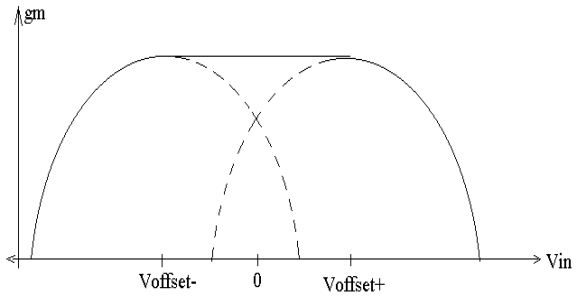


Fig. 2-11 The idea of unbalanced $g_m$ compensation

In the schematic, $K_1$=$K_2$ and $K_3$=$K_4$. The differential pairs $M_{1,4}$ and $M_{2,3}$ have symmetrical offset voltage because the sizes of the transistors are different in each differential pair. To find the offset voltage, the point where $I_{d1}$=$I_{d4}$ and $I_{d2}$=$I_{d3}$ has to be found:

$$I_{d1,2} = I_{d3,4} \Rightarrow K_{1,2}(V_{gs} - V_t - V_{offset})^2 = K_{3,4}(V_{gs} - V_t + V_{offset})^2$$
$$\Rightarrow V_{offset} = \frac{\sqrt{K_{1,2}} - \sqrt{K_{3,4}}}{\sqrt{K_{1,2}} + \sqrt{K_{3,4}}}(V_{gs} - V_t) \qquad (2\text{-}23)$$

If the non-linear $g_m$ expression of (2-6) is included, the compensation is not complete due to the squared term:

$$g_{meff} = g_{m1,2} + g_{m3,4} = \frac{1}{2}\sqrt{2I_{ss}K}\left[\frac{(1-\frac{(V_{off}-V_{id})^2 K}{I_{ss}})}{\sqrt{1-\frac{(V_{off}-V_{id})^2 K}{2I_{ss}}}} + \frac{(1-\frac{(V_{off}+V_{id})^2 K}{I_{ss}})}{\sqrt{1-\frac{(V_{off}+V_{id})^2 K}{2I_{ss}}}}\right] \quad (2\text{-}24)$$

But this just considers the first order characteristic. With the second order effects and by choosing different lengths of the transistors of each pair, a fairly constant $g_m$ for a range of about ±200 mV is obtained as shown in Fig. 2-12.

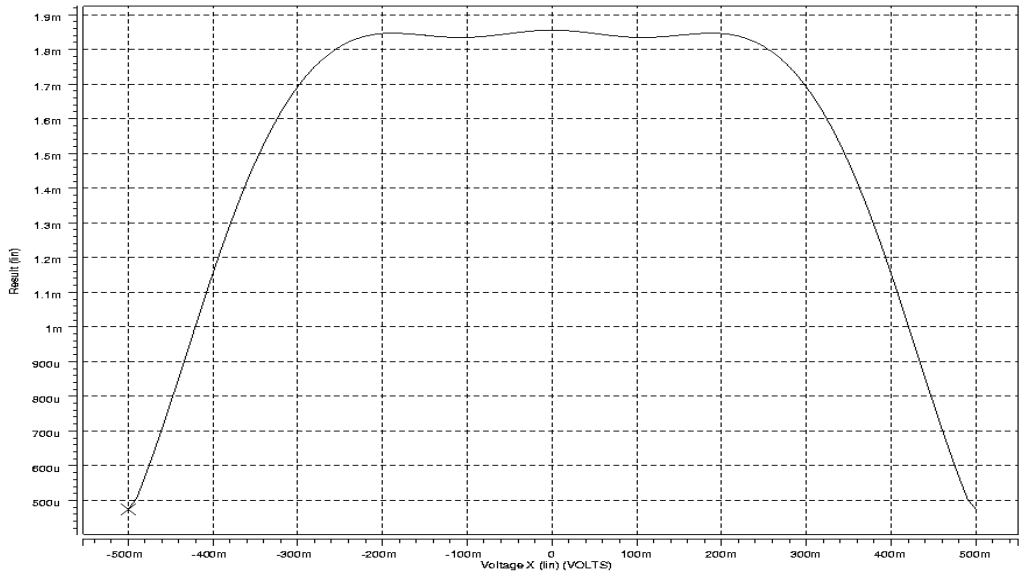


Fig. 2-12 Simulated $g_m$ variation with input signal voltage of the design of Fig. 2-10

The linear range of this $g_m$ cell is worse than the others. But the $g_m$-to-power efficiency is much better than the previous designs. Since there are 2 differential pairs with different offsets, the power consumption is less than double of that of a simple differential pair with the same $g_m$. This is a win because for a simple differential pair with $V_{gs}$-$V_t$ = 200 mV, the input range with < 1% $g_m$ variation is about ± 40 mV only! This makes the unbalanced $g_m$ cell suitable for the requirement of high power efficiency. Another

advantage is that unlike the cross-coupled $g_m$ cells, the differential pairs *reinforce* the differential gain. This does not hurt the CMRR and therefore the design is stable when used in gyrators.

The noise performance is worse than that of a simple differential pair because 2 differential pairs are connected. However, the noise is not doubled because $K_{3,4} < K_{1,2}$.

### *2.4.4 Active biasing*

From Eqs. (2-5) and (2-6), the nonlinear characteristic of differential pairs is observed to come from the expression $\sqrt{1-\frac{V_{id}{}^2 K}{2I_{ss}}}$. This term can be cancelled by canceling the $V_{id}$ term in the expression. The method is to make the biasing current compensate for the non-linear term:

$$I_{ss} = I_{DC} + K\frac{V_{id}^2}{2} \tag{2-25}$$

where $I_{DC}$ is the DC bias current.

Now the bias $I_{ss}$ supplies $I_{DC}$ when $V_{id} = 0$ for the static bias. When there is a signal, an additional bias current $KV_{id}{}^2/2$ will compensate for the drop of the $g_m$. This can be verified by inserting the new $I_{ss}$ into Eq. (2-4):

$$I_{D1} + I_{D2} = 2K(V_{gs} - V_t)^2 = I_{DC} \tag{2-26}$$

As a result, a constant $g_m$ is obtained because $V_{gs}$-$V_t$ of each input transistor is constant. One of the designs is shown in Fig. 2-13 [8].

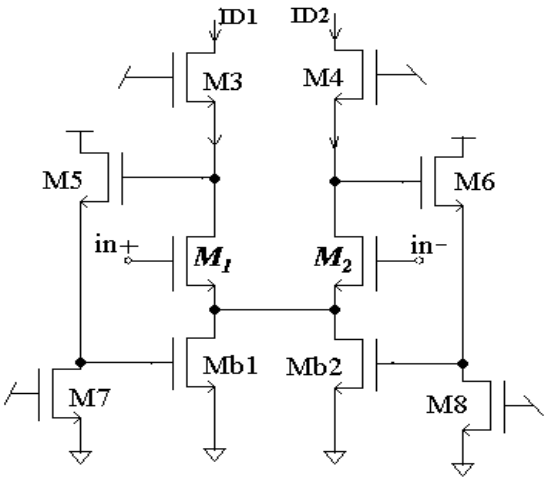

Fig. 2-13 A design of active biasing

In this design, all transistors are matched except $M_5$-$M_8$. For this cascode circuit, when there is an input signal, the same amplitude appears at the drains of $M_1$ and $M_2$ because the loading is $1/g_{m3,4}$ and $g_{m3,4}=g_{m1,2}$. Here, $r_{o1,2} >> 1/g_{m1,2}$ is assumed and the capacitance at that node and the loss of the level shifter $M_5$-$M_8$ are ignored. Both gates of $M_{b1}$ and $M_{b2}$ sense the differential voltage. Because the drains of $M_{b1}$ and $M_{b2}$ are connected together, a bias current is obtained as in Eqs. (2-4) and (2-26). The required active biasing is then established.

When the $g_m$ cell is used for high frequency applications, say 70 MHz, the capacitance effect at the drains of $M_1$ and $M_2$ and the sources of $M_5$ and $M_6$ will reduce the effective signal voltage sensed by $M_{b1}$ and $M_{b2.}$ Therefore, the actual size of $M_{3,4}$ is smaller than that of $M_{1,2}$ to increase the voltage gain of $M_1$ and $M_{2.}$ This ensures that the $KV_{id}^2/2$ is enough to compensate for the non-linearity.

The same linearization effect can be achieved by connecting the gates of $M_{b1}$ and $M_{b2}$ to the 2 inputs respectively. But in the common-mode sense, now the conductance of $M_{b1}$ and $M_{b2}$ increases in phase with the input signal. This is a kind of feed-forward and thus

causes a boost-up of the common-mode gain. As a result, CMRR drops and common-mode instability will be resulted.

Fig. 2-14 shows the simulated $g_m$ plot with the input voltage. The linear range is about ±300 mV. Its efficiency is the highest among all designs. This is because for small signal amplitude the $g_m$ cell is just the same as a simple differential pair without the non-linearity; when the output current swing is greater than $I_{DC}$, the additional squared term of the bias current is not limited by $I_{ss}$ but continues to increase.

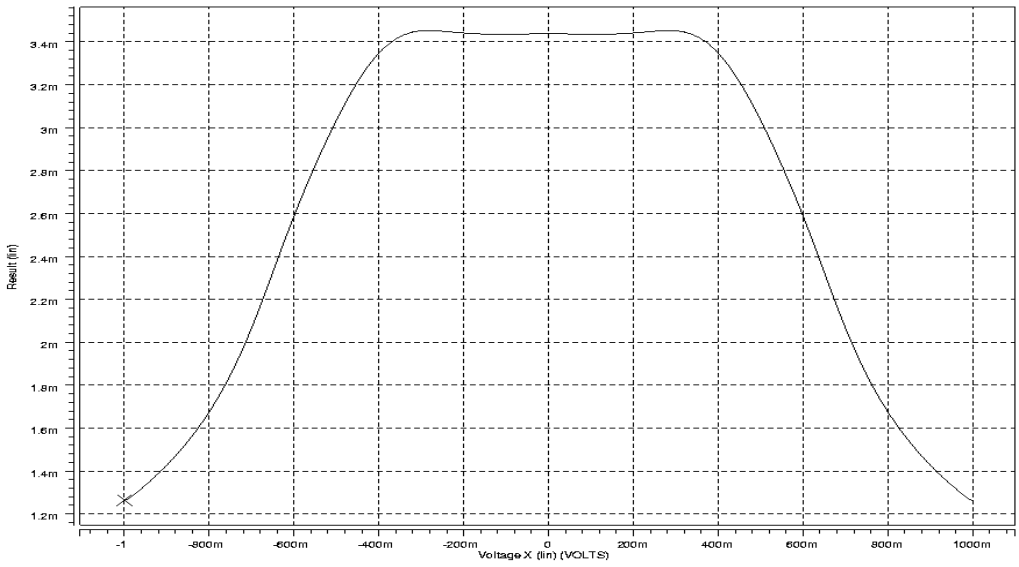


Fig. 2-14 Simulated $g_m$ variation with input signal voltage of the design of Fig. 2-13

The problem of this design is the requirement of high voltage supply for an acceptable linearity. For example, if a linearity range of ± 300 mV is required, the $V_{gs}$-$V_t$ is required to be at least 150 mV for every transistor. Then for $M_{b1}$ and $M_{b2}$, the gate bias has to be at least 0.85 V. For $M_6$ and $M_7$, $V_{gs}$ is at about 1 V. For M3 and M4 to work in saturation region, the $V_{ds}$ has to be at least 0.2 V. Typically $V_{ds}$ is chosen to be 0.3 V - 0.4 V for

ensuring saturation. If an active PMOS loading is used, one more V is needed. Therefore the supply voltage has to be at least 3 V.

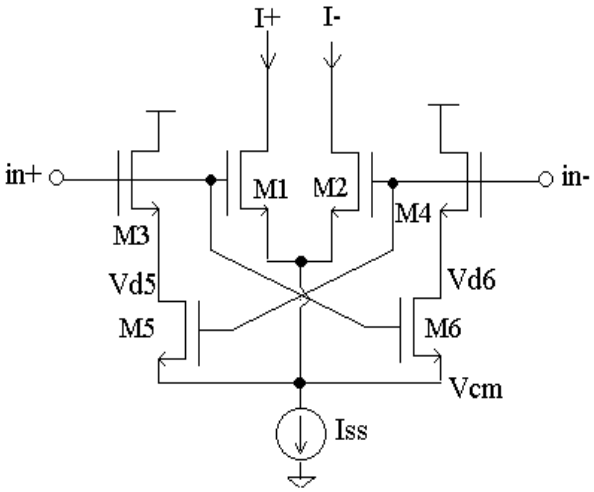


Fig. 2-15 Another design of active biasing

There is a modified design that can operate at a lower supply voltage. The schematic is shown in Fig. 2-15 [9]. Instead of controlling the gate bias of the bias transistor $M_{b,}$ a differential pair $M_3$-$M_6$ acts as a "pool" of bias current. Both pairs share the same bias current source.

When the signal amplitude is small, $M_3$ and $M_4$ are in saturation region while $M_5$ and $M_6$ are in triode region. $M_3$-$M_6$ drain out some of the bias current. When the signal amplitude is positive and large, $M_6$ will go into saturation region and $M_5$ will be cut off. Smaller sum of the bias current will be drained out by $M_3$-$M_6$. That means more current will be supplied to $M_1$ and $M_2$ to compensate for the drop of $g_m$. As a result, an active biasing is achieved.

For the details of quantitative treatment please refer to Appendix 2.1 [9]. The best linearity is achieved when:

$$K_{1,2} : K_{3,4} = \frac{1}{2}(\sqrt{2} - 1) : 1 \approx 0.914 : 1 \qquad (2\text{-}27)$$

The effective bias current supplied to $M_1$ and $M_2$ varies with the input voltage $V_{in}$ according to the following equation:

$$(I_{D1}+I_{D2})+(I_{D3}+I_{D4})=(2K_{1,2}+K_{3,4})(V_{cn}+V_t)^2+[2K_{1,2}-K_{3,4}(2^{\frac{3}{2}}-1)](\frac{V_{in}}{2})^2=I_{ss} \quad (2\text{-}28)$$

When the signal amplitude is small, about 65.4% bias current is supplied to $M_1$ and $M_2$. The efficiency of bias current increases with $|V_{in}|$. The ratio of ($I_{D3}$+$I_{D4}$) to the total bias current is shown in Fig.2-16.

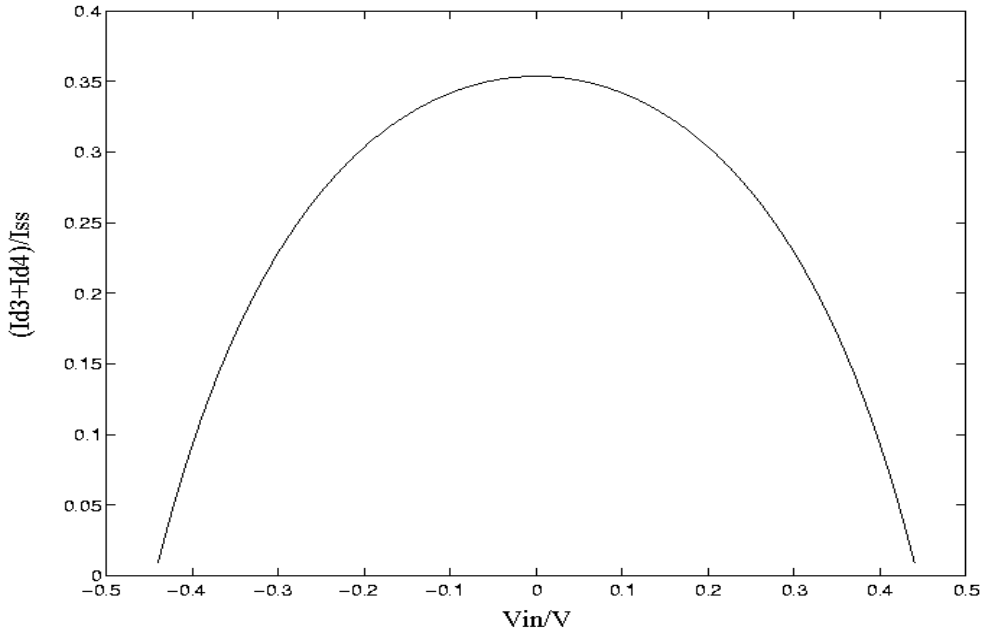


Fig.2-16 Calculated ratio of $I_{D3}$+$I_{D4}$ to the bias current with the input voltage

The efficiency reaches its maximum at $V_{in} \approx 0.45$ V. That is the maximum range that $M_3$-$M_6$ can compensate for. The range is obtained with $V_{gs}$-Vt = 0.25 V. The actual linear range is less than 0.45 V. Besides the body effect and mobility degradation, $V_{ds}$ of $M_5$ and $M_6$ is another restriction. If $M_3$-$M_6$ are matched, then the $V_{ds5}$ and $V_{ds6}$ would be only about 100 mV. That means the differential input swing is restricted to be < 200 mV. The linearity range is not optimized. In the design of the filter that will be introduced in Chapter 6, some modification to the circuit that can extend the linear range will be

discussed. The noise of both actively biased $g_m$ cells is just the same as that of a differential pair and therefore is the smallest.

Fig.2-17 shows the simulated $g_m$ plot with the input voltage. The range is about ± 180 mV. Although the linear range is smaller than that of the design in Fig. 2-13, it can work at voltage supply at as low as 2.5 V with active loading or 2 V with resistive loading. Therefore for the same power consumption a larger $g_m$ can be obtained. When used in gyrators, the loss of the linear range can be compensated for by the increase of $g_m$. Detailed design of the filter using this $g_m$ cell will be discussed in Chapter 6.

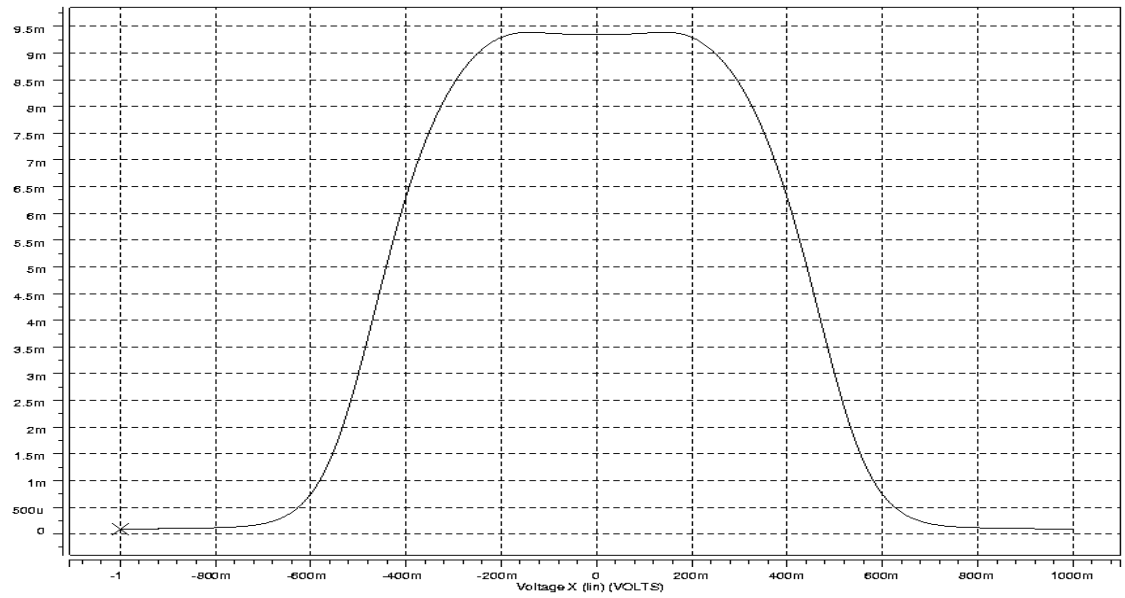


Fig.2-17 Simulated $g_m$ variation with input signal voltage of the design in Fig. 2-15

### *2.4.5 Summary and comparison of different designs*

Several designs of the $g_m$ cells have been discussed. A qualitative comparison is shown in Table 2-1:

| Type of linearization | Advantage | Disadvantage |
|---|---|---|
| Degeneration of Fig. 2-4 (a) | 1. Simple<br>2. Fast response | Not effective, require much power consumption for good linearity. |
| Degeneration of Fig. 2-4 (b) | 1. Simple<br>2. Wider linear range than simple degeneration. | 1. Large variation of $g_m$ making it not suitable for small distortion circuits.<br>2. Low power efficiency |
| Degeneration of Fig. 2-4 (c) | Small variation of $g_m$ over a wide range. | Low power efficiency |
| Cross-coupling | 1. Small variation of $g_m$ over a wide range<br>2. Better power efficiency then source degeneration. | 1. Reduced CMRR.<br>2. Noisy. |
| Unbalanced $g_m$ cell | 1. Good power efficiency.<br>2. Good CMRR. | 1. Small $g_m$ variation for a limited range only.<br>2. No accurate analysis to optimize the linearity. |
| Active biasing | 1. Best power efficiency.<br>2. Lowest noise.<br>3. Small $g_m$ variation over a wide range | 1. Requires good matching of biasing transistors. |

Table 2-1 Table of comparison of various $g_m$ cell designs

To determine which design should be selected for the filter, the power efficiency to the linearity and $g_m$ has to be cared for as well. The results are shown in Table 2-2. From the results, the source degeneration methods are noticed to generally have low power efficiency to both $g_m$ and linear range and also high noise. But they are stable and can achieve a very wide linear range if high power consumption is allowed. The cross-coupled pair can achieve a very good linear range to power ratio. But the $g_m$ and the CMRR attained are too low. Therefore it is only suitable for small but very linear $g_m$ cells such as the input $g_m$ cell of a high-Q biquad. Both the unbalanced $g_m$ cell and the actively biased $g_m$ cell of Fig. 2-15 and Fig. 2-13 have similarly high power efficiency towards both the linear range and the $g_m$. They are suitable for applications of which high power

efficiency towards $g_m$ and linearity is required. Therefore they are suitable for the $g_m$ cells of the gyrators.

| Type of linearization | $g_m$(mA/V) | Power( mW) | Linearity( mV) | Remark(s) |
|---|---|---|---|---|
| Degeneration of Fig. 2-4 (a) | 0.46 | 1.955 | 100 | No flat region |
| Degeneration of Fig. 2-4 (b) | 0.33 | 1.955 | 250 | Large ripple |
| Degeneration of Fig. 2-4 (c) | 0.82 | 9.75 | 400 | |
| Cross-coupling | 0.0144 | 0.815 | 380 | Low CMRR |
| Unbalanced $g_m$ cell | 1.83 | 4.678 | 200 | |
| Active biasing of Fig. 2-13 | 0.84 | 1.669 | 220 | |
| Active biasing of Fig. 2-15 | 1.593 | 3.83 | 180 | |

| Type of linearization | $g_m$/power (mA/V/mW) | Linear range /power (mV/mW) | Linearity x $g_m$ /power (μA/mW) | Noise ratio (Nominal is 1 for a simple differential pair.) |
|---|---|---|---|---|
| Degeneration of Fig. 2-4 (a) | 0.235 | 51.15 | 23.53 | 2 |
| Degeneration of Fig. 2-4 (b) | 0.169 | 127.9 | 42.21 | 3.5 |
| Degeneration of Fig. 2-4 (c) | 0.084 | 41.03 | 33.6 | 7 |
| Cross-coupling | 0.018 | 466.3 | 6.715 | 1.4 |
| Unbalanced $g_m$ cell | 0.391 | 42.75 | 78.23 | 1.3 |
| Active biasing of Fig. 2-13 | 0.503 | 131.8 | 110.7 | 1 |
| Active biasing of Fig. 2-15 | 0.416 | 47.0 | 74.87 | 1 |

Table 2-2 A comparison of power efficiency to both linear range and $g_m$ of different designs of the $g_m$ cells.

## Appendix 2.1 Quantitative analysis of the active biasing circuit of Fig. 2.17

The connection of $M_{3,4}$ and $M_{5,6}$ is a series one with $M_3$ working in saturation and $M_5$ working in triode region. The following relation is immediately obtained:

$$I_{D3} = I_{D5} \Rightarrow K_3(V_{in}/2 - V_{d5} - V_t) = 2K_5[-(V_{in}/2 + V_{cm} + V_t)V_{ds5} - \frac{1}{2}V_{ds5}^{\ 2}] \tag{2-29}$$

Now $K_3 = K_5$. Let $V_{cm}+V_t = V_{cm}^*$. $V_{ds5}$ can then be expressed as:

$$V_{ds5} = -V_{cm}^* + \frac{1}{\sqrt{2}}\sqrt{V_{cm}^{*\ 2} + V_{cm}^* V_{in} - (\frac{V_{in}}{2})^2} \tag{2-30}$$

Then $V_{ds5}$ and $V_{cm}^*$ are substituted into the expression of $I_{D3}$:

$$I_{D3} = K_3\{\frac{V_{in}}{2} - \frac{1}{\sqrt{2}}\sqrt{V_{cm}^{*\ 2} + V_{cm}^* V_{in} - (\frac{V_{in}}{2})^2}\}^2 \tag{2-31}$$

$I_{D4}$ has a similar expression with negative $V_{in}$. By expanding Eq. (2-31) the total current drained by $M_3$-$M_6$ is obtained:

$$I_{D3} + I_{D4} = K_{3,4}[V_{cm}^{*\ 2} - (2^{\frac{3}{2}} - 1)(\frac{V_{in}}{2})^2] \tag{2-32}$$

On the other hand, the sum of $I_{D1}$ and $I_{D2}$ is similar to Eq. (2-4):

$$I_{D1} + I_{D2} = 2K_{1,2}[V_{cm}^{*\ 2} + (\frac{V_{in}}{2})^2] \tag{2-33}$$

Now to keep $V_{cm}$ constant, expressions (2-32) and (2-33) are added together:

$$(I_{D1}+I_{D2})+(I_{D3}+I_{D4}) = 2K_{1,2}[V_{cm}^{*\,2}+(\frac{V_{in}}{2})^2]+K_{3,4}[V_{cm}^{*\,2}-(2^{\frac{3}{2}}-1)(\frac{V_{in}}{2})^2]$$
$$= (2K_{1,2}+K_{3,4})(V_{cn}+V_t)^2+[2K_{1,2}-K_{3,4}(2^{\frac{3}{2}}-1)](\frac{V_{in}}{2})^2 = I_{ss} \quad (2\text{-}34)$$

By eliminating the $V_{in}$ term such that $V_{cm}$ remains constant, the ratio of $K_{1,2}$ and $K_{3,4}$ is obtained:

$$K_{1,2} : K_{3,4} = (2^{\frac{3}{2}}-1) : 2 = 0.914 : 1 \quad (2\text{-}35)$$

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# Chapter 3 The Biquad

## 3.1 Background

Figure 3.1 shows the structure of a single biquad [1]. $G_{m1}$ acts as a V-I converter while its output current drives the L-C resonator to give the $V_o$. The resonator can be synthesized with a gyrator constructed by connecting 2 $g_m$ cells, namely $G_{m2}$ and $G_{m3}$, back to back. The block diagram is shown in Fig. 3-2. In both cases, $I_n$ is the noise source.

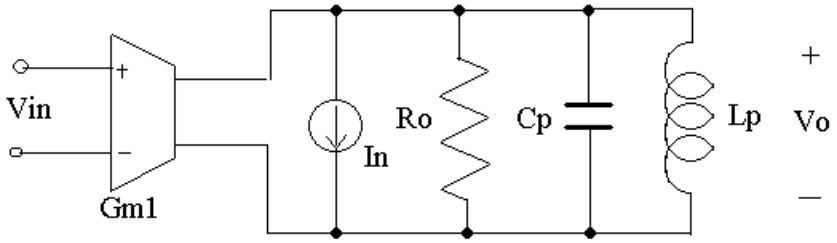


Fig. 3-1 A simple bandpass biquad

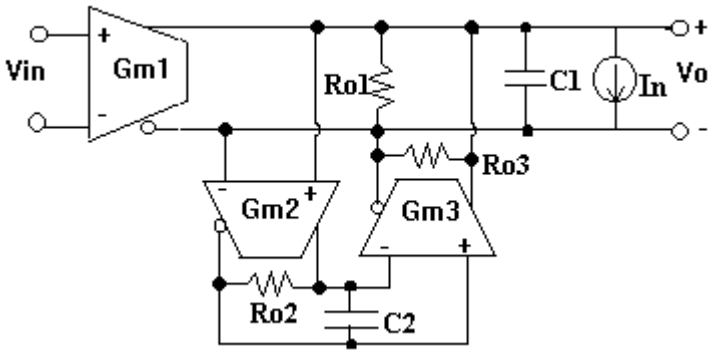


Fig. 3-2. A biquad stage: $G_{m2}$ and $G_{m3}$ form a synthesized inductor

The equivalent inductance $L_p$ of the gyrator is given by:

$$L_p = \frac{C_2}{g_{m2} g_{m3}} \tag{3-1}$$

The center frequency $\omega_o$ is given by [1]:

$$\omega_o = \frac{1}{\sqrt{C_p L_p}} = \sqrt{\frac{g_{m2} g_{m3}}{C_1 C_2}} \tag{3-2}$$

But this is the case with infinite output impedance of the $g_m$ cells and thus infinite Q. With a finite Q, the transfer function is given by:

$$H(s) = \frac{V_o}{V_{in}} = g_{m1}\left[\frac{1/R_{o2}C_1C_2 + s/C_1}{s^2 + s(1/C_1R_o + 1/C_2R_{o2}) + (g_{m2}g_{m3}/C_1C_2 + 1/R_{o1}R_{o2}C_1C_2)}\right] \tag{3-3}$$

where $R_{oi}$ is the output impedance of the i-th $g_m$ cell and $R_o = R_{o1}//R_{o3}$.

For high Q purposes, $1/R_{o2}C_1C_2 << s/C_1$ and $1/R_{o1}R_{o2}C_1C_2 << g_{m2}g_{m3}/C_1C_2$. Therefore, the transfer function H(s) can be approximated as:

$$H(s) = \frac{V_o}{V_{in}} = g_{m1}\left[\frac{s/C_1}{s^2 + s(1/C_1R_o + 1/C_2R_{o2}) + g_{m2}g_{m3}/C_1C_2}\right] \tag{3-4}$$

The Q is given by:

$$Q = \frac{\omega_o}{BW} = \omega_o C_1 R_o = g_{m2,3} R_o \tag{3-5}$$

When $s = j\omega_o$ and $C_1=C_2$, the phase of H(s) is 0° and the gain is simply $Q(g_{m1}/\omega_o C_1)$. This characteristic is applied for automatic Q tuning which will be introduced in the next chapter. Fig. 3-3 shows the Bode-plot of the filter function.

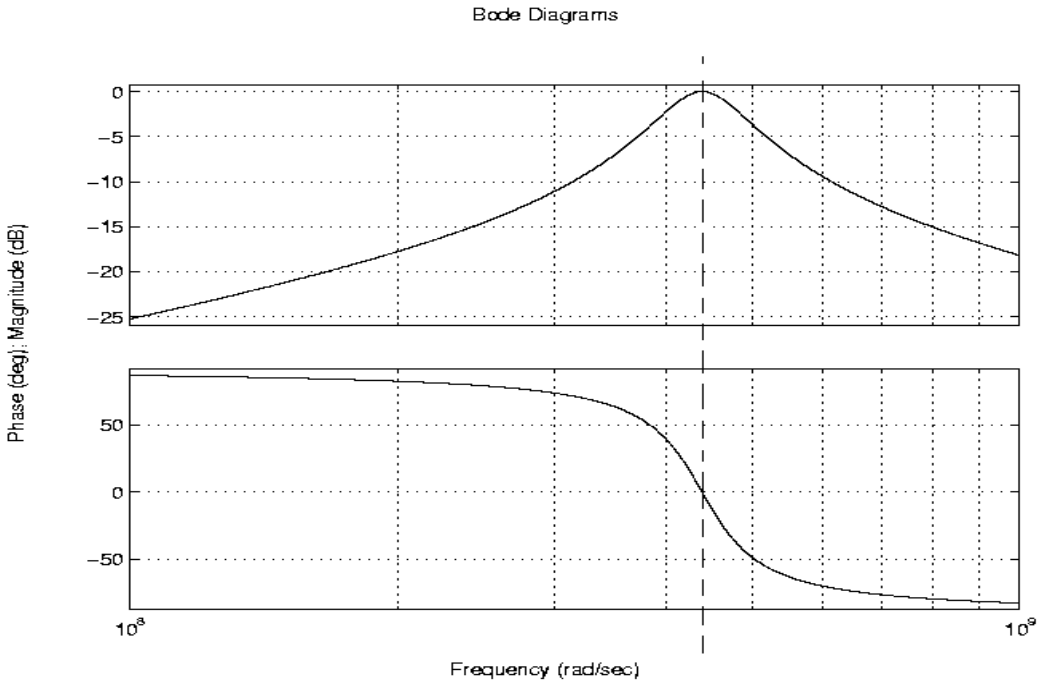


Fig. 3-3 The amplitude and the corresponding phase plots of a bandpass filter

For this design, the Q value is greater than 390, implying a $R_o$ of several tens of KΩ. Thus for linearity consideration the $g_{m1}$ has to be very small (in the order of 10μA/V) for small voltage gain (<30dB). This causes problems of high equivalent noise.

## 3.2 Frequency and Q control

The $f_o$ of the filter depends on the $g_{m2,3}$ of the $g_m$ cells of the gyrator. The $f_o$ can be controlled by varying the bias voltage of the bias transistors. The variation of $g_{m2,3}$ is linear because $g_{m2,3} \propto I_{ss}^{1/2}$ while $I_{ss} \propto (V_{gs}-V_t)^2$ where $V_t$ is the threshold voltage of the bias transistor and $V_{gs}$ is the control voltage.

For many biquads, the Q varies with an additional synthesized resistance $G_{m4}$ connected in parallel at the output node. But this is suitable for low Q (<50) purpose only. If a high Q is needed, cascode stacks can be used to boost up the output impedance of the $g_m$ cells. However, for low voltage supplies such as 3 V or 2.5 V, the dynamic range is severely reduced by the cascode stacks. The impedance can only be tuned down, limiting the extension to higher Q. Another approach is to compensate for the finite output impedance connected in parallel with a negative $g_m$ cell. By doing so, the output impedance can be either tuned up or down. The resultant output impedance $R_o$ is given by:

$$R_o = \frac{1}{g_L + g_o - g_{m-}} \tag{3-6}$$

where $g_L$ is the output conductance of the $g_m$ cell, $g_o$ and $g_{m-}$ are respectively the output conductance and the $g_{m-}$ of the negative $g_m$ cell itself. The $g_m$ is controlled by the bias voltage $V_{qtune}$ of the bias transistor. For a small variation of $V_{qtune}$, the $g_{m-}$ is partly proportional to $V_{qtune}$ by Eq. (2-5):

$$g_{m-} \approx \frac{1}{2}\sqrt{2KI_{ss}} = \frac{1}{2}\sqrt{2KK_{I_{ss}}}(V_{qtune} - V_t) \tag{3-7}$$

Let $\rho = \frac{1}{2}\sqrt{2KK_{I_{ss}}}$. Then the Q is given by (3-6) and (3-7) as:

$$Q = g_{m2,3}R_o = \frac{g_{m2,3}}{g_{o+} - g_{m-}} = \frac{g_{m2,3}}{g_{o+} - \mathrm{r}\,(V_{qtune} - V_t)} \tag{3-8}$$

Thus unlike the frequency tuning, the Q has a partial reciprocal relation with the $V_{qtune}$.

## 3.3 Linearity of a Biquad

### *3.1.1 Quantitative analysis of the linearity of a biquad*

The variation of the $g_m$ of a $g_m$ cell has been discussed in the previous chapter. To investigate its effect to the linearity of the $g_m$ cell, the biquad function has to be expressed as a Taylor series according to $g_{m2,3}$. The variable of the filter function H(s) is changed to the $g_{m2,3}$ of the filter. The first order approximation is listed out below:

$$H(g_{m2,3}) = H(g_{m2,3o}) + H'(g_{m2,3o})(g_{m2,3} - g_{m2,3o}) + \ldots \tag{3-9}$$

where $g_{m2,3o}$ is the preset value of $g_{m2,3}$. The $g_m$'s and the loading capacitance C are assumed to be equal for both $g_m$ cells of the gyrator as for the usual designs. Suppose now the $g_{m2,3}$ is not $g_{m2,3o}$ but $g_{m2,3o}+\Delta g_{m2,3}$, then Eq. (3-9) is re-written as:

$$H(g_{m2,3o} + \Delta g_{m2,3})$$

$$= g_{m1}\left[\frac{s/C}{s^2 + s(1/CR_o + 1/CR_{o2}) + g_{m2,3o}^2/C^2}\right] + g_{m1}\left\{\frac{2g_{m2,3o}s/C^3}{[s^2 + s(1/CR_o + 1/CR_{o2}) + g_{m2,3o}^2/C^2]^2}\right\}\Delta g_{m2,3} + \ldots \tag{3-10}$$

The amount of variation of the gain $H(g_{m2,3o}+\Delta g_{m2,3})$-$H(g_{m2,3o})$ is:

$$H(g_{m2,3o} + \Delta g_{m2,3}) - H(g_{m2,3o}) \approx g_{m1}\left\{\frac{2g_{m2,3o}s/C^3}{[s^2 + s(1/CR_o + 1/CR_{o2}) + g_{m2,3o}^2/C^2]^2}\right\}\Delta g_{m2,3} \tag{3-11}$$

On the other hand, there are also variations of $g_{m1}$ by $\Delta g_{m1}$ and of the $g_{m-}$ by $\Delta g_{m-}$. The combined effect of the fractional variation of the gain of H(s) is then:

$$\frac{\Delta H(s)}{H(s)} \approx \frac{\Delta g_{m1}}{g_{m1}} + \left| \frac{2g_{m2,3o}/C^2}{s^2 + s(1/CR_o + 1/CR_{o2}) + g_{m2,3o}^2/C^2} \right| \Delta g_{m2,3} + \frac{\Delta g_{m-}}{g_{m-}} \qquad (3\text{-}12)$$

At $s = j2\pi 70\ M = jg_{m2,3o}/C$, (3-12) can be simplified as:

$$\left.\frac{\Delta H(s)}{H(s)}\right|_{s=j70MHz} \approx \frac{\Delta g_{m1}}{g_{m1}} + \frac{2\Delta g_{m2,3}}{(1/R_o + 1/R_{o2})} + \frac{\Delta g_{m-}}{g_{m-}} \qquad (3\text{-}13)$$

For high Q filters, $R_o$ and $R_{o2}$ are large and therefore the linearity of the filter becomes very sensitive to the variation of $g_{m2,3}$. A very linear $g_m$ cell is then required for the gyrator. Therefore the variation of $g_{m2,3}$ causes more variation of the gain for filters with higher Q values.

By combining the result of Eqs. (2-6) and (3-13), the non-linearity in terms of the input voltage can then be expressed as:

$$\frac{\Delta H(s)}{H(s)} \approx \frac{6K_{gm1}V_{id}\Delta V_{id}}{4\sqrt{2}I_{ss} - 3KV_{id}^2} + g_{m1}R_o\left[\frac{3K_{gm2,3}^{\frac{3}{2}}V_{id}\Delta V_{id}}{\sqrt{2I_{ss}}(1/R_o + 1/R_{o2})} + \frac{6K_{gm-}V_{id}\Delta V_{id}}{4\sqrt{2}I_{ss} - 3KV_{id}^2}\right] \qquad (3\text{-}14)$$

From the result the percentage of distortion can be observed to increase proportionally with the input voltage.

### *3.1.2 Measurement of the linearity of a filter*

For a real circuit, which is non-linear, the transfer function $H(V_{in})$ can always be broken down into a polynomial of the input signal [2]:

$$H(V_{in}) = a_1 V_{in} + a_2 V_{in}^2 + a V_{in}^3 + \ldots \tag{3-15}$$

If the input is a sinusoidal one, e.g. $V\cos\omega_c t$, then the non-linearity creates harmonics:

$$H(V\cos w_c t) = \frac{a_2 V^2}{2} + (a_1 + \frac{3}{4} a_3 V^2) V\cos w_c t + \frac{a_2 V^2}{2}\cos 2w_c t + \frac{a_3 V^3}{4}\cos 3w_c t + \ldots \tag{3-16}$$

The result is a set of harmonics. The linearity of a filter is usually expressed as total harmonic distortion (THD) which is the ratio of the sum of the power of all harmonics to the fundamental itself. For differential pairs, the even-order harmonics are cancelled. When the input signal strength is moderate (<100 mV), the 3rd harmonic is usually much higher than the higher odd-order ones and is therefore used to approximate the THD.

For this filter, however, the two-tone input-referred third-order intercept ($IIP_3$) is employed. The filter is used for IF filtering in the wireless receivers and there exist interferers to the receiver. When 2 interferers with different frequencies, e.g. $V\cos\omega_1 t$ and $V\cos\omega_2 t$, are fed into a non-linear circuit, inter-modulation will occur and may create in-band interference. In particular, the effects of $2\omega_1 \pm \omega_2$ and $2\omega_2 \pm \omega_1$ are significant when $\omega_1$ is close to $\omega_2$ [2]:

$$\begin{aligned} &H(V_1\cos w_1 t + V_2\cos w_2 t) = \\ &a_1(V_1\cos w_1 t + V_2\cos w_2 t) + \frac{3a_3}{4}\{V_1^2 V_2[\cos(2w_1 + w_2)t + \cos(2w_1 - w_2)t] + \\ &V_2^2 V_1[\cos(2w_2 + w_1)t + \cos(2w_2 - w_1)t]\} \end{aligned} \tag{3-17}$$

For GSM receivers, $\omega_1$ is 70.6 MHz and $\omega_2$ is 71.8 MHz, i.e. the 3rd channel and the 6th channel. The $IIP_3$ can be either found accurately by plotting the 3rd order inter-modulation

products ($IM_3$) together with the fundamental output for different input signal amplitudes, or can be estimated by simple triangular principles as:

$$IIP_3 = \text{Signal in(dBV)} + \frac{\text{Fundamental output voltage (dBV)} - \text{IM}_3\text{(dBV)}}{2} \qquad (3\text{-}18)$$

The plot of the fundamental output and the $IM_3$ to find the $IIP_3$ is demonstrated in Fig. 3-4. Note that the gradient of the $IM_3$ is triple of the fundamental. Voltage is preferred to power for both the input and output signals because both the input and the output of the filter are not 50Ω matched. Expression in voltages can avoid the confusion.

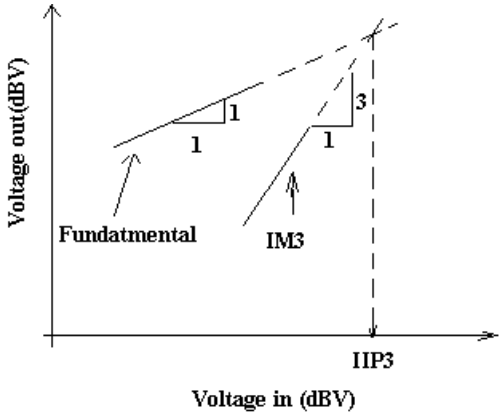


Fig. 3-4 The relation of IM3, fundamental signal and IIP3

## 3.4 Noise Analysis of a simple biquad

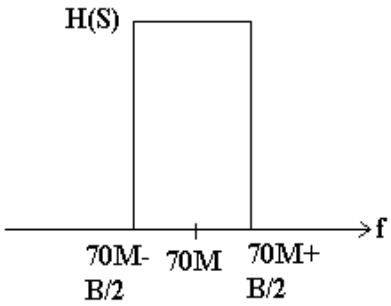


Fig. 3-5 The approximation of the noise function of the filter

Here the calculation is restricted to thermal noise only which is the main source of noise of MOS transistors. Flicker noise is minor here because the frequency interested is 70 MHz.

Let the input noise = $V_{n\,In}^2$, the total output noise = $V_{n\,out}^2$ and the noise of filter H(s) = $V_{n\,H(S)}^2$, The bandwidth interested is 180 KHz. As this filter is a

high-Q one, H(s) can be approximated as a brick-wall filter with the in-band gain = gain at 70 MHz as shown in Fig. 3-5. Then the total output noise $V_{n\,out}^2$ is:

$$V_{n\,out}^2 = |H(s)|^2 V_{n\,in}^2 + V_{n\,H(s)}^2 \approx A_{70\,MHz}^2 V_{n\,in}^2 + V_{n\,H(s)}^2 \tag{3-19}$$

$$\text{Noise Figure N.F.} = \text{SNR}_{\text{in}}/\text{SNR}_{\text{out}} = 10\log\ (1 + \frac{V_n^{\,2}{}_{H(s)}}{A^2{}_{70MHz} V_n^{\,2}{}_{in}}) \tag{3-20}$$

To analyze the noise of a biquad, main concern should be put on the gyrator shown in Fig. 3-6 because both $G_{m2}$ and $G_{m3}$ have large channel conductance and thus impose a dominant noise current to the output of $G_{m1}$.

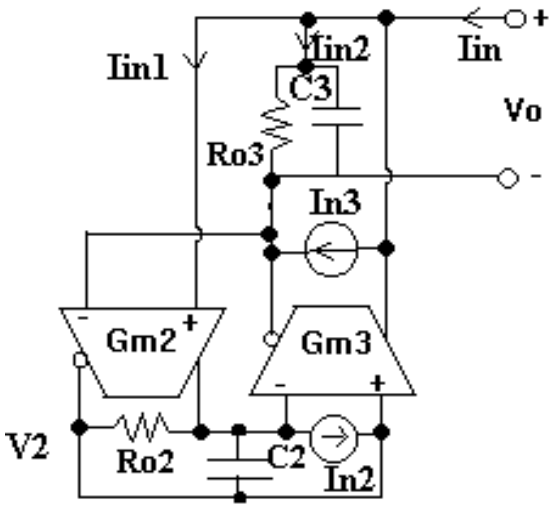


Fig. 3-6 The noise sources of a gyrator

The input voltage $V_2$ of $G_{m3}$ is given by:

$$V_2 = -(g_{m2}V_o + I_{n2})(\frac{R_{o2}}{1 + sR_{o2}C_2}) \tag{3-21}$$

The $V_2$ is then converted back to current and is added directly with the noise current of $G_{m3}$ to generate a total current at the output of $G_{m3}$:

$$I_{in1} = -G_{m3}V_2 + I_{n3} = (G_{m3}G_{m2}V_o + G_{m3}I_{n2})[R_{o2}/(1 + sR_{o2}C_2)] + I_{n3} \tag{3-22}$$

The total current $I_{in}$ at the output is given by:

$$I_{in} = I_{in1} + I_{in2} = \frac{G_{m2}G_{m3}R_{o2}}{1+sR_{o2}C_2}V_o + (\frac{1+sR_{o3}C_3}{R_{o3}})V_o + \frac{G_{m3}I_{n2}R_{o2}}{1+sR_{o2}C_2} + I_{n3} \quad (3\text{-}23)$$

The total current $I_{in}$ consists of the input current $I_o$ and the noise currents $I_{n3}$ and $I_{n2}G_{m3}R_{o2}/(1+sR_{o2}C_2)$. The output voltage is just the output current times the impedance function of the gyrator:

$$V_o \approx (I_o - \frac{G_{m3}R_{o2}}{1+sR_{o2}C_2}I_{n2} - I_{n3})[\frac{s/C_1}{s^2 + s(1/R_{o2}C_2 + 1/R_{o3}C_3) + \frac{G_{m2}G_{m3}}{C_1C_2}}]$$

$$= (I_o - \frac{G_{m3}R_{o2}}{1+sR_{o2}C_2}I_{n2} - I_{n3})H_R(s) \quad (3\text{-}24)$$

where $H_R(s)$ is the impedance function $V_o/I_o$ of the gyrator. Note that $I_o$ contains the noise current of the input $g_m$ cell $G_{m1}$ as well.

From the previous chapter, the noise $V_n^2$ of a simple differential pair is:

$$V_n^2 = 2g \times [\frac{8}{3}KTBg_m R_{out}^2] \quad (3\text{-}25)$$

The full expression of the in-band noise of a biquad can thus be obtained. To calculate the in-band noise, the noise has to be integrated within the bandwidth. For simple calculations, the approximation of the transfer function as a brick-wall as introduced previously is employed. That is, the loading of the gyrator is assumed to be $R_o$ where $R_o = 2R_{out}$ throughout the band. From Eq.(3-3), the relation of $R_o$ in Fig. 3-6 to Q and $g_{m2,3}$ of $G_{m2}$ and $G_{m3}$ is obtained:

$$R_o = Q/g_{m2,3} \quad (3\text{-}26)$$

Then, Eqs. (3-25) to (3-24) can be directly applied to calculate the total noise voltage $V_n^2$ at the output of a biquad:

$$V_n^2 \approx V_{n1}^2 + (\frac{G_{m3}R_{o2}}{1+sR_{o2}C_2})^2 V_{n2}^2 + V_{n3}^2$$
$$= (\left|\frac{G_{m3}R_{o2}}{1+sR_{o2}C_2}\right|^2 + 1)(\frac{8gKTQ^2B}{3g_{m2,3}}) + V_{n1}^2 \quad (3\text{-}27)$$

Some approximations can be done here. Since the $R_{o2}$ is high (in the order of 10 KΩ), the term $\frac{G_{m3}R_{o2}}{1+sR_{o2}C_2}+1$ can be approximated as –j if $s=j\omega_o$. also, since $V_{n1}^2 << V_{n2,3}^2$, it can be ignored. Then $V_n$ can be simplified as:

$$V_n = \frac{2Q}{g_{m2,3}}\sqrt{\frac{2g}{3}KTBg_m} \quad (3\text{-}28)$$

The N.F. of the filter to 50 Ω differential input is then calculated by (3-20) as:

$$N.F. = 10\log(1+\frac{\frac{8gQ^2KTBg_m}{3g_{m2,3}^2}}{g_{m1}^2R_o^2[4KT(50)B]}) = 10\log(1+\frac{gg_m}{75g_{m1}^2}) \quad (3\text{-}29)$$

It appears that the N.F. drops with $g_{m2,3}$ and is independent of Q is true if the linearity of the filter is not considered. If everything is kept constant but $g_{m2,3}$ is reduced, $R_o$ will increase according to Eq.(3-26). The immediate result is the increase of the voltage gain of the filter results in the decrease of the N.F. However, the linearity is inversely proportional to the gain too. To be realistic, the gain of a filter has to be kept constant, say A, and then compare the noise performance. A relationship between $g_{m1}$ and $g_{m2,3}$ then evolves:

$$A = g_{m1}R_{out} \Rightarrow g_{m2,3} = \frac{Qg_{m1}}{A} \quad (3\text{-}30)$$

For a simple differential pair, $g_m=2g_{m2,3}$. When this relationship is put back to (3-29), a different picture appears:

$$N.F. = 10\log(1+\frac{2gQ}{75Ag_{m1}}) \tag{3-31}$$

This is the true picture of the noise performance of a filter. The N.F. is actually proportional to log of Q and inversely proportional to log of $g_{m1.}$

## 3.5 Relation among noise, linearity and power consumption

The main reason why $G_m$-C filters have high input equivalent noise is that there is a large current noise added at the output due to the gyrators. On the other hand, the $g_m$ of the input $g_m$ cell $G_{m1}$ is restricted by the gain of the filter. Increasing the gain can reduce the input equivalent noise but hurts the linearity of the filter.

The figure of merit of a filter can be measured by the dynamic range DR. The DR is the ratio of the maximum input power to the minimum detectable signal power, which is usually the input equivalent noise:

$$DR = \frac{V_{\max}^2}{V_{n\ in}^2} \tag{3-32}$$

For GSM receivers which require IF-Filter to have high linearity, the ratio of $IIP_3$ to the input equivalent noise is used as a ruler for comparison. Note that the comparison is done for fixed power consumption. Increasing the $g_m$ of the $g_m$ cells by increasing power consumption of the gyrator allows a lower $R_o$ for the same Q. Thus it lowers the gain and enhances the linearity for the *same* noise performance. On the other hand, it allows a larger $g_{m1}$ to keep the same gain of the filter which improves the noise performance. But

for mobile handsets, the filter should not consume too much power. A power consumption of less than 120mW is then restricted for the whole filter.

## 3.6 Effects of process variation

Because the $g_m$ of a $g_m$ cell is proportional to $2K(V_{gs}-V_t)$ of the transistors, both $f_o$ and Q will be affected by process variation. For a variation of 5% of W and L, $\Delta K=10.5\%$ for the worse case. Moreover, there are also variations of the threshold voltage $\Delta V_t$ and the capacitance $\Delta C$. Usually, $\Delta V_t=10\%$ and thus the $g_m$ can vary by 20.5%; The dimensions of capacitors vary by 5% which implies that $\Delta C$ is about 10%. The combined effect of $f_o$ is then $\Delta K+\Delta V_t+\Delta C = 30.5\%$. That means a variation of 21.4 MHz can be resulted from an $f_o$ of 70 MHz. Therefore the filter designed should be tunable from 48.6 MHz to 91.4 MHz.

For the Q of the filter, since it depends on the product of $g_{m2,3}$ and $R_o$, it is affected by $\Delta g_{m2,3}$, the $\Delta g_m$ of the $g_m$ cell for impedance compensation and the $\Delta R$ of the loading resistance. The $\Delta R$ can be as much as 20% if polysilicon resistors are used or the same variation as a transistor if triode mode MOS resistors are used. Therefore the variation of Q can be 61%! Such a wide range of Q requires the $-g_m$ cell to be able to be widely tuned.

## Reference


1. J.E.Kardontchik, "Introduction to the design of Transconductor-Capacitor Filters", *KWP*, 1992.
2. Behzad Razavi, “RF Microelectronics”,pp.14-22, Prentice-Hall Inc., 1998.

# Chapter 4 Automatic Tuning for $G_m$-C filters

## 4.1 Introduction

$G_m$-C filters, unlike the switched-capacitor counterparts, do not have a reference clock. The center frequency $f_o$ and Q of a $G_m$-C filter can vary a lot due to process variation and parasitics. This is particularly serious for high-Q filters. Therefore automatic tuning of $f_o$ and Q has to be employed. For most of the automatic tuning circuits, the idea of master-slave controlling is used. The master filter refers to the one in the automatic tuning loops while the slave filter refers to the main filter. The idea assumes that both the master and slave filters match. Therefore by using the same control voltage that controls the master filter to control the slave filters, both filters should show the same characteristics [1]. In this chapter, several designs of automatic tuning circuits will be discussed.

## 4.2 Automatic frequency tuning

### *4.2.1 Automatic frequency tuning using a Delay-Locked Loop (DLL)*

Automatic frequency tuning with delay-locked loop makes use of the phase characteristic of the bandpass filter. From Fig. 3-3**,** the phase varies from 90° when $f<<f_o$ to -90° when $f>>f_o$. When $f = f_o$, the phase is 0°. That is, the filter becomes an in-phase DC amplifier at $f_o$. Therefore by sensing the phase difference between the filter output and a 90°-shifted reference $V_{ref}$ with a phase detector (PD), the error voltage $V_{ftune}$ can be applied to control the frequency. The block diagram is shown in Fig. 4-1.

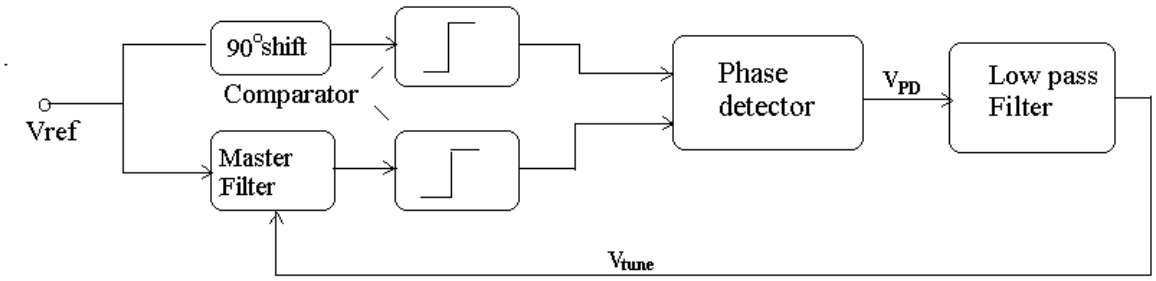


Fig. 4-1 The block diagram of automatic frequency tuning with DLL

A simple multiplier can be used as a PD. Suppose the input reference $V_{ref}$ is $V\sin\omega_o t$, and the master filter has an error in $f_o$ such that there is an excess phase $\Delta\phi$ at $\omega_o$. Then the output of the multiplier is given by:

$$V_{PD} = VK_f K_m \frac{(1+\cos 2w_o t)\sin\Delta f + \sin(2w_o t)\cos\Delta f}{2} \tag{4-1}$$

where $K_f$ and $K_m$ are the gains of the filter and the multiplier respectively. After the lowpass filter, the time average is obtained, and only the DC output remains:

$$V_{ftune} = \frac{VK_f K_m K_{lpf}\sin\Delta f}{2} \approx \frac{VK_f K_m K_{lpf}}{2}\Delta f \tag{4-2}$$

where $K_{lpf}$ is the lowpass filter gain. From the equation, $V_{fune}$ is proportional to $\sin\Delta\phi$ and thus proportional to the $\Delta\phi$ when $\Delta\phi$ is small enough. $V_{ftune}$ also depends on the gains of the master filter, the multiplier and the lowpass filter. The latter two are constant and can be well determined. However, as discussed in the previous chapter, the filter gain depends on the center frequency and Q, which can vary a lot due to process variation. As a result, $V_{ftune}$ cannot report the true variation of the phase difference.

In order to minimize the amplitude effect, a pair of comparators is used to amplify the input signals to the PD to square waves. An XOR gate can then be used as a PD. The XOR gate output has 50% duty cycle for which the averaged output is 0 [3]. The duty cycle reduces when the phases of the 2 signals are closer, and increases for the opposite situation. Therefore the $V_{ftune}$ depends on the phase difference around 90°. But the limited gain of the comparators still cannot solve the problems of time delay in zero crossing of both signals if the Q of the filter is too low. This is illustrated in Fig. 4-2.

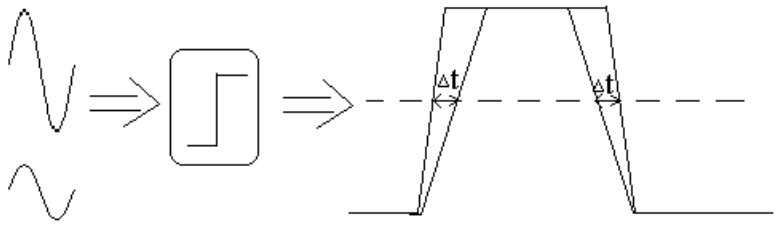


Fig. 4-2 The zero-crossing time error Δt due to different amplitude of the sine waves

During the two zero-crossings, the XOR gate will still output "1" even the two waves should be in-phase. The problem becomes more serious if the Q of the filter deviates more from the preset value. The result is that the DLL will tune the filter until $\Delta t = 0$ and thus an over-tuned $f_o$ will occur. Note that, however, the problem is less serious for a high Q filter because the slope of the phase change is steep. In other words, the deviation of $f_o$ is less for the same deviation of phase.

### *4.2.2 Automatic frequency tuning using a phase-locked loop (PLL)*

Using a phase-locked loop (PLL) instead of a DLL can ease the problem of the tuning error due to the error of the Q of the filter. Although the oscillation amplitude still depends on the Q of the filter, the amplitude is usually above several tens of mV.

Therefore the gain of the comparator need not to be too large to achieve satisfactorily steep rising and falling edges. The block diagram is shown in Fig. 4-3.

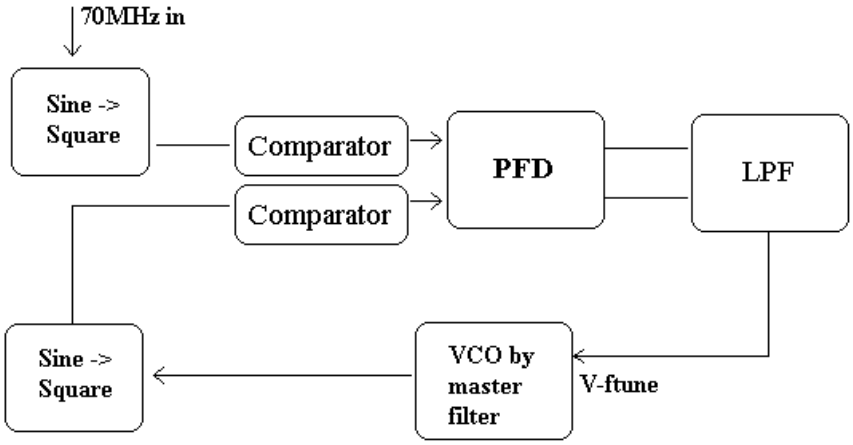


Fig. 4-3 The block diagram of the automatic frequency tuning with PLL.

A PLL is a negative feedback system involving the relation between the VCO control voltage $V_{ftune}$ and the phase error $\phi_e$ from the PD output. For a simple PLL, a multiplier can be used as the PD. The model is given as follows:

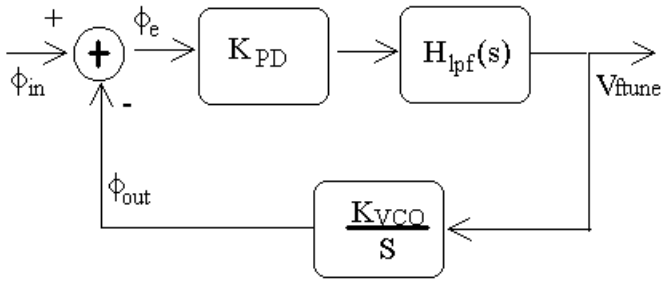


Fig. 4-4 The model of a simple PLL

Suppose the lowpass filter is a simple first order filter given by $H_{lpf}(s) = \frac{K_{LPF}(1+st_z)}{1+st_p}$ The loop transfer function of $\phi_e$ to $\phi_{in}$ is then given as [3]:

$$H_e(s) = \frac{f_e}{f_{in}} = \frac{s(1+st_p)}{s^2t_p + s(K_{PD}K_{VCO}K_{LPF}t_z + 1) + K_{PD}K_{VCO}K_{LPF}} = \frac{s(1+st_p)}{s^2 + 2\zeta\omega_n s + \omega_n^2} \qquad (4\text{-}3)$$

where $\zeta = \frac{1}{2}(\frac{t_z\sqrt{K_{PD}K_{VCO}K_{LPF}} + 1}{t_p})$ is the damping factor and $\omega_n = \sqrt{\frac{K_{PD}K_{VCO}K_{LPF}}{\hat{o}_z t_p}}$ is the loop bandwidth [2]. To ensure a stable response, 90° phase margin is chosen with $\zeta$ chosen to be 1. The zero $\tau_z$ is inserted for fast settling and less ripple after settling [3].

The corresponding frequency tuning voltage $V_{ftune}$ is simply $K_{PD}H_{lpf}(s)\phi_e$. Since the VCO is actually constructed from the same generic $g_m$ cells as the slave biquads, the $K_{VCO}$ is determined by the sensitivity of the $f_o$ of the biquads towards the $V_{ftune}$.

The use of a multiplier as the PD, however, has the problems as mentioned in the DLL. Besides, the capture range of a PD, no matter a multiplier or an XOR gate, is limited by $\omega_n$ and $\zeta$. On the other hand, the $f_o$ of the VCO can vary by 30% as calculated in the previous chapter. Thus a phase frequency detector (PFD) is preferred to a multiplier to ensure locking. However comparators are required before the PFD to amplify the sine waves to square waves. The model of a PFD can be approximated as a sampling system when the phase error is small [3]. The expression is given as:

$$K_{PFD} = \frac{I}{2\pi} \qquad (4\text{-}4)$$

where I is the current of the charge pump.

The structure of a PFD is shown in Fig. 4-5:

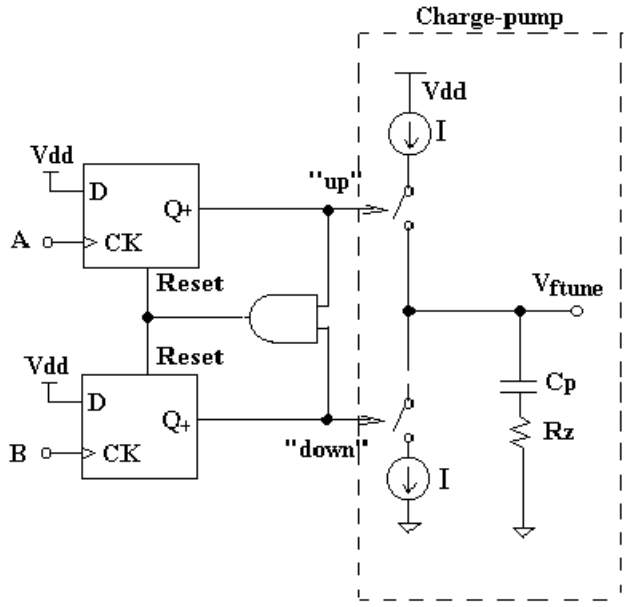


Fig. 4-5 The structure of a PFD with charge-pump

The D input of both the two D-Flip/Flops are connected to logic "1". When input A has a positive edge trigger, the Q+ of the upper D F/F will output a logic "1" ("up" signal). The upper switch of the charge pump connected to the Q+ will then be closed and the $C_p$ will be charged up. When B is triggered, the lower switch of the charge-pump is closed by the "down" signal instead. This time $C_p$ is discharged. When both A and B are triggered, both the Q+ of the D F/F's are reset to "0".

If both A and B are fed with square waves with the phase of A leading that of B, the CK of the upper D F/F is triggered first. As a result, $C_p$ is charged up continuously and vice versa. If the frequency of A is higher than that of B, then the number of "up" signals generated is more than the "down" signals. Therefore the $C_p$ is charged for a longer time than it is discharged. In either case, the $V_{ftune}$ still goes up. Thus the circuit can detect both frequency and phase differences.

When used in a PLL, A is connected to $V_{ref}$ and B is connected to the output of the VCO. Both the $V_{ref}$ and the output of VCO are converted to square waves with comparators.

The $V_{ftune}$ tunes the VCO frequency to keep track with $V_{ref}$.

The charge pump acts as an integrator. If there is no $R_z$, together with the VCO, the PLL will become unstable since $H_e(s)$ is now [2]:

$$H_e(s) = \frac{f_e}{f_{in}} = \frac{s^2}{s^2 + K_{PFD}K_{VCO}} \tag{4-5}$$

Now there exist poles $\pm j(K_{PD}K_{VCO})^{1/2}$ on the jω axis which implies instabilities. As a remedy, an $R_z$ is inserted to create a zero [2]:

$$H_e(s) = \frac{s^2}{s^2 + s\frac{I}{2p}K_{VCO}R_z + \frac{I}{2pC_p}K_{VCO}} \tag{4-6}$$

For 90° phase margin, $\zeta = \frac{R_z}{2}\sqrt{\frac{IC_p}{2p}K_{VCO}} = 1$ and $R_z$ is expressed as:

$$R_z = 2\sqrt{\frac{2p}{IC_pK_{VCO}}} \tag{4-7}$$

The VCO may be constructed by using a biquad with over-compensated impedance. The other design, as will be introduced in Chapter 6, is realized by connecting 2 master biquads back-to-back. The advantage is that the same Q tuning voltage from the automatic Q tuning loop can be used to control the Q of the VCO.

## 4.3 Automatic Q tuning

### *4.3.1 General problem of automatic Q tuning*

In the previous chapter, from Eqs. (3-6) and (3-8), a partial reciprocal relation exists between the Q of a filter and the $g_{m-}$ of the $-g_m$ cell. Normally, the $V_{qtune}$ is preset to be

lower than the required value such that the Q of the biquad is far lower than the required one. Then the $V_{qtune}$ is ramped by the automatic tuning loop. But for this filter, the Q is as high as 200 for each stage. That implies the difference of the positive output conductance and the $g_{m-}$ should be tuned to be less than 20μA/V. Suppose ρ in Eq. (3-8) is $2mA/V^2$, which is usually the case, then a further increase of the $V_{qtune}$ by 10 mV already causes oscillation. This requires the ramp of the $V_{qtune}$ to be very slow. That is, the Q tuning loop bandwidth has to be very small. Fortunately, for the automatic tuning loop of this filter, frequent tuning is not required. Even 1000 cycles per second is more than enough for the variation of the parameters due to temperature and process variations.

Several Q tuning methods are introduced in the following sections. The main concern of automatic Q tuning is the accuracy and the range of variation when the loop is steady.

### *4.3.2 Using a magnitude locked loop (MLL)*

The most straight-forward way of automatic Q tuning is to compare the signal amplitudes between the output of a biquad and $V_{ref.}$ By Eq. (3-4), the gain of biquad is directly proportional to its Q. Therefore, the residue signal $E_r$ is dependent of the Q of the filter. After this $E_r$ is filtered by a lowpass filter, it can be used to tune the Q of the filter. The block diagram of an MLL is given in Fig. 4-6.

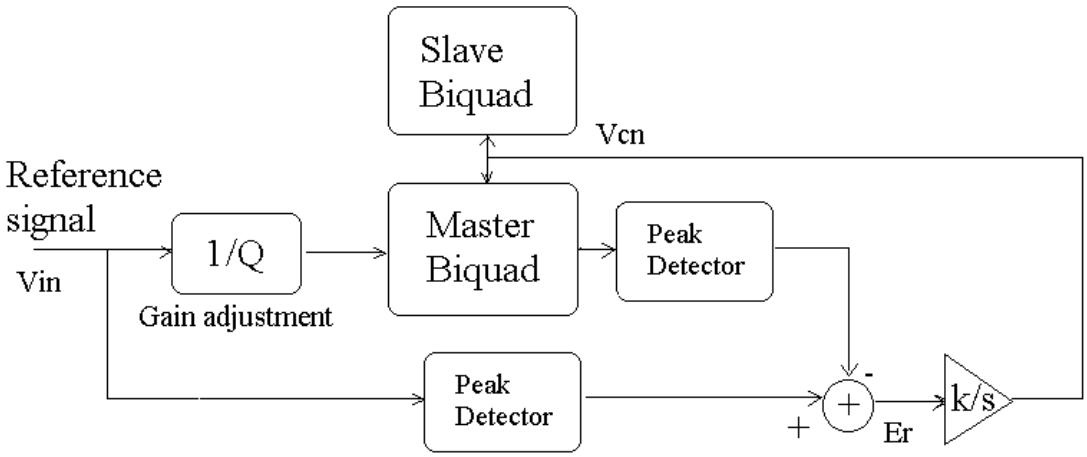


Fig. 4-6 The block diagram of an MLL for Q tuning

The peak detectors are used to search for the point where the Q is the highest so that it can determine whether to tune up or tune down the Q of the biquad. The input signal is scaled with 1/Q so as to ensure that $E_r$ is zero when the desired Q is achieved. By varying the scaling factor, one can determine the required Q of the filter as well.

The use of MLL, however, lacks the immunity to the effect of the $f_o$ deviation of the filter. The MLL just compares the amplitude but not the phase. As a result, when $f_o$ deviates from the preset value, the Q tuning voltage $V_{qtune}$ will continue to increase to minimize $E_r$. This may over-tune the Q of the biquads and thus may cause oscillation.

### *4.3.3 Q tuning by tracking the step response of a biquad*

The other method of Q tuning is by detecting the step response of a biquad. The block diagram is shown in Fig. 4-7.

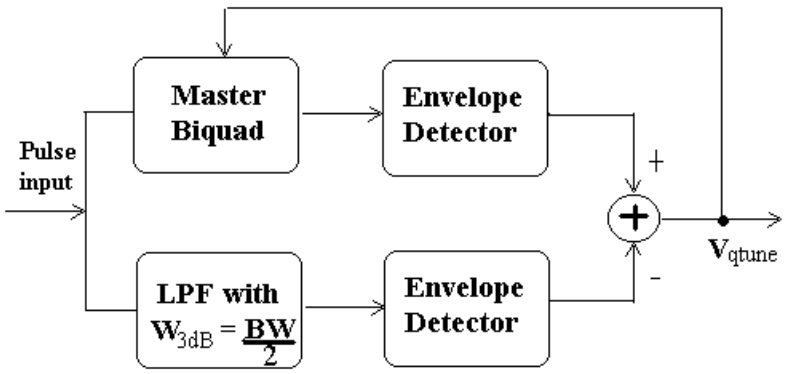


Fig. 4-7 The block diagram of the Q tuning by Envelope detection

A train of step inputs are simultaneously fed into the master biquad and a low pass filter. The $\omega_{3\text{-dB}}$ of the lowpass filter is the same as half of the bandwidth BW of the master biquad. Theoretically, the envelope of both filters should be the same if BW=$\omega_o$. This is especially true for high Q biquads. Envelope detectors then detect the envelopes of the outputs, and the difference is filtered to form the $V_{qtune.}$ This tuning method, however, subjects to the gain and $\omega_o$ mismatch of the lowpass filter. Therefore a tuning error of about 30% may be resulted [1].

### *4.3.4 Adaptive Q tuning*

An approach for accurate Q tuning is done by tracking the coefficients of all the terms of a filter function. This is known as adaptive tuning. The block diagram is shown in Fig. 4-8 [4].

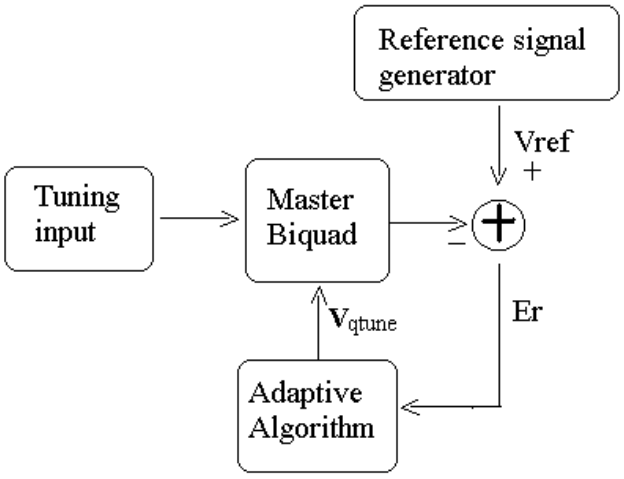


Fig. 4-8 The block diagram of adaptive Q tuning

A sequence of tuning input, preferably a pseudo random signal (pseudo white noise), is fed into the master biquad. The reference signal generator contains oscillators that generate the $V_{ref}$'s with frequencies of poles and zeros of the biquad with the proper gain factors. The difference $E_r$ of the $V_{ref}$'s and the biquad output will be passed to a circuit with the adaptive algorithm and then tune the coefficients of the biquad. The voltage is then the Q tuning voltage. This tuning scheme can accurately tune the response of a filter. But a pseudo white noise as a tuning signal is required. Also, the number of signal generators increases with the number of the poles and zeros of the filter. This requires a number of oscillators and thus consumes power. Also, the pseudo random signals and the reference signals from the oscillators increases the noise in the band.

### *4.3.5 Adaptive Q tuning with multiplier and MLL.*

There is a simplified adaptive version that can use only one sinusoidal or square wave as the tuning input. The block diagram is shown in Fig. 4-9.

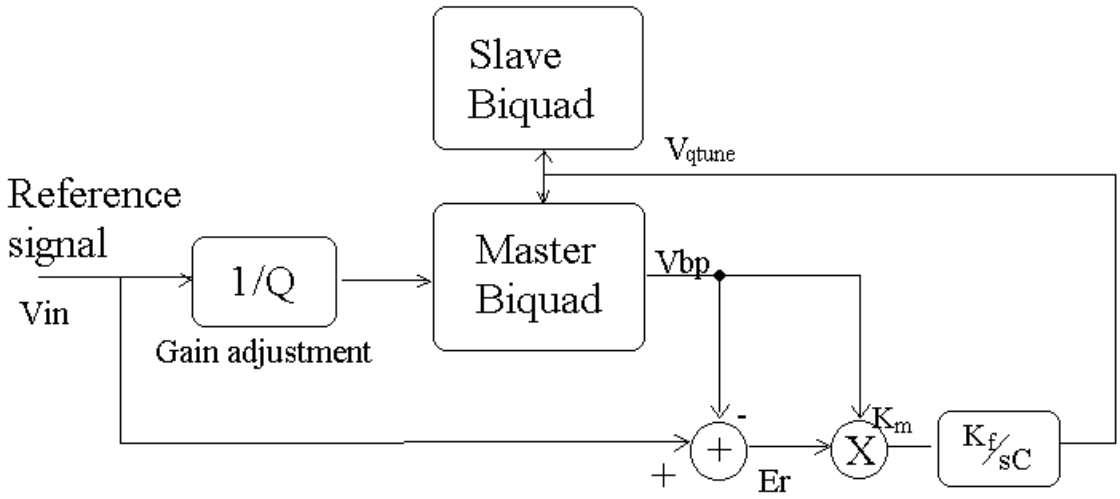


Fig. 4-9 The block diagram of the simplified adaptive Q tuning

The first part is the same as a MLL without the peak detectors. The residue $E_{r,}$ however, is not used to tune the Q directly, but is multiplied with the bandpass output $V_{bp}$ of the master biquad and then filtered by the lowpass filter to give $V_{qtune}$. If the filter function is H(s), then $V_{qtune}$ is related to $V_{in}$ and H(s) by [5]:

$$\frac{\partial V_{qtune}}{\partial t} = K_m K_f V_{bp}(V_{in} - V_{bp}) \tag{4-8}$$

where $K_m$ and $K_f$ are the gain of the multiplier and the integrator respectively and $V_{bp}$= $H(s)V_{in}$. Eq.(4-8) is a recursive relation and becomes zero when $E_r$=0. The $V_{bp}$ multiplied provides the gradient of tuning and is a good approximation of the adaptive tuning introduced in the last section [5]. This design has the immunity to the frequency variation. To understand this, the filter can be assumed to have a phase error $\Delta\phi$ due to the deviation of the $f_o$, and $V_{bp}=V_{in}\cos\Delta\phi$. From Eq. (4-8), the filter can still be tuned until the new $V_{bp}$, $V_{bp}$*, to be $V_{bp}/\cos\Delta\phi$. Then the tuning is complete with the desire Q but a deviated $f_o$.

To analyze the loop, Eq.(4-8) is rewritten in s-domain as:

$$V_{qtune} = \frac{K_m K_f V_{bp}(V_{in} - V_{bp})}{sC} \tag{4-9}$$

On the other hand, the bandpass output $V_{bp}$ also depends on the $V_{qtune}$ by Eq.(3-8):

$$V_{bp} = \frac{g_{m1}Q}{\omega_o C} = \frac{g_{m1}g_{m2,3}R_o}{\omega_o C} = (\frac{g_{m1}g_{m2,3}}{\omega_o C})(\frac{g_{m2,3}}{g_{o+} - \rho (V_{qtune} - V_t)}) \tag{4-10}$$

Finally, the loop dynamic of the $V_{bp}$ is obtained:

$$V_{bp} = (\frac{g_{m1}g_{m2,3}}{\omega_o C})(\frac{g_{m2,3}}{g_{o+} + \rho V_t - \frac{K_m K_f V_{bp}(V_{in} - V_{bp})}{sC}}) \tag{4-11}$$

A complete analysis of the stability of $V_{bp}$ is out of the scope of this thesis. Qualitatively speaking, if small variation of the Q is required, either the DC gains of the multiplier and of the integrator should be decreased or the capacitance C should be increased. However, by reducing $K_m$ and $K_f$, the capture range of the Q will be severely reduced. Therefore increasing C is the best method to stabilize the $V_{bp}$.

A comparison among the 4 types of automatic Q tuning is shown in Table 4-1.

| Method of Q tuning | Advantages | Disadvantages |
|---|---|---|
| Magnitude locked loop | 1.Simple and straight forward | 1. Over-tuning if $f_o$ deviates.<br>2. Error in tuning due to gain mismatch. |
| By comparing the step response | 1. Increased accuracy due to the use of low $\omega_o$ integrator for comparison. | 1. Hard to make accurate Envelope detector.<br>2. Also affected by $f_o$ deviation |
| Adaptive tuning with pseudo-random signal | 1. Very accurate | 1. Needs a lot of oscillator for higher order filters.<br>2. Requires a pseudo-random signal which provides wide-band noise. |
| Simplified adaptive tuning | 1. Simpler than adaptive tuning.<br>2. Needs only one tuning reference. | 1. Not as accurate as adaptive tuning.<br>2. Suitable for tuning a single biquad only. |

Table 4-1 Comparison among the 4 schemes of automatic Q tuning

## References


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2. Behzad Razavi, "*RF Microelectronics*",pp.14-22, Prentice-Hall Inc., 1998.
3. D.A.Johns, K.Martin, "Analog Integrated Circuit Design*",* Ch.16, John Wiley & Sons Inc., 1997.
4. K.A.Kozma, D.A. Johns, A.S. Sedra, "An Approach for Tuning High-Q Continuous-Time Bandpass filters, *" IEEE JSSC*, pp.1037-1040, 1995.
5. J.M. Stevenson, E.S. Sinencio, "An Accurate Quality Factor Tuning Scheme for IF and High-Q Continuous-Time Filters", *IEEE ISSCC Feb 1998* : Analog, Sensor, and Communcation Circuits.

# Chapter 5 First design of filter

## 5.1 Introduction

This chapter presents the deisgn of a 6th order filter constructed with a cascade of 3 biquad stages as shown in Fig. 5-1.

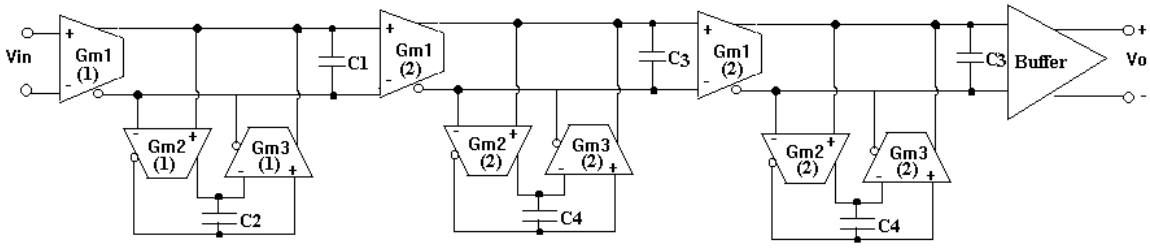



Fig. 5-1 The architecture of the whole filter

The unbalanced $g_m$ cells are chosen due to their wide linear range and high power efficiency as shown in Table 2-2**.** On the other hand, the input $g_m$ cell $G_{m1}$ is required to be linear. Meanwhile, the $g_m$ required is small (< 0.5 mA/V) as the output impedance is above 15 KΩ and a gain of <15dB is required. Therefore the cross-coupled $g_m$ cells are employed for such purpose for its high efficiency of power to linearity as shown in Table 2-2.

The supply voltage is 3 V. The process fabricated is 0.8 μm HP process. Since the purpose of the first design was to investigate the relationship among linearity, noise and power of a filter, automatic tuning was not included.

## 5.2 Design and linearity of the $g_m$-cell

### *5.2.1 The input $g_m$-cell*

Cross-coupled $g_m$ cell is employed for the input $g_m$-cell for their high linearity which is suitable for the requirement of the input $g_m$ cell. The design is just the same as the one discussed in section 2.4.2. The schematic is shown in Fig. 5-2 and the sizes of the transistors are shown in Table 5-1.

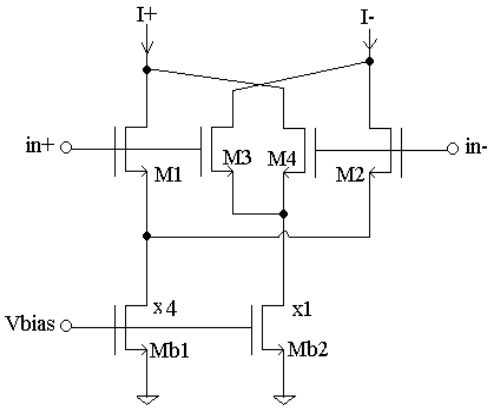



Fig. 5-2 Schematic of the cross-coupled $g_m$ cell

| | Stage1 | Stages 2 and 3 |
|---|---|---|
| $M_1$, $M_2$ | 6.8 μm/2 μm x 3 | 7.6 μm/4 μm x 1 |
| $M_3$, $M_4$ | 3.6 μm/2 μm x 3 | 4 μm/4 μm x 1 |
| $M_{b1}$ | 9 μm/0.8 μm x 12 | 8 μm/0.8 μm x 4 |
| $M_{b2}$ | 9 μm/0.8 μm x 3 | 8 μm/0.8 μm x 1 |

Table 5-1 Sizes of the input $g_m$ cells of all stages

The bias current ratio between $M_{1,2}$ and $M_{3,4}$ is 4. The transistor size ratio between them, however, is not $4^{1/3}$. This is because there are effects of mobility degradation that requires larger $M_3$ and $M_4$ to compensate for. The ratio between the effective $g_m$ of the $g_m$ cell and $g_{m1,2}$ is 0.603 as given in Eq.(2-22). The linear range obtained is about ± 420 mV.

### *5.2.2 The unbalanced $g_m$ cells for the gyrator*

Unbalanced $g_m$ cell is employed for its good power efficiency towards noise and linearity. The schematic is shown in Fig. 5-3 and the sizes of the transistors are shown in Table 5-2.

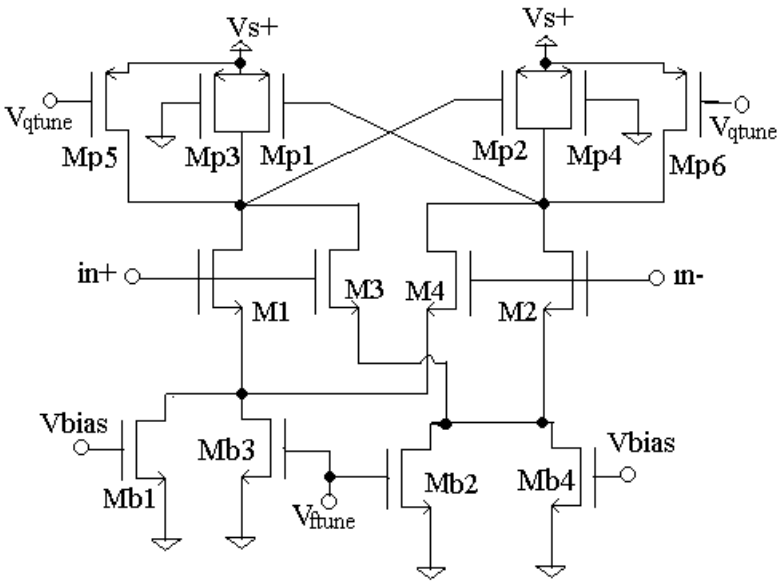



Fig. 5-3 The schematic of the unbalanced $g_m$ cell for the gyrators

| | Stage 1 | Stages 2 and 3 |
|---|---|---|
| $M_1$, $M_2$ | 62 μm/1.2 μm x 65 | 30 μm/1 μm x 14 |
| $M_3$, $M_4$ | 29.6 μm/1.6 μm x 30 | 21.6 μm/2 μm x 10 |
| $M_{b1,}M_{b2}$ | 40 μm/2 μm x 36 | 40 μm/2 μm x 6 |
| $M_{b3,}M_{b4}$ | 16.2 μm/2 μm x 8 | 16 μm/2 μm x 3 |
| $M_{p1}$,$M_{p2}$ | 29.2 μm/2 μm x 11 | 29.2 μm/2 μm x 7 |
| $M_{p3}$,$M_{p4}$ | 28 μm/2 μm x 4 | 6.8 μm/2 μm x 4 |
| $M_{p5}$,$M_{p6}$ | 6.8 μm/2 μm x2 | 7.2 μm/2 μm x1 |

Table 5-2 Sizes of transistors of the gyrators of all stages

The offset of each differential pair is 300 mV. The resultant linear range is ± 200 mV. The ratio of the sizes of $M_{1,2}$ to $M_{3,4}$ is about 6 for stage 1 and about 3.9 for stages 2 and 3. The reason why both stages attain the same linear range with different size ratios is that the gate length chosen are different. Different gate lengths have the difference in mobility, saturation velocities, and other second-order effects. The difference causes different offset voltages to achieve the same flat $g_m$ response.

The bias transistors are divided into two groups, namely $M_{b1,2}$ and $M_{b3,4.}$ The bias of $M_{b1,2}$ is for coarse frequency tuning while that of $M_{b3,4}$ is for fine tuning.

The active loading $M_{P1}$ and $M_{P2}$ are designed with the gates cross-connected to form a negative impedance cell. The advantage is the utilization of the drain current of $M_1$ and $M_2$ to provide the $-g_m$. No extra power is required. This is essential for low power designs due to the effective use of the bias current for the $g_m$ cells of the gyrator. The voltage drop across the loading will be too much to cut off $M_1$ and $M_2$ if only $M_{P1}$ and $M_{P2}$ are used as the loading unless $M_{P1}$ and $M_{P2}$ are made very large (W/L > 1000). The capacitance loading will cause the gyrator to have $f_o$ even lower than 70 MHz. Therefore, in order to better control the $V_{gs}$ of $M_{P1}$ and $M_{P2}$, a pair of triode-mode transistors $M_{P3}$ and $M_{P4}$ are connected in parallel to limit the $V_{gs}$ of $M_{P1}$ and $M_{P2}$ to be within 1.2 V. $M_{P3}$ and $M_{P4}$ also compensate the excess negative impedance of $M_{P1}$ and $M_{P2}$ to prevent over-compensation of the output impedance. $M_{P5}$ and $M_{P6}$ are connected in parallel with $M_{P3}$ and $M_{P4}$ and are controlled by the Q tuning voltage to vary the resultant output impedance so as to control the Q. For fine tuning of the Q, $M_{P5}$ and $M_{P6}$ are made much smaller than $M_{P3}$ and $M_{P4}$.

## 5.3 The architecture of a biquad

The schematic and the corresponding block diagram of a biquad stage is shown in Fig. 5-4. Three biquads are cascaded together to form a 6th-order bandpass filter.

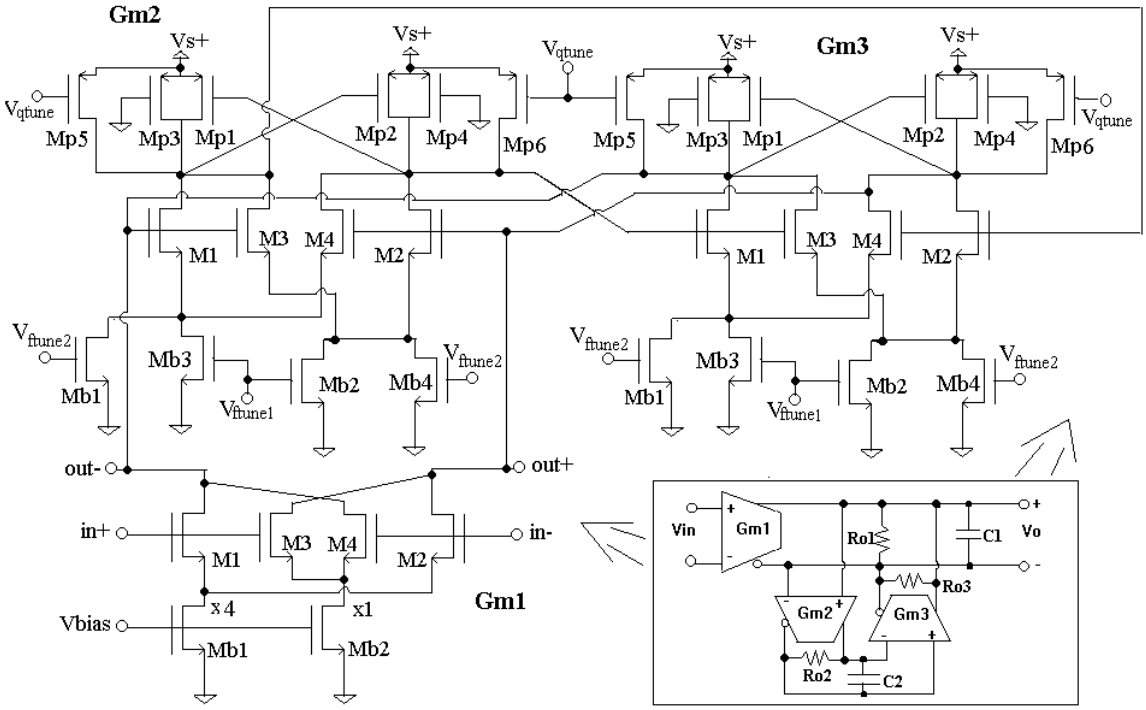



Fig. 5-4 The schematic of a biquad stage of this filter

The drain current of $G_{m1}$ is supplied by the loading of $G_{m3}$. The $g_m$ of the $G_{m1}$ of the 1st stage is designed to be about 18 times larger than that of the other 2 stages. About 13.5 dB of gain is distributed to the first stage. The reason why not all the gains are assigned to the front end of the filter is that the effect of filtering has been taken into account. The first stage should have a suppression of about 15 dB and 25 dB respectively for the 70.8 MHz and 71.6 MHz interferes. Thus less intermodulation happens for the 2nd and the 3rd stages than the 1st stage even with larger signal amplitude. Owing to this reason, the 1st stage dominates the linearity and noise performance. The gyrators of the 2nd and the 3rd stages can be made smaller with the same noise performance. On the other hand, their linearity performance is not affected much though the signal is larger there. Then more supply power can be assigned to improve the 1st stage by increasing its size so that the noise and linearity performance of the whole filter can be improved. For this filter, the

size of the 1st stage is about 6 times of that of each other 2 stages. About 75% of power is allocated for the 1st stage and 12.5% is assigned for each of the latter 2 stages. By doing so, with the same noise performance, $IIP_3$ can be improved by about 3.5 dB.

Besides the above 3 stages, there are 2 stages of output buffers after the 3rd biquad stage. The first buffer stage has the same size as the $g_{m1}$ of the 3rd stage to ensure the same capacitance loading as the 2nd stage. However, the loss will be about 8dB if only the output of the first buffer is connected directly to the output pad. The second stage is a source follower such that it has a gain of –2 dB with a 0.5 pF loading which is more than enough for driving an output pad (<0.2 pF).

The loading capacitor required for the 1st stage is 15 pF while that for the 2nd and 3rd stages are both 2 pF. Parallel-plate capacitors using the metal and the ploysilicon layers will consume too much area for such capacitance. Because the 0.8 μm HP process has no linear capacitor option, MOS gate capacitors in saturation mode have to be used to provide the capacitance with a smaller area. The total capacitance per $\mu m^2$ for metal and polysilicon plates including parasitic capacitance to ground is 0.16 fF while that for a MOS capacitor is about 2.2 fF. However, a MOS capacitor must be grounded and biased well above its $V_t$, say 1.5 V, for operation in saturation mode throughout the signal swing. Compared to a floating capacitor, the total equivalent grounded capacitance required is 4 times as shown in Fig. 6-6.

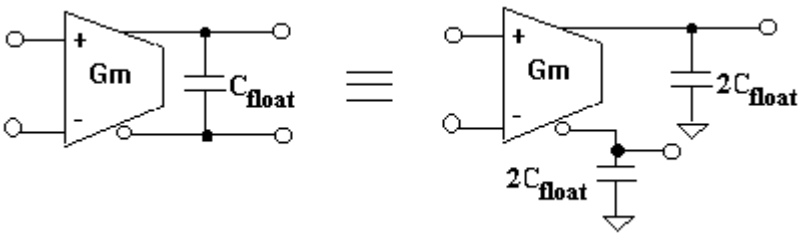



Fig. 5-5 The equivalence of grounded capacitance and floating capacitance

Therefore the capacitance density for a MOS floating capacitor is 2.2 $fF\mu m^{-2}/4$ = 0.55 $fF\mu m^{-2}$. Even so, 71% of the area is saved by using MOS capacitors when compared to metal parallel-plate capacitors.

The use of MOS capacitors, however, has the problem of variation of capacitance due to process variation of dimension and doping. The variation due to dimension and $V_t$ error can be up to 30% according to the previous chapter. Therefore the filter is required to be tunable for a frequency range of more than 40 MHz.

## 5.4 Noise of the filter

The derivation of the noise of a biquad in Chapter 3 can be used to calculate the noise of the filter within a bandwidth of 180 KHz. Firstly, the noise of the $g_m$ cells has to be found. The noise sources of the $G_{m1}$ and the $G_{m2,3}$ are shown in Fig. 5-6 and Fig. 5-7 respectively.

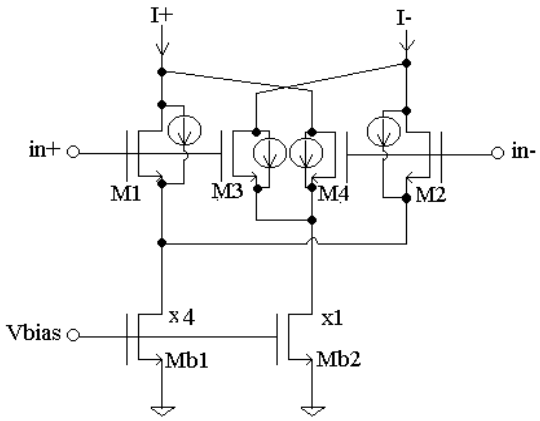



Fig. 5-6 Noise sources of the input $g_m$ cell

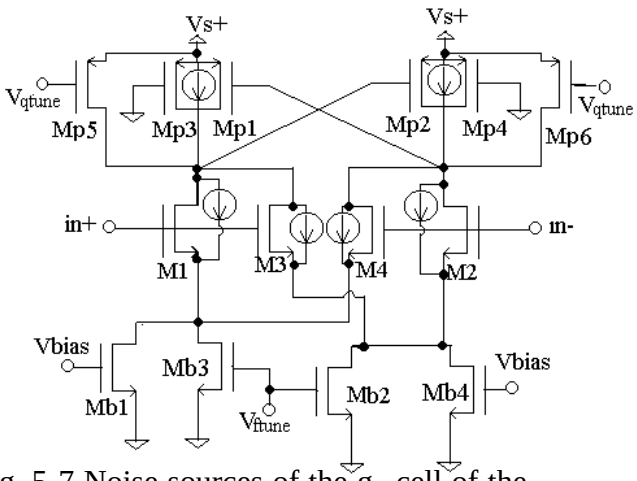



Fig. 5-7 Noise sources of the $g_m$ cell of the gyrator

For the input $g_m$ cell $G_{m1}$, the noise comes mainly from $M_1$-$M_4$. Table 5-3 lists out the $g_m$ of those transistors of each stage and the corresponding noise of the $G_{m1}$ of each stage.

| Transistor | $g_m$ | Noise of each $G_{m1}$ ( bandwith =180 KHz) |
|---|---|---|
| $M_1$-$M_2$ of $G_{m1}$ of stage 1 | 600μA/V | $3.07\text{x}10^{-18}A^2$ |
| $M_3$-$M_4$ of $G_{m1}$ of stage 1 | 100μA/V | |
| $M_1$-$M_2$ of $G_{m1}$ of stages 2&3 | 63μA/V | $3.91\text{x}10^{-19}A^2$ |
| $M_3$-$M_4$ of $G_{m1}$ of stages 2&3 | 36.0μA/V | |

Table 5-3 The $g_m$ of each noise source and the corresponding noise of the $G_{m1}$ of each stage

On the other hand, the noise sources of $G_{m2}$ and $G_{m3}$ of each stage include not only $M_1$-$M_4$ but also the active loading $M_{P1}$-$M_{P6}$. Table 5-4 shows the $g_m$ of each transistor and the corresponding $R_o$ and noise of the $G_{m2}$ and $G_{m3}$ of each stage.

| | $G_{m2,3}$ of 1st stage | $G_{m2,3}$ of stages 2&3 |
|---|---|---|
| $g_m$ of $M_1$, $M_2$ | 43.6mA/V | 7.12mA/V |
| $g_m$ of $M_3$, $M_4$ | 5.67mA/V | 1.03mA/V |
| $g_m$ of $M_{P1}$, $M_{P2}$ | 3.02mA/V | 803μA/V |
| $g_m$ of $M_{P3}$, $M_{P4}$ | 1.81mA/V | 293μA/V |
| $g_m$ of $M_{P5}$, $M_{P6}$ | 224μA/V | 84.3μA/V |
| $R_o$ of the biquad | 18.6KΩ | 127KΩ |
| Output $V_n^2$ of the gyrator ( bandwith =180 KHz) | $1.86x10^{-8}V^2$ | $1.49x10^{-7}V^2$ |
| Output $V_n^2$ of the biquad ( bandwith =180 KHz) | $1.92x10^{-8}V^2$ | $1.55x10^{-7}V^2$ |

Table 5-4 The $g_m$ of each transistor and the corresponding $R_o$ and noise of each $G_{m2}$ and $G_{m3}$ of each stage

The output noise power of the biquads of a bandwidth of 180 KHz is calculated by Eqs. (3-27) and (3-28). The corresponding output noise voltage of stage 1 is then 195 μV and that of stages 2 and 3 is 476 μV. The gain of stage 1 is 4.65 while that of the latter two stages is 1.71. By this gain distribution among the 3 biquads the total equivalent input noise at the output is equal to 82 μV or 193 nV/√Hz.

## 5.5 Layout of the filter

### *5.5.1 The floorplan*

The floorplan of the filter is shown in Fig. 5-8.

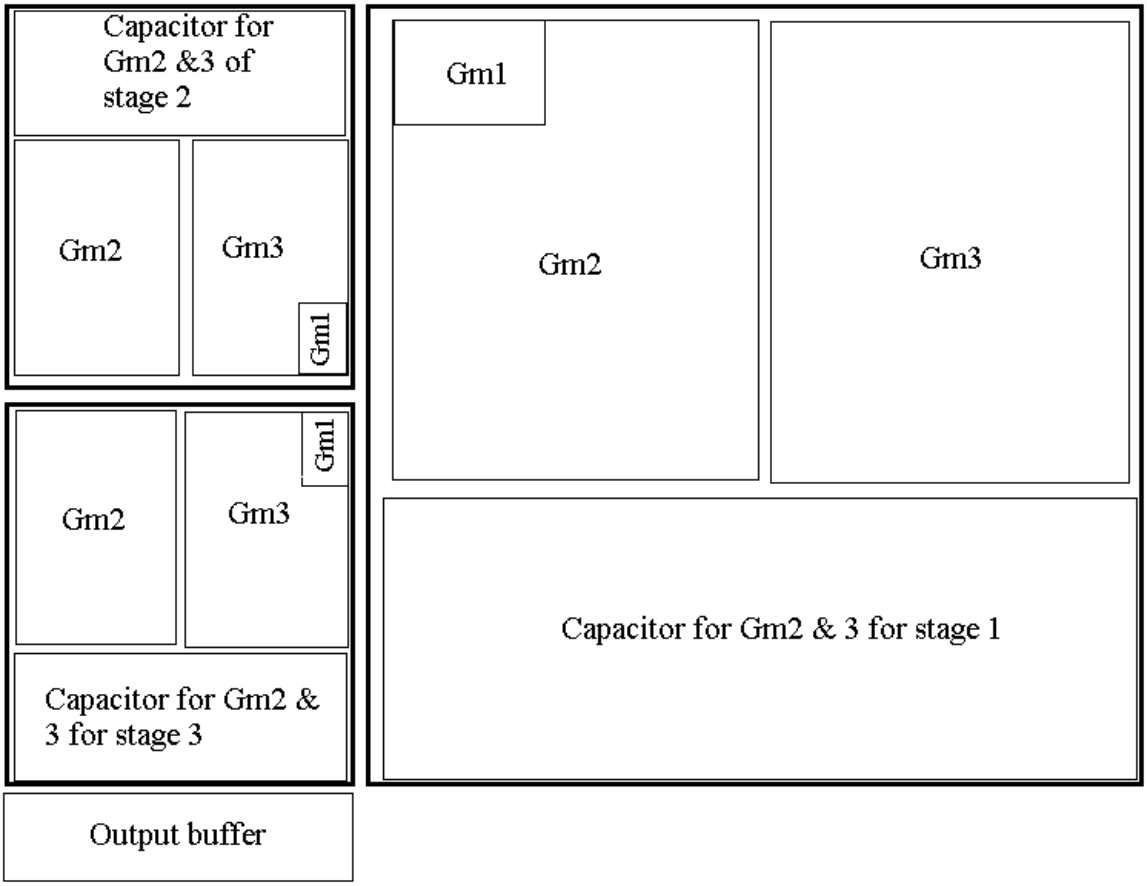



Fig. 5-8 Floorplan of the filter layout

The basic unit is the whole stage. For good matching among the $G_{m2}$ and $G_{m3}$, they are put close together. The 2nd and 3rd stages are put head-to head such that the $G_{m2}$ and $G_{m3}$ of both stages can be put closer together for better matching. The capacitors among the three stages, however, are then far from each other. This is unavoidable because the path from the $g_m$ cells to the capacitors needs to be kept short. Since matching among $g_m$ cells is harder than matching among the capacitors, the capacitors matching is sacrificed.

### *5.5.2 The capacitors*

The capacitors of the $G_{m2}$ and $G_{m3}$ of each stage, are interleaved for good matching. As mentioned above, all capacitors are grounded ones. Therefore totally there are four capacitors to be interleaved. The layout of a pair of 2 pF capacitors for the stages 2 and 3 is shown in Fig. 5-9.

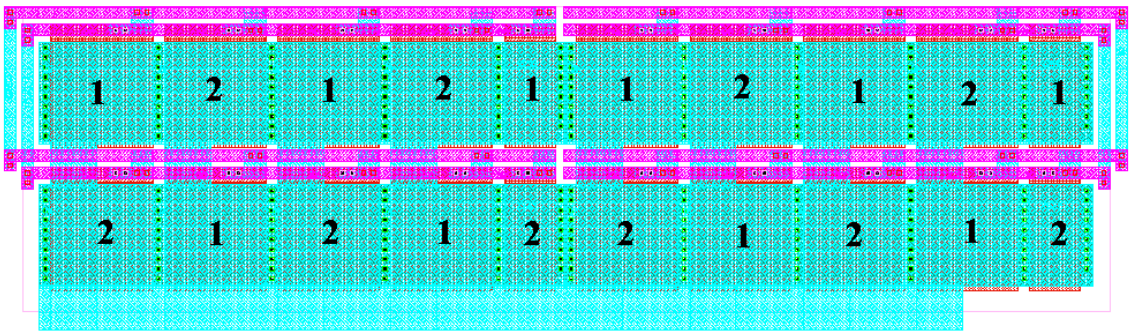



Fig. 5-9 The layout of a pair of 2pF capacitor

The capacitor contains four 4 pF grounded capacitors. Each unit capacitor is about 0.9 pF. The remaining capacitance is compensated by a rectangular-shaped capacitor whose value is determined after the consideration of all other parasitic capacitance. The 15 pF loading capacitor of the 1st stage is also constructed in a similar way with altogether 64 unit capacitors. The capacitance of each unit capacitor is about 1.8 pF. The parallel-plate capacitance between the metal and the polysilicon layers is not utilized because they are too small when compared to the MOS capacitors. On the other hand, eliminating these parallel-plate capacitors can free more layers for interconnections among the unit capacitors. The dimension of the 2 pF capcitor is 220 μm by 67 μm while that of the 15 pF capacitor is 0.55 mm by 0.17 mm.

### *5.5.3 The complete layout of the filter*

The complete layout of the filter is shown in Fig. 5-10.

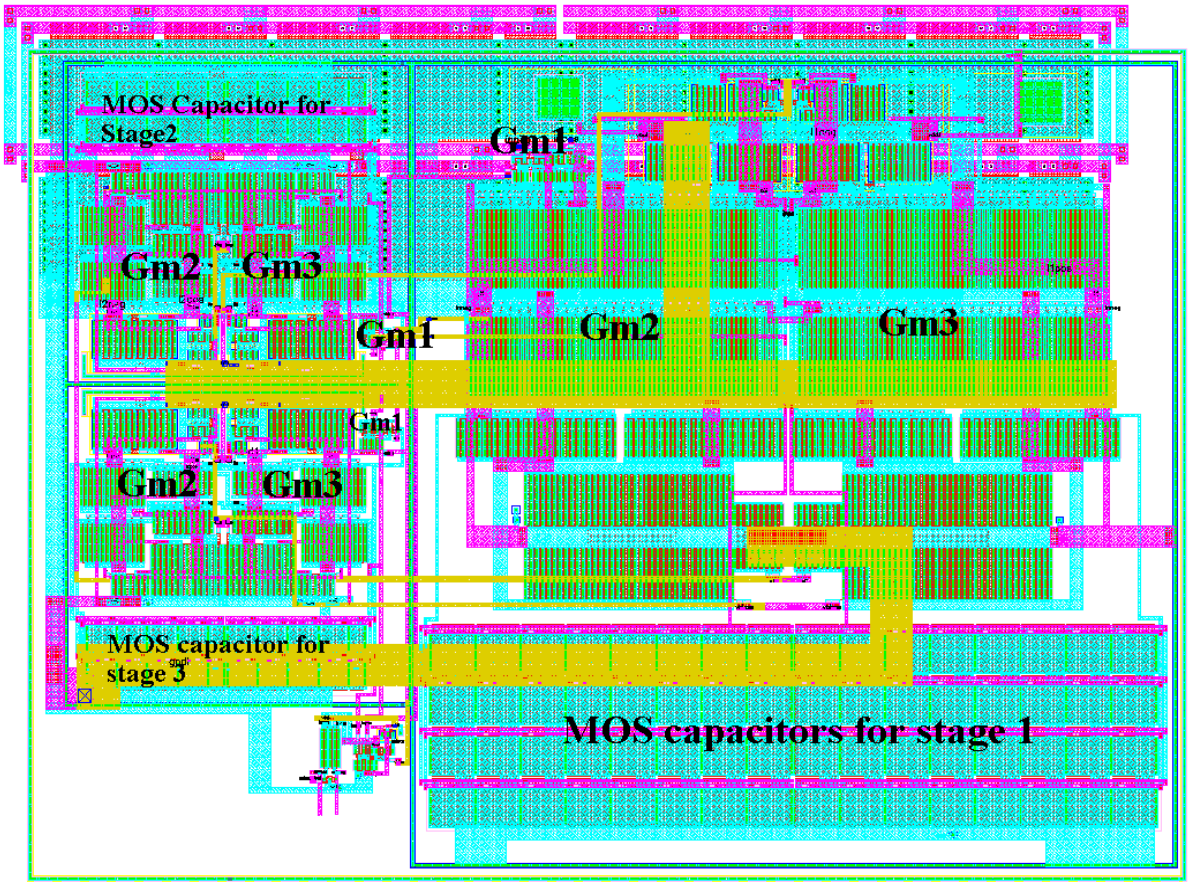



Fig. 5-10 The complete layout of the whole filter

The core dimension of the whole filter is 0.88 mm by 0.65 mm . About 21% of the area is used for the capacitors. Nearly 30% of the loading capacitance comes from the parasitics of the $g_m$ cells themselves. Extra care has to be put on the width of the main power line. The filter consumes about 80 mW of power. It means a current of about 27 mA for a 3 V supply. The metal layers can bear a current of 1 mA per μm width. For safety, 100% more width is allocated for secured connection. Therefore the width of the power line and the ground is about 55 μm.

## 5.6 Simulation results and discussions

The filter can be tuned from 40 MHz to 110 MHz to accommodate the process variation. The Q of the filter also varies with the $f_o$ because the output impedance compensation depends on the drain current of $G_{m2}$ and $G_{m3}$. This limits the frequency tuning range to be from 55 MHz to 85 MHz so that the same Q can still be restored by the Q tuning.

For the noise of the filter, HSpice simulation shows an equivalent input noise of 80 μV or 189 nV/√Hz which is close to the calculated result. The calculation overestimates the output noise power because of the assumption of the brick-wall transfer function of the bandpass filter. The plot of the $IIP_3$ and the 1-dB compression point is shown in Fig. 5-11

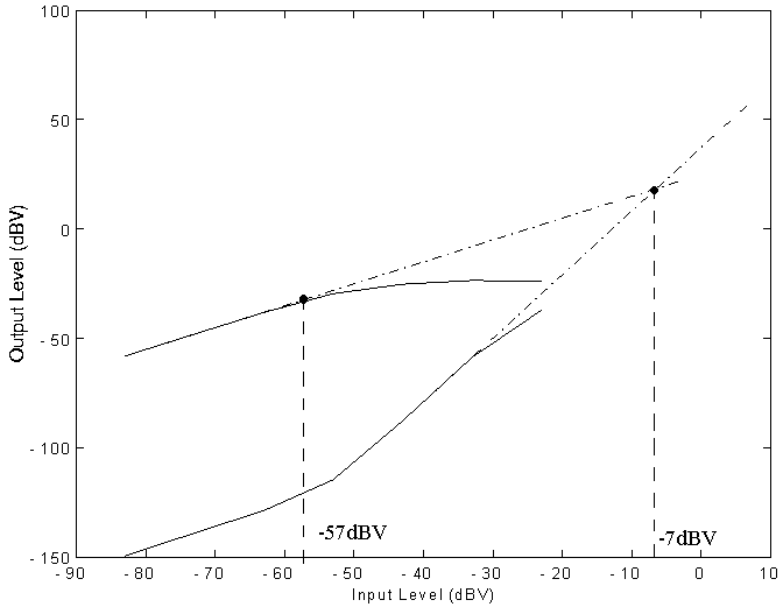



Fig. 5-11 The plot of the $IIP_3$ and the 1-dB compression point of the filter

.

For the $IIP_3$ of the filter, two tones of interference, namely 70.8 MHz and 71.6 MHz, of the same amplitude are injected and the 70 MHz intermodulation product is observed. The $IIP_3$ of the filter is –7 dBV or +6 dBm and the 1-dB compression point is –57 dBV or –44 dBm. The large difference between the 1-dB compression point and the $IIP_3$ is due to the filtering effect of the biquads. The filter should have been saturated when input amplitude > –57 dBV. But the intermodulation is not significant yet because the interferers are suppressed by the biquad stages. For GSM receivers channel intermodulation is more serious than gain mismatch. So the focus of linearity is still put on the $IIP_3$ rather than the 1-dB compression point. The small 1-dB compression point actually helps because it enhances the automatic gain control (AGC) of the receiver.

A summary of the simulation results is listed in Table 5-5.

| | |
|---|---|
| $F_o$ | 70 MHz |
| Q | 390 |
| No. of orders | 6 |
| Gain | 23 dB |
| Noise | 189 nV/√Hz |
| Linearity $IIP_3$ | +6 dBm |
| Dynamic Range | 74 dB |
| Power consumption | 82 mW |
| Voltage | 3 V |
| Process | 0.8 μm HP |
| Chip area | 0.88 x 0.65 $mm^2$ |

Table 5-5 Summary of the simulation results of the filter

## 5.7 Measurements

### *5.7.1 The testing setup*

The following items are to be measured for the performance of the filter:

1. The center frequency $f_o$ and the tuning voltage required to keep this $f_o$.
2. The nominal Q at $f_o$ and the tuning voltage required to keep this Q.
3. The $IIP_3$ of the filter.
4. The noise of the filter.

To measure the $f_o$ and the Q, a network analyzer is needed. On the other hand, to measure the $IIP_3$ of the filter, two signal sources and a spectrum analyzer are needed. The two signal sources generate 70.8 MHz and 71.6 MHz interferes and then the intermodulation product at 70 MHz is observed in the spectrum analyzer. The whole setup is shown in Fig. 5-12.

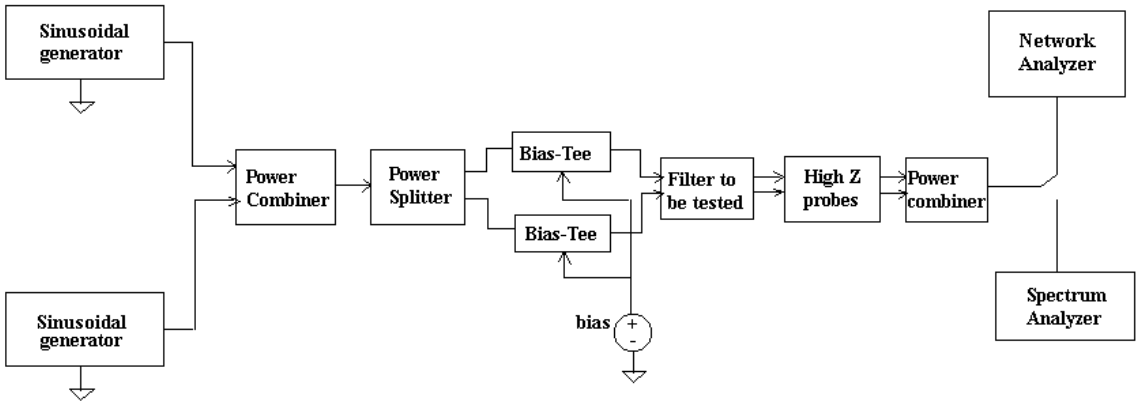



Fig. 5-12 The setup for the measurement of the filter

At the input, a power combiner followed with a power splitter is required for fully balanced input to the filter. The input bias is fed to the filter via a pair of bias-tees. The output of the filter is probed with a pair of high-impedance probes followed with a power combiner. High-impedance probes are required because the output of the filter is not 50Ω matched. If the output is probed with a high-speed probe instead, the input impedance of the digital scope or the spectrum analyzer will cause a severe lowering of the output, making it undetectable.

For the noise measurement of the filter, noise figure meter is required. Another method is by observing the jump of the noise level in the spectrum analyzer after the connection of the filter output. This is a rather coarse approximation but is suitable if the noise is too large to be measured by the noise figure meter.

### *5.7.2 The measurement results*

The first stage has a Q value below 2 even the Q tuning voltage is tuned to the highest value and the frequency tuning voltage is tuned up. On the other hand, the center frequency of the 2$^{nd}$ and 3$^{rd}$ stages has shifted to 95.2 MHz with a high Q of above 150. In order to study the filter with a reasonably high Q (>150). Only the latter two stages are measured. The plot of the combined frequency response of the stages 2 and 3 is shown in Fig. 5-13.

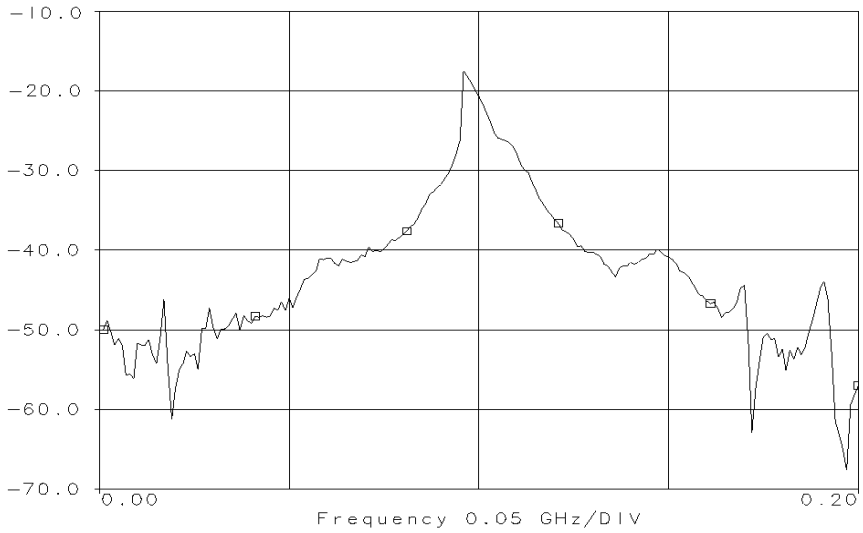



Fig. 5-13 The measured frequency response of stages 2 amd 3

The plot is swept from 30 KHz to 200 MHz. The Q that can be kept stable to be observed on the network analyzer is about 190. Although the filter can be tuned back to 70 MHz, because of the correlation between the frequency and the Q tuning, the Q of the filter is only 2.5 at 70 MHz. The variation of $f_o$ is up to 36% which is out of expectation. The main reasons of the deviation include the $g_m$ variation due to variation of transistor parameters, variation of MOS capacitance and resistance of the induced channel of MOS capacitors. There were no testing structures of the MOS capacitors to verify the capacitance. Only the $g_m$ of the input $g_m$ cells could be measured by measuring its voltage gain with the gyrators turned off. The measured and simulated results are listed together in Table 5-6.

| | Measured | Simulated |
|---|---|---|
| $G_{m1}$ of Stage 1 | 240 μA/V | 250μA/V |
| $G_{m1}$ of Stages 2 & 3 | 12.5μA/V | 13.5μA/V |

Table 5-6 The measured and simulated $g_m$ of the $G_{m1}$ of all stages

The measured $g_m$ drops by 4-6% from the simulated ones. Other transistors in the same chip could be considered to have the similar deviation. The loading capacitance then accounts for the remaining 36%+6% = 42% of variation. Even if the loading capacitance has got its maximum dimension error, it only accounts for 10% of $f_o$ variation. What remains is the effect of the resistance in MOS capacitors. More detailed discussion of the effects of the resistance in capacitors will be delivered in Chapter 7.

The output of the two stages is probed with high impedance probes, which have a loss of 26 dB. Therefore the peak gain of the two stages is 8 dB. This is lower than the simulated gain of the 2 stages (9.3 dB). The reason is due to the deviation of the Q of the two stages and the gain error of the input $g_m$ cell of each stage.

The noise figure of the filter is large (expected 46 dB). 26 dB more is added due to the loss of the high impedance probes. As a result, the noise figure meter overflows even external LNA is inserted to increase the capability of the noise figure meter. Instead, spectrum analyzer is used. Only the noise of the latter two stages is tested. The noise floor with a resolution bandwidth of 3 KHz is about –95 dBm. This corresponds to an output noise power of about 20 nW for 200 KHz bandwidth or an equivalent input noise voltage of 413 μV or 923 nV/√Hz. This corresponds to a noise figure of 43 dB. The measured input equivalent noise voltage is larger than the expected voltage 322 μV because the gain of the two stages is only 8 dB and also there is error of reading on the spectrum analyzer.

The measurements of 1-dB compression point and the input $IIP_3$ are shown in the plot of Fig. 5-14.

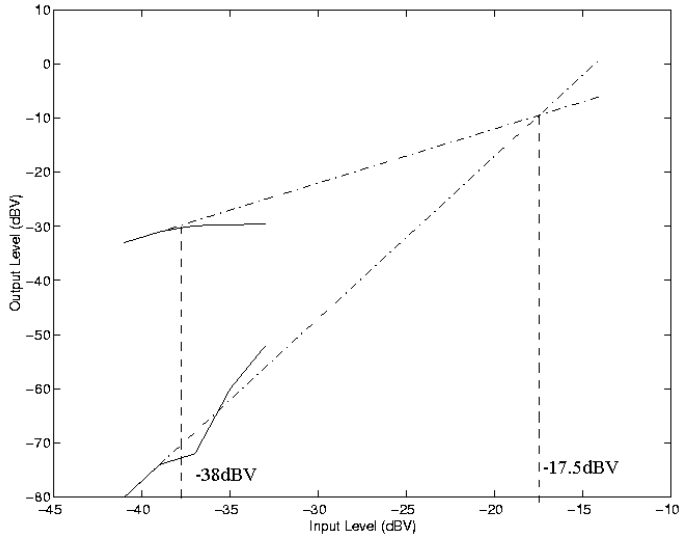



Fig. 5-14 The measured $IIP_3$ of stages 2 and 3.

The measured input $IIP_3$ is –17.5 dBV or equivalently –4.5 dBm which is 10.5 dB lower than the simulated result. The reason is that for the design the first stage of the filter should have an attenuation of 15 dB and 25 dB respectively for the 70.8 MHz and 71.6 MHz interferers. With a simulated gain of 13.5 dB of the first stage, the suppression of the interferers should be respectively –1.5 dB and –11.5 dB. Now the signal is injected directly into the 2nd stage. Thus the $IIP_3$ should drop by at most 13 dB. The mismatch among the transistors in the unbalanced cell is considered as the main reason. This causes the cancellation the higher order harmonics, especially the even-order ones, incomplete.

The 1-dB compression point appears at –38 dBV which is 19 dB higher than the simulation result. The reason is that the signal gain before the 2nd stage and the 3rd stage

reduces from 13.5 dB and 18.2 dB respectively to 0 dB and 4 dB respectively.

To conclude, the 2nd and 3rd stages of the filter can function as a high Q filter at a shifted $f_o$ of 92.5 MHz. The noise and the linearity are within expectation. The reason of the malfunctioning of the filter comes from the process variation of capacitance and $g_m$ which can cause a variation of 30% as discussed in Chapter 3. The series resistance of the capacitors is suspected to be another main reason. A summary of the measured performance of the 2 stages is given in Table 5-7.

| | |
|---|---|
| $F_o$ | 92.5 MHz |
| Q | 190 |
| No. of orders | 4 |
| Gain | 8 dB |
| Noise | 923 nV/√Hz |
| Linearity $IIP_3$ | –4.5 dBm |
| Dynamic Range | 51 dB |
| Power consumption | 21 mW |
| Voltage | 3 V |
| Process | 0.8 μm HP |
| Chip area | 0.88 x 0.65 $mm^2$ |

Table 5-7 Summary of the measurement results of the stages 2 and 3.

The chip photo is shown in Appendix of this thesis.

# Chapter 6 Final design of filter with automatic tuning

## 6.1 Introduction

Another design of the filter is implemented. The structure is still a 3-stage 6-th order biquadratic bandpass filter as shown in Fig. 5-1, but another design of the $g_m$ cell is employed. The most important reason for not using the structure of an unbalanced $g_m$ cell is that the circuit is too difficult to be optimized.

For this filter, the design of $g_m$ cells shown in Fig. 2-15 is employed with some modifications which will be introduced later. Although the design of Fig. 2-13 has the highest power efficiency of both $g_m$ and linearity, it requires at least 3 V to operate. It is then not suitable for the purpose of 2.5 V supply or lower.

This biquad can operate at a supply voltage of 2.5 V. That means for the same power consumption the supplied bias current can be increased by 20%. Moreover, master-slave automatic tuning of frequency and Q are included in this filter to make it practical. In order to provide better matching among the 3 stages of biquads and the master biquads of both tuning loops, the idea of using generic $g_m$ cell is implemented.

## 6.2 Design and linearity of the $G_m$-Cell

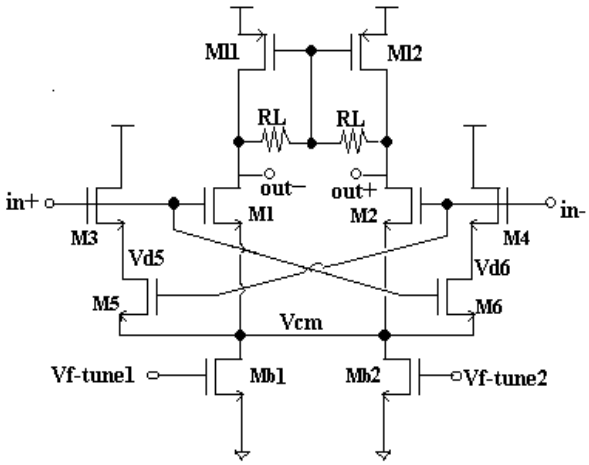



Fig. 6-1 The schematic of the $g_m$ cell for this filter

Fig. 6-1 shows the schematic of the $g_m$ cell used in the gyrator of filter. The $g_m$ cell has the same structure as the one shown in Fig. 2-15. However, the sizes of $M_3$-$M_6$ are not matched as suggested in paper [1]. As mentioned in Section 2.4.4, the $V_{ds}$ of $M_5$ and $M_6$ are too small such that the linear range of the structure cannot be fully utilized. Therefore instead of choosing $K_{5,6} = K_{3,4}$, we assign $K_{3,4}= C\ K_{5,6}$. The detailed calculation for the relation of $K_{1,2}$ and $K_{3,4}$ is presented in Appendix 6.1. Here the necessary relationship between $K_{1,2}$ and $K_{3,4}$ is listed out:

$$K_{1,2} = \frac{K_{3,4}}{2(1+C)^2}(4\sqrt{1+C}+3C-5) \tag{6-1}$$

Note that when C=1, Eq. (6-1) will be equal to Eq. (2-34). Eq. (6-1) is a more general relationship.

In general, the larger the C, the higher the $V_{ds5}$ and $V_{ds6.}$ However, there is restriction for the value of C. It can be understood by first looking at the voltage of each node. As the $g_m$ cell is connected back-to-back to another one to form a gyrator, the input bias is the same as the output bias of the other. Because there is a drop of about 1 V by the active loading, the gate bias at in+ and in- is then about 1.5 V for a supply voltage of 2.5 V.

If $V_{gs}$-$V_t$ of $M_3$ and $M_4$ is designed to be 0.2 V, then the following relationship comes out:

(6-2)

$$1.3 - V_{To} - \gamma(\sqrt{\phi_B + V_1} - \sqrt{\phi_B}) = V_1$$

The relationship is the body effect due to $V_{d5,6}$. All the symbols have the same meaning as those given in Eqs. (2-7) and (2-8). From the MOSIS parameters of 0.5 μm HP process, $V_{To}$ = 0.6684 V, $\varphi_B \approx$ 0.41 V, $\gamma$ = 0.54. Then $V_{d5,6}$ can be readily solved to be approximately 0.5 V. With $V_b$ = 0.35 V, $V_{ds5.6}$ = 0.15 V. $V_b$ have to be at least 0.3 V to prevent $M_b$ from going into the triode region due to the process variation. The CMRR of the $g_m$ cell will drop if the bias transistor $M_b$ is in the triode region and as a result the common-mode stability of the gyrator will be ruined. The other limitation of C is that the size of $M_3$ and $M_4$ would increase dramatically with C. Too large $M_3$ and $M_4$ would impose too much parasitic capacitance loading to the gyrator and thus affect the tuning range of the center frequency and the Q of the filter. Therefore C is chosen to be 2. The variation of $g_m$ to the input voltage is shown in Fig. 6-2.

It may be noticed that the linear range is not extended too much. This is due to the body effect of $M_3$ and $M_4$ which depends on $V_{ds5,6}$ and $V_b$ which limits $V_{ds5}$ and $V_{ds6}$. Also, there is a serious effect of mobility degradation, as discussed in Section 2.2.3, that causes the compensation by active biasing not effective for an input voltage higher than 200 mV.

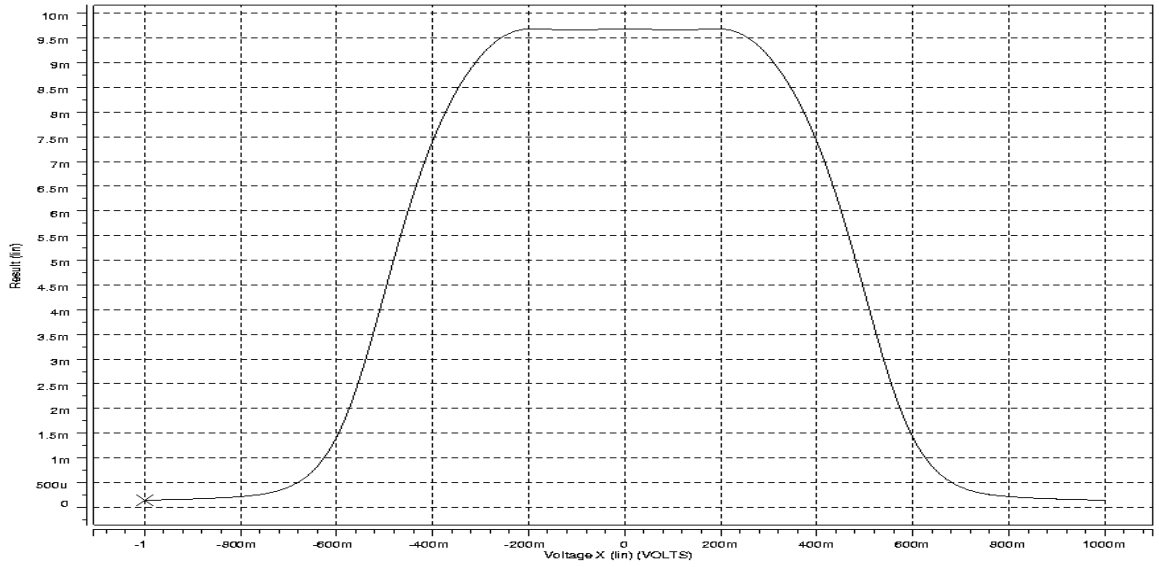



Fig. 6-2 The $g_m$ variation with the input voltage of the $g_m$ cell design in Fig. 6-1

The loading for the $g_m$ cells of the gyrator is a differential active load (DAL) [2]. The gates of $M_{l1}$ and $M_{l2}$ sense the mid-point of the differential voltage, which is a virtual ground. Therefore only common-mode current flows through $M_{11}$ and $M_{12}$. On the other hand, the differential current flows through the loading resistors $R_{L.}$ Therefore the output impedance depends on the value of $R_L$ only. Theoretically speaking, in order to reduce the common-mode gain, the impedance of $M_{l1}$ and $M_{l2}$ should be as small as possible. But that is not the case. No differential current will flow in $M_{l1}$ and $M_{l2}$ only when both the 2 loading resistors $R_L$ are matched and also $M_{l1}$ and $M_{l2}$ are matched. In addition, if the impedance of $M_{l1}$ and $M_{l2}$ are too low, then any mismatch will seriously affect the Q of the gyrator.

In order to save chip area, NMOS transistor in the triode region should be used to implement $R_L$. The resistance is given, as a first order approximation, by:

$$R_L = \frac{1}{2K(V_{gs} - V_t - V_{ds})} \tag{6-3}$$

But this is again not true for high Q filters. The main problem is the $V_{ds}$ term in Eq. (6-3). For this design, the difference of conductance between the positive and negative impedance loading is only 20 μA/V. Then when the output signal amplitude is above several tens of mV, the impedance of $R_L$ will increase and over-compensation of the output impedance will be resulted. This causes oscillation of the filter. Therefore only real polysilicon resistor is suitable. Another reason for using polysilicon resistors is that the real resistor has better linearity and would not degrade the linearity of the filter.

## 6.3 The architecture of the filter

The schematic of a biquad stage is shown in Fig. 6-3 and the equivalent block diagram is shown in Fig. 6-4.

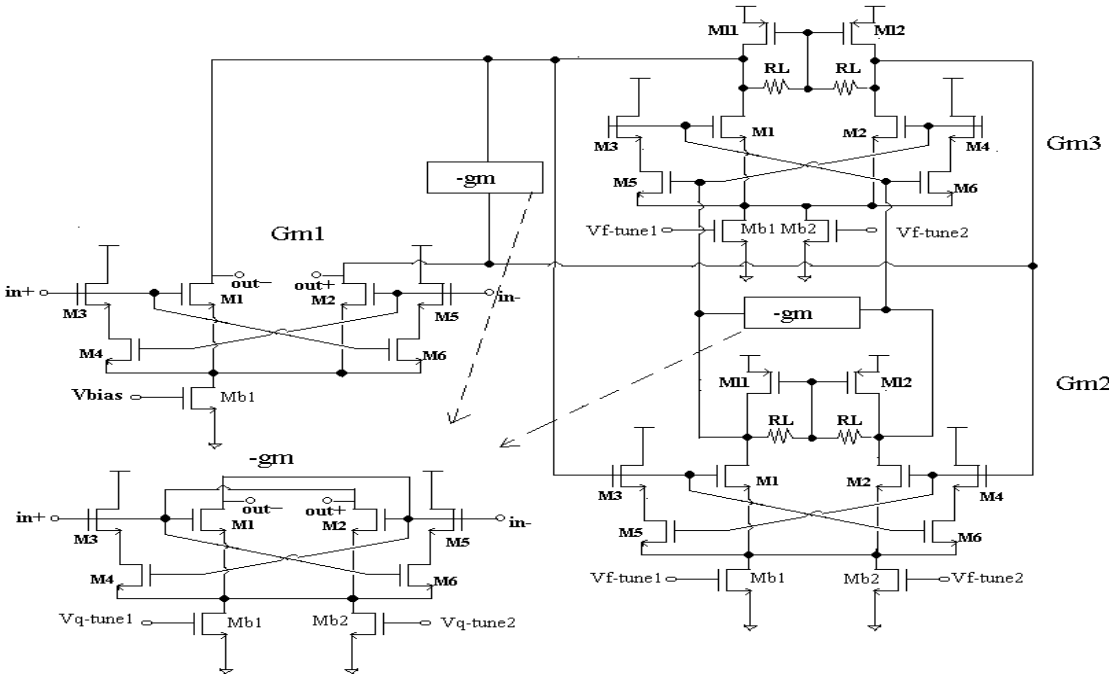



Fig. 6-3 The whole schematic of a biquad stage.

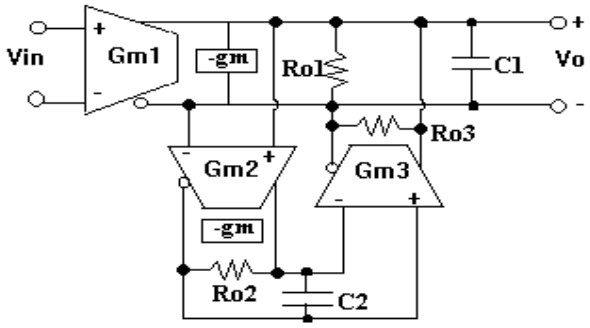



Fig. 6-4 The block diagram of a biquad stage

The input $g_m$ cell $G_{m1}$ and the negative impedance $-g_m$ have the same structure as $G_{m2}$ and $G_{m3}$ of the gyrator except that their bias current is supplied by the loading of the gyrator. The $G_{m1}$ of the 1st stage is designed to be 12 times larger than that of the latter two stages so that most of the gain (20 dB) is distributed to stage 1 and the remaining 12 dB are distributed the stages 2 and 3 as similar to the previous design.

The filter is constructed by cascading 3 stages of biquads like the previous design. Similar to the previous design, the three stages are not identical in size. The size of the gyrator of the 1st stage is double to that of the 2nd and 3rd stages, with the latter two being the same size. But this time the 1st stage is not re-designed as each stage is constructed with a number of generic $g_m$ cells. The $G_{m1}$ of the 1st stage uses 12 generic $G_{m1,}$ 6 generic $G_{m2}$ and $G_{m3}$ for each of the $g_m$ cells of the gyrator and 2 negative $g_m$ cells for each $G_{m2}$ and $G_{m3}$ for impedance compensation. For each of the latter two stages, all the number of $g_m$ cells are halved except that only 1 $G_{m1}$ is used as the input $g_m$ cell. For the master biquad of the automatic Q tuning loop and each of the biquads of the VCO in the automatic frequency tuning loop, only one generic $G_{m2}$ and $G_{m3}$ are used to construct the gyrator. The $G_{m1}$ and the $-g_m$ cells are redesigned.

The sizes of the transistors of each generic $g_m$ cell are listed in Table 6-1.

| | $G_{m1}$ | $G_{m2}$ and $G_{m3}$ | $-g_m$ |
|---|---|---|---|
| $M_1$ | 3 μm/1.2 μm x2 | 18 μm/1.2 μm x 6 | 2.7 μm/1.2 μm x2 |
| $M_2$ | 3 μm/1.2 μm x2 | 18 μm/1.2 μm x 6 | 2.7 μm/1.2 μm x2 |
| $M_3$ | 4.8 μm/1.2 μm x2 | 27 μm/1.2 μm x 6 | 4.2 μm/1.2 μm x2 |
| $M_4$ | 4.8 μm/1.2 μm x2 | 27 μm/1.2 μm x 6 | 4.2 μm/1.2 μm x2 |
| $M_5$ | 4.8 μm/1.2 μm x1 | 27 μm/1.2 μm x 3 | 4.2 μm/1.2 μm x1 |
| $M_6$ | 4.8 μm/1.2 μm x1 | 27 μm/1.2 μm x 3 | 4.2 μm/1.2 μm x1 |
| $M_{l1}$ | N/A | 21 μm/1.2 μm x15 | N/A |
| $M_{l2}$ | N/A | 21 μm/1.2 μm x15 | N/A |
| $M_{b1}$ | 7.5 μm/1.2 μm x2 | 20.4 μm/1.2 μm x9 | 12.9 μm/1.2 μm x3 |
| $M_{b2}$ | N/A | 20.4 μm/1.2 μm x9 | 12.9 μm/1.2 μm x2 |

Table 6-1 The size of each transistor of the biquads

The sizes of the $g_m$ cells can then be easily scaled. Unlike the previous design, for which each stage is constructed with the loading capacitor and the loading transistors to form a unit, this time the generic units are gathered to form an array. The array also contains the $g_m$ cells required for the automatic tuning loops. This can improve the problem of mismatch among the master and slave biquads. The idea is shown in Fig. 6-5.

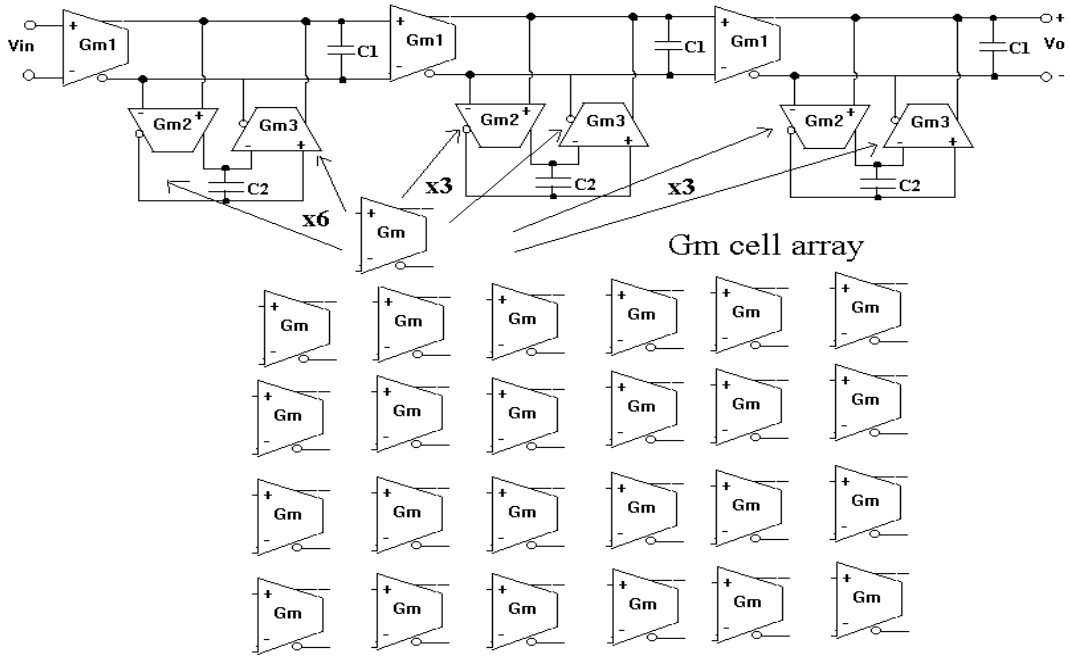



Fig. 6-5 The idea of using generic $g_m$ cell array to construct the biquads.

The best way of connection among the generic units is to interleave the generic units for best matching. However this is not practical because the routing will be too difficult. The routing of the $g_m$ cells will be discussed in the layout of the filter.

The other advantage of using generic units is that the power consumption of the automatic tuning loops can be reduced. The frequency-tuning loop requires 2 biquads to form the VCO while the Q tuning loop requires one and the sizes of these biquads need not be the same as that of the stages of the filter. Only 2 generic units are needed to construct a master biquad. This saves 2/3 of the power. Theoretically, for minimizing the power consumption, the biquads should be divided into as many units as possible. But this is not realistic. The mismatch of the generic units to the $g_m$ cells they constructed is proportional to the number of the generic units required. So a division of 3 is chosen.

The reason for having 2 bias transistors for both the $g_m$ cells of the gyrator and the $-g_m$ cells is to allow manual and automatic tuning at the same time. One bias pin is connected to the automatic tuning circuitry and the other is left outside for manual tuning.

As in the previous design, besides the above 3 stages, there are 2 stages of output buffers after the 3$^{rd}$ stage. The first buffer stage has the same size as the $g_{m1}$ of the 3$^{rd}$ stage to ensure the same capacitance loading as the 2$^{nd}$ stage. The second stage is just the first stage scaled up by 7 times such that it has a gain of 0 dB with a 0.5 pF loading which is more than enough for driving an output pad (<0.2 pF).

As discussed in the previous chapter, the use of MOS gate capacitance in strong inversion as the loading for each biquad is not reliable if the bias varies due to the process variation. Therefore, linear capacitor option of the 0.5 μm HP process is used instead. The capacitance is 16.16 pF for the 1st stage and 8.08 pF for the latter two stages.

The other modification is that the negative $g_m$ cell for impedance boosting is connected in parallel to the output nodes of the gyrator. Although the telescopic structure used in the previous design can utilize the drain currents of $G_{m2}$ and $G_{m3}$ to provide the negative impedance, the tunings of frequency and Q are *correlated*. That is why, although the frequency tuning range of the last filter is very wide, the filter cannot attain the required Q at 70 MHz. The power consumption of this filter, increased due to the "folded" structure of the impedance compensation, is only 2 mW. The small power consumption of the negative $g_m$ cells comes from the high designed value which are 2.5 KΩ for the 1st stage and 5 KΩ for the last two stages of the polysilicon resistors.

## 6.4 Noise and linearity of the filter

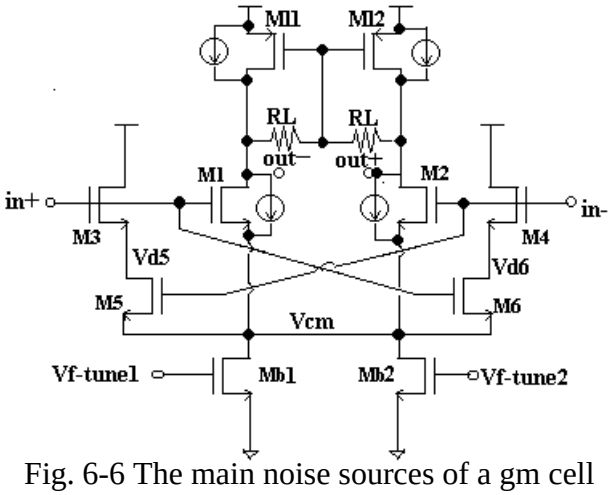


Fig. 6-6 The main noise sources of a gm cell

The noise of this filter can be analyzed as described in Chapter 3**.** The noise of $M_3$-$M_6$ and $M_{b1}$-$M_{b2}$ has little effect on the total noise as they are connected to a ground or a virtual ground. The main noise sources are still $M_1$-$M_2$, the

loading transistors $M_{l1}$-$M_{l2}$ and the resistors $R_L$ as shown in Fig. 6-5. Therefore the noise analysis of a simple differential pair shown in Chapter 3 can be employed.

For the first stage, the $g_m$ of $M_{l1}$ and $M_{l2}$ is 20.79 mA/V and that of $M_1$ and $M_2$ is 19.13 mA/V. Moreover, each loading resistor has a conductance of 0.66 mA/V. After lumping all these noise sources together, $\gamma$ is then equal to 2.12. Then by Eq. (3-28), $V_n$ of the 1st stage equals 190 μV. The $V_n$ of the 2nd and 3rd stages are both 340 μV. In order to achieve the noise requirement of equivalent input noise (about 30 μV), the gain has been distributed unequally among the 3 stages. The first stage has a gain of about 20 dB while the last two stages have a gain of about 5 dB each.

Similar to the previous design, the gain distribution is employed by taking the $IM_3$ into consideration. Due to the filtering effect, the 70.8 MHz and 71.6 MHz interferes are suppressed. Therefore some gain can be distributed between the 2nd and 3rd stages without significant increase of $IM_3$ of the filter while the linearity of the first stage can be improved.

## 6.5 Automatic tuning strategies

### *6.1.1 Frequency tuning*

The automatic frequency-tuning loop employs the PLL with PFD as introduced in Chapter 4. As mentioned in Chapter 4, the PLL with PFD has the advantage of theoretical infinite capture and lock ranges. This is especially suitable for the wide variation of the $G_m$-C filter.

The comparator is constructed by an Opamp followed by 2 inverters. An input signal of a few mV amplitude is already enough for invoking rail-to-rail square wave output. Therefore the loop should be able to operate even the Q of the VCO drops to below 10. The charge pump of the PFD is a simple single-end one with the schematic shown in Fig. 6-7 [3].

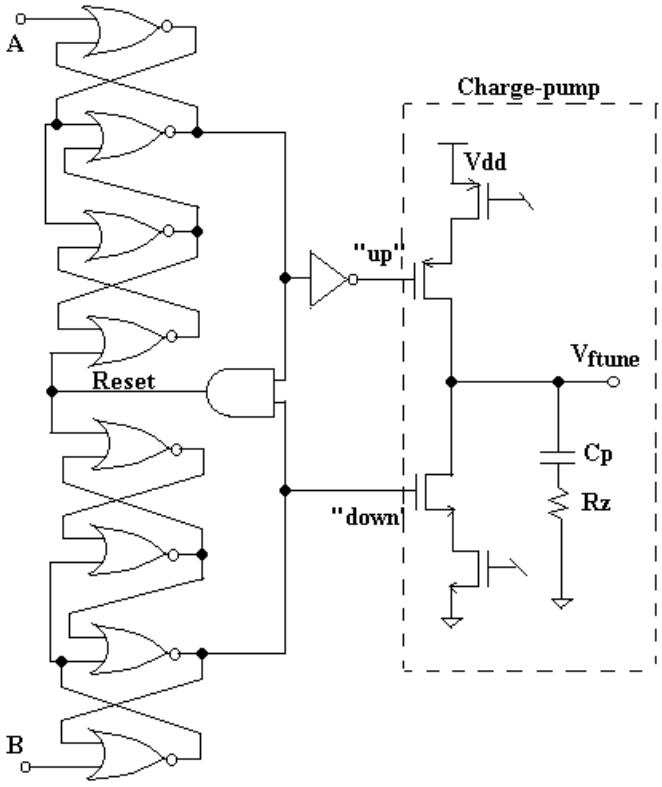



Fig. 6-7 The structure of the PFD used in the filter

Although a differential charge pump can provide a more balanced charge and discharge current for $C_p$, it cannot obtain a balanced initial condition as it is connected to the digital output of the PFD, which is undefined at the beginning. The result is that the unbalanced "up" and "down" signals may cause the $V_{ftune}$ to a value that prohibits the oscillation of the VCO.

The value of $C_p$ and $R_z$ are calculated by Eqs. (4-6) and (4-7). With the bias current of the charge to be about 1 μA and $K_{VCO}$ = 691Mrad/V and a required loop bandwidth of 100 KHz, the $C_p$ required is about 280 pF and the corresponding $R_z$ for a phase margin of 90° is 11.4 KΩ. The VCO is constructed by connecting two biquads back-to-back. As

mentioned in Chapter 4, the advantage is that the same Q tuning voltage can be used to tune the Q of the VCO which is especially suitable for high-Q purposes. Moreover, the gain is the product of two biquads. This ensures the VCO has enough gain for oscillation for a very wide range of Q. The $g_m$ cells used to construct the VCO have a linear range of about 200mV as shown in Fig. 6-2. For oscillation amplitude greater than the linear range, the $g_m$ of the $g_m$ cells will drop and that means a drop of $f_o$ of the VCO. This will cause tuning error. Therefore a limiter has to be connected in parallel at the output of each master biquad. The method employed in this design is to reduce the linear range of the negative $g_m$ cell so that the compensated impedance drops with large amplitude. The $-g_m$ cells used for the VCO is a modified version of the $g_m$ cell used for the slave biquads whose bias transistors are resized from 12.9 μm / 1.2 μm to 4.2μm / 1.2μm. This reduces the $V_{gs}$-$V_t$ of the differential pairs $M_1$-$M_4$ of the $g_m$ cell and thus limits the linear range. The same $-g_m$ cell is employed in the master biquad of the Q tuning loop also. The plot of $g_m$ variation of the $-g_m$ cell with the input voltage amplitude is shown in Fig. 6-8.

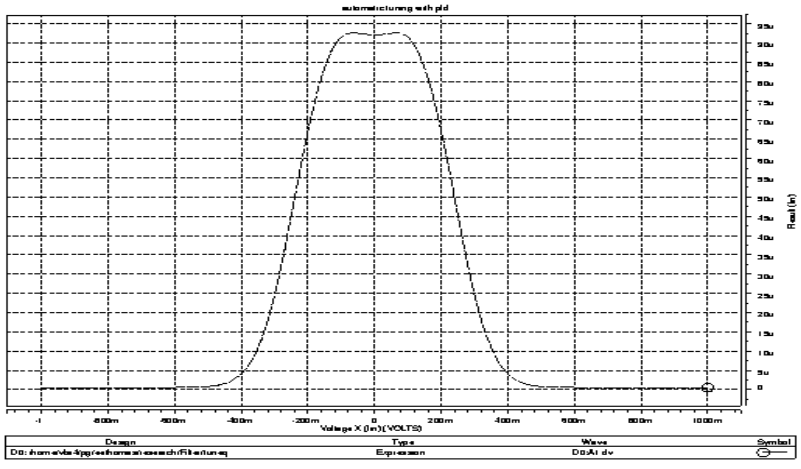


Fig. 6-8 The $g_m$ variation with input voltage of the $-g_m$ cell of the master biquads

### *6.1.2 Q tuning*

The automatic Q tuning employs the design of the simplified adaptive tuning by combining a magnitude locked loop and a multiplier as shown in Section 4.3.4 to achieve a simple but effective automatic tuning. The requirement of the linearity of the multiplier after the MLL is not strict. The reason is that after integration, all other harmonics are greatly suppressed and become negligible.

The input $g_m$ cell of the master biquad is redesigned to be 1/6 of that of the stages 2 and 3 such that the gain is 0 dB with a Q of 200. The input amplitude of the reference signal is 100 mV which is the maximum linear range of the $-g_m$ cell. The gain of the multiplier and the integrator are respectively –10 dB and 20 dB. In order to keep the variation of the Q within 1%, the C of the integrator has to be about 1 nF. With the consideration of the chip area, C is chosen to be 100 pF. External capacitance could be connected to reduce the ripple of the Q.

## 6.6 Layout of the filter

### *6.6.1 The floor plan and macroscopic placement*

The floor plan of the filter is shown in Fig. 6-9.

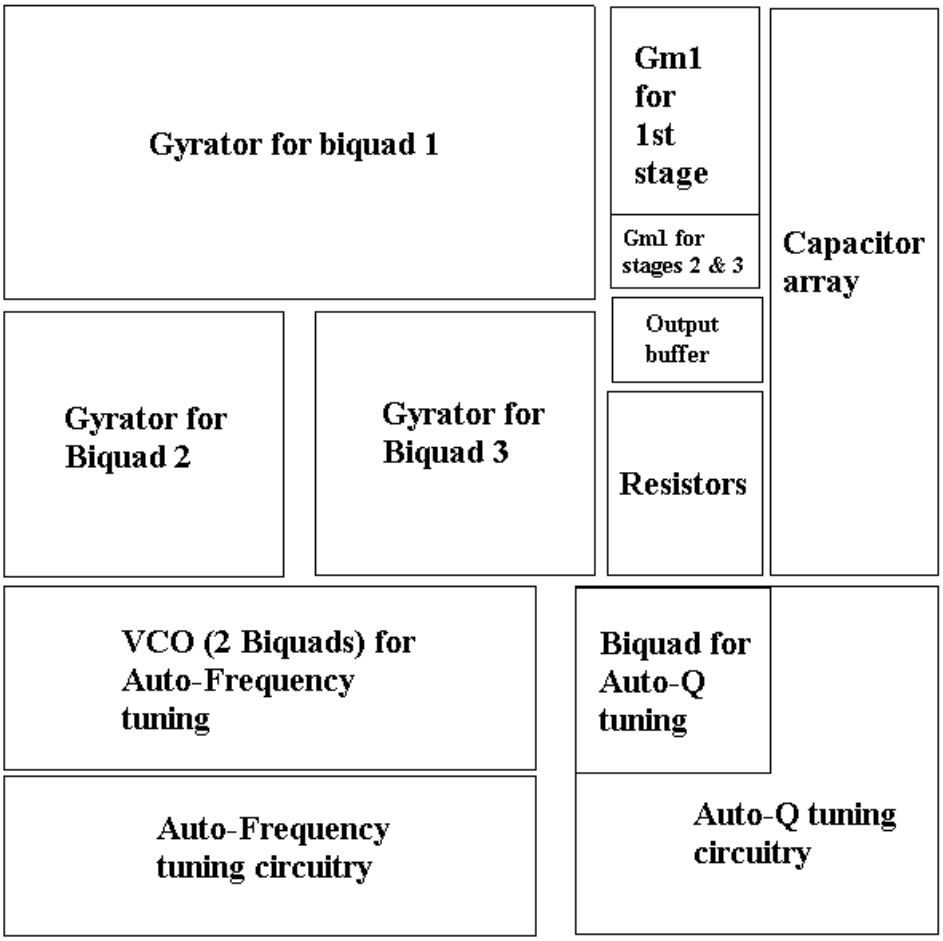



Fig. 6-9. The floor plan of the filter with automatic tuning

As mentioned in Section 3 of this Chapter, the generic unit $g_m$-cells of the gyrators of the 3 stages and the automatic tuning loops are grouped into an array. The best way to connect them is by interleaving for best matching among all the gyrators.

The connection among the generic units is shown in Fig. 6-10.

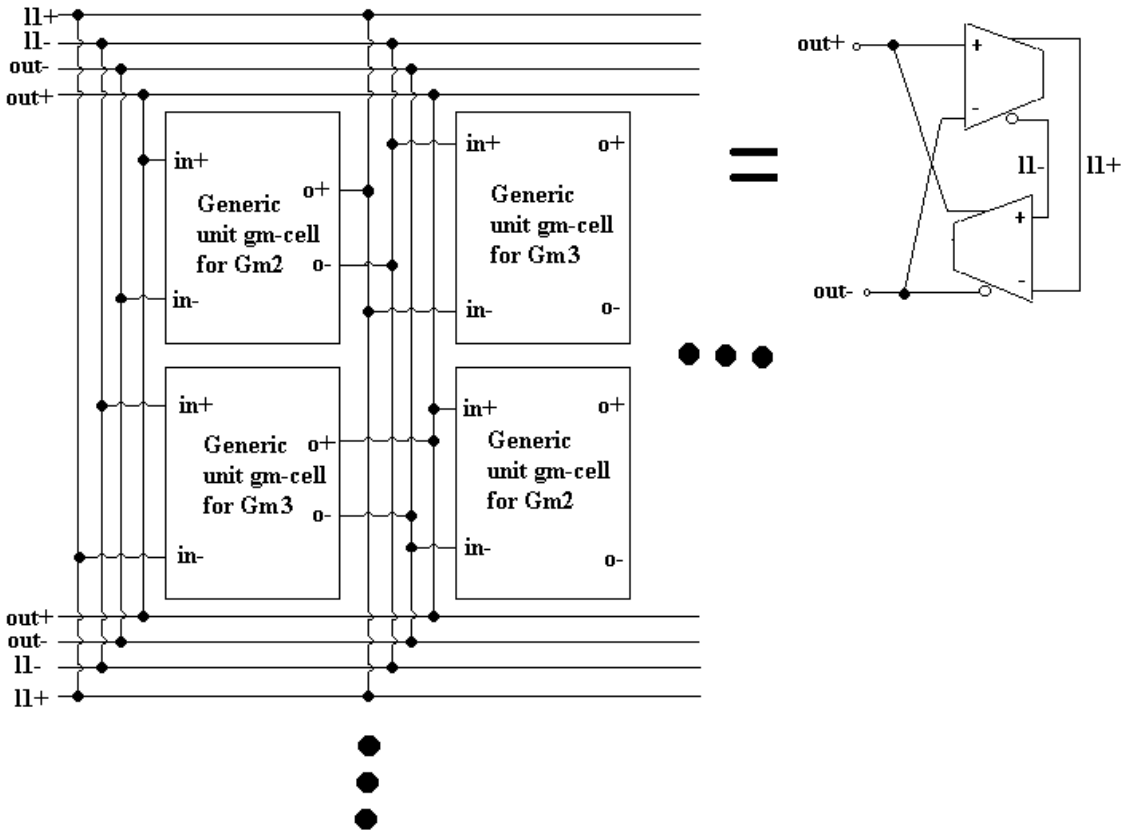



Fig. 6-10 The connection among the $g_m$ cell units by using rails

There are 4 wires forming horizontal and vertical rails for systematic routing. The 4 wires are namely the 2 pairs of inputs and outputs of each $g_m$ cell. Interleaving among all the generic units of the 3 biquads is impractical because 12 wires would be needed for the rails. This wastes a lot of area for the wires and also separates the generic units far apart which worsens the matching among them. Instead, only the 2 $g_m$ cells of each biquad are interleaved. By placing all the biquads close together, a good matching among them can still be obtained.

The connection in this way solves the difficulty of cross-connections within a gyrator. Moreover, the size of a biquad can be scaled up or down easily by simply cascading more blocks of generic units.

The biquads of the automatic tuning circuits are placed close to the 3 slave biquads for matching. However, there are large signal amplitudes (2.5 V digital) existing in those biquads of the VCO and the Q tuning loop. As a result, the tuning loops have to be surrounded by 2 layers of guard rings, with both P and N guard rings. Moreover, each generic $g_m$ unit is surrounded by another P guard ring. This should reduce the amount of interference. Care is also taken for the signal path of the reference signal and the output of the VCO. Metal-2 layer is used for the signal paths and is covered with the grounded Metal-1 and Metal-3 layers to shield from the electromagnetic interference.

Like the previous filter, the power line width has to be determined carefully. Since the total power consumption of the filter is about 90 mW and the automatic tuning loop is approximately 30 mW, the corresponding current is approximately 36 mA and 12 mA respectively. For secured connection, the width of the power line of the filter and that of the tuning loops are 72 μm and 24 μm respectively. The power lines are separated in order to isolate the interference from the large signals of the tuning loops.

### *6.6.2 Layout of the components*

Unlike the filter of the previous chapter, the unit capacitors of all 3 biquads are put together to provide a better matching among them. For the tuning loops, however, large signals (~400 mV) exist across the capacitors. So they are put close to the tuning loops rather. The layout of a pair of 8 pF capacitors is shown in Fig. 6-11. The remaining 80 fF capacitance is for fine adjustment with the routing parasitics and the parasitic capacitance of the polysilicon resistor. Again, the capacitor is divided in unit capacitors for better matching. This time, the linear capacitor option for which there is N+ diffusion below the gate oxide is used. It provides a better-controlled capacitance than the MOS gate capacitance. The capacitance density is about 2.2 fF per $\mu m^2$. The total area of the capacitor is 110x710 $\mu m^2$ (64 pF total) for the filter, 356x356 $mm^2$(280 pF) for the charge pump of the automatic frequency tuning and 213x213 $mm^2$ (100 pF) for the automatic Q tuning loop.

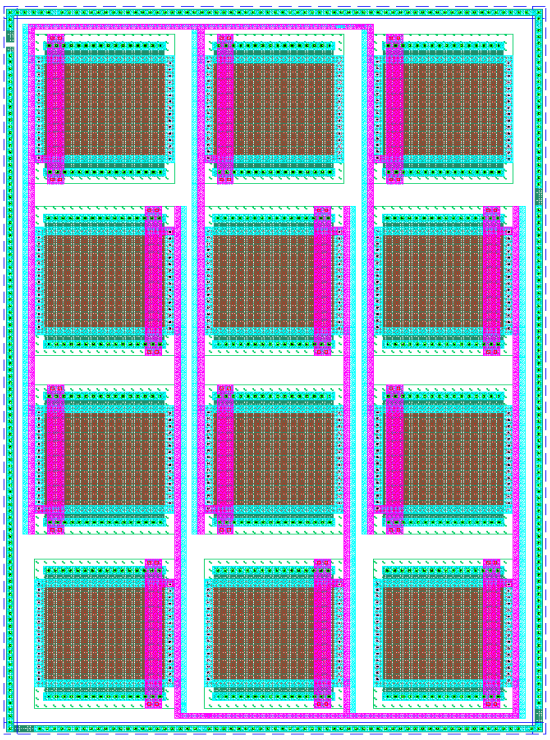


Fig. 6-11 The layout of the block of a pair of 8pF capacitors

However, since the capacitors for the charge pump and the automatic Q tuning are grounded capacitors, the structure is not the one shown in Fig. 6-11 but just a large single capacitor.

On the other hand, the resistors are constructed in blocks. Each block

contains a pair of 3 KΩ resistors interleaved for matching purpose. The resistivity of polysilicon can vary by 20% due to process variation. Therefore, although the resistance required in the design is just 2.5 KΩ for the 1st stage, the resistor is made to be 3 KΩ such that the negative $g_m$ cell can still give enough compensation even the resistance drops by 20%. The layout of the resistor is shown in Fig. 6-12.

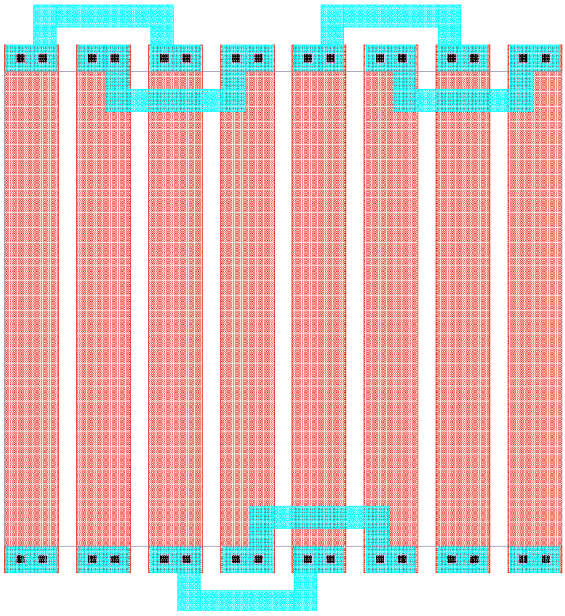


Fig. 6-12 The layout of a resistor block of a pair of 3 KΩ resistors

Unlike the capacitors, the resistors of all the biquads are not put together to form a pool. The difference of the path length affects the resistance. Routing will be very troublesome too because there is a center-tap for the gates of $M_{l1}$ and $M_{l2}$. The resistors are therefore placed close to the biquads. The largest biquad uses only 2 blocks while the biquad for the Q tuning loop uses 12. The inductance due to the length of the polysilicon is negligible not only because the frequency is low (70 MHz) but also because the Q is very low for the resistor. The resistance of ploysilicon with silicide block is about 130 Ω per square. The required area for each resistor block is 36x38 $\mu m^2$. The capacitance of the polysilicon has already been taken into account.

### *6.6.3 The complete layout of the filter*

The complete layout of the filter is shown in Fig. 6-13. The core area is 800x1200 $\mu m^2$. Note that not all bias and signal pins are connected to the pads because the filter has to be integrated to the RFIC receiver system.

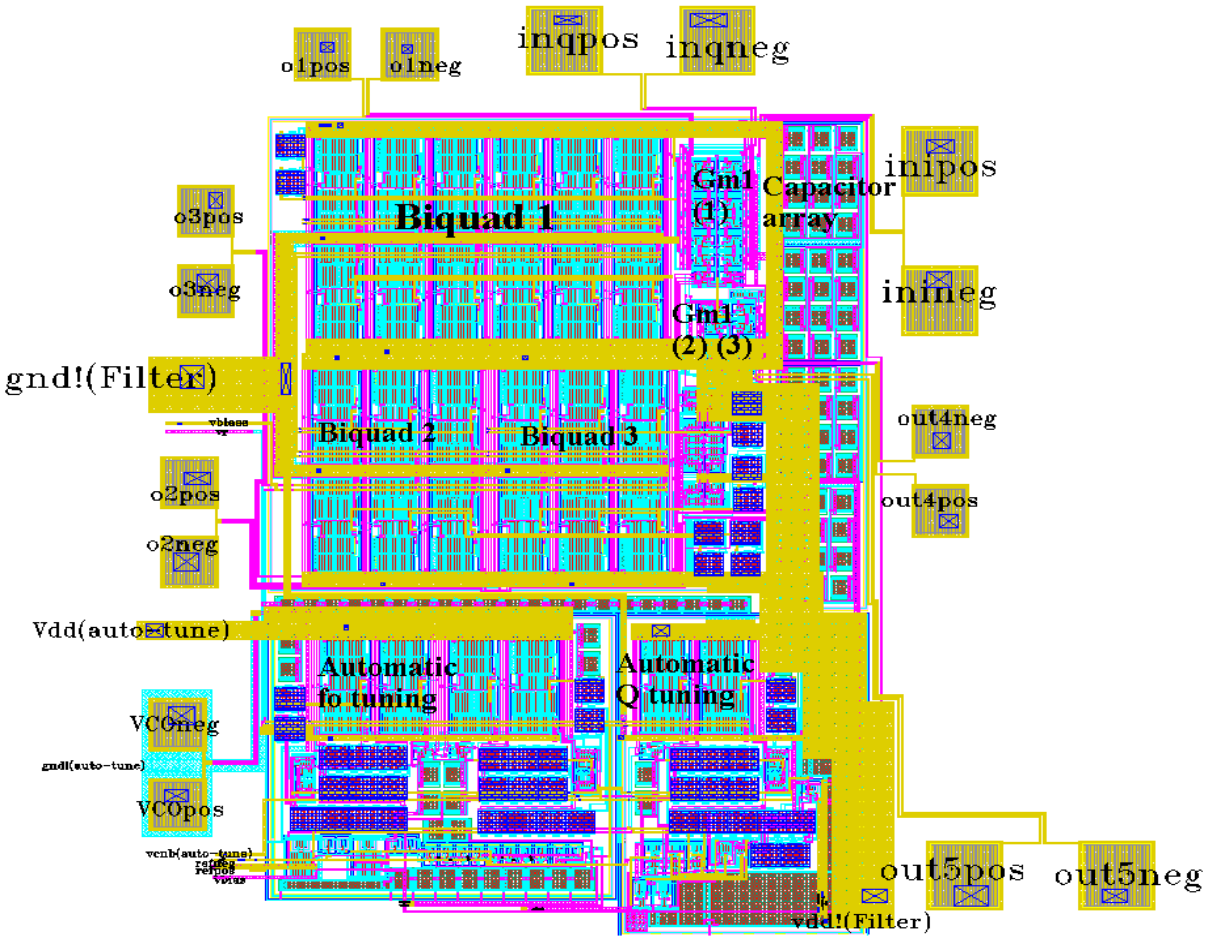



Fig. 6-13 The complete layout of the filter

## 6.7 Simulation Results

### *6.7.1 Filter performance*

HSpice simulation results show that the $V_n$ of the 1st stage is 163 μV while that of the last 2 stages is 224 μV. The calculation has over-estimated the noise of the filter. The reason is the brick-wall approximation of the transfer function. The equivalent input noise is 29.8 μV, or 70.2 nV/√Hz. The plot of the $IIP_3$ of the filter is shown in: Fig. 6-14.

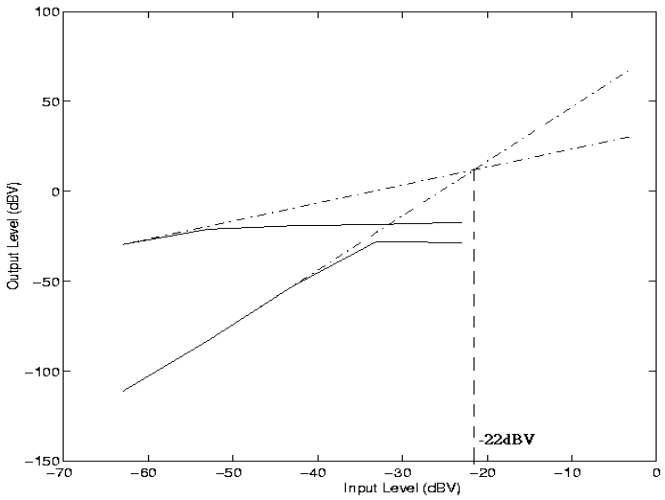



Fig. 6-14 The plot of the $IIP_3$ of the filter

The $IIP_3$ of the filter is –22dBV or –9dBm equivalently. The $IIP_3$ to noise ratio is 68.7 dB which is smaller than the previous filter. Note that the 1-dB compression point occurs at about –53 dBV, which is 31 dB smaller than the $IIP_3$.

The maximum frequency tuning range is from 40 MHz to 100 MHz. As shown in Fig. 6-15 the bandwidth does not change too much with the variation of frequency from 58 MHz to 82 MHz. This can prove the little correlation between the $R_o$ and the $f_o$.

The Q can be varied from 10 to infinity. The nominal value is 390. The plot of the variation of Q in Fig. 6-16 shows that the center frequency does not virtually vary with the variation of Q. The nominal voltage gain from the output buffer is 30 dB. The power consumption of the filter excluding the automatic tuning part is 90 mW.

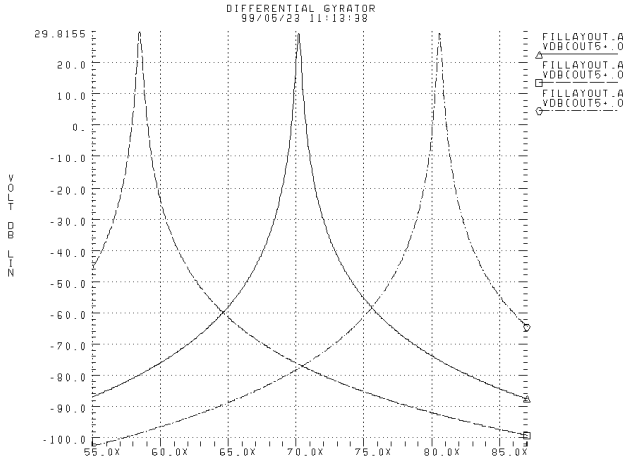



Fig. 6-15 Variation of $f_o$

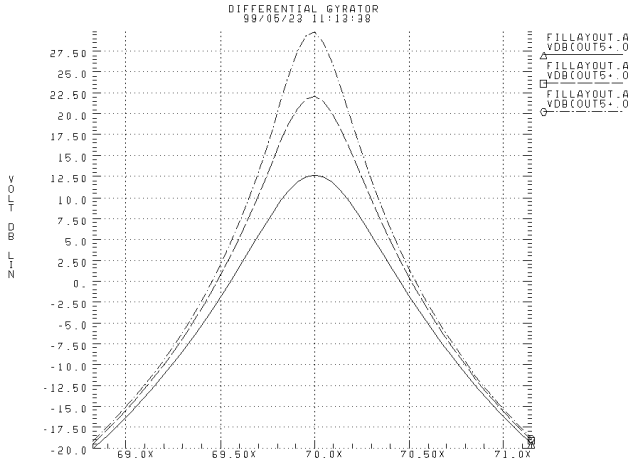



Fig. 6-16 Variation of Q

### *6.7.2 Automatic tuning performance*

The nominal frequency tuning voltage for $f_o$=70 MHz is 0.9 V. By deliberately increasing the loading capacitance, the steady tuning voltage increases to 0.915 V as shown in Fig. 6-17. From the corresponding FFT plot of the oscillation output of the VCO in Fig. 6-18, the center frequency is observed to be 70 MHz. The plots show the ability of the automatic frequency tuning.

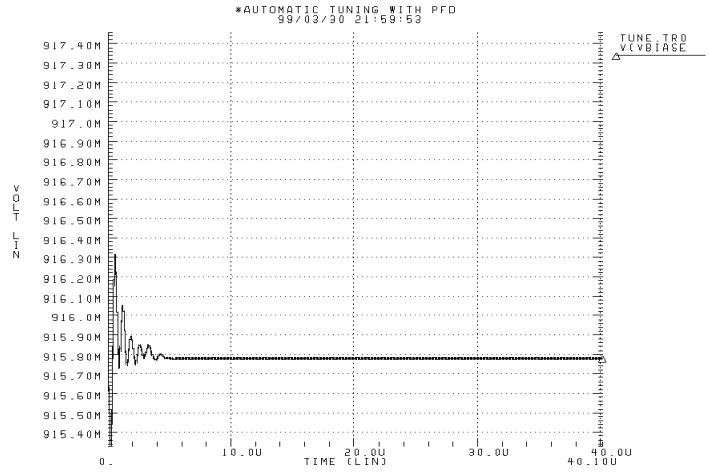



Fig. 6-17 The plot of the $f_o$ tuning voltage with time

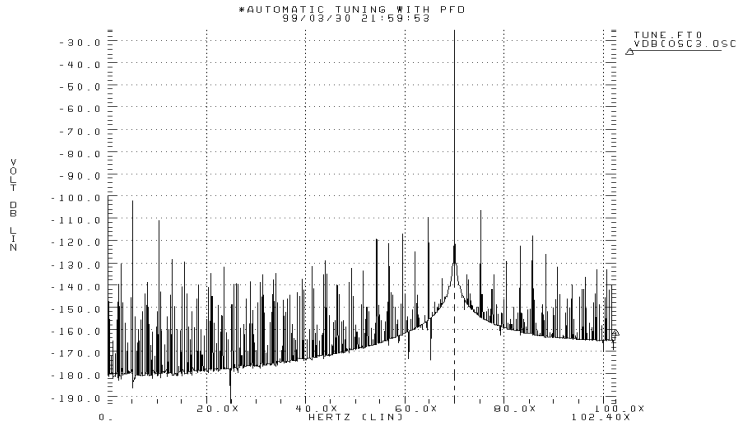



Fig. 6-18 The FFT plot of the frequency of the VCO of the frequency auto-tuning

For the automatic Q tuning, from Fig. 6-19, the Q tuning voltage becomes steady at 0.743V. This is close to the nominal value 0.741 V. The error of the tuning voltage can be adjusted by varying the gain of the input $g_m$ cell of the master biquad.

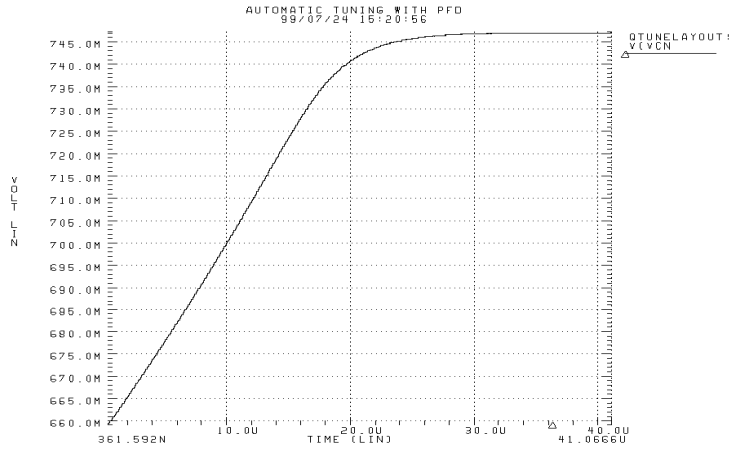



Fig. 6-19 The transient plot of the Q tuning voltage.

A summary of the simulated performance of the filter is given in Table 6-2.

| | |
|---|---|
| $F_o$ | 70 MHz |
| Q | 390 |
| No. of orders | 6 |
| Auto-tune? | Q and $f_o$ |
| $F_o$ tuning sensitivity | 691 Mrad/V |
| Gain | 30 dB |
| Noise | 70 nV/√Hz |
| Linearity $IIP_3$ | –9 dBm |
| Dynamic Range | 67 dB |
| Power consumption | 120 mW<br>Filter: 90 mW<br>Auto-tuning: 30 mW |
| Voltage | 2.5 V |
| Process | 0.5 μm HP |
| Chip area | 0.8x1.2 $mm^2$ |

Table 6-2 Summary of the performance of the filter

The chip photo is shown in Appendix of this thesis.

## Appendix 6.1 Derivation of the size ratio of $M_{1,2}$ and $M_{3,4}$ of the design of Fig. 6-1

From Appendix 2.1**,** the size ratio of $M_{1,2}$ to $M_{3,4}$ is 0.914. The sizes of $M_3$ to $M_6$ are all matched. Now suppose the size of $M_{3,4}$ is C times that of $M_{5,6}$**,** the size ratio of $M_{1,2}$ to $M_{3,4}$ has to be derived again. Similar to the Appendix 2.1, the analysis starts from $I_{D3}$ and $I_{D5}$ first:

$$I_{D3} = I_{D5} \Rightarrow CK_3(V_{in}/2 - V_{d5} - V_t) = 2K_5[-(V_{in}/2 + V_{cm} + V_t)V_{ds5} - \frac{1}{2}V_{ds5}^{\ 2}] \tag{6-4}$$

Let $V_{cm}+V_t = V_{cm}^{\ *}$ and expand (6-4), the following relationship is obtained:

$$(C+1)V_{ds5}^{\ 2} - [(C-1)V_{in} - 2(C+1)V_{cm}^{\ *}]V_{ds5} + C(V_{in}/2 - V_{cm}^{\ *})^2 = 0 \tag{6-5}$$

Solve for $V_{ds5}$:

$$V_{ds5} = \frac{C-1}{2(C+1)}V_{in} - V_{cm}^{\ *} + \frac{1}{2}\sqrt{[\frac{(C-1)V_{in} - 2(C+1)V_{cm}^{\ z}}{C+1}]^2 - \frac{4C(\frac{V_{in}}{2} - V_{cm}^{\ *})^2}{C+1}} \tag{6-6}$$

Then $I_{D3}$ can be expressed as:

$$\begin{aligned} I_{D3} &= K_3[V_{in}/2 - (V_{ds5} + V_{vm}^{\ *})]^2 \\ &= \frac{K_3}{4(C+1)^2}[2V_{in} - \sqrt{(1-3C)V_{in}^2 + 4(C+1)V_{in}V_{cm}^{\ *} + 4(C+1)V_{cm}^{2\ *}}]^2 \end{aligned} \tag{6-7}$$

$I_{D4}$ has a similar expression, with $V_{in}$ replaced by $-V_{in.}$ Then have $I_{D3}+I_{D4}$ is expressed as:

$$I_{D3} + I_{D4} = \frac{K_{3.4}}{2(C+1)^2}[(5-3C+4\sqrt{C+1})V_{in}^2 + 4(C+1)V_{cm}^{2\ *}] \tag{6-8}$$

and $I_{D1}+I_{D2}$ the same as Eq. (2-33):

$$I_{D1} + I_{D2} = 2K_{1,2}[V_{cm}^{*\,2} + (\frac{V_{in}}{2})^2] \tag{6-9}$$

The total current of $I_{D1}$-$I_{D4}$ is then:

$$\sum_{i=1}^{4} I_{Di} = [\frac{K_{1,2}}{2} - \frac{K_{3,4}}{2(C+1)^2}(5-3C-4\sqrt{C+1})]V_{in}^2 + 2[K_{1,2} + (C+1)K_{3,4}](V_{d5} + V_t)^2 \tag{6-10}$$

To cancel the $V_{in}^2$ term, the expression of the ratio of $K_{1,2}$ to $K_{3,4}$ is given below:

$$K_{1,2} : K_{3,4} = \frac{4\sqrt{C+1} + 3C - 5}{(C+1)^2} : 1 \tag{6-11}$$

Note that when C=1, then $K_{1,2}$ : $K_{3,4}$ = 0.914 : 1 , this agrees with the result of the paper of Appendix 2.1 [1].

## References


1. C.S. Kim, Y.H. Kim, S.B. Park, “New CMOS Linear Transconductor,” *Electronics Letters*, Vol.28 No.21, October 1992.
2. Vladimir I.Prodanov, “A Differential Active Load and its Applications in CMOS Analog Circuit Designs”, *IEEE Transactions on Circuits and System II. Analog and Digital Signal Processing*, Vol.44, No.4, April 1997.
3. I.Shahriary et al., “GaAs Monolithic Phase/Frequency Discriminator,” *IEEE GaAs IC Symp. Dig. of Tech. Papers*, pp. 183-186, 1985.

# Chapter 7 Measurement Results and discussion

## 7.1 The testing setup

The testing setup for the filter is similar to that of the first filter measurement. However, this time the automatic tuning loops have to be tested as well. Therefore one more sinusoidal generator, one more power splitter and two more bias-tees are required. The whole setup is shown in Fig. 7-1.

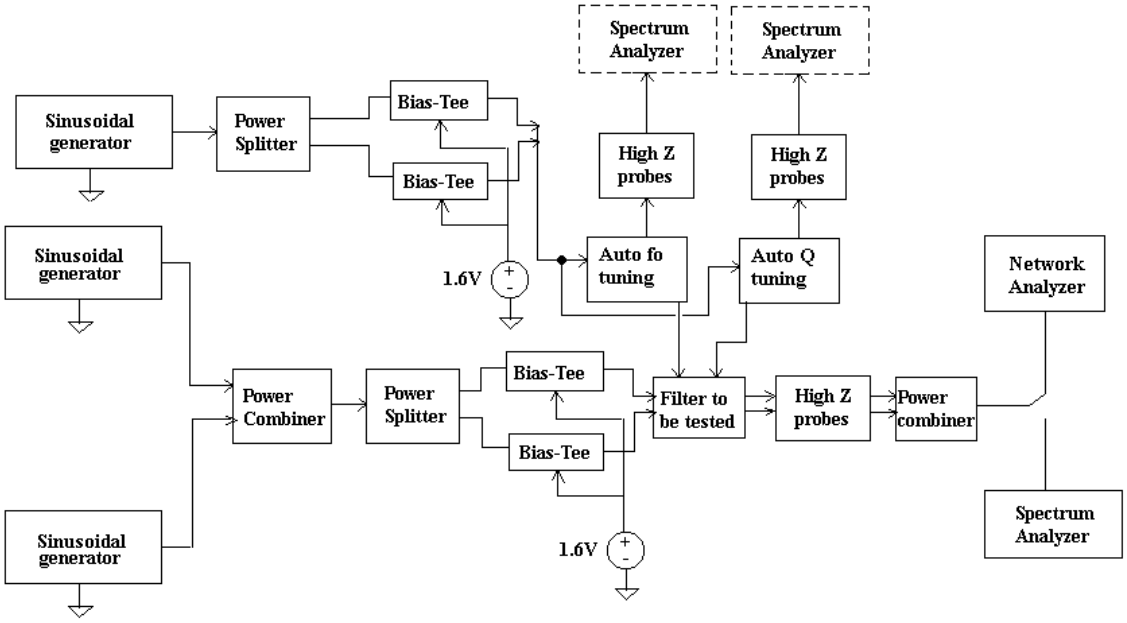



Fig. 7-1 The block diagram of the testing setup of this filter

Again, the noise figure of the filter, which is expected to be about 64 dB when measured with high impedance probes, is still too large to be measured with the noise figure meter. Therefore the filter noise is still measured with the spectrum analyzer.

## 7.2 The measurement procedure

1. The filter is tested with all automatic tuning loops off. The tuning voltages are tuned manually. The filter is then tested for the same parameters as the previous filter.
2. The automatic tuning loops are tested, and the nominal tuning voltages are adjusted to be the same as that of the filter.
3. Both the filter and the automatic tuning loops are connected together to form a practical filter.

## 7.3 Measurement results of the filter

The filter indeed performs a filtering function. However, the maximum Q drops to about 14 at 70 MHz. The measured frequency response is shown in Fig. 7-2.

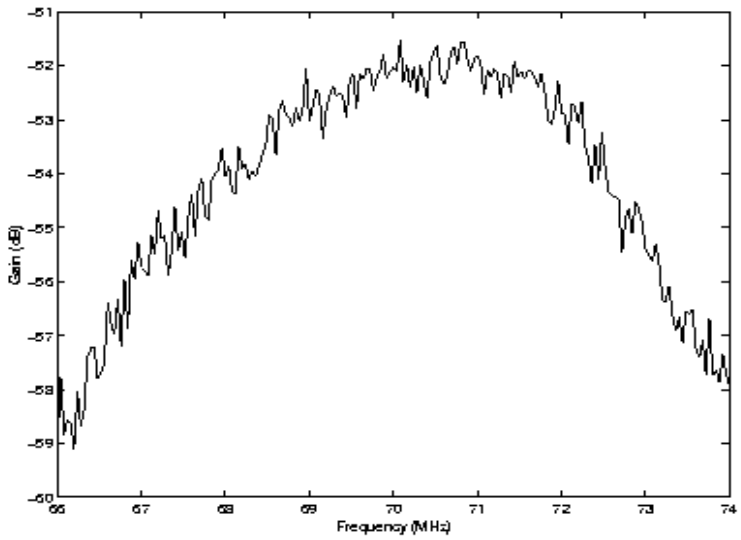



Fig. 7-2 The measured frequency response of the whole filter

The gain drops to about –51.5 dB. The low Q is out of expectation. Another unexpected phenomenon is that the bandwidth reduces when $f_o$ decreases. The responses at $f_o$ = 26

MHz and at $f_o$ = 40 MHz are shown respectively in Fig. 7-3 and Fig. 7-4. This is not expected by simulation. The bandwidth should be little correlated to the variation of $f_o$. Some component effects were not considered during the design stage.

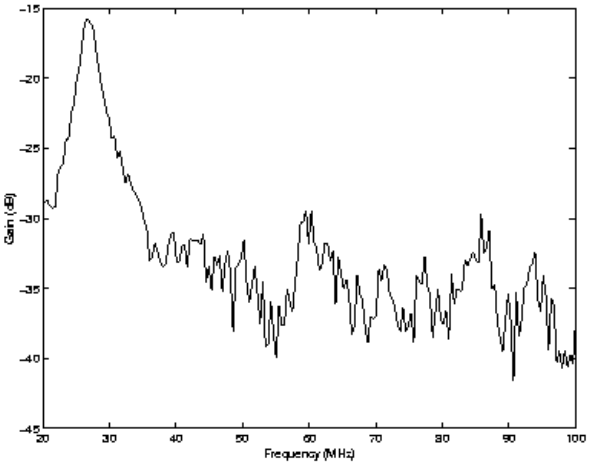



Fig. 7-3 The response of the filter with $f_o$ = 26 MHz

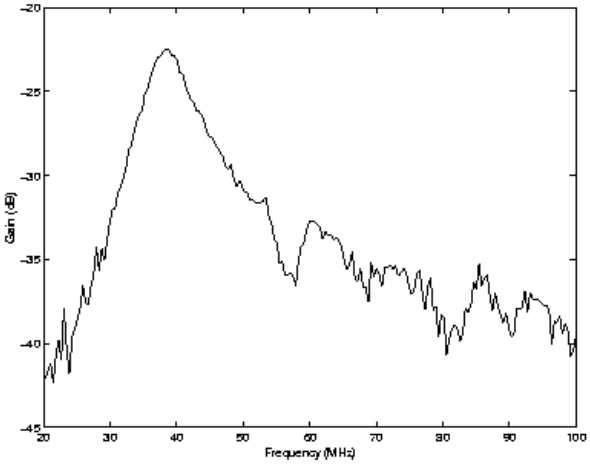



Fig. 7-4 The response of the filter with $f_o$ = 40 MHz

The linearity of the filter could not be measured because the gain is too low. In order to observe the 70 MHz intermodulation component in the spectrum analyzer, the input strength of the two interferes has to be above 0 dBm. The filter has already been saturated by this amplitude and the $IIP_3$ measured would not be accurate. The output noise of each stage, however, could be observed in the spectrum analyzer. Stage 1 has an output noise level of –77 dBm while that of each of the other two stages is –61 dBm. This corresponds to an output noise voltage of 2.43 μV/√Hz for stage 1 and 14.6 μV/√Hz for stages 2 & 3. To compare the performance with the simulation results, the Q of the filter schematic is adjusted to 14 and re-simulated. Both results are shown in Table 7-1.

| | Measurement | Simulation after Q adjustment |
|---|---|---|
| $F_o$ | 70 MHz | 70 MHz |
| Q | 14 | 14 |
| No. of orders | 6 | 6 |
| Gain | -51.5 dB | - 55.3 dB |
| Input equivalent noise | Stage 1 : 2.34 μV/√Hz<br>Stage 2 & 3:<br>14.6 μV/√Hz | Stage 1: 1.28 μV/√Hz<br>Stages 2 & 3:<br>11.4 μV/√Hz |
| Linearity | N/A | 76.3 dBm |
| Power consumption | 91 mW | 92 mW |
| Voltage | 2.5 V | 2.5 V |

Table 7-1 Summary of the measurement result and the simulated result with Q adjusted to 14

From the table, the measured noise is observed to be a bit greater than the simulated one. This is due to noise coupling from the external enviroment and the error of reading in the spectrum analyzer. The corresponding noise figure of the whole filter is about 90 dB due to the low gain.

## 7.4 Measurement results of a generic biquad

Since the measurement of the filter has deviated much from the simulation, the master biquad of the Q tuning loop, which is constructed with only 2 generic $g_m$ cells, is tested with manual tuning to identify the problem. Unlike the filter stages, the generic biquad works well. The Q could be tuned to the nominal value. The frequency response is shown in Fig. 7-5. The gain is 0 dB. The frequency tuning range is from 25 MHz to 72 MHz.

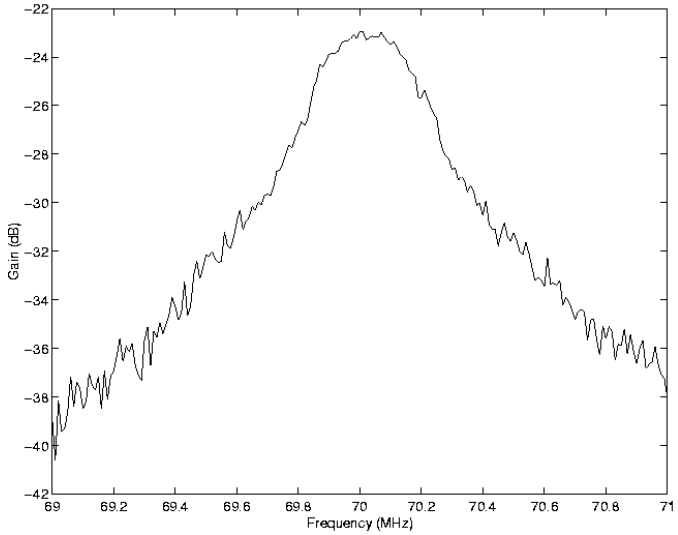



Fig. 7-5 The measured frequency response of a generic biquad.

Further increase of the $f_o$ tuning will cause oscillation. The reason is that the bias transistors of the gyrator have been operating in triode mode. The CMRR of the gyrator drops and thus introduces common-mode stabiliy. The upper limit of the frequency tuning range can be extended to 82 MHz with a 3-V supply. The measured $IIP_3$ is –9 dBV or +4 dBm as shown in Fig. 7-6. The 1-dB compression point is –32 dBV which has been increased by 20 dB because the input signal has not been amplified by the 20-dB gain of the first stage.

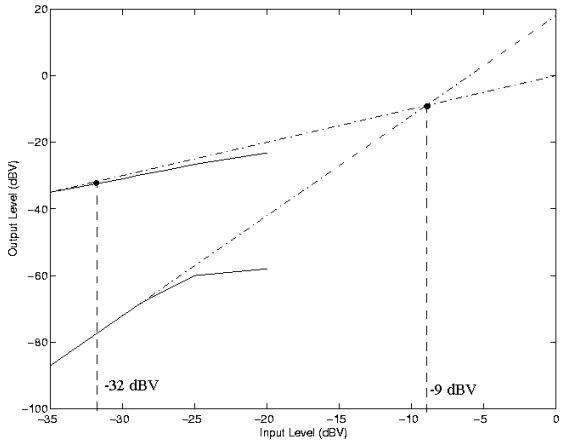



Fig. 7-6 $IIP_3$ and the 1-dB compression point of the biquad

The measured noise of the filter is –81.5 dB which corresponds to 1.48 μV/√Hz or totally 630 μV for 180 KHz bandwidth. A summary of the measured results is shown in Table 7-2.

| | Biquad Measurement |
|---|---|
| $F_o$ | 70 MHz |
| Q | 200 |
| No. of orders | 2 |
| Gain | 0 dB |
| Noise | 1.48 μV/√Hz |
| Linearity | $IIP_3$ +5 dBm |
| Dynamic Range | 55.8 dB |
| Power consumption | 7.8 mW |
| Voltage | 2.5 V |

Table 7-2 Measurement results of a generic biquad

Because the filter stages are just constructed with the generic $g_m$ cells, for the ease of comparison with the simulation result, the above measurement result is projected back to the should-be performance of the whole filter. The results are shown in Table 7-3.

| | Projected performance of a whole filter | Simulation results of a whole filter |
|---|---|---|
| $F_o$ | 70 MHz | 70 MHz |
| Q | 390 | 390 |
| No. of orders | 6 | 6 |
| Gain | 30dB | 30 dB |
| Noise | 77 nV/√Hz | 70 nV/√Hz |
| Linearity $IIP_3$ | –15 dBm | –9 dBm |
| Dynamic Range | 61.7 dB | 67 dB |
| Power consumption | 93.6mW | 90 mW |
| Voltage | 2.5 V | 2.5 V |

Table 7-3 Comparison between the projected performance of the whole filter and the simulation results.

The projected result has a degraded linearity when compared to the simulated result due to the mismatch of transistors that leads to the variation of the linear range of the $g_m$ cells of the biquads. The noise performance, however, is close to the simulated result. From the table we can predict the filter, which is constructed with generic $g_m$ cells, should perform with a high Q value and gain. The reason for the performance deviation will be discussed later.

## 7.5 Measurement result of the automatic loops

### *7.5.1 The Q tuning loop*

The master biquad of the automatic Q tuning loop is probed with high impedance probes for Q tracking and measurement. The $-g_m$ cells of the master biquad have bias pins for both manual tuning and automatic tuning. When the manual tuning voltage is reduced, the automatic tuning voltage should rise to compensate the drop of the Q. The plot between the manual tuning and automatic tuning voltages is shown in Fig. 7-7.

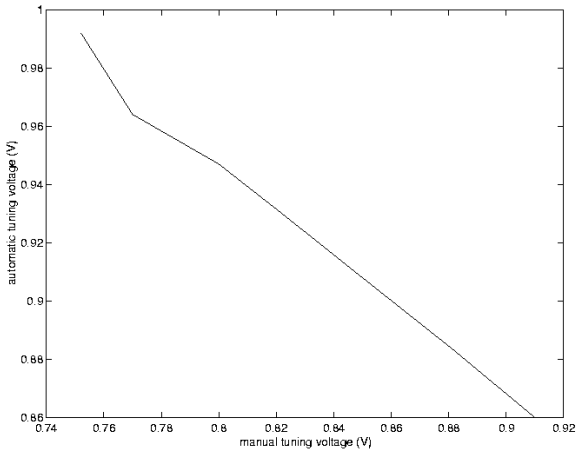



Fig. 7-7 Manual Q tuning voltage Vs Automatic Q tuning voltage

Unlike for the magnitude-locked loop, Q for the Q tunng loop can be kept constant as long as the difference between the $f_o$ of the master biquad and the reference frequency is smaller than 8 MHz. The range of frequencies that the Q tuning loop operates is from 25 MHz to 72 MHz. Again, the range could be extended up to 82 MHz with a 3-V supply which is the same as the same range of the master biquad. The power consumption is about 10.2mW.

### *7.5.2 The $f_o$ tuning loop*

The VCO output is probed with high impedance probes to observe the oscillation frequency. The loop can lock from 35 MHz to 68 MHz. The lower frequency is limited by the bias current required for sustain oscillation while the upper frequency is limited by the common-mode instability of the biquads. The upper range can be extend to 80 MHz with a 3-V supply. The lock range is about 10.8 MHz when the frequency is locked at 57MHz. The total power consumption is about 19.2mW. The loop bandwidth of about 150 KHz is measured with the frequency of the input reference modulated with a train of square waves. The VCO output is observed with a spectrum analyzer. A series of VCO frequencies can be observed if the loop can track the change of the reference. The square wave frequency is increased, and the frequency at which the loop fails to track is approximately the bandwidth of the loop.

## 7.6 Discussion

The difference between the Q of the main filter and the generic biquad is out of expectation from the simulation results. The polysilicon resistor variation was at first

suspected to be the cause. The value of the resistors could be measured directly. The maximum $g_m$ of the –gm cells of each stage and the generic biquad is measured as well. The results are shown in Table 7-4.

| | Stage 1 | Stages 2&3 | Biquad of auto-Q tuning |
|---|---|---|---|
| Max. $g_m$ of $-g_m$ cell | 231 μA/V | 116 μA/V | 130 μA/V |
| Poly-silicon Resistance | 8.67KΩ | 17.37KΩ | 52.4 KΩ |
| Surplus $-g_m$ | 116 μA/V | 88 μA/V | 111 μA/V |

Table 7-4 The measured result of the maximum $-g_m$ and polysilicon resistance of each biquad

It is clear that the $-g_m$ is more than enough to compensate the physical positive conductance. The $R_o$ of transistors is more than 10 times higher than the corresponding polysilicon resistors and thus can be ignored. The Q of the capacitors was considered to be negligibly large during the design stage. Actually it turns out to be quite low and has a serious effect to the Q of the circuit.

### *7.6.1 Effects of the capacitor Q*

A simple model of a capacitor $C_p$ with a series resistance $R_s$ is shown in Fig. 7-8.

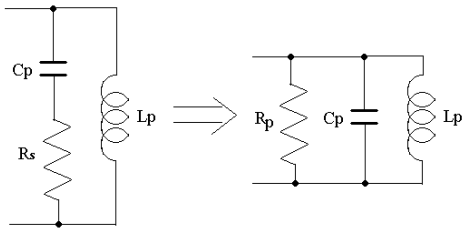



Fig. 7-8 The model of a capacitor with finite Q and the equivalent parallel resistance

The resistance of a linear cap-well capacitor comes from the doping resistance which is distributive. The Q of a capacitor is given as:

(7-1)

$$Q = \frac{1}{\omega R_s C_p}$$

The finite Q of the capacitor adds an extra positive conductance at the output of a biquad. The equivalent parallel resistance $R_p$ is given by L-matching as :

$$R_p = R_s(Q^2 + 1) \approx \frac{1}{\omega^2 R_s C_p^{\ 2}} \tag{7-2}$$

No testing structure of the linear capacitor is available in this run. Instead, the Q is estimated from the measurement results from one of our colleaques, Mr. Yan Shing Tak. The capacitance he measured is about 7.3 pF with a Q of about 10 at 70 MHz. The series resistance is about 24Ω. On the other hand, the size of the unit capacitors used in this filter design is about 1.34 pF. Since the resistance of a capacitor is roughly inversely proportional to the capacitor width, Q is then roughly proportional to the capacitor width. By scaling, the resistance of the unit capacitors is estimated to be about 56 Ω which corresponds to a Q of 55.

Another effect of finite capacitor Q is the shifted $\omega_o$ of the LC tank. The new $\omega_o$ with $R_s$ in series with capacitors is given by :

$$\omega_o' = \frac{1}{\sqrt{L_p C_p}} \frac{\sqrt{C_p / L_p} R_s + \sqrt{C_p R_s^{\ 2} / L_p + (1 - C_p R_s / L_p)}}{1 - C_p R_s / L_p} \tag{7-3}$$

Note that if $R_s = 0$, then $\omega_o' = \frac{1}{\sqrt{L_p C_p}} = \omega_o$.

As a result, the conductance $sL_p - \frac{1}{sC_p}$ is no longer zero but with a finite resultant reactance which also loads down the output. The total positive conductance and the resultant maximum Q are listed in Table 7-5.

| | Stage 1 | Stages 2&3 | Biquad of auto-Q tuning |
|---|---|---|---|
| Normalized Size of $M_1$-$M_6$ of $-g_m$ cell | 2 | 1 | 1 |
| Bias transistor sizes of $-g_m$ cell | 12.9μm/1.2μm x 10 | 12.9μm/1.2μm x 5 | 4.2μm/1.2μm x 3 |
| Max. bias current of $-g_m$ cell | 480 μA | 240 μA | 265 μA |
| Max. $g_m$ of $-g_m$ cell | 231 μA/V | 116 μA/V | 130 μA/V |
| Poly-silicon Resistance | 8.67KΩ | 17.37KΩ | 52.4 KΩ |
| Capacitor Q | 55 | 55 | 55 |
| Number of unit capacitors used | 12 | 6 | 2 |
| $R_p$ of capacitor | 2.5 KΩ | 5KΩ | 15 KΩ |
| Conductance due to shifted $\omega_o$ | j2.1KΩ | j5.2KΩ | j15.6KΩ |
| Uncompensated conductance | 506 μA/V | 253 μA/V | 0 |
| Q max. after compensation | 14 | 14 | ∞ |
| Extra $-g_m$ required for nominal Q | 471 μA/V | 235.5 μA/V | 0 |

Table 7-5 Calculated results of the effects of finite capacitor Q to the biquads

The calculated result is close to the measured one and thus can explain the pheonomenon. The reason why the maximum $g_m$ of the $-g_m$ cells are not scaled between the main filter biquads and the generic biquad in the Q tuning loop is that the differential pairs above the bias transistors are not scaled as the bias transistors. The drop of $V_{ds}$ of the bias transistor due the increase of $V_{gs}$ of the differential pair of the generic biquad when the bias current rises is smaller than that of the main filter. As a result, the simulated bias current of the negative $g_m$ cell of the generic biquad is less limited by the $V_{ds}$ of the bias transistor. A comparison among the simulated bias currents of the $-g_m$ cells of each biquad are shown in Fig. 7-9. When the supply voltage is increased to 3V, the maximum bias currents increase by about 100%. This corresponds to an increase of $-g_m$ by 41%. The calculated

maximum Q for each biquad stage of the main filter increases from 14 to 19. This agrees with the measured Q of each stage which increases from 7 to 10. This corresponds to an increase of the Q of the whole filter from 14 to 20.

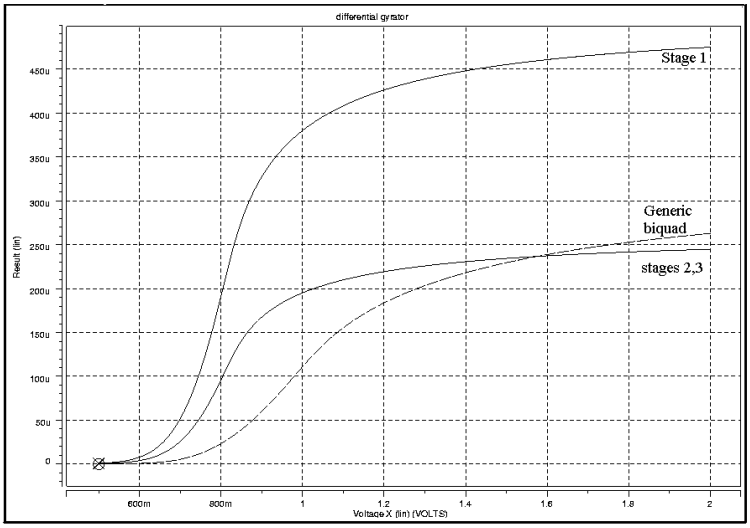



Fig. 7-9 Bias currents Vs Q tuning voltage of the $-g_m$ cells of the three biquads

The bandwidth decreases with lower $f_o$ because the Q of the capacitors increases with a lower $\omega$. The loading effect is thus less for lower frequencies and the output impedance can be boosted up more. For the first filter design, the finite Q of the MOS capacitors has the similar effect. The $-g_m$ compensation of the first stage has not enough $-g_m$ to significantly boost up the impedance while the latter two stages could still provide enough compensation with the increase of the bias current to the gyrators. This increased the $f_o$ as well. That is why a high-Q could still be restored at 92.5 MHz.

# Chapter 8 Conclusion

$G_m$-C filters are capable of operating at 70 MHz as bandpass filters. However, the limited linearity and noise performance of $G_m$-C filters pose challenges for them to be employed in monolithic GSM receivers. In this research, the relationship among power, noise and linearity of a filter was fully investigated. With fixed power consumption, the noise of a filter is intrinsic and can only be minimized by increasing the gain of the filter at the cost of linearity degradation. In order to optimize the performance of the $G_m$-C filter, linearization techniques are investigated and proposed.

Another shortcoming of $G_m$-C filters is the wide variation of center frequency and Q due to process variations. This requires the $G_m$-C filter to be tunable over a wide range. Automatic tuning of frequency and Q is also implemented. Several automatic tuning techniques are compared and finally a charge-pump PLL is employed for the automatic frequency tuning and a magnitude-locked loop with a multiplier for approximated adaptive tuning is used to control the Q of the filter.

Two filters were fabricated and tested. Both are 6-th order filters and are constructed by cascading 3 biquad stages. The filters are intended to be used as IF filtering in GSM receivers. The desired Q of the filter is 390 and the center frequency is 70 MHz.

The first one is designed with cross-coupled $g_m$ cells as the input $g_m$ cells and unbalanced $g_m$ cells as the $g_m$ cells for the gyrator. MOS capacitors are used as the loading. The filter

is fabricated in 0.8 μm HP process. The chip area is 0.88 x 0.65 $mm^2$. Strategic allocation of the gain among the 3 stages optimizes the linearity and noise performance with a power consumption of 80 mW with a single 3-V supply. The measurement result, however, shows a Q of below 5 for the first stage while the nominal center frequency of the latter 2 stages has shifted to 92.5 MHz with a Q of 190. The gain has dropped to 8 dB. The measured output noise power of the last 2 stages is –77 dBm which corresponds to an *input* equivalent noise of 413 μV or 923 nV/√Hz. This corresponds to a noise figure of about 43 dB. The measured $IIP_3$ of the 2 stages is –4 dBm with the 1-dB compression point being –38 dBV. The measurement results are close to the simulated ones.

The second filter employs actively biased $g_m$ cells for all the $g_m$ cells of the filter. Modification of the $g_m$ cell has been carried out to improve its linearity. Linear capacitors are used as the loading instead of MOS capacitors. Automatic tuning circuitry is also implemented. The filter is fabricated in 0.5 μm HP process. The chip area is 0.8 x 1.2 $mm^2$. The power consumption is 120 mW with a single 2.5 V supply. For the layout of the filter, the method of using generic $g_m$ cell units to construct the 3 stages is employed for good matching. The measured Q of the filter is about 14 with a gain of –51.5 dB at 70 MHz. The noise measured for the first stage is about –86 dBm which is equivalent to an input equivalent noise voltage of about 984 μV. On the other hand, the noise measured for each of the $2^{nd}$ and $3^{rd}$ stage is –84 dBm which is equivalent to an input noise voltage of 6.2 mV of each stage. The total noise figure of the filter is 90 dB due to the low gain. The measured noise agrees with the simulated result after gain adjustment.

The linearity could not be accurately measured because the gain of the filter is too low. Interferers with input strength above 0 dBm has to be injected so that the intermodulation product can be seen. Such strength has already saturated the filter.

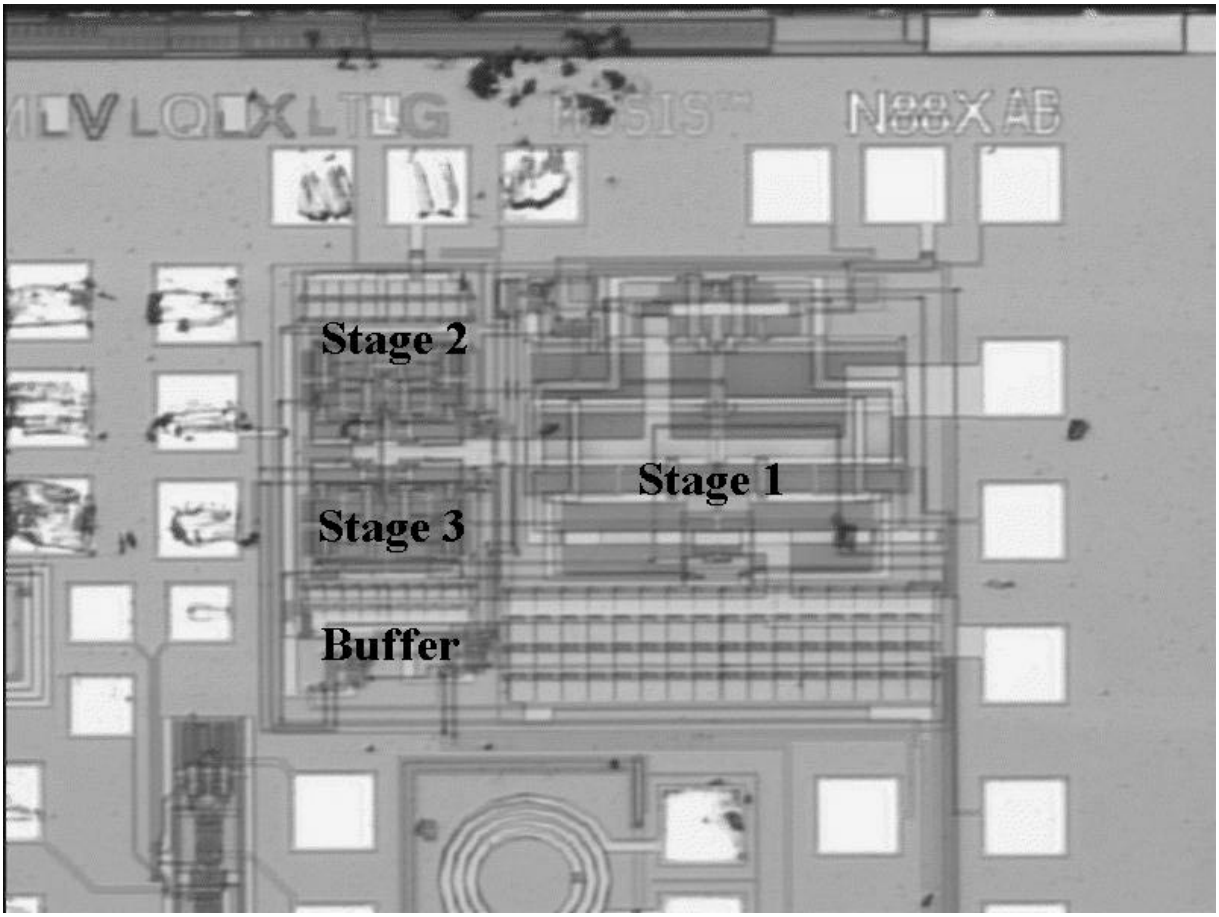
The master biquad in the automatic Q tuning loop, however, works properly. The measured Q of the biquad is 200 with a center frequency of 70 MHz and a gain of 0 dB as designed. The frequency tuning range is from 25 MHz to 72 MHz, and is limited by the common-mode instability. The maximum center frequency increases to 82 MHz by increasing the supply voltage to 3 V. The measured output noise power is –81 dBm and the corresponding input equivalent noise voltage is 630 μV or 1.41 μV/√Hz. The $IIP_3$ is +5 dBm. The measurement results agree with the simulated ones after gain and size adjustment and mapped back to the filter performance. The linearity has, however, degraded by 5 dB.

The limited Q of the linear capacitors, which was not considered quantitatively during the design stage, is suspected to account for the difference of the Q of the whole filter and the master biquad of the Q tuning loop and the low Q of the first filter design at 70 MHz. The limited capacitor Q adds an extra positive conductance to the output that causes the low Q of the filters. The negative $g_m$ cell of the master biquad of the Q tuning loop has enough $g_m$ to compensate the extra loading while the one in each stage of the filter cannot. Special attention has to be paid on the capacitor Q during the further design of the filter.

The automatic loops function properly in the sense that they show the negative feedback action. The VCO of the automatic frequency-tuning loop works properly for frequencies from 35 MHz to 68 MHz because of the common-mode instability again. Like the case of the biquad of the Q tuning loop, the situation can be improved by increasing the supply voltage. The maximum frequency increases to 80 MHz with a supply of 3 V. The Q tuning loop, on the other hand, functions properly within the nominal frequency range of the master biquad. The master biquad is not over-compensated to oscillation for a range of center frequency variation of ± 8MHz showing that the tuning loop can compensate the change in Q due to the variation of the center frequency without causing oscillation.

# Appendix Chip photos of the two filter designs

## I. First filter design



## II. Second filter design