Hong Kong University of Science and Technology

10-MHz 60-dB Dynamic-Range 4th-Order Butterworth Lowpass Filter

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by

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To

my mother and dad

Contents

List of Figures

List of Tables

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Abstract

CMOS circuits for integrated continuous-time analog filters, applicable to 10-bit resolution video-rate signal processing systems, are presented. The filters utilize transconductance-C integrators as fundamental building blocks.

A differential transconductance element comprising a source-coupled pair with a poly-silicon degeneration resistor and a cross-coupled high-impedance load is described. With this transconductor, tunable integrators for very-high-frequency integrated filters can be realized. Good high-speed properties stem from the absence of internal nodes, which pushes non-dominant poles to the gigahertz range. These integrators are optimized for the maximum dynamic-range of greater than 64-dB, which occurs for input signal levels of 200-mV.

Dual feedback loops stabilize circuit performance against temperature- and process-variations. The resonant frequency of a master VCO, comprising back-to-back integrators, tracks the frequency of a stable reference clock by virtue of an on-chip PLL. The VCO control voltage is broadcast to all matched transconductors, thus accurately controlling the natural frequencies of the filter. A separate Q-tuning loop controls the dissipation of the integrator, thus insuring a 90-degree phase shift at the resonant frequency.

Experimental results of a 10-MHz, 60-dB dynamic-range, 4th-Order Butterworth lowpass filter, realized in a 0.8-μm CMOS process, are given. The filter consists of a cascade of two biquadratic sections. Results show total harmonic distortion of less than -60-dB for a 130-mV input signal at 2-MHz. Third-order inter modulation distortion is below -56-dB for inputs of 8-MHz and 9-MHz. The measured filter responses agree with simulation results for the passive prototype filter to within 10%. The circuit occupies an area of 0.91mm $\times$ 0.65mm $=$ 0.59mm^2, and dissipates 40-mW from a single 5V supply.

Chapter 1

Continuous-Time Integrated Filters: An Introduction

Electronic filters are used in virtually all communication and signal processing circuitry. Among their many functions, filters are needed to select channels from a wide frequency spectrum, reject noise, prevent aliasing in sampling systems, and smooth discrete-time outputs. As modern electronics systems become more and more highly integrated, the associated filters should also be integrated. Therefore, it is necessary to investigate filter structures that are realizable as integrated circuits (ICs).

Because filters comprise only a fraction of a complete system, they need to be low in power and small in size to allow room for the integration of extensive signal-processing functions on the same IC. In addition the filters must not limit the performance of the overall system. Therefore, the dynamic-range of the filter must exceed that of the system. As bandwidth continues to broaden, IC filters must keep pace and operate at ever-higher frequencies. The goal of this research is to design a filter, realizable in a standard digital CMOS process, that meets the above constraints and achieves a dynamic-range of 60-dB at 10-MHz. Such a filter will find applications in broadband communication systems, such as digital video, wireless telephony, and computer networking.

1.1 Background

To understand how the proposed filter design is related to previous work, we consider the evolution of IC filters from early passive RLC filters, to those available today. The frequency range over which various types of filters operate is summarized in Fig. 1.1. Nearly all IC filters are active, meaning that they require gain elements

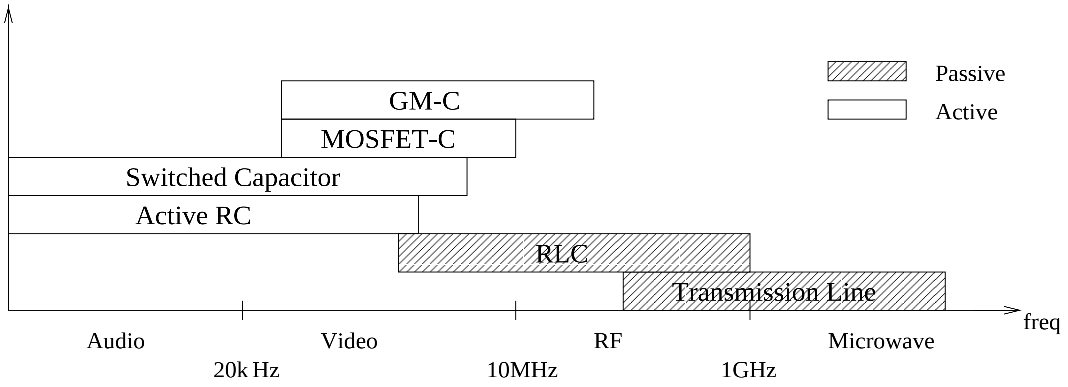


Figure 1.1: The Frequency Range of the Filters

to synthesize the desired transfer function. The motivation behind active filters lies in the desire to have inductorless filter realizations. It is well known that of the three passive RLC elements the inductor is the most difficult to realize in integrated form.[1] This is especially true at low frequencies, where inductors become bulky and have increased losses, or equivalently, lower Q-factors.

Despite this effort, the inductor has yet to disappear. For radio-frequencies (RF) an RLC filter still remains the best option in many cases. An inductor can have low-losses (high-Q), dissipates no power, and be virtually free of nonlinear distortion. IC designers face a difficult challenge to design integrated RF filters that approach the performance of their passive RLC counterparts.

[1]Integrated inductors require a huge area (500-μm $\times$ 500-μm for a 100-nH planar inductor), have a low quality factor (Q = 3–6) due to resistance in the metal winding, and have a large capacitance to the substrate, resulting in self-resonance at frequencies often well below 1-GHz.

1.1.1 Inductorless Filters

Research in active filters began in earnest in the late 1950s with work on opamp-based active RC filters. However, the demand for their existence, as well as the impetus for their mature development, should be credited to the rapid progress of IC technology in the mid- and late-sixties. As communication and instrumentation systems became smaller in size, due to increased utilization of ICs, RLC filters remained unchanged and represented the bulkiest portion of the system. A direct miniaturization of these filters in integrated form was thwarted, since passive LC technology is not compatible with the IC technology that dominates most of today's systems. The search therefore started for an alternative technology to implement filters without inductors.

Active Filter Principle

The inductor is needed to realize complex poles passively. However, RC networks can be used to realize complex transmission zeros. When such a network is placed in the feedback path of an opamp, the overall circuit will have complex poles, which can mimic those in an RLC circuit. Therefore, we can utilize active elements to move the poles of RC networks from the negative real axis into the complex $s-$plane as close to the $j\omega$-axis as necessary to produce a given filter response. The closer the natural modes are to the $j\omega$-axis, the more selective the filter will be [1].

Generally speaking, active filters are feedback structures designed to realize a given transfer function. The desired transfer function is obtained from the solution to the approximation problem, in which the ideal filter specification is approximated by one that is physically realizable. The active-filter design approach can be divided into two steps:

Select Gain Block : The first step consists of identifying and defining an idealized active element or gain block. For this element to be useful in the synthesis of active filters, it must be easy to use in the synthesis process, and easy to realize and construct using standard IC technology.

Follow Synthesis Procedure : The second step is to synthesize the filter using a methodology for the realization of a given filter transfer function for the selected active element together with frequency selective components, such as resistors and capacitors.

Various active elements, as well as synthesis procedures employing them, have been proposed [2]. A partial list includes : the Negative Impedance Converter (NIC), Negative Impedance Inverter (NIV), Positive Impedance Converter (PIC), Gyrator, Generalized Impedance Converter (GIC), Current Conveyor (CC), Operational Amplifier (OPAMP) and Operational Transconductance Amplifier (OTA).

Opamp-Based Active RC Filters

Despite the great variety of available methods, very few gain-elements and corresponding synthesis procedures have found their way into large-scale production as off-the-shelf items. The reason for this is primarily an economic one. For a device to become available at low cost, it has to be used in substantially large quantities. It follows that such a device has to be versatile enough to be of use in a number of applications. In the sixties and seventies the analog-circuit design community found these attributes in opamps. Therefore, opamp-based active RC filters were quite popular. However, these filters were typically hybrid circuits, which allowed the R's and C's to be well-controlled. In an IC the absolute spread in component values makes it nearly impossible to design a filter with moderate selectivity. In the eighties a new technique was developed, known as Switched-Capacitor (SC) filters.

Switched Capacitor Filters

Switched-Capacitor (SC) filters are also based on the use of opamps. However, the resistor is replaced with a switched-capacitor having an equivalent average resistance of T/C_G, where T is the period of an associated oscillator which is extremely stable. The time constant of an SC integrator is then $T(C/C_G)$, which is proportional to T and a ratio of capacitors. Both quantities can be also well-controlled and, therefore, reliably utilized in volume production. The disadvantage of SC filters is that they are sampled systems and need anti-alias pre-filters; they also need to maintain an oversampling ratio with the clock frequency being about 5–10 times higher than the maximum signal frequency. This limits the maximum signal frequency that can be processed by SC filters. These limitations have prevented wide-spread usage of SC filters at video-rates. Continuous-time filter structures then surfaced in an attempt to circumvent these problems.

Continuous-Time OTA-based Filters

In contrast to discrete-time analog signal-processing circuits, continuous-time analog circuits are free from Nyquist constraints, have no switching noise (as in switched-capacitor circuits), have no noise aliasing into the baseband, and do not need anti-aliasing or smoothing filters. Nonidealities of operational amplifiers and switches limit conventional switched-capacitor (SC) filters to frequencies that are lower than that for continuous-time filters.

Current-Mode vs. Voltage-Mode Filters : Current-domain signal processing has advantages within ICs, since stray-inductance effects are less severe in low-impedance circuits than are stray-capacitance effects in high-impedance circuits. Thus, current-mode circuits with low-impedance internal nodes are potentially faster than their high-impedance voltage-mode counterparts [3, 4, 5].

With the trend toward multi-media communication, higher bandwidths are needed. As a result, signal-processing systems are increasingly based on Operational Transconductance Amplifiers (OTAs), rather than on opamps, because of their simpler circuitry and improved frequency response. In monolithic filter structures, the OTA-C (G_m-C) approach normally uses operational transconductance amplifiers (OTAs) and capacitors.

Nowadays, continuous-time filters operating at cut-off frequencies exceeding 10-MHz constitute a large potential market in applications such as video signal-processing and magnetic-disk-drive read-channel systems. Several OTA-C filters have been realized in CMOS technology [6, 7, 8, 9, 10, 11, 12, 13], and more recently in BiCMOS [14, 15] and GaAs MESFET technologies [16] at frequencies approaching or beyond 10-MHz.

Process Insensitivity : A disadvantage of continuous-time filters, which is not found in SC filters, is that they are severely affected by process- and temperature-variations. Therefore, continuous-time filters usually require tuning of the circuits to yield accurate performance. A conventional master-slave automatic tuning strategy can be used. Some designers [7, 2] implement an on-chip phase-locked loop (PLL), which is the method employed here in this research. Others [14] incorporate a novel technique for setting the G_m value of the transconductor as a function of an external precision resistor. This technique, in conjunction with a poly-fuse wafer-sort trim technique or thin-film-resistor (TFR) laser-trimming [17], results in a filter with a frequency response independent of the power supply, temperature, and process. Thus, this technique eliminates the need for a PLL to tune the frequency response.

It is difficult to predict the dissipation in the gain-elements. This causes excess phase in the filter poles, which distorts the passband. Therefore, so called Q-tuning is also generally required to tune out dissipative effects. We use a Q-tuning loop in this design to desensitize the shape of the passband to process and environmental changes.

1.2 Goals of This Research

Despite the success of many continuous-time filters designs, the range of linear operation of OTAs has often been restricted, which in turn has precluded their use in many potential applications where low distortion is needed, such as in High-Definition-Television (HDTV) and broadband communications. A considerable amount of research [18, 19, 20, 21, 22, 23, 24] has gone into improving the linearity of OTAs and widening the input signal range over which OTAs exhibit linear operation. Fig. 1.2 shows the SNR (at THD = -40-dB) of filter designs reported in recent literature (see Bibliography).

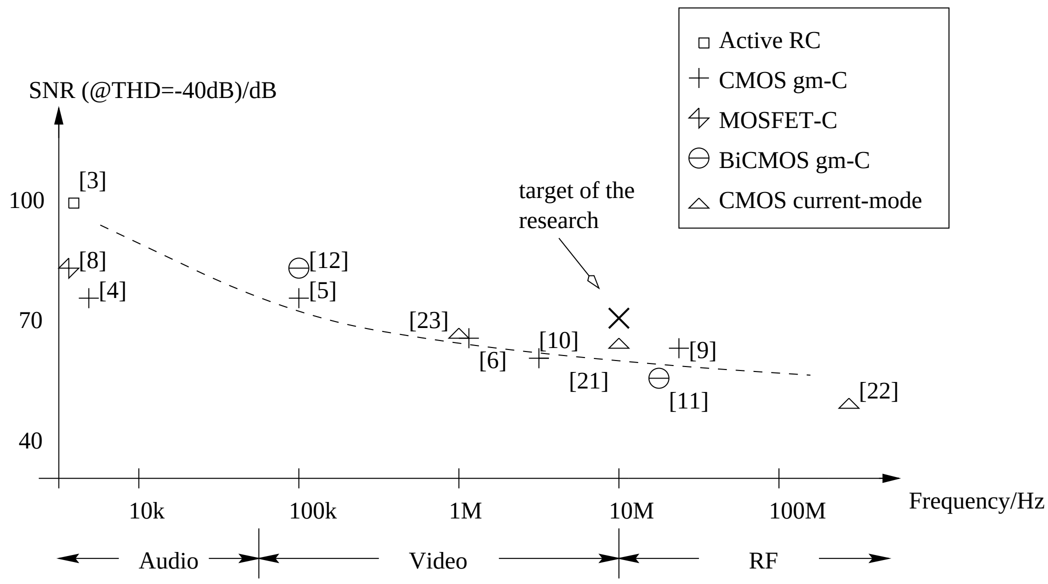


Figure 1.2: The trend of the SNR of continuous-time filters reported in the recent literature

Many of the reported designs use linearization techniques, which rely on either feedback or matching, to reduce distortion. Both techniques have limitations at high speeds, where loop gain is low and uncontrolled parasitic elements degrade high-frequency matching.

The goal of this research is to design, fabricate and test a CMOS continuous-time lowpass filter which achieves a dynamic-range of 60-dB at 10-MHz. As shown in Fig. 1.2, the target SNR of the proposed filter is beyond the values reported recently. *Therefore, the primary challenge of this design is to choose an acceptable gain element and optimize the circuit performance for low-noise and low-distortion in order to extend the dynamic-range of this filter beyond that currently available.*

Definition of Dynamic-Range : For high-resolution systems, the IC filter must have a large dynamic-range. Often the dynamic range is defined as the ratio of the rms signal level at a given level of total-harmonic-distortion (THD) or total-intermodulation distortion (TIMD) divided by the total rms noise in a specified bandwidth. Typically, the distortion level is chosen to be 1% (40-dB). However, in many systems the distortion (THD or TIMD) is just as important as the noise — if not more. Here, we define a much more stringent dynamic-range measure as

$$\text{Dynamic Range} = \max(\text{SNDR}) \quad \text{where} \quad \text{SNDR} = 10\log_{10}\left[\frac{P_{Sig}}{P_{Noise} + P_{Dist}}\right]. \tag{1.1}$$

The SNDR represents the Signal-to-(Noise-plus-Distortion)-Ratio, where the distortion power, P_{Dist}, can be either the THD or the TIMD. The worst case of the distortion power, but most appropriate measure, is TIMD for a two-tone test near the passband edge. This is the criteria we will adopt here.

1.3 Application of IC Filters to the Digital Cable-TV and Cable-Modem Markets

The application of high-speed analog-to-digital converters in state-of-the-art video systems makes considerable demands on their accompanying anti-aliasing filters. At video frequencies, highly-oversampled systems are usually impracticable. Consequently, Nyquist filters with sharp selectivity (having attenuation curves with regions of steep slope) are needed. For the integrated filter described in this thesis, we have adopted a set of specifications based loosely on the baseband video-receiver requirements.

Proposed next-generation digital cable television services (CATV) are slated to deliver far greater information capacity and channel versatility than current analog cable television systems, while using the existing cable infrastructure. Broadband QAM systems can accommodate data rates up to 40-Mb/s in a standard 6-MHz video channel, which can contain 3 compressed TV channels in the bandwidth of one previous NTSC band. Thus, there is great demand for circuit designs to meet this growing market. However, this task is difficult: generally speaking, the signal received is quite weak (-50 to -30-dBm) and corrupted with noise and inter-symbol interference. In order to strengthen the signal and minimize the noise, a *signal-*

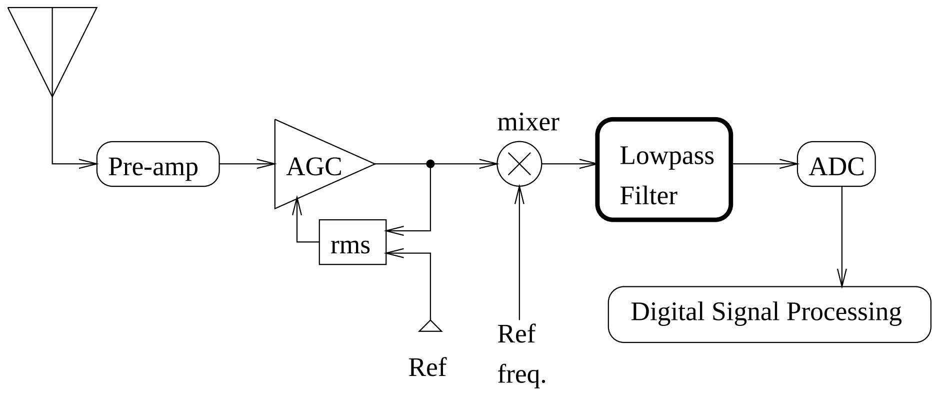


Figure 1.3: Signal-conditioning circuit (SCC)

conditioning circuit (SCC) is essential at the front-end of the signal-processing circuitry.

Fig. 1.3 shows a highly simplified block diagram of an SCC where the anti-aliasing lowpass filter developed in this thesis is represented by the bold-outlined block. The low-noise pre-amplifier establishes the system signal-to-noise ratio (SNR). The AGC maintains accurate signal levels in the presence of receiver-gain uncertainties and signal variations. The received signal is demodulated to produce a baseband video signal [17]. The anti-aliasing filter bandlimits this signal prior to analog-to-digital conversion (ADC). The demanding target specifications for this research were extracted from those needed for a CMOS continuous-time lowpass filter for a digital CATV front-end with a resolution equivalent to 10-bits. The complete specifications for this filter are listed in Table 1.1. A 4th-Order Butterworth lowpass filter will

Input signal :	200 mV
Output level :	200 mV
Linearity (THD) :	< - 60dB
Dynamic range (SNDR) :	> 60dB
Stopband attenuation :	> 60dB
Passband edge :	8 $\sim$ 10.0 MHz
Stopband edge :	79.44 MHz
	or 89.56 MHz

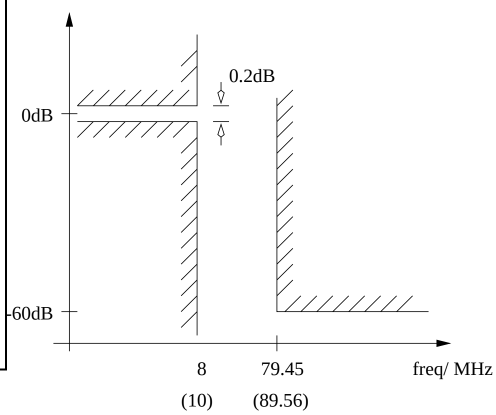


Table 1.1: Specifications of the lowpass filter

satisfy the above specifications. However, great care must be taken in the design in order to achieve a dynamic-range above 60-dB.

1.4 Outline

This thesis is organized in the following way. Chapter 2 introduces some basic concepts relevant to OTAs, such as linearity and noise performance. With this background information, a practical transconductors are presented in the same chapter.

Chapter 3 reviews relevant filter topologies and terminology, particularly cascaded biquad filters based on building blocks involving OTAs and capacitors. Simulation results are included.

Chapter 4 describes the master-slave architecture that enables automatic tuning. Dual feedback loops are described, which desensitize the circuit's performance against process and temperature variations. Simulation results are included.

Chapter 5 presents details of the VLSI implementation of the filter. Layout considerations are also covered.

Chapter 6 presents the measured results of the filter. The floor-plan and layout are included. Testing techniques are discussed. Some improvements in the circuits are suggested and the implementation of these improvements in a second-generation filter, fabricated in a 0.5-μm CMOS process are outlined. Finally, a brief summary of this research is given.

Chapter 2

Low-Distortion Transconductor

2.1 Introduction to OTA Circuits

In this section we will review some of the basic properties of Operational Transconductance Amplifiers (OTAs). It can be shown that a large class of transfer functions can be synthesized using four basic operations: integration, scaling, summation and inversion. An OTA can easily perform an integration when loaded with a capacitor. Scaling can be accomplished by choosing the relative magnitude of the load capacitor, the G_m of the transconductor, or both. Summation comes for free in the current domain, as signal currents can be summed simply by tying them to the same node. In a fully-differential implementation, inversion also comes for free, as the positive and negative signal can be crossed to invert the signal. Therefore, a large class of filters can be designed using only OTAs and capacitors.

2.1.1 Operation of an OTA

In the ideal case, an OTA is a voltage controlled current source described by the relation:

$$I = g_m(V_+ - V_-) \tag{2.1}$$

where the input and output impedances are both infinite. Fig. 2.1a shows the circuit symbol of the OTA in a differential configuration and Fig 2.1b shows the single-ended OTA integrator. The transconductor designed in this research is fully-differential, which provides a good common-mode rejection ratio (CMRR) and power-supply rejection ratio (PSRR). Therefore, if extraneous signals contaminate both sides of the transconductor equally, the error will appear as a common-mode signal and be rejected by the differential circuitry. The single-ended configuration is shown here for simple analysis purposes only.

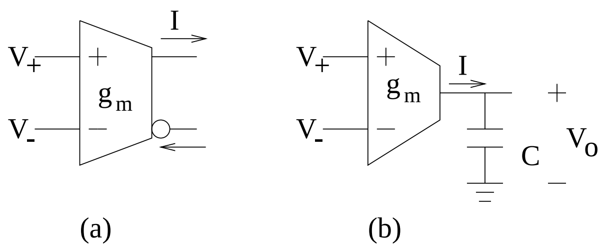


Figure 2.1: (a) Circuit symbol in differential configuration and (b) single-ended OTA integrator

In Fig. 2.1b, an OTA-C integrator is formed by connecting a capacitor C at the output. The voltage V_o is given by

$$V_o = \frac{g_m}{sC}(V_+ - V_-) \tag{2.2}$$

We can decompose the OTA integrator into 3 parts, namely:

- *The V-to-I converter;* this converts the input voltage V into the current change i superimposed on the nominal bias current I.
- *The ideal current source loading I;* This provides the high output impedance of the OTA, only allowing the current i to pass through the capacitor C.
- *The capacitor C;* The current i charges the load C, to provide the output voltage $V_o = \frac{1}{C}\int idt$.

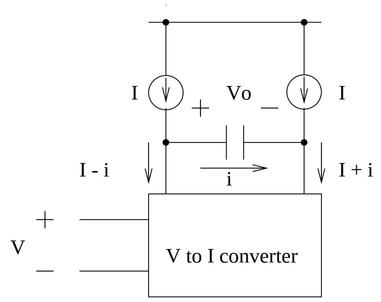


Figure 2.2: OTA Schematic

In addition to featuring superior high-frequency performance, transconductors are tunable. The time-constant of an OTA-C integrator is determined by the ratio of a fixed capacitance to an *electronically tunable* transconductance: $\tau = \frac{C}{gm}$.

2.1.2 High-Speed Advantage of OTAs

A major advantage of OTA-based continuous-time filters is their extremely large frequency range. A comparison of the useful frequency range for both opamp- and OTA-based circuits is shown in Fig. 2.3. The OTA has a significant speed advantage over opamp-based circuits. A minimum opamp gain (around 30-dB) is needed for well-behaved opamp-based filters. Otherwise the gain-bandwidth (GBW) effects of the opamp (lower loop-gain, uncontrolled phase-shifts) degrades the characteristics of the system. For example, a filter designed using single-pole opamps, will attain a useful frequency range on the order of $\frac{GBW}{30}$. For low-power CMOS opamps GBW is approximately 100–300MHz. This makes it extremely difficult to design high-frequency opamp-based filters above 10-MHz. Because the OTA-based integrator is implemented in open-loop mode, the requirement to keep the loop-gain large to reduce unwanted effects is no longer necessary. As a result, the useful frequency range of such circuits is limited only by the OTAs gain-bandwidth product.

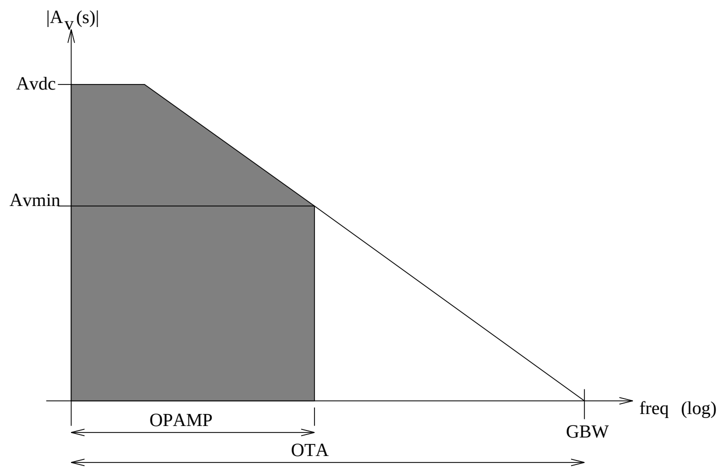


Figure 2.3: Frequency response for a typical single-pole opamp / OTA.

The performance of the filter for a given architerture will depend on the performance of the OTA. Likewise, different filter architectures can be chosen to provide immunity to some of the performance limitations of OTA. Thus, the transconductor becomes a crucial part of the filter design, since it may limit the overall linearity, frequency response, and noise performance attainable from any system in which it is used. Therefore, in order to optimize the overall filter performance, it is essential to study the performance limitations of OTAs and consider how these affect the performance of the overall filter.

2.1.3 Performance Limitations of the OTA

In classic integrated OTA-C filters, the OTA acts as a voltage-to-current transducer. The capacitor is either a poly-poly capacitor (provided two poly layers are available), or a sandwich composed of metal and poly layers. In the ideal case, the capacitor is a noiseless device with $(kT)/C$ noise associated with it's leakage conductance. Provided that C is chosen large enough, the noise level of the associated integrator is determined primarily by the OTA. In the past, a major drawback of OTA-C filters has been the lack of very linear and efficient voltage-to-current converters. Due to the relatively high nonlinearity of first-generation V-to-I converters, the harmonic distortion components of earlier designs were large, being on the order of -40-dB for input signals up to 1-Volt at frequencies above 1-MHz.

2.1.4 Dynamic-Range Optimization

The performance of OTA-C filters depends on: (i) the OTA circuit, which is the main noise and distortion contributor in the filter, and (ii) the OTA-C filter structure. Concerning the latter, even though several filter structures ideally can provide the same transfer function, when real OTAs are considered, the resulting transfer functions yield quite different behaviors with respect to frequency deviations, noise-bandwidth distortion, sensitivity and quality-factor (Q) enhancement.

In order to optimize the dynamic-range of an OTA-C filter, we should first optimize the dynamic-range of the OTA integrators that constitute the filter. The non-linearity of the OTA directly degrades the system dynamic-range. Such non-linearity shows up as a signal-dependent delay, which can severely degrade the performance of any practical tuning loop. The major source of nonlinearity in CMOS transconductance amplifiers is the voltage-to-current conversion mechanism in the input stage. Most recently, the use of linearized topologies has increased the signal-to-harmonic-distortion-ratio (SNDR) of continuous-time filters [18, 19, 21, 22]. OTA-C filters with signal-to-noise ratios (SNR) in the range of 60–90-dB are feasible with very linear and efficient transconductor [9, 10, 7]. This SNR range is comparable with that obtainable with SC filters, however, OTA-C filter extends operation by nearly an order of magnitude in frequency.

2.2 Non-idealities of an OTA Integrator

Finite Output Impedance : In reality, the OTA has finite input and output impedances that can be modeled as shown in Fig. 2.4. In many applications it is not only the intrinsic, and always-present frequency dependence of g_m that imposes limits on the transconductance operation, but also the two time-constants set by the input and output impedances in combination with possible loading effects. The overall transfer function, when these parasitics are included, becomes

$$V_o = \frac{g_m(s)R_o}{1+sR_oC_o}(V_+ - V_-) = \frac{A_{v_o}}{1+sR_oC_o}(V_+ - V_-). \tag{2.3}$$

The effect of C_0 can be absorbed by the load of the OTA, C_{out}. In fact, C_0

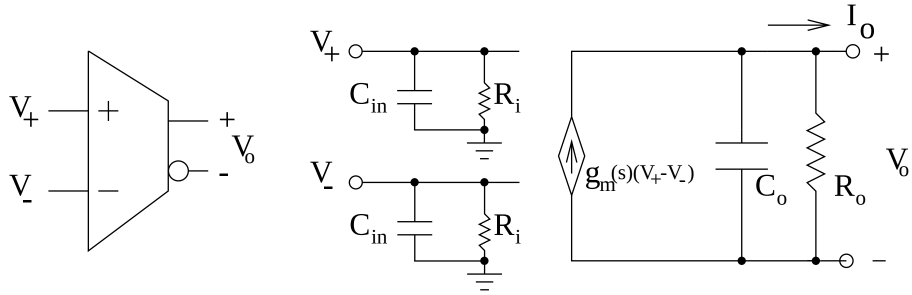


Figure 2.4: Circuit symbol and the small-signal equivalent circuit of an OTA.

(the bottom-plate parasitic) in many cases, can be up to 25% of the value of the integrating capacitor C. The output resistor R_o will make a lossless integrator into a lossy one. The (ideal) unity gain frequency for a voltage integrator is, $\omega_o = \frac{g_m}{C}$ and the phase is -90^o. In this case, the voltage gain remains roughly unity, but the phase at $\omega = \omega_o$ becomes

$$\begin{aligned}\phi = -\tan^{-1} g_m R_o &= -\tan^{-1} A_{V_o} \\ &= -\frac{\pi}{2} + \tan^{-1}\frac{1}{A_{V_o}},\end{aligned}$$

from which, we see that the phase lead of the integrator at the unity-gain frequency is given by

$$\phi_R \sim \tan^{-1}\frac{1}{A_{V_o}} = \tan^{-1}\left(\frac{1}{\text{dc gain}}\right) \tag{2.4}$$

2.2.1 Frequency-Dependant Transconductance:

The transconductor will have parasitic poles that cause $\mathrm{g_m}$ to be frequency dependent. This will effect both the magnitude and the phase of $\mathrm{g_m}$. The magnitude will not vary significantly near the natural frequencies of the filter and is much less critical to the performance than the excess phase. We can, therefore, model the transconductance as an allpass function, such that, $g_m e^{-sT_p} \cong g_m(1 - sT_p)$ for $\omega T_p << 1$; where T_p is the inverse of the effective 3-dB radian cutoff frequency ω_p due to the parasitic pole, which is designed to be much larger than the resonant frequency of the integrator ω_o. Thus, for $\omega = \omega_o$, the gain is still unity, but the phase yields

$$\phi_q = -\tan^{-1}\omega_o T_p - \frac{\pi}{2} \tag{2.5}$$

where $\omega_o T_p << 1$. The term $\tan^{-1}\omega_o T_p \approx \omega_o T_p$ is known as the excess phase.

Simultaneously taking into account the effects of the parasitic poles of the transconductor, T_p and the dissipation in the integrator R_o, the phase of the actual integrator phase becomes:

$$\phi = -\frac{\pi}{2} - \tan^{-1}\omega_o T_p + \tan^{-1}\frac{1}{A_{V_o}} \tag{2.6}$$

which can be approximated as

$$\phi \cong -\omega_o T_p + \frac{1}{A_{V_o}} - \frac{\pi}{2} \tag{2.7}$$

$$\phi \cong -\frac{\omega_o}{\omega_p} + \frac{1}{A_{V_o}} - \frac{\pi}{2} \tag{2.8}$$

We therefore see, that for a first-order approximation, the excess phase is due to the ratio of the signal frequency to the parasitic pole frequency ω_o/ω_p, and the dc-loss of the integrator (inverse of the dc gain).

2.2.2 Design Considerations to Reduce Excess Phase

The excess phase of the integrator limits the designers control over the actual transfer function. In precision designs this excess phase should be eliminated. When these non-idealities are considered in a two-integrator-loop biquadratic (biquad) filter, a severe quality factor (Q) deviation is obtained. For instance, the actual Q_a of the filter becomes

$$Q_a \cong \frac{Q}{1 + 2Q(\frac{1}{A_{V_o}} - \omega_o T_p)} \tag{2.9}$$

Therefore, high-Q natural frequencies require a very small excess phase.

One possible method to eliminate the excess phase is simple cancellation. From (2.7) it is clear that at a critical frequency, $\omega = \omega_c = \frac{1}{A_{V_o} T_p}$, the non-idealities cancel and the ideal $-\frac{\pi}{2}$ phase is reachable. However, in reality, the cancellation approach is not a practical method to achieve an exact 90-degree phase shift. Neither the parasitic pole location, nor the dissipation, are well controlled; both will vary significantly with process-parameters. Furthermore, the nonlinear variations of A_{V_o} and T_p with respect to the control bias voltage of the OTA, will make this cancellation only valid at one bias point.

A sound design approach requires A_{V_o} to be as large as possible, and T_p to be as small as possible. The effect of A_{V_o} can be partially compensated by using OTAs with large output impedance stages (i.e., folded cascode, regulated cascode). The effect of the parasitic pole T_p requires a fast OTA. However, this effect can be reliably canceled by using a phase compensation-circuit tuning systems which operates as a closed-loop negative feedback system and relies on the matching accuracy between identical g_m cells.

Deviations in Q are dependent on both R_o and T_p and also on the biquadratic OTA-C architectures. Thus, for a set of filter specifications, not only the OTA characteristics must be considered, but also the filter architecture. The topic of choosing the filter architecture will be considered in greater detail in Chapter 3. In the following sections initial design constraints of the OTA will be discussed.

2.3 OTA Design Constraints

In the design of a linearized transconductance input stage, linearity is only one of many important specifications that allows different designs to be compared. Other important criteria that must be taken into account are as follows:

Total input capacitance : The input capacitance of a transconductance amplifier, C_{in}, as shown in Fig. 2.4, becomes part of the load capacitance of the previous stage. Moreover, the input capacitance is signal-dependent, so it should be kept small to reduce high-frequency distortion.

The noise excess factor (NEF) : The NEF indicates how much more input-referred noise is generated [22] by the V-I converter than by a single transistor with the same transconductance g_m. Large values of NEF result in low effective signal-to-noise ratios (SNRs). V-I converters in which non-linear terms are canceled by subtracting currents, generally have high, to very-high NEF figures. This makes these techniques unsuitable for filter applications requiring high dynamic range.

Symmetry and similarity of the transistor in the cell : Many linearization schemes perform well under nominal conditions, but degrade heavily if some parameters of the technology, such as the channel mobility μ of the MOS transistor, changes. Also, if the transistors are mismatched, the nonlinear terms cannot be totally canceled, thus increasing distortion. As a result, circuits that are built with all critical transistors of the *same* type, having *identical* aspect ratios ($\frac{W}{L}$) and fabricated *closely* together with the same *orientation* in the *same* well, will perform much better than circuits that rely on transistors of different aspect ratios, and definitely better than fool-hardy designs that rely on matching between NMOS and PMOS transistors, to linearize the V-I characteristic.

Power and area : In integrated mixed analog-digital circuits, the analog portion of the circuit usually consumes less area than the digital sections. Therefore, minimization of the area of the filter should not be given the highest priority, especially if it comes at the cost of reduced performance. However, the total power consumption is relatively more important, especially for high-frequency applications, where the analog sections, though small in area, can consume as much power as the larger digital sections.

After considering the non-ideal effects of transconductors, we can develop the following list of objectives for the improved design of a linearized transconductance element.

Reduce C_{in} A linearized transconductor should employ only a single transistor gate connected to the differential input in order to minimize the input capacitance.

Low Sensitivity to Process Variations The linearized transconductor should have low sensitivity to mismatch errors. This means that the transconductance element might consist of many transistors, each of which has a less-dominant impact on the overall performance. In this way, the random device-parameter deviation will be averaged out.

Regular Layout to Improve Matching Accuracy A linearized transconductor should consist of transistors of the same aspect ratios, put in the same well, with the same orientation. As a result, the systematic and random variations in the technological parameters of a given circuit will be minimized.

Tunability The transconductance g_m should be made tunable to allow for automatic tuning to compensate for errors due to the absolute inaccuracies of on-chip components. This will be discussed further in chapter 4. This tunability tends to limit the dynamic range, because extra noise or distortion is introduced, and in most cases, the maximum signal level, before clipping, is decreased.

With these objectives in mind we now have a criteria in which to compare competing OTA designs.

2.4 Summary of Dynamic-Range Limitations: Noise and Distortion

In order to optimize an OTA for maximum dynamic-range we need to consider two fundamental limitations: noise, and distortion. Noise will limit the lowest signal level that the circuit can distinguish without being drowned in the background noise. Distortion will limit the largest signal level before nonlinearities dominate the error.

It is important to have a solid background on the analysis of both noise and distortion before proceeding to design the OTA for this research. A brief review of noise in CMOS circuits is given in Appendix A and distortion analysis if reviewed in Appendix B. The basic equations that we need for the following analysis are given below.

Noise The noise in a MOSFET consists of low-frequency noise, which is process dependent and is due to traps in the the oxide among other contributing factors. The spectral density of this noise is

$$\overline{v_{nf}^2} = \frac{K}{C_{ox}WL}\frac{\triangle f}{f} \tag{2.10}$$

The other source of noise is independent of processing. This noise is a physical limitation of the electronic device. In a MOSFET the channel current is modulated by the thermal noise in the channel. This noise is constant with frequency. When referred to the gate of the transistor, this current noise can be expressed as a voltage noise. The spectral density is given by

$$\overline{v_{nT}^2} \simeq \overline{(i_{nT}/g_m)^2} = \frac{8}{3}\frac{kT}{g_m}\triangle f \tag{2.11}$$

Therefore, we have the fundamental relationship that the noise power at the gate of a transistor is inversely proportional to g_m .

Distortion The nonlinear distortion of a circuit will generate harmonics when a single sinusoid is applied at the input. If a multi-sinusoidal input is applied, the output can have spurious frequencies which are not contained in the input signal. For circuits that are approximately linear, we use the Taylor series to model the nonlinear perturbations and make some simplifying assumptions due to the fact that these distortion component are small with respect to the linear part of the signal.

The fundamental results, which are derived in Appendix B are that if the transfer characteristic can be expressed as a power-series expansion around the quiescent operating point (x_o, y_o):

$$y - y_o = a_1(x - x_o) + a_2(x - x_o)^2 + a_3(x - x_o)^3 + \cdots, \tag{2.12}$$

then the harmonic distortion of the circuit is given by

$$\begin{aligned} \mathrm{HD}_2 &\triangleq \frac{\text{Signal amplitude at } 2\omega}{\text{Signal amplitude at } \omega} \approx \frac{1}{2}\frac{a_2}{a_1}\rho_x \\ \mathrm{HD}_3 &\triangleq \frac{\text{Signal amplitude at } 3\omega}{\text{Signal amplitude at } \omega} \approx \frac{1}{4}\frac{a_3}{a_1}\rho_x^2 \end{aligned} \tag{2.13}$$

If the circuit is analyzed anti-causally, such the the input is written as an explicit expression of the output, where

$$x - x_o = b_1(y - y_o) + b_2(y - y_o)^2 + b_3(y - y_o)^3 + \ldots \tag{2.14}$$

Then the harmonic *pre*-distortion is defined similarly,

$$\begin{aligned} \mathrm{HP}_2 &\approx \frac{1}{2}\frac{b_2}{b_1}\rho_y \\ \mathrm{HP}_3 &\approx \frac{1}{4}\frac{b_3}{b_1}\rho_y^2 \end{aligned} \tag{2.15}$$

This is the distortion that would have to be added to the input to produce an undistorted output. It is often more convenient to write the equations of a circuit anti-causally, especially when the circuit contains negative feedback. Therefore, it is useful to have expressions to relate harmonic distortion to harmonic pre-distortion. For a circuit operating in the mild-distortion regime, the following equations provide these relationships

$$\mathrm{HD}_2 = \begin{cases} \mathrm{HP}_2, & \text{if } b_1 < 0 \\ \text{-}\mathrm{HP}_2, & \text{if } b_1 > 0 \end{cases} \tag{2.16}$$

$$\mathrm{HD}_3 = 2\mathrm{HP}_2^2 - \mathrm{HP}_3.$$

2.5 Brief Review of Possible OTA Designs

Based on the constraints mentioned above, we will consider two types of OTA designs. Both of them show good linearity and their transconductance is voltage-controlled. The first OTA design uses the triode-region operation of MOS transistor for the V-to-I conversion. The second makes use of square-law-operated transistors with constant source-bulk voltage to perform the transconductance operation.

2.5.1 A Tunable OTA using a Triode-operated Transistor

In this design [23], the OTA is based on the transistor operated in the triode region with its drain-source voltage V_{DS} kept small and constant. The drain current of an MOS transistor in the triode region can be expressed using a Taylor series expansion with respect to V_{DS}:

$$I_D = K[\alpha_1 V_{DS} + \alpha_2 V_{DS}^2 + \alpha_3 V_{DS}^3 + \cdots] \tag{2.17a}$$

with

$$\alpha_1 = 2(V_{GS} - V_T), \qquad \alpha_2 = -[1 + \frac{1}{2}\gamma(V_{SB} + \phi_B)^{-1/2}],$$
$$\alpha_i = \gamma A(i)(V_{SB} + \phi_B)^{-(2i-3)/2} \qquad \text{for } i \geq 3, \tag{2.17b}$$

where $A(3) = \pm\frac{1}{12}$, $A(4) = -\frac{1}{32}$, $A(5) = \frac{1}{64}$. Here we have defined $V_T = V_{FB} + \phi_B + \gamma(V_{SB} + \phi_B)^{\frac{1}{2}}$, and $K = \frac{\mu C_{ox}}{2}\frac{W}{L}$. V_{FB} is the *flat-band voltage* and V_{SB} is source-bulk voltage. Note that the coefficients α_i for $i \geq 2$ contain only functions of the source and substrate potentials and the process parameters. Therefore, by keeping both V_{SB} and V_{DS} constant, we have:

$$I_D = 2K(V_{GS} - V_T)V_{DS} + \text{DC term} \tag{2.18}$$

where the DC term depends on V_{SB} and V_{DS} only.

For the fully-differential configuration shown in Fig. 2.5a, M_1 and M_4 are identical and operate in the triode region with the same drain and source voltages. From (2.18), the output differential current is,

$$I_{out} = (I_{o1} - I_{o2}) = 2KV_{DS}V_{in}, \tag{2.19}$$

with $G_m = 2KV_{DS}$, and the DC terms canceled. This OTA behaves as a variable G_m cell with V_{DS} as a control input; the result is independent of V_T.

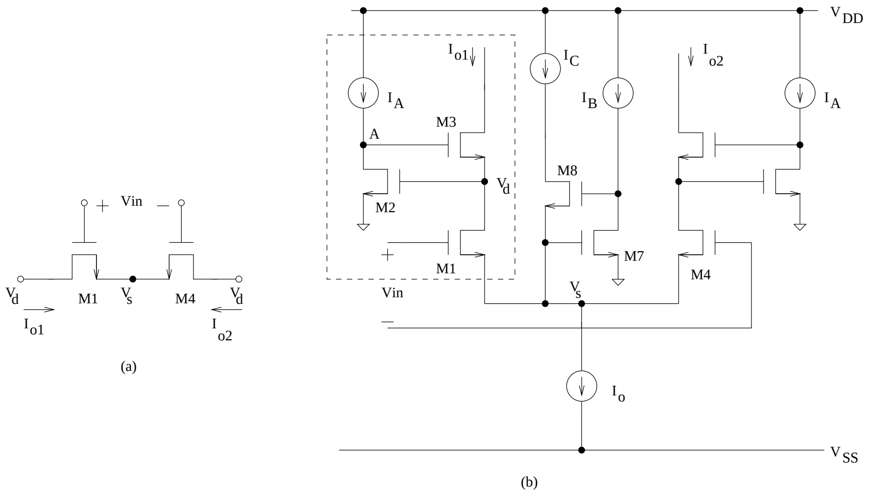


Figure 2.5: Basic concept of a tunable OTA

In Fig. 2.5b, M_1 and M_4 operate in the triode region, while the other transistors operate in the saturation region. Transistors M_2 and M_3, together with the current source I_A form a negative-feedback loop shown in the dotted-line box. This acts to keep V_{GS2} constant[1] at $V_{GS2} = \sqrt{\frac{I_A}{K_2}} + V_{T2}$.

[1]In small-signal terms, if V_d increases, V_{GS} of M_2 increases; For I_A constant, the voltage at

The output differential current is

$$\begin{aligned}(I_{o1} - I_{o2}) &= 2K_1(V_d - V_s)V_{in} \\ &= 2K_1(V_{GS2} - V_{GS7})V_{in} \\ &= \frac{2K_1}{\sqrt{K_2}}(\sqrt{I_A} - \sqrt{I_B})V_{in} \quad \text{for } I_A > I_B,\end{aligned}$$

for K_2 identical to K_7. The above result can be rewritten as

$$\Delta I = (I_{o1}-I_{o2}) = \sqrt{2\mu_n C_{ox} I_A (W_1/L_1)} \left[\frac{\sqrt{W_1/L_1}}{\sqrt{W_2/L_2}}\right] \left(1 - \sqrt{I_B/I_A}\right) V_{in} \quad \text{for } I_A > I_B. \tag{2.20}$$

We can define an equivalent transconductance g_{mA} as

$$g_{mA} \triangleq \sqrt{2\mu_n C_{ox} I_A (W_1/L_1)}, \tag{2.21}$$

Then the transconductance of the triode-based circuit of Fig. 2.5b is given by

$$G_m = \Delta I/V_{in} = g_{mA} \left[\frac{\sqrt{W_1/L_1}}{\sqrt{W_2/L_2}}\right] \left(1 - \sqrt{I_B/I_A}\right) \quad \text{for } I_B/I_A < 1. \tag{2.22}$$

Although this circuit gives a transconductance that is linear to a first-order and electronically tunable, it has the following disadvantages for a high dynamic-range application.

- Though the transconductance G_m can be tuned by I_A, it is not economical as extra currents I_A, I_B and I_C consume power but are not involved in the signal current paths.
- The small-signal output impedance is increased by a factor of $\frac{g_{m2}}{(g_{o2}+g_{oA})}$ due to negative feedback. But, in order to provide low impedance node at V_d, gm_3 should be greater than gm_1. Correspondingly, the noise generated at A will be amplified in the signal path by M_3, resulting in a significant drop in dynamic range.

A decreases. Since M_3 acts as a voltage-follower, the reduced voltage at A appears at V_d, thus reducing the initial increase and keeping V_d stable.

- The input-range must be limited to ensure that the input transistors M_1 and M_4 operates in the triode region. Also, for the same aspect ratio of transistors, the value of G_m for a triode-operated transistor is smaller than that of the same transistor operated in the saturation region. Correspondingly, the overall G_m from this circuit is not too high.

2.5.2 Tunable OTA Based on the Square-Law I-V Characteristic

A linear transconductor can be realized by taking advantage of the square-law behavior of a MOSFET operated in the saturation region, which is given by

$$I_d = K(V_{gs} - V_T)^2 \quad \text{where} \quad K = \frac{\mu C_{ox}}{2}\frac{W}{L}$$

The circuit shown in Fig. 2.6 shows one possible implementation of such a linear transconductor [18]. Transistors $M1$ and $M2$ are square-law transistors that perform the transconductor function. Transistors $M3$–$M8$ constitute three differential matched pairs with equal tail currents $2I_o$. These pairs are connected in such a way that $M5$–$M6$ and $M7$–$M8$ carry the same currents as $M3$–$M4$. As a result of this, the voltage V_{in} is copied to the transconductor transistors $M1$ and $M2$. This is shown as follows: presume that $M3$ and $M4$ are characterized by K_3 and V_{T3}, $M5 - M8$ by K_5 and V_{T5} and all wells are connected to the supply voltages. The following relations can be written as:

$$V_{in} = (\sqrt{I_o + i} - \sqrt{I_o - i})/\sqrt{K_3} \tag{2.23a}$$

$$\begin{aligned} V_{gs5} - V_{gs6} = V_{gs7} - V_{gs8} &= (\sqrt{I_o + i} - \sqrt{I_o - i})/\sqrt{K_5} \\ &= \sqrt{K_3/K_5}V_{in} \end{aligned} \tag{2.23b}$$

Thus, two proportional copies of V_{in} appear across the lower differential pairs. These voltage are added to and subtracted from the transconductance control voltage V_c. Assuming that $M1$ and $M2$ are characterized by K_1 and V_{T1}, and assuming,

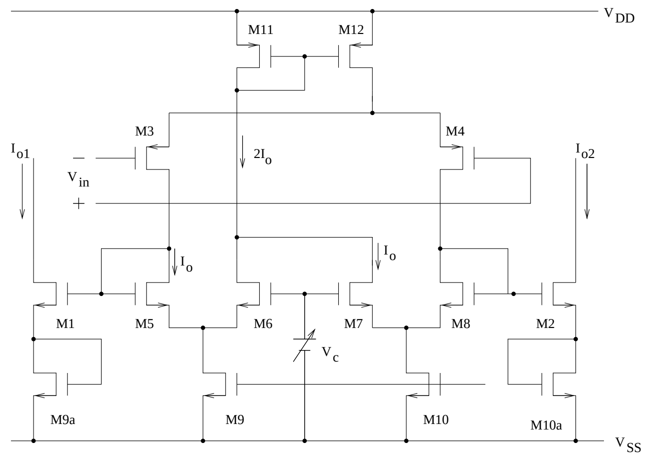


Figure 2.6: Basic linear transconductor circuit

for the time being, that $M9a$ and $M10a$ are shorted, the output currents I_{o1} and I_{o2} are given by,

$$I_{o1} = K_1(V_c + \sqrt{K_3/K_5}V_{in} - V_{T1})^2 \tag{2.24a}$$

$$I_{o2} = K_1(V_c - \sqrt{K_3/K_5}V_{in} - V_{T1})^2 \tag{2.24b}$$

The difference of these currents is

$$I_{o1} - I_{o2} = 4K_1(V_c - V_{T1})\sqrt{K_3/K_5}V_{in} \tag{2.24c}$$

(2.24c) describes the transfer function of a linear transconductor. Its transconductance value is linearly controlled by the voltage V_c.

The stacked transistors ($M1$ with $M9a$) and ($M2$ with $M10a$) operate as square-law voltage-to-current transducers. The drain current of the stacked pair can be written as

$$I_{o1} = K_{eq}(V_{g1} - V_{s9a} - V_{Teq})^2 \tag{2.25}$$

with

$$K_{eq} = (\frac{1}{\sqrt{K_1}} + \frac{1}{\sqrt{K_{9a}}})^{-2}$$

and

$$V_{Teq} = V_{T1} + V_{T9a}$$

These equations also have a square-law relation. An analysis of second-order effects reveals that mobility reduction is the most important cause of deviations from the square-law model. As $V_{Teq} > V_T$ and the voltage $(V_{g1} - V_{s9a} - V_{Teq})$ is distributed over two transistors, these deviations are smaller for the stacked pair than for a single transistor operating at the same voltage. Although V_{T1} is significantly enlarged by the body effect, the variation in V_{T1} due to V_{in} has a negligible effect on the drain current when compared to deviations caused by mobility reduction. This deviation comes from sub-threshold conduction at low currents and mobility fall-off at high current as the carriers approach the scattering-limited velocity.

Like the triode-based transconductor, the square-law transconductor also has disadvantages for achieving a high dynamic-range at high frequencies. Some of these are as follows:

- Additional circuitry, is used to couple V_c for g_m control. This leads to an increase in the number of the high impedance nodes, which reduces the bandwidth.
- At high frequency, parasitic effects cannot be ignored. Therefore an exact cancellation of 2nd-order distortion cannot be achieved.
- Linearity depends on the mobility variation of K_3 and K_5. But $M3$ is a PMOS transistor, while $M5$ is an NMOS; these can never be expected to match. As a result of the mismatch, linearity will degrade at high frequencies.
- Current mirrors are needed for the transconductor. A mismatch in mirror transistors also leads to a degradation in linearity.
- More power is consumed by extra currents in the differential-pairs.

Several other linearized transconductors have been designed[8, 17, 25, 26]. However, only a few can be used for high-frequency operation. The general reason is that these designs apply the first-order model behavior of the MOS transistors, with addition and subtraction to enhance the linearity of the OTA. But this not only increases the circuit complexity, but also degrades the signal-to-noise ratio. That is, whenever the signal is added or subtracted, the amplitude of the signal will decrease, while at the same time, the increase in circuit complexity will lead to an increase in noise. This is because the noise cannot be canceled by addition or subtraction. The result will be in increased SNR and, therefore, a reduced dynamic-range.

Hence, the key to designing an OTA for high-frequency operation is that it should have simple circuitry. This will minimize the noise and eliminate high-impedance internal nodes, which will reduce the bandwidth. Furthermore, a successful wide-band low-distortion design requires careful trade-offs in signal-path complexity. With noise and distortion requirements.

2.6 OTA Design For Maximum Dynamic-Range

The strategy of the design of this high-frequency OTA will be to start from the simplest intrinsic circuit. This will keep the bandwidth high and the noise low. We will then add complexity as needed to meet linearity requirements.

The most basic and wide-band design for a differential transconductor is the source-coupled differential-pair. To determine the basic characteristic of this circuit, we will assume a square-law transistor models and perfect transistor matching. For MOSFETs, operating in the saturation region, the drain current is

$$I_d = K(V_{GS} - V_T)^2,$$

where $K = \frac{\mu C_{ox}}{2}\frac{W}{L}$. Whereas in the triode region the drain current is,

$$I_d = 2K[(V_{GS} - V_T)V_{DS} - \frac{1}{2}V_{DS}^2].$$

These equations will be used to analyze the linearity of competing designs.

2.6.1 Linearity Analysis

Five sub-circuits, Fig. 2.7, including the two examples discussed previously, will be analyzed in this section.

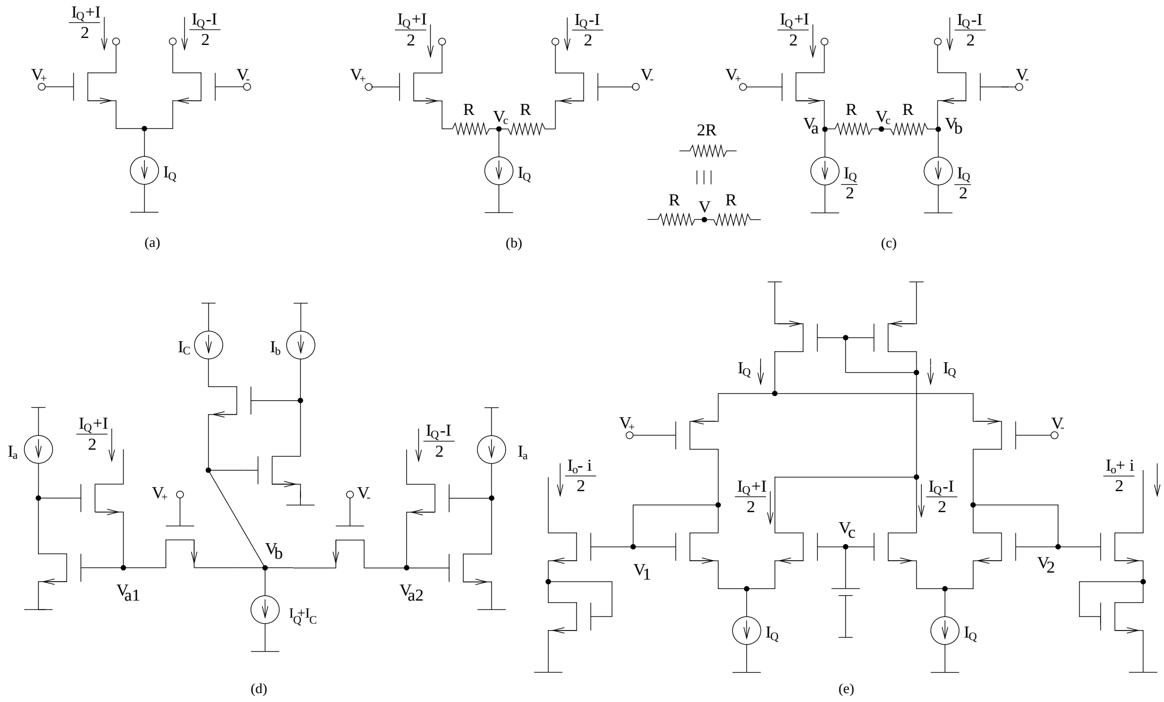


Figure 2.7: OTA cells

Differential Pair: Circuit (a) Consider the simple differential pair in Fig. 2.7a. The differential voltage can be written as a function of the drain currents.

$$V = V_+ - V_- = \frac{\sqrt{\frac{I_Q+I}{2}}}{\sqrt{K}} - \frac{\sqrt{\frac{I_Q-I}{2}}}{\sqrt{K}} \tag{2.26a}$$

The bias quantities can be factored out such that

$$V = \sqrt{\frac{I_Q}{2K}}\left[\sqrt{1+\frac{I}{I_Q}} - \sqrt{1-\frac{I}{I_Q}}\right] \tag{2.26b}$$

We recognize the quantity $\sqrt{I_Q/(2K)}$ as the effective gate voltage V_{gt0} of the the transistor biased in the balanced state with a drain current of $I_Q/2$. If we expand the remaining square-root terms in a Taylor series we obtain the normalized result,

$$\begin{aligned}\frac{V}{V_{gt0}} = & \left[1+\frac{1}{2}\frac{I}{I_Q} - \frac{1}{8}(\frac{I}{I_Q})^2 + \frac{1}{16}(\frac{I}{I_Q})^3 - \frac{5}{128}(\frac{I}{I_Q})^4 + \frac{7}{256}(\frac{I}{I_Q})^5 + \cdots\right] \\ & - \left[1-\frac{1}{2}\frac{I}{I_Q} - \frac{1}{8}(\frac{I}{I_Q})^2 - \frac{1}{16}(\frac{I}{I_Q})^3 - \frac{5}{128}(\frac{I}{I_Q})^4 - \frac{7}{256}(\frac{I}{I_Q})^5 + \cdots\right].\end{aligned} \tag{2.26c}$$

Due to the differential nature of the circuit with perfect matching all the second-order terms cancel and the V-I characteristic is given by the following series.

$$\boxed{\frac{V}{V_{gt0}} = \left[\frac{I}{I_Q} + \frac{1}{8}(\frac{I}{I_Q})^3 + \frac{7}{128}(\frac{I}{I_Q})^5 + \cdots\right]} \tag{2.27}$$

The linear is $\frac{V_{gt0}}{I_Q}$, which is the nominal g_m of this differential pair. The 2nd- and 3rd-order harmonic pre-distortions (Appendix B.1) are

$$\mathrm{HP}_2 = 0, \tag{2.28a}$$

$$\mathrm{HP}_3 = \frac{1}{32}(\frac{I_\rho}{I_Q})^2 \tag{2.28b}$$

where I_ρ is the peak incremental current of I. As there is no 2nd-order distortion in a matched differential circuit, the 3rd-order harmonic distortion is simply the negative of the pre-distortion:

$$\mathrm{HD}_3 = -\frac{1}{32}(\frac{I_\rho}{I_Q})^2 \tag{2.28c}$$

Distortion can be reduced by increasing the quiescent current I_Q, but power consumption efficiency, noise performance, and higher-order transistor behaviors become problematic.

Differential Pair with Degenerated Resistors: Circuit (b) Consider the resistor-degenerated NMOS differential pair in Fig. 2.7b, the differential voltage can be written as a function of the drain currents

$$\begin{aligned}V_+ - V_- = & \frac{1}{\sqrt{K}}(\sqrt{\frac{I_Q+I}{2}}) + (\frac{I_Q+I}{2})R \\ & - (\frac{I_Q-I}{2})R - \frac{1}{\sqrt{K}}(\sqrt{\frac{I_Q-I}{2}})\end{aligned} \tag{2.29a}$$

If we expand the square-root terms in a Taylor series and assume perfect matching, the V-I characteristic is given by the following series.

$$\boxed{V = I_Q R\frac{I}{I_Q} + \sqrt{\frac{I_Q}{2K}}\left[\frac{I}{I_Q} + \frac{1}{8}(\frac{I}{I_Q})^3 + \frac{7}{128}(\frac{I}{I_Q})^5 + \cdots\right]} \tag{2.29b}$$

Here, the 3rd order distortion is

$$\mathrm{HD}_3 = -\mathrm{HP}_3 = \frac{-\frac{1}{32}\sqrt{\frac{I_Q}{2K}}}{I_Q R + \sqrt{\frac{I_Q}{2K}}}(\frac{I_\rho}{I_Q})^2 = \frac{-1}{32(1+\frac{I_Q R}{V_{GE}})}(\frac{I_\rho}{I_Q})^2 \tag{2.30}$$

where $V_{GE} = V_{GS} - V_T = \sqrt{\frac{\frac{I_Q}{2}}{K}}$, the effective gate voltage of the transistor biased in the balanced state with a drain current of $I_Q/2$. HD_3 is a factor of $\frac{1}{1+I_Q R/V_{GE}}$ less than that of a NMOS pair (Eqn. 2.28c). The circuit's transconductance is determined from the linear terms in (2.29b):

$$G_m = \frac{I}{V} = \frac{1}{R+\sqrt{\frac{1}{2KI_Q}}} = \frac{\sqrt{2KI_Q}}{1+R\sqrt{2KI_Q}} \tag{2.31}$$

Note that $\sqrt{2KI_Q} = \frac{I_Q}{V_{GE}}$ is the quiescent transconductance of a MOS transistor.

The sub-circuit in Fig. 2.7c is similar. The harmonic distortions is same as before. Both voltage nodes V_c experience **no** voltage variation differentially, but voltage nodes V_a and V_b do not. The performance of the sub-circuits (b) and (c) depend on the matching between the resistors or the current sources respectively.

A tunable OTA using Triode-operated Transistor : Circuit (d) Consider sub-circuit in Fig. 2.7d, if V_{DS} are fixed for the input transistors, i.e. V_{a1}, V_b and V_{a2}, and $V_{a1} = V_{a2}$, we have (see Section 2.5.1)

$$V_{GS} - V_T = \frac{\frac{I}{2K} + \frac{1}{2}V_{DS}^2}{V_{DS}} \tag{2.32}$$

$$\begin{aligned} V =& V_+ - V_- \\ =& \frac{I_Q + I}{4KV_{DS}} - \frac{I_Q - I}{4KV_{DS}} \\ =& \frac{I}{2KV_{DS}} \end{aligned} \tag{2.33}$$

Hence, the transconductance G_m is $2KV_{DS}$. This G_m is small as V_{DS} is small.

Tunable OTA Based on the Square-Law I-V Characteristic : Circuit (e)

From Eqn. 2.24c, to sub-circuit in Fig. 2.7e: (see Section 2.5.2)

$$\begin{aligned}\frac{I_o + i}{2} &= K_{eq}(V_c - \sqrt{\frac{K_3}{K_5}}V_{in} - V_{eq})^2 \\ \frac{I_o - i}{2} &= K_{eq}(V_c + \sqrt{\frac{K_3}{K_5}}V_{in} - V_{eq})^2\end{aligned} \tag{2.34a}$$

$$G_m = \frac{i}{V_{in}} = 4K_{eq}\sqrt{\frac{K_3}{K_5}}(V_c - V_{eq}) \tag{2.34b}$$

Although this shows only a linear term, it does not show good performance after the consideration of *second-order* transistor behaviors.

2.6.2 Second-Order Transistor Behavior

In this section we will consider the performance degradation of the basic OTA circuits with respect to non-ideal, second-order transistor behavior. The analysis of the harmonic distortion from Appendix B will be applied. The effects of the non-ideal transistor behavior will be consider one at a time.

Mobility Degradation A simple model for mobility degradation is given by

$$I = K\frac{(V_{GS} - V_T)^2}{1 + \theta(V_{GS} - V_T)} \tag{2.35}$$

The mobility reduction factor $\theta = \frac{1}{T_{ox}E_c}$ has units of inverse voltage. (T_{ox} is the gate oxide thickness and E_c is the critical vertical field.) This mobility dependence upon the gate voltage can have a significant effect on distortion for thin-oxide devices. Rearranging (2.35) as a quadratic equation in $(V_{GS} - V_T)$ and solving it, we get

$$V_{GS} - V_T = \frac{\theta}{2K}I + \sqrt{\frac{I}{K}}\sqrt{1 + \frac{\theta^2 I}{4K}} \tag{2.36}$$

When $|(\theta^2 I/K)| \ll 1$,

$$V_{GS} - V_T \approx \frac{\theta}{2K}I + \sqrt{\frac{I}{K}} \tag{2.37}$$

This result shows a term linear in the drain current added to the square-law effective gate voltage.

A Resistor Degenerated Differential Pair: Substitute the modified effective gate voltage from (2.37) into (2.29b), the differential voltage can be written as

$$V = \frac{\theta}{2K}(\frac{I_Q+I}{2}) + \sqrt{\frac{I_Q+I}{2K}} + \frac{I_Q+I}{2}R - \Big\{\frac{\theta}{2K}(\frac{I_Q-I}{2}) + \sqrt{\frac{I_Q-I}{2K}} + \frac{I_Q-I}{2}R\Big\} \tag{2.38a}$$

then, we have

$$V = \frac{\theta}{2K}I + IR + \sqrt{\frac{I_Q+I}{2K}} - \sqrt{\frac{I_Q-I}{2K}} \tag{2.38b}$$

This is equivalent to a series resistor with value $R = \theta/K$ degenerating the transistor. When $R = 0$, we get the result of sub-circuit (a). The sub-circuit (c) is the same as that of sub-circuit (b). This effect can be minimized by using a larger device.

Tunable Triode-Based OTA: Consider the sub-circuit in Fig. 2.7d, assuming the transistor model at triode region with mobility degradation is:

$$I = \frac{K[(V_{GS}-V_T)V_{DS} - \frac{1}{2}V_{DS}^2]}{1+\theta(V_{GS}-V_T)} \tag{2.39a}$$

Rearranging the equation, we get

$$V_{GS} - V_T = \frac{I + \frac{K}{2}V_{DS}^2}{KV_{DS} - \theta I} \tag{2.39b}$$

Substitute (2.39b) into (2.32), the differential input voltage us

$$V_{GS1} - V_{GS2} = \frac{\frac{I_Q+I}{2} + \frac{K}{2}V_{DS}^2}{KV_{DS} - \theta(\frac{I_Q+I}{2})} - \frac{\frac{I_Q-I}{2} + \frac{K}{2}V_{DS}^2}{KV_{DS} - \theta(\frac{I_Q-I}{2})} \tag{2.39c}$$

and thus,

$$V = \frac{KV_{DS}(1+\frac{\theta}{2}V_{DS})}{(KV_{DS} - \frac{\theta I_Q}{2})^2 - \frac{\theta^2}{4}I^2}I \tag{2.39d}$$

express the denominator in a Taylor series,[2]

$$V = KV_{DS}(1+\frac{\theta}{2}V_{DS})I\Big\{1 + (\frac{\frac{\theta}{2}}{KV_{DS} - \frac{\theta}{2}I_Q})^2 I^2 + (\frac{\frac{\theta}{2}}{KV_{DS} - \frac{\theta}{2}I_Q})^4 I^4 + \cdots\Big\} \tag{2.39e}$$

Then, $\mathrm{HD}_3 = -\mathrm{HP}_3 = -\frac{1}{4}(\frac{\frac{\theta}{2}}{KV_{DS}-\frac{\theta}{2}I_Q})^2 I_\rho^2$ where I_p is the peak incremental current at the output. The distortion is significant as KV_{DS} is small.

[2] $\frac{1}{1-x} = 1 + x + x^2 + x^3 + \cdot.$

Tunable Square-Law Based OTA: From (2.34b), the linearity performance is degrades with the terms: K_{eq} and $\sqrt{\frac{K_3}{K_5}}$. Without direct substitution, we can see that not only will a linear term be added, but more non-linear terms will be included. Furthermore, the mobility reduction factor θ for NMOS and PMOS are different (M3 is PMOS, M5 is NMOS). So this kind of configuration will be seriously affected by mobility degeneration and temperature variations.

Body-Effect Modulation of Threshold Voltage The modulation of the body-effect can be modeled as

$$V_T = V_{T0} + \tau(\sqrt{2\phi - V_{bs}} - \sqrt{2\phi}) \tag{2.40}$$

where V_{bs} is the potential of the transistor's body with respect to its source, V_{T0} is the threshold voltage when $V_{bs} = 0$, τ is a device constant and ϕ is a material constant of the bulk.

A Resistor Degenerated Differential Pair In Fig. 2.7b, $V_{bs1} = V_c + \frac{I_Q+I}{2}R$ and $V_{bs2} = V_c + \frac{I_Q-I}{2}R$. Substitute the modified equation 2.40 into Eqn. (2.29b), we obtain

$$\begin{aligned} V =& \frac{1}{\sqrt{K}}\Big(\sqrt{\frac{I_Q+I}{2}} - \sqrt{\frac{I_Q-I}{2}}\Big) + IR \\ &+ \tau\Big(\sqrt{2\phi + V_c + \frac{I_QR}{2} + \frac{IR}{2}} - \sqrt{2\phi + V_c + \frac{I_QR}{2} - \frac{IR}{2}}\Big) \end{aligned} \tag{2.41a}$$

and then, we have

$$\begin{aligned} V =& \sqrt{I_Q}2K\Big\{\frac{I}{I_Q} + \frac{1}{8}\Big(\frac{I}{I_Q}\Big)^3 + \cdots\Big\} + IR \\ &+ \tau\sqrt{2\phi + V_c + \frac{I_QR}{2}}\Big\{\frac{I}{\frac{I_Q}{2} + \frac{V_c+2\phi}{R}} + \frac{1}{8}\Big(\frac{I}{\frac{I_Q}{2} + \frac{V_c+2\phi}{R}}\Big)^3 + \cdots\Big\} \end{aligned} \tag{2.41b}$$

With small R, the distortion is not significant. When $R = 0$, it results in a simple differential pair and $V_{bs1} = V_{bs2}$ and the body-effect modulation of threshold voltage will be canceled out.

Triode-Based OTA Assume that the negative feedback works properly, voltages V_{a1}, V_{a2} and V_b are fixed. Then the modulated threshold voltage will be canceled out if the transistors are matched.

Square-Law OTA In Fig. 2.7e, the modulated threshold voltages of $M3..M8$ will be canceled out by 3 sets of differential pair. However, the body effect due to the stacked pair cannot be neglected. The V_{bs} of $M1$ is equal to V_{GS} of $M9a$. Also, V_{bs} of $M2$ is equal to V_{GS} of $M10a$.

Considering the body effect, we get

$$\begin{aligned} I_{o1} &= K_{eq}(V_c - \sqrt{\frac{K_3}{K_5}}V_{in} - V_{Teq})^2 \\ &= K_{eq}(V_c - \sqrt{\frac{K_3}{K_5}}V_{in} - V_{T0_1} - V_{T0_{9a}} - \tau(\sqrt{2\phi + \sqrt{\frac{I_{o1}}{K_1}}} - \sqrt{2\phi}))^2 \end{aligned} \tag{2.42a}$$

and

$$\begin{aligned} I_{o2} &= K_{eq}(V_c + \sqrt{\frac{K_3}{K_5}}V_{in} - V_{Teq})^2 \\ &= K_{eq}(V_c - \sqrt{\frac{K_3}{K_5}}V_{in} - V_{T0_2} - V_{T0_{10a}} - \tau(\sqrt{2\phi + \sqrt{\frac{I_{o2}}{K_1}}} - \sqrt{2\phi}))^2 \end{aligned} \tag{2.42b}$$

By subtraction,

$$\begin{aligned} I_{o2} - I_{o1} =& K_{eq}(2\sqrt{\frac{K_3}{K_5}}V_{in} + \tau\Big(\sqrt{2\phi + \sqrt{\frac{I_{o1}}{K_1}}} - \sqrt{2\phi + \sqrt{\frac{I_{o2}}{K_1}}}\Big) \\ & \times (2V_c - 2V_{T0_1} - \tau\Big[\sqrt{2\phi + \sqrt{\frac{I_{o1}}{K_1}}} + \sqrt{2\phi + \sqrt{\frac{I_{o2}}{K_1}}} - 2\sqrt{2\phi}\Big]) \end{aligned} \tag{2.42c}$$

The equation becomes more complicated. and it proves that the linearity drops when second-order effects are considered. Thus, this configuration is not useful for high linearity at high speed application.

2.6.3 Noise Analysis

It is stated [28] that the thermal noise is the most common noise generated in the CMOS circuit. Besides, less complexity circuits will have less transistors, which will generate less noise. Or we can increase the signal current to have a large noise margin.

Fig. 2.7a shows the minimum noise as it is the basic building block for any differential-inputs circuit. In Fig. 2.7b and c, both circuits are symmetric, the noise performance of the sub-circuit (b) and (c) are the same.

2.6.4 Linearization by Degeneration Resistors

The simple configuration of a resistor-degenerated differential pair is then chosen to be the input stage of the OTA. No addition and subtraction techniques are employed to enhance the linearity. There is no extra circuitry to tune the transconductance as in Fig. 2.7d and e. The power dissipation is not large. The noise generated in this circuit is comparable to a simple differential-pair. This may be the optimum structure of V-to-I conversion for maximum dynamic range.

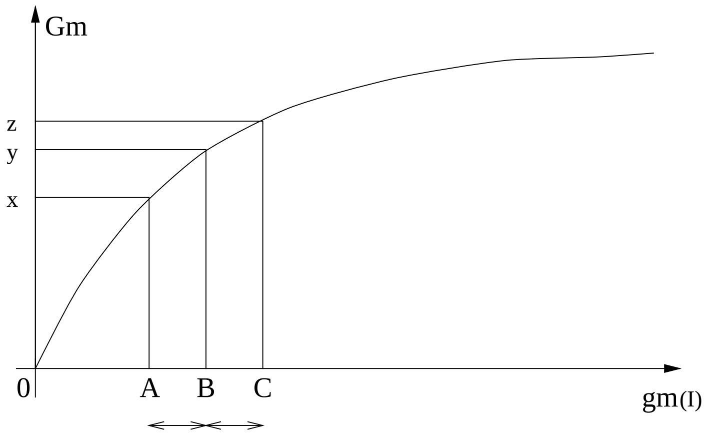


Figure 2.8: The tunability of total transconductance

Drawbacks The penalty of using degenerated resistors for linearization is the addition of the poly-silicon resistors and the limit on transconductance tunability. Firstly, it results in an increase of the area in layout. The sheet resistance of poly-silicon is about 5 ohm/□. It takes about 50 $\mu \times 1$ μ to create 250 Ω resistive strip.

Secondly, linearization is achieved by the trade-off between the G_m tunability and linearity. From Eqn.(2.31), the total transconductance is,

$$G_m = \frac{\sqrt{2KI_Q}}{1 + R\sqrt{2KI_Q}} = \frac{g_m}{1 + g_m R} \approx \frac{1}{R} \quad \text{when } g_m \text{ is large}$$

The curve is shown in Fig. 2.8. Although we can control the overall transconductance G_m by the current I_Q, the ease of tuning G_m decreases. For example, the nominal operating point is at B, with $G_m = y$. With the same change of $g_m(I)$ in each direction, the corresponding change of G_m is different, i.e. $z - y < y - x$. It leads to difficulties in tuning the G_m at one side, i.e. when large G_m is required. Moreover, there is about $\pm 40\%$ process variation of the sheet resistance.

2.6.5 Output stage

The role of the output stage is to offer a large output impedance or a large DC gain. Generally the high DC gain requirement leads to a multistage design with long-channel length transistors biased at low current level, which degrades the frequency performance. The most commonly used structure for gain enhancement, without affecting the bandwidth, is folded-cascode. However, the DC gain of this conventional solution is limited by the drain-source resistance, r_{ds}, which decreases with large biasing current and short-channel length transistors. Of course, we can apply the gain-boosting technique for gain enhancement [28]. In this design, we apply *cross-coupled simple current mirror pairs* for active loads.

Here, we use two cross-coupled pairs and 2 triode transistors to provide a very high output impedance as shown in Fig. 2.9. Transistors M4,M5,M6 and M7 are matched. Transistors M8 and M9 are operating in the triode region, acting as degeneration resistors to provide different operating points at V_+ and V_-. Using $r_{op} = (g_{op})^{-1}$, and $r_{om} = (g_{om})^{-1}$ to model respectively, the small-signal diagram is shown in Fig. 2.9(b).

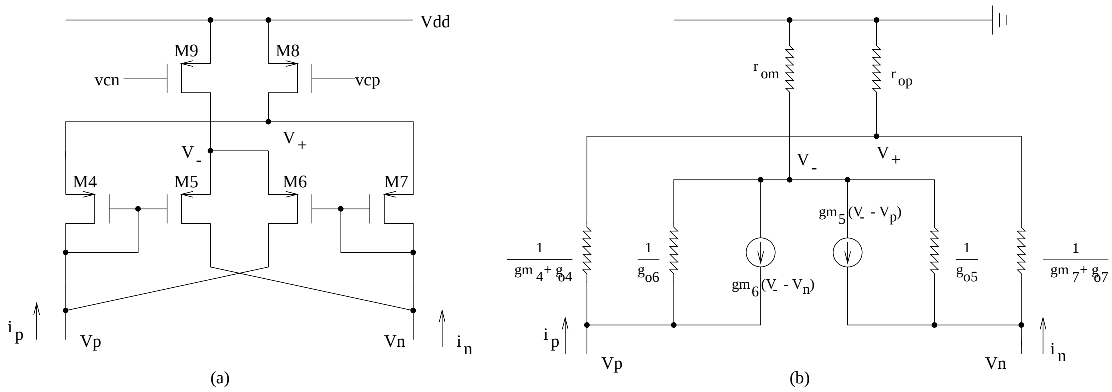


Figure 2.9: (a) Cross-coupled pairs and 2 triode transistors and (b) small-signal model

In Fig. 2.9a, since transistors M4 and M7 are connected in diode configuration, they act like a pair of positive resistors. Transistors M5, M6 act like a pair of negative resistors. Hence, all resistors are parallel across the terminals V_p and V_n. Voltages vcp and vcn control the magnitude of +R and -R respectively. They will cancel each other for suitable combination of vcp and vcn, that is, $-R \| R \rightarrow \infty$.

In reality, they cannot completely cancel each other due to the parasitic components. In general, it is a good way to provide a very high output impedance. Appendix C shows how this configuration can provide very high output impedance by small-signal model analysis.

2.7 A Practical Transconductor Design

After considering all of the above analysis, we have finally arrived at the transconductor that will be used in this filter design. A schematic of this circuit is shown in Fig. 2.10. The value of the degeneration resistors determines the overall transconductance of the circuit. For the filter application in this project, a differential transconductance of $1/800\Omega = 1.25\text{m}S$ is required.

Transistor Dimensions. The transistor geometries in the transconductor circuit are enumerated in Table 2.1. All the sizes of transistors in this OTA are multiples

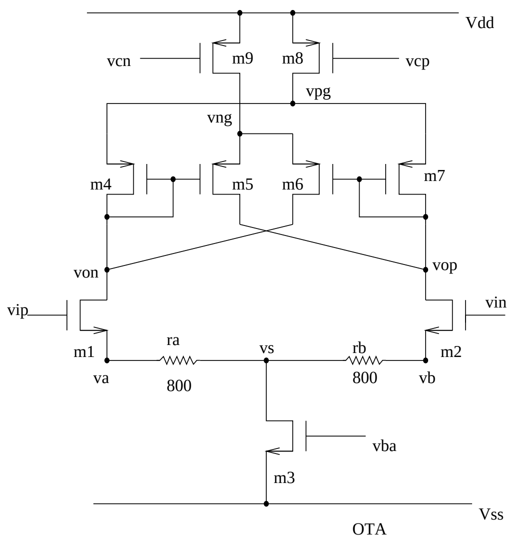


Figure 2.10: The CMOS implementation of the transconductor

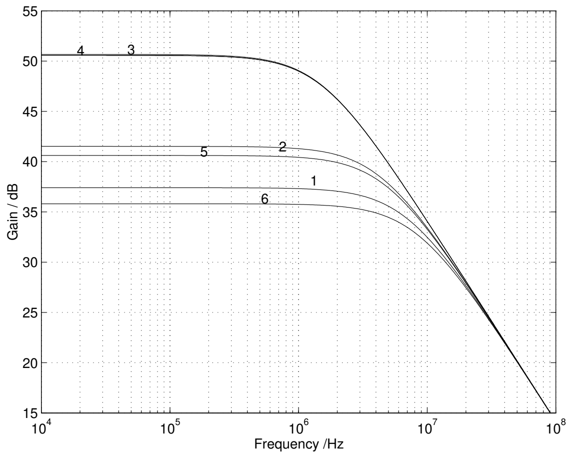
of 12/1. Using the *unit-cell* layout approach provides better matching performance, and is easier for layout.

Transistor(s)	Gate Dimensions (μm)
M_1 - M_3	$12/1 \times 4$
M_4 - M_7	$12/1 \times 2$
M_8,M_9	$12/1 \times 4$

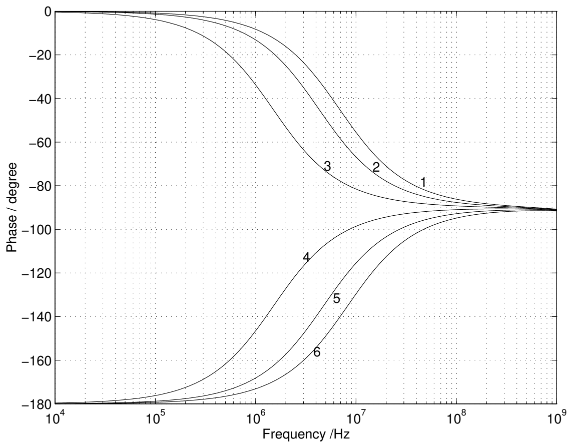
Table 2.1: Transistor dimensions for transconductor circuit

Choice of Operating Point To determine the optimal operating point and bias values, we can consider Fig. 2.10, where $M8$ and $M7$ are connected between voltage nodes vop and Vdd. The transistor $M8$ operates in the triode region, and transistor $M7$ is diode connected. There is approximately $2V_T$ between vop and Vdd. In order to operate in a optimum region, the operating point of this OTA is set to $3.5V$ with $5V$ supply. For small signal inputs, the output signals will swing at 3.5V (around $2V_T$ from the Vdd). So the common-mode feedback (CMFB) loop is not necessary, resulting in a simpler circuit.

Simulated Performance The transconductor design of Fig. 2.10 shows a very high output impedance in the HSPICE simulations. Fig. 2.11 shows the frequency response of the circuit with the variation of the voltage *vcp*. The results are plotted



(a) Simulated magnitude response



(b) Simulated phase response

Figure 2.11: Simulation result of varying vcp

for the voltage *vcp* increasing from 3.4077V to 3.5077V in steps of 0.02V. The voltage *vcn* is set to be 2.5V by a reference voltage. This result shows that the maximum DC gain is achieved when *vcp* approaches the point where the impedances of the cross-coupled pairs match that of the differential input pair. Moreover, the phase of the response changes from positive to negative when vcp increases, because the negative impedance becomes dominant.

When this OTA is loaded with a 5pF capacitive load, the total-harmonic-distortion (THD) is less than -60dB (0.1%, $\sim$ 10-bits resolution) for the input range within 230mV. The simulation results at $f = 10MHz$ are shown in Fig. 2.12.

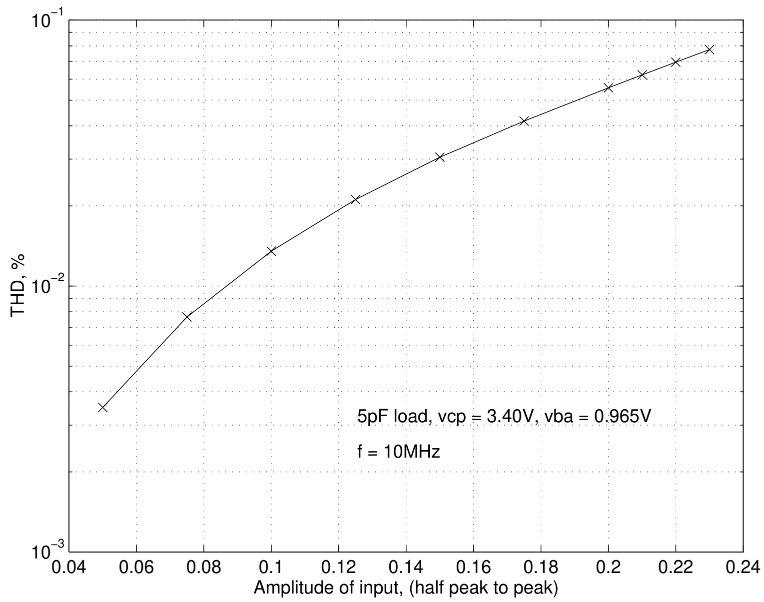


Figure 2.12: Total harmonic distortion (THD) of the OTA (at $f = 10MHz$)

From the noise analysis of HSPICE, the total equivalent input noise of the OTA, with the same load as before is shown in Fig. 2.13. The noise level at 10MHz is around $34\mu V_{rms}$, so the signal-to-noise ratio (SNR) at THD = -60 dB is 73.6 dB. At the signal level of 200-mV, the THD is -65.1dB (0.055%) and the dynamic-range (SNDR) is about 64.4-dB.

Tunability The correction voltage vcp will be tuned by the amplitude control loop, which will be discussed in Chapter 4. The transconductance can be varied by changing the bias voltage of $M3$, vba as shown in Fig. 2.14. It is tuned by the frequency-control loop.

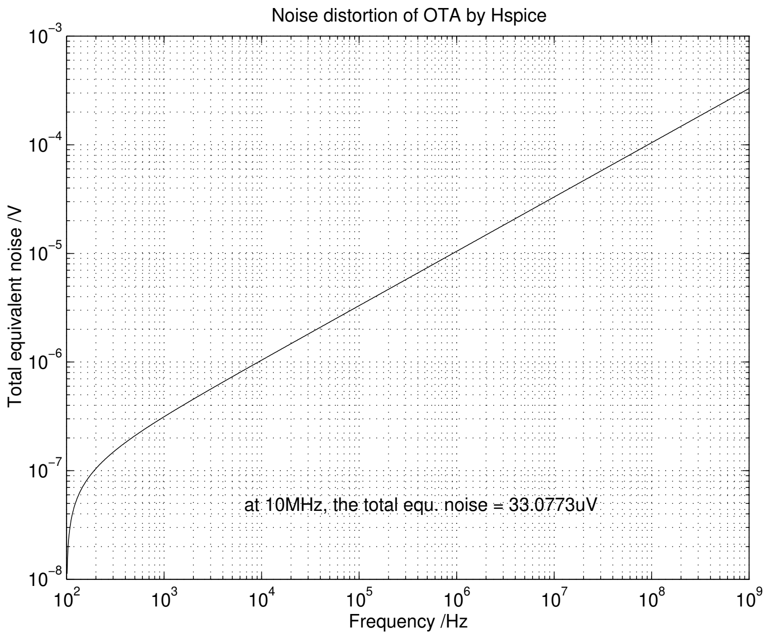


Figure 2.13: Total equivalent noise of the OTA

2.8 Summary

In this chapter design considerations for maximizing the dynamic-range of an OTA operating at 10-MHz have been presented. It was found that it is difficult to achieve better than a differential pair. If complicated linearization techniques are utilized the noise increases substantial and one is usually better off to simply use all the extra current in the differential pair to reduce the modulation index and thus improve the linearity and the noise simultaneously.

After extensive analysis an design was chosen based on a simple differential pair with a cross-coupled load. The load provides a high output impedance and provide a means for tuning the integrators dissipations and, therefore, canceling the excess phase. Simulation results show that a dynamic-range of greater then 64-dB is achievable with this circuit for the application intended with the given power constraints. The following chapter will discuss how this transconductor is utilized to construct a 4th-order Butterworth filter as a cascade of two biquadratic sections.

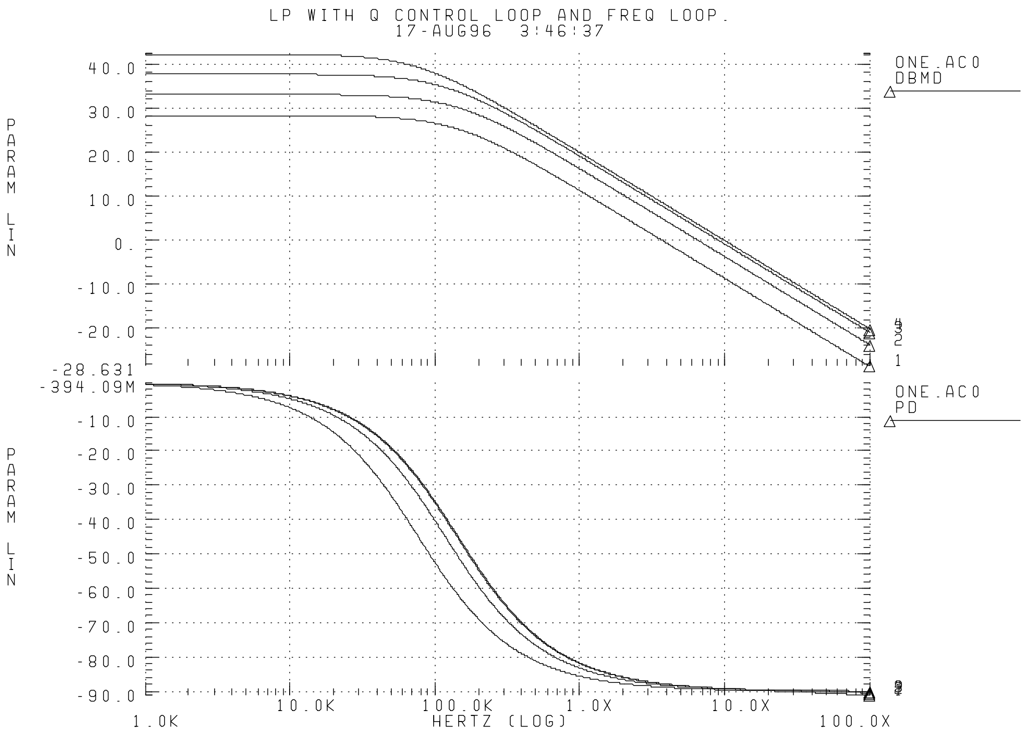


Figure 2.14: Simulated results of varying *vba*

Chapter 3

Realization of a Low Distortion Video Filter

3.1 Introduction

The objective is to design a video filter that can operate at high-frequency with a wide dynamic range. The goal is to meet a set of video specifications with good yield, thus demonstrating the commercial viability of continuous-time filters in current VLSI design.

Components fabricate on a chip cannot be matched precisely. This inaccuracy leads to a mismatch of the gains of the various integrators in the slave filter, thus *altering the shape* of its frequency response. This problem is severe in video-filters because the value of the capacitors used in the integrators are of the order of a few picofarads and matching them across the chip to the required degree of precision is difficult.

The first step in confronting this problem is to use filter topologies that are insensitive to component mismatches, e.g., inductance simulation, and leapfrog realization. The second step is to over-design the ripple amplitude and the roll-off rate so that there is more room to allow for response deviations due to component mismatches. This strategy inevitably increases the order of the filter and leads to two problems.

1. As the order of the filter increases, the physical size of the filter increases, thus worsening the matching between components that are already separated by large distances;

2. The sensitivity of the passband edge to phase error increases with filter order.

Thus, the order should be chosen such that the filter remains within specifications with finite tolerances of the components and worst-case phase error in the integrators of the slave filter. Excess phase shift at unity-gain frequency is usually due to parasitics poles of the integrator.

There are two basic methods by which to build a filter:

1. By cascading biquadratic sections

2. By emulating a passive LC ladder filter

3.2 Biquadratic Sections

The transfer function of a g_m-C first order section (Fig. 3.1a) is

$$\begin{aligned} \frac{V_1}{V_{in}} &= \frac{g_{m1}}{g_{m2} + sC_1} \\ &= \frac{g_{m1}}{g_{m2}} \frac{1}{\left(1 + s\frac{C_1}{g_{m2}}\right)} \\ &= \frac{A_o}{s + \omega_o}, \end{aligned} \tag{3.1a}$$

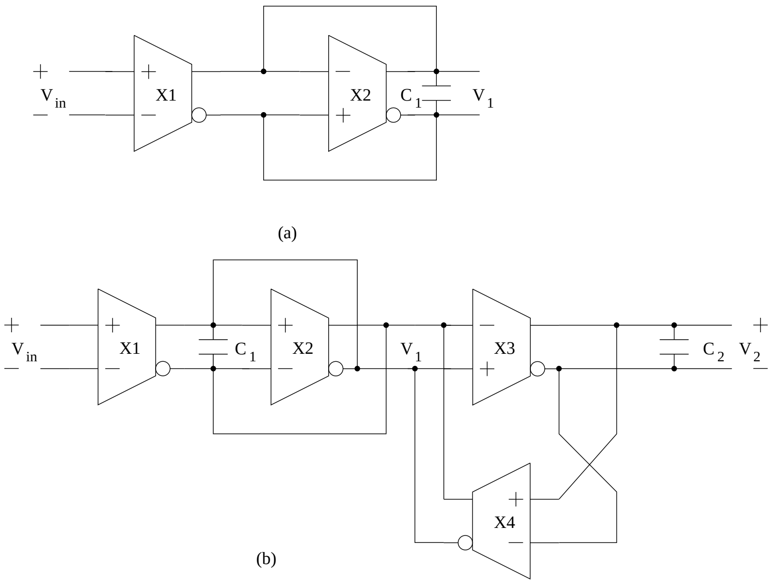


Figure 3.1: Block diagrams of (a) first-order (b) second-order biquad configuration

and that of a second order section (Fig. 3.1b), is

$$\begin{aligned}\frac{V_2}{V_{in}} &= \frac{g_{m1}g_{m3}}{g_{m3}g_{m4} + sg_{m2}C_2 + \ s^2C_1C_2} \\ &= \frac{\frac{g_{m1}g_{m3}}{g_{m3}g_{m4}}}{1 + \frac{g_{m2}}{\sqrt{g_{m3}g_{m4}}}\sqrt{\frac{C_2}{C_1}}\frac{s}{\sqrt{\frac{g_{m3}g_{m4}}{C_1C_2}}} + \frac{s^2}{\frac{g_{m3}g_{m4}}{C_1C_2}}} \\ &= \frac{A_o}{1 + \frac{1}{Q}\frac{s}{\omega_o} + \frac{s^2}{\omega_o^2}}\end{aligned} \tag{3.1b}$$

High-order filters can be obtained by cascading biquads and either with or without a first-order section depending on whether the order of the filter is even or odd. In this design, a 4th order Butterworth filter is implemented and a first-order section is not needed. This filter achieves a 80-dB/decade in the stopband. Also, the frequency response is maximally flat in the passband for a Butterworth filter.

Matching between 2 OTAs with equal g_m's is better than that between 2 OTAs with non-integral g_m ratios. So non-integral g_m should be avoided. In this design, all the g_m's are the same. i.e. $gm_i = gm, i = 1, 2, 3, 4$, and Eqn. 3.1b becomes,

$$\frac{V_2}{V_{in}} = \frac{\omega_o^2}{s^2 + s\frac{\omega_o}{Q} + \omega_o^2} \tag{3.2}$$

where $\quad \omega_o = \frac{gm}{\sqrt{C_1C_2}}$ is the center frequency and $Q = \sqrt{\frac{C_1}{C_2}}$ is the quality factor of the biquad

3.2.1 Advantages and Disadvantages of the Biquad Filter Topology

For the cascaded biquad filters, the features are:

- more general; they can implement any filter whose transfer function may be represented as a quotient of two polynomials (with the order of the denominator larger or equal than the order of the numerator)
- easier to lay out; the same biquads may be used for different filters with only minor changes.

Compared to the filters emulating passive LC ladders [30], it is relatively sensitive to component variations. But the cascade approach was adopted in this design in order to facilitate the requirements of automatic tuning.

3.3 Denormalization of the Transfer Function

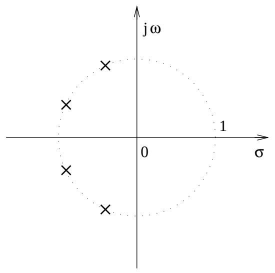


Figure 3.2: The pole locations of the 4th order Butterworth filter

The normalized transfer function of the 4th order lowpass Butterworth filter is given by,

$$H_n(s) = \frac{1}{(s^2 + 0.765s + 1)(s^2 + 1.848s + 1)} \tag{3.3}$$

The poles are on the unit circle as shown in Fig. 3.2. To denormalize $H_n(s)$ such that the passband edge frequency is $s_p = 2\pi f_p$, we substitute,

$$s \rightarrow \frac{s}{s_p} \tag{3.4a}$$

$$H(s) = H_n(\frac{s}{s_p}) = \frac{s_p^2}{s^2 + 0.765s_p + 1} \frac{s_p^2}{s^2 + 1.848s_p + 1} \tag{3.4b}$$

By cascading 2 biquads in Fig. 3.1b, its transfer function is

$$\frac{V_o}{V_{in}} = \frac{\frac{g_m^2}{C_1C_2}}{\left(s^2 + \frac{g_m}{C_1} + \frac{g_m^2}{C_1C_2}\right)} \frac{\frac{g_m^2}{C_3C_4}}{\left(s^2 + \frac{g_m}{C_3} + \frac{g_m^2}{C_3C_4}\right)} \tag{3.5}$$

Comparing Eqn. 3.4b and Eqn. 3.5, we get

$$s_p^2 = \frac{g_m^2}{C_1C_2} = \frac{g_m^2}{C_3C_4} \tag{3.6a}$$

$$\frac{g_m}{C_1} = 0.765s_p, \quad \frac{g_m}{C_3} = 1.848s_p \tag{3.6b}$$

with known g_m,

$$C_1 = \frac{1}{0.765} \times \frac{g_m}{s_p}, \qquad C_2 = 0.765 \times \frac{g_m}{s_p}$$

$$C_3 = \frac{1}{1.848} \times \frac{g_m}{s_p}, \qquad C_4 = 1.848 \times \frac{g_m}{s_p} \tag{3.6c}$$

3.3.1 Parasitics Capacitances and Mismatches

Refer to Fig. 2.4 shown below, a real transconductor consists of parasitic input and output capacitances, C_{in} and C_o respectively. Since the poles of a filter are of the order of g_m/C, we must decrease the capacitance in order to increase the pole frequency. Therefore, for realizing high-frequency poles and zeros, the integrating capacitors are small. Although we may increase the transconductance g_m to achieve the same result, but higher g_m are usually associated with larger input device, which in turn means larger parasitic input capacitances C_{in}, which should be avoided.

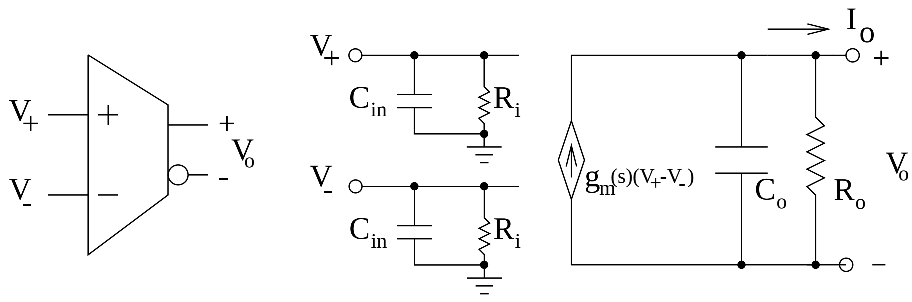


Figure 3.3: Small signal equivalent of OTA

At high frequencies, we are also interested in increasing the output current driving capability of the transconductor to be able to charge the integrating capacitor faster. However, large driving capability requires larger output devices large parasitic output capacitance C_o.

Besides, the parasitic input and output capacitances of the transconductor are no longer negligible compared with the integrating capacitors that we implement on the filter. These parasitics will modify the transfer function of the filter and change the locations of the poles.

One approach to solve this problem is by estimating these parasitics and taking them into account in designing the values of capacitors of the g_m-C stage. Yet, the problem with this approach is that the parasitics depend on process parameters and temperature, so their values are difficult to be predicted accurately.

Another approach is to make all the capacitances of all the nodes the same by construction, including parasitics, by adding appropriate dummy devices. However, this method needs different transconductances for each OTA. And it needs more chip area and consumes more power. In this design, we will use the first approach.

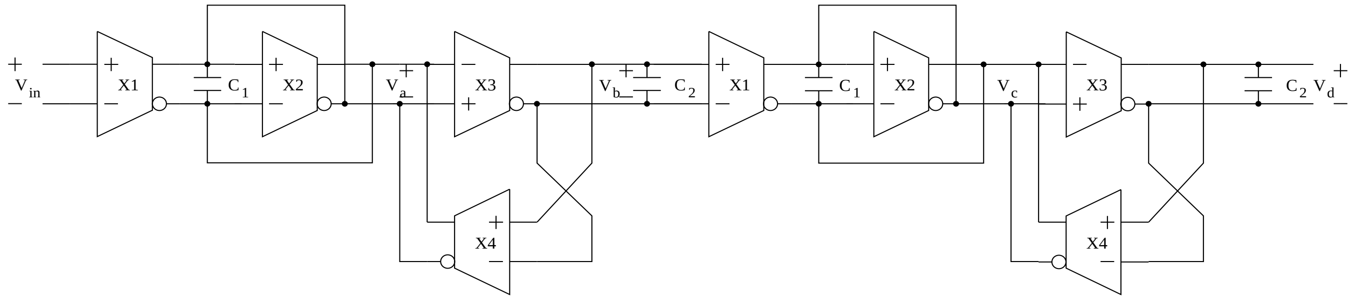


Figure 3.4: The biquads configuration of the filter

Consider the terminals across C_1 in Fig. 3.4, the total capacitance connected to V_a is

$$C(V_a, total) = C_1 + 2 \times C_{in} + 3 \times C_{out}$$

where C_{in} and C_{out} are the input and output capacitances respectively.

The other nodes are:

$$C(V_b, total) = C_2 + 2 \times C_{in} + C_{out}$$

$$C(V_c, total) = C_3 + 2 \times C_{in} + 3 \times C_{out}$$

$$C(V_d, total) = C_4 + C_{in} + C_{out}$$

In order to minimize the mismatches of the transconductances, all the transconductors will have the same g_m. As discussed in Chapter 2, the tunability of the OTA is limited due to the narrow range. That is, to achieve better linearity and noise immunity, g_m should be large, resulting in bigger parasitic capacitances and resulted in smaller tuning range. We design g_m to be approximately $\frac{1}{R}$ to provide good tunability of the overall transconductance G_m.

We estimate that $C_{in} = C_{out} \approx 0.1pF$, and g_m is obtained by simulation. To get $f_p = 10MHz$, we have

C_1	6.40pF
C_2	3.84pF
C_3	2.40pF
C_4	9.60pF

Table 3.1: The size of the filter capacitors

3.3.2 Signal Level Scaling

The frequency responses of the internal nodes of the filter, V_1, V_2 and V_3 also need to be considered. If those amplitudes are higher than the input amplitude, the internal node may saturate and affect the linearity of the transconductor. So, scaling is necessary to reduce those internal nodes amplitude [29].

Usually, scaling is carried out by varying the transconductance and capacitor values appropriately so that the voltage gain from the input to the internal node voltages are less than unity, and does not change the overall transfer function at the output. This voltage-scaling technique makes maximum use of the limited available voltage range.

Although such scaling increases the dynamic range of the filter, it considerably complicates its design and especially its mask layout. Transconductance scaling requires each transconductor in the integrator to be treated separately in the design and layout; resistor value and possibly bias currents are altered, leading to difficulty to the tuning. At this point, we have an unscaled low-pass filter, each transconductor is identical.

3.4 Simulation Results

The total current consumed by each OTA is $400\mu A$. The total power dissipation of cascading 2 biquads is $16.00mW$. Figs. 3.5 and 3.6 show the frequency response of the slave filter in HSPICE simulations.

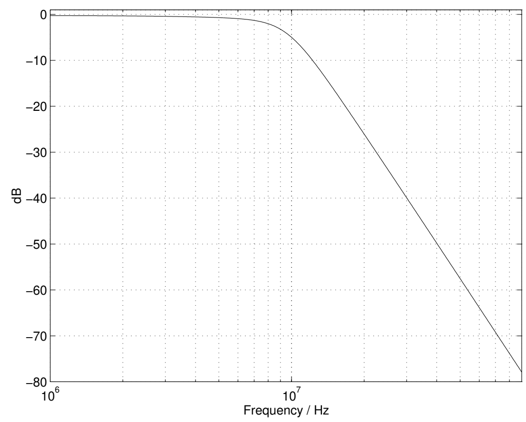


Figure 3.5: The magnitude response of the slave filter

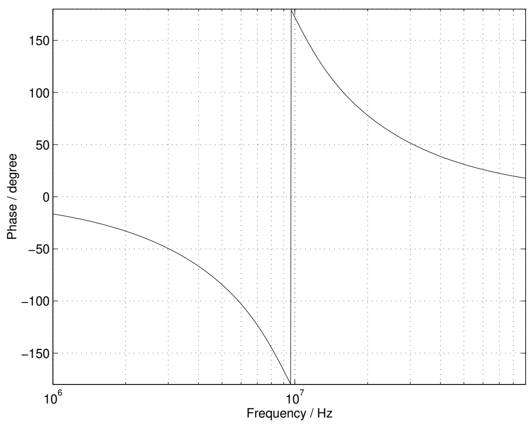


Figure 3.6: The phase response of the slave filter

Besides, with noise analysis of the HSPICE simulation, the total equivalent input noise and the total output noise over the range of 100kHz to 1GHz are shown in Figs. 3.7 and 3.8 respectively. From 3.7, the noise level within $10MHz$ is less than $100\mu V_{rms}$.

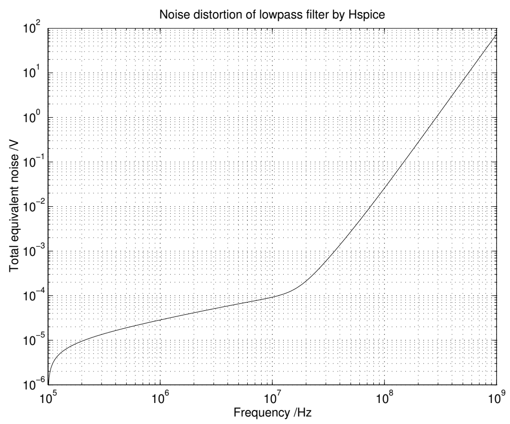


Figure 3.7: The Total Equivalent Input Noise

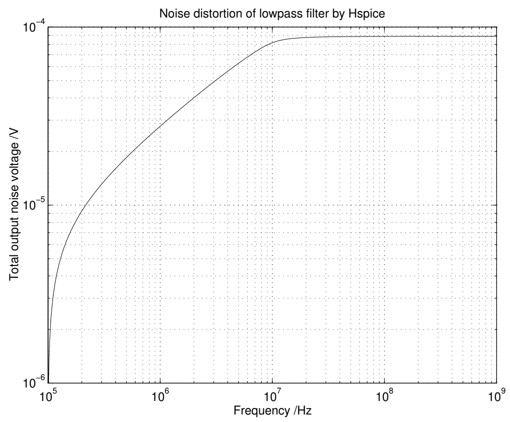


Figure 3.8: The Total Output Noise

Tunability As mentioned in section 2.7, the filter response also depends on the control voltages vcp and vba. Automatic adjustment of the filter cutoff frequency and the output impedance of the integrators are performed using a master-slave tuning system. Indeed, the vcp can control the quality factor (Q) of the filter, will be discussed in Appendix D.

Fig. 3.9 shows the response of the filter for different values of vcp. At high vcp, the quality factor (Q) increases, resulting to a peak at the passband edge. The voltage vba controls the cut-off frequency of the filter as shown in Fig. 3.10. Since the cut-off frequency ω_o is directly proportional to the transconductance of the OTAs, and vba controls the current passing through it, thus ω_o increases when vba increases.

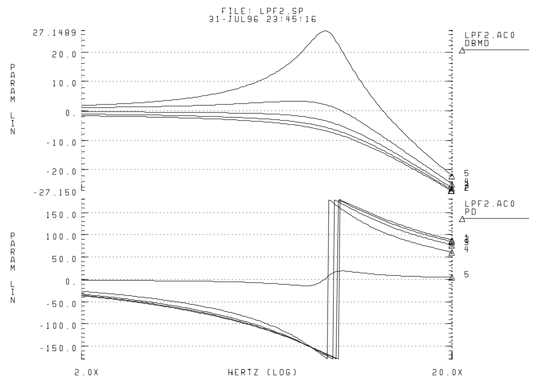


Figure 3.9: Frequency response of the filter versus *vcp*

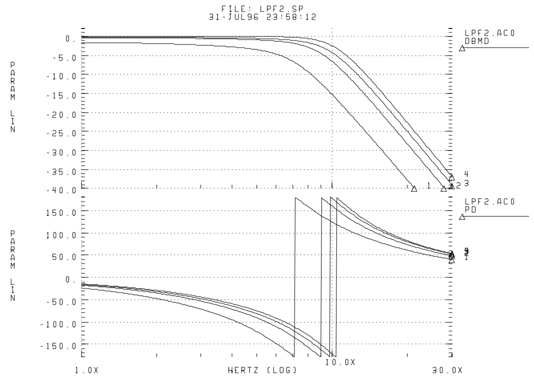


Figure 3.10: Frequency response of the filter versus *vba*

Table 3.2 shows the specification of this filter. Simulation with 200mV input signal indicates that total-harmonic-distortion (THD) for 8MHz signal is less than -76dB.

	Simulation Result
Input common mode :	3.5 V
Input signal swing :	200 mV
Output common mode :	3.4583 V
Output signal swing :	200 mV
Power dissipation :	16.0 mW
Cut-off frequency :	8 MHz (-1 dB)
Linearity/THD :	
1 tone (@2MHz)	-59.4 dB
1 tone (@10MHz)	-68.38 dB
2 tones (@$7, 8MHz$)	-53.4 dB
Total Output Noise :	
1MHz	$26.95\mu Vrms$
10MHz	$76.39\mu Vrms$
100MHz	$84.29\mu Vrms$
1GHz	$84.47\mu Vrms$

Table 3.2: Specifications of the filter

Chapter 4

Automatic Tuning

4.1 Background

Although in many modern IC fabrication technologies, resistors, capacitors, and operational amplifiers are available, the design of integrated circuit filters incurs additional difficulties by these realizations. The reasons are as follows :

The first problem is due to *the limited range of available passive elements.* If no special processing technique, such as resistive thin films on a silicon IC, is employed, the maximum resistivity for building integrated resistors is of the order of $1k\Omega/\Box$.

The other problem is due to *the difficulty in obtaining accurate and stable component values.* To set precise frequency parameters, e.g. $\omega_0 = \frac{gm}{C}$, we require accurate **absolute values** of resistors and capacitors. Although ratios of similar components can be realized very accurately in integrated circuit technologies, absolute-value tolerances are generally quite poor. Fabrication tolerances ε_r of resistors and ε_c of capacitors of the order of 40% or more are not uncommon [28].

One of the important filter parameter, the quality factor Q, is a *dimensionless* quantity and depends only on ratios of similar components. It may appear initially that Q can be realizable quite accurately in IC form. However, it states that small phase errors caused by parasitic effects in the active devices can give rise to significant deviations in quality factor, which adjusts the passband shape to minimize component dissipation effects [30]. The parasitics are difficult to predict and cannot be eliminated by design. In stringent high-frequency applications, tuning of the quality factor is required to compensate the errors.

Consider the implementation an OTA-C filter, very accurate absolute values of resistors, transconductance, and capacitors are not normally available because of fabrication tolerances or varying operating conditions. Thus, the generally adopted solution is to design onto the IC an *automatic electronic tuning scheme* as part of the total continuous-time filter circuitry.

4.2 Master-Slave Technique

In this project, we apply the master-slave technique for automatic tuning [2]. The steps involved in the *tuning* procedure are to *measure* the filter performance, *compare* it with a reference signal, *calculate* the error, and *apply a correction* to the filter to reduce the error.

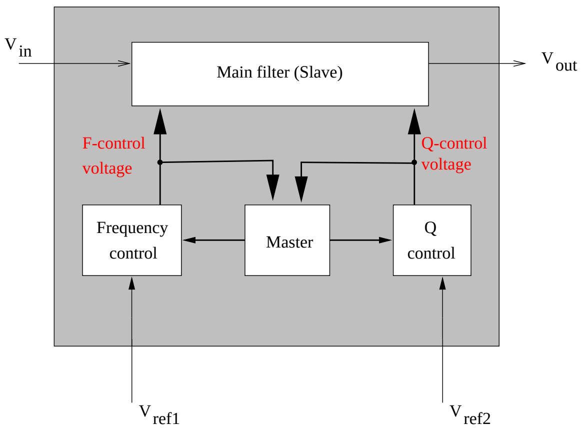


Figure 4.1: Block diagram of master-slave control system for integrated continuous-time filters.

We need to construct a *master*, which represents all relevant performance criteria of the main filter, the *slave*, with adequate accuracy. This tuning strategy applies the reference signal to the master and relies on matching and tracking between this master and the sufficiently identical slave on the same chip to tune the main filter. Tuning is accomplished by applying the control voltage simultaneously to both the master and the slave.

In Fig. 4.1, there are two tuning loops: *frequency-control loop* and *amplitude-control loop*. Each tuning loop contains a *control* block that compares the master's response with the reference signal V_{ref} and generates a *control* voltage to the master and the slave. For frequency-control loop, the reference signal is either from a system clock or crystal oscillator. Notice that the reference signal may couple to the outputs of the slave filter and cause undesirable feed-through or intermodulation [9].

Consider the realization of a transfer function $H(s, \vec{t}, \vec{u})$ where s is the complex frequency and $\vec{t}$ and $\vec{u}$ are vectors of the tuned and the untuned circuit parameters respectively. Both $\vec{t}$ and $\vec{u}$ are subject to errors and tolerances,

$$\vec{t} = \vec{t}_0 + \triangle\vec{t} \qquad \vec{u} = \vec{u}_0 + \triangle\vec{u} \tag{4.1}$$

where $\vec{t}_0$ and $\vec{u}_0$ are the nominal values. The control system should adjust the values of $\triangle\vec{t}$ such that[1]

$$\begin{aligned} H(s, \vec{t}, \vec{u}) &= H(s, \vec{t}_0 + \triangle\vec{t}, \vec{u}_0 + \triangle\vec{u}) \\ &= \frac{N_m(s, \vec{t}_0 + \triangle\vec{t}, \vec{u}_0 + \triangle\vec{u})}{D_n(s, \vec{t}_0 + \triangle\vec{t}, \vec{u}_0 + \triangle\vec{u})} \Rightarrow H(s, \vec{t}_0, \vec{u}_0), \end{aligned} \tag{4.2}$$

by varying $\triangle\vec{t}$, the inaccurate transfer function $H(s, \vec{t}_0 + \triangle\vec{t}, \vec{u}_0 + \triangle\vec{u})$ is to be tuned to its nominal value $H(s, \vec{t}_0, \vec{u}_0)$. Note that $\triangle\vec{t}$ consists of the "tuning changes" $\triangle\vec{t}_t$

[1] For example, MOS capacitors are not tunable and belong to the vector $\vec{u}$; on the other hand, junction capacitor can be tuned by changing the reverse bias voltage: they would belong to $\vec{t}$ if they are used for tuning purpose, but to the set $\vec{u}$ if they are not tuned.

and the "errors" $\triangle\vec{t}_\varepsilon$ caused by processing tolerances, temperature variations, and so forth:

$$\triangle\vec{t} = \triangle\vec{t}_t + \triangle\vec{t}_\varepsilon$$

In other words, tuning the components in the vector $\vec{t}$ will not only compensate for the errors in $\vec{u}$, but also for errors in $\vec{t}$ itself. More discussion will be mentioned in [30, Chapter 7].

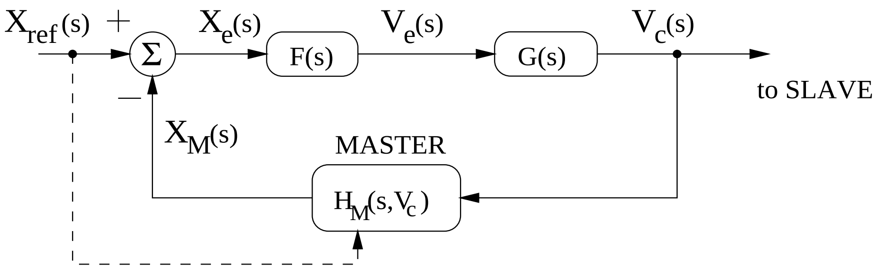


Figure 4.2: Operational diagram of an on-chip tuning system.

We now consider the operation of a control loop in Fig. 4.1 by drawing the functional block diagram in Fig. 4.2.

$X_{ref}(s)$	is a reference signal.
$X_M(s)$	is an output signal from the master.
$X_e(s)$	is the error in X_M obtained by comparing X_M to X_{ref}.
$F(s)$	converts the error information X_e into V_e.
$V_e(s)$	is the error voltage produced by $F(s)$ from $X_e(s)$.
$G(s)$	is the controller which converts V_e into a control voltage V_c for the tunable components used in the design.
$V_c(s)$	is the tuning control voltage.
$H_M(s, V_c)$	is the transfer characteristic of the master as a function of frequency for a specific value of the parameter V_c.

The error function of the control system is

$$X_e(s) = \frac{1}{1 + F(s)G(s)H_M(s, V_c)} X_{ref}(s) \tag{4.3}$$

Using the Final Value Theorem of Laplace transformation[2], assuming $x_{ref}(\infty)$ is defined and finite,

$$x_e(\infty) = \frac{1}{1 + F(0)G(0)H_M(0, V_c)} x_{ref}(\infty) \tag{4.4}$$

the steady-state value of the filter error, $x_e(\infty)$ can be made arbitrarily small if the low-frequency loop gain $F(0)G(0)H_M(0, V_c)$ is sufficiently large and accurate tuning is achieved.

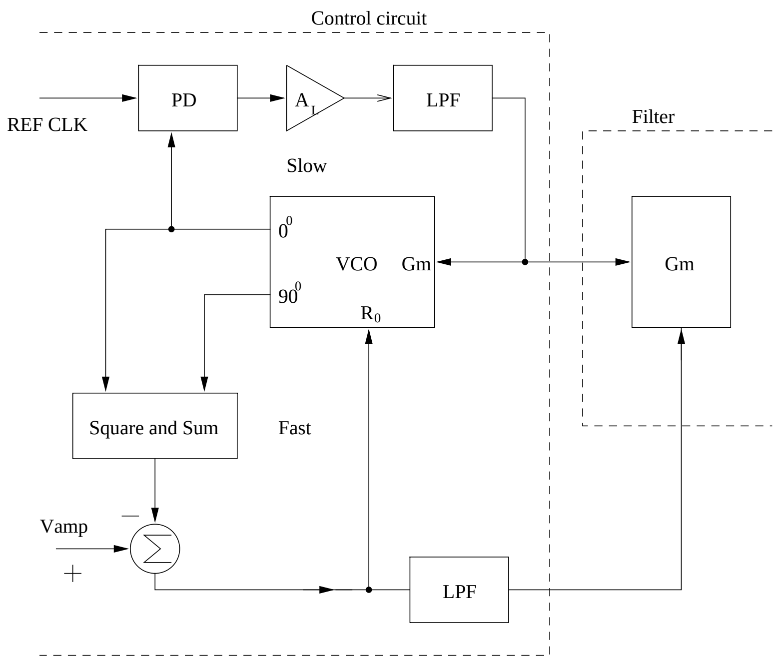


Figure 4.3: Master-slave control system

Next, the frequency-control and the amplitude-control blocks will be discussed. The schematic of the control blocks is shown in Fig. 4.3.

4.3 Frequency Control Loop

[2]Final Value Theorem : $\lim_{t\to\infty} x(t) = \lim_{s\to 0} sX(s)$

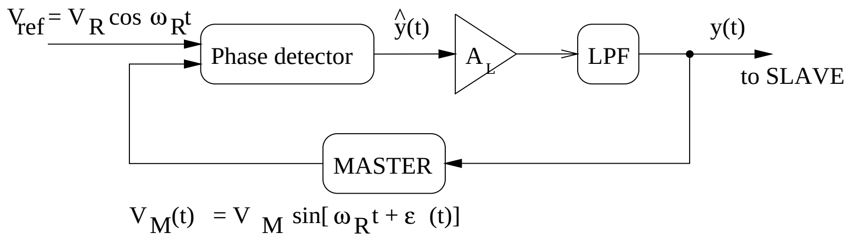


Figure 4.4: Phase-locked loop frequency tuning scheme

In this project, the frequency-control block is realized by using a phase-locked loop (PLL) with a generic schematic as shown in Fig. 4.4. The loop consists of a phase detector (PD), an error amplifier A_L, a low-pass filter (LPF), and a voltage-controlled oscillator (VCO).

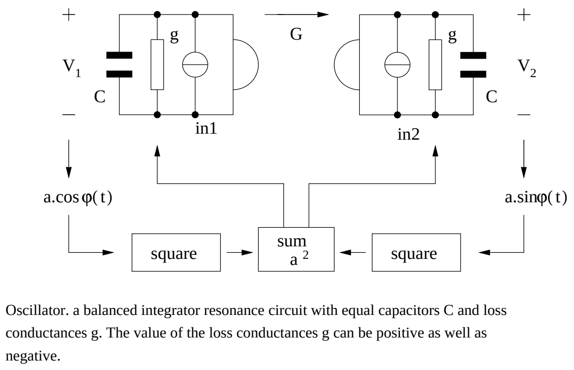
The phase detector compares the reference signal v_{ref} with the signal $v_M(t)$ generated by the master to produce a raw error signal $\hat{y}(t)$, which passes through the gain stage A_L and the lowpass filter LPF. The undesirable high-frequency components are eliminated, and the cleaned error signal $y(t)$ is then applied to the master and the matched-and-tracking slave to correct the detected errors [30]. The phase detector here is an analog multiplier/mixer and the master is a voltage-controlled oscillator (VCO).

4.3.1 Sinusoidal Quadrature Oscillator

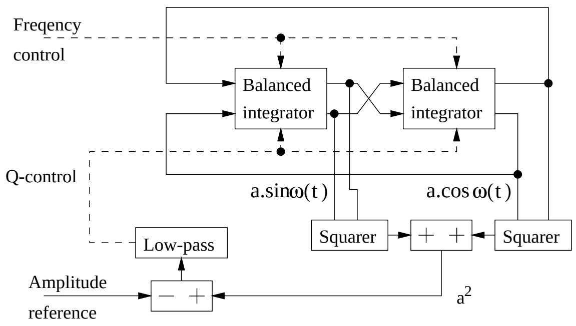
The VCO is a sine-wave quadrature oscillator, which produces two signals: $a\sin(\omega t)$ and $a\cos(\omega t)$. The main part of the oscillator is a resonance circuit composed of two cross-coupled integrators (Fig. 4.5). Each integrator consists of a V-to-I converter with transconductance G, followed by the integration of the current into a capacitor C. The detail of how the oscillator works is mentioned in [2].

The equations for the oscillator are

$$\begin{aligned} C\frac{du_1}{dt} + g(a)u_1 + Gu_2 &= i_{n_1}, \\ C\frac{du_2}{dt} + g(a)u_2 - Gu_1 &= i_{n_2}. \end{aligned} \tag{4.5}$$



(a) oscillator



(b) Sine-wave quadrature oscillator

Figure 4.5: Sine-wave quadrature oscillator

where u_1 and u_2 are the input/output signals (single-ended), $g(a)$ is a variable conductance which may take positive or negative values to control the circuit to be damped or undamped. i_{n_1} and i_{n_2} are the differential-mode noise currents of the (trans)conductances. Approximately we have

$$< i_{n_1}^2 >=< i_{n_2}^2 >= 2kTGdf$$

It can be shown [2] that the resonance circuit is damped or undamped when the signals amplitude of u_1, u_2 is too high or too low. The square of the amplitude is obtained using two squarers and an adder. The equations are the same as for a gyrator oscillator. Insertion of $u_1 = a\cos(\vartheta)$ and $u_2 = a\sin(\vartheta)$ in the noise-free equations (4.5) yields

$$\begin{aligned} \frac{d\vartheta}{dt} &= \frac{G(t)}{C}, \\ C\frac{da}{dt} &+ ag(a) = 0. \end{aligned} \tag{4.6}$$

we can see that the amplitude-control and frequency-control are independent. Only one VCO is sufficient for both tuning controls.

4.3.2 Mixer

The operation of this circuit allows the mixer to handle large input signals while operating from a lower supply voltage [31]. Assume that $V_{o1} = V_{o2} = V$ and all transistors are operating in the triode region. Consider the case when the circuit

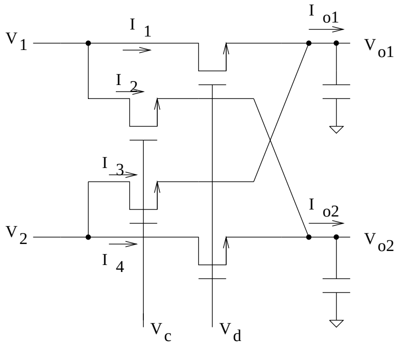


Figure 4.6: The 4-transistor multiplier implementation

is biased so that V_1 and V_2 are greater than V, both input nodes V_1 and V_2 act as drains and two V nodes act as sources. The gate-source voltage of two outer transistors are equal, and the two inner transistors have the same V_{GS}.

$$I_1 = \frac{K}{2\alpha}[(V_d - V_T - \alpha V_{o1})^2 - (V_d - V_T - \alpha V_1)^2] \tag{4.7a}$$

$$I_2 = \frac{K}{2\alpha}[(V_c - V_T - \alpha V_{o2})^2 - (V_c - V_T - \alpha V_1)^2] \tag{4.7b}$$

$$I_3 = \frac{K}{2\alpha}[(V_c - V_T - \alpha V_{o1})^2 - (V_c - V_T - \alpha V_2)^2] \tag{4.7c}$$

$$I_4 = \frac{K}{2\alpha}[(V_d - V_T - \alpha V_{o2})^2 - (V_d - V_T - \alpha V_2)^2] \tag{4.7d}$$

By subtraction and addition,

$$I_{o1} - I_{o2} = I_1 - I_4 + I_3 - I_2 = K(V_1 - V_2)(V_c - V_d) \tag{4.7e}$$

The output current is not only independent of the value of V, but also insensitive to both the body-effect α and the threshold voltage V_T. (More information will be discussed in [28, 31].) However, the output of the VCO cannot connect to the mixer directly. A gain stage buffer should be there to provide the driving impedance to the mixer.

The mixer acts as a phase detector in the frequency control loop. The sinusoidal signal from the VCO is multiplied by the reference-clock signal, and the product goes to the differential-input single-ended output amplifier to produce the control signal vba. An off-chip capacitor or a second order RC compensation is added to implement the loop filter and to remove all undesirable high-frequency components. The whole frequency control circuit is shown in Fig. 4.7.

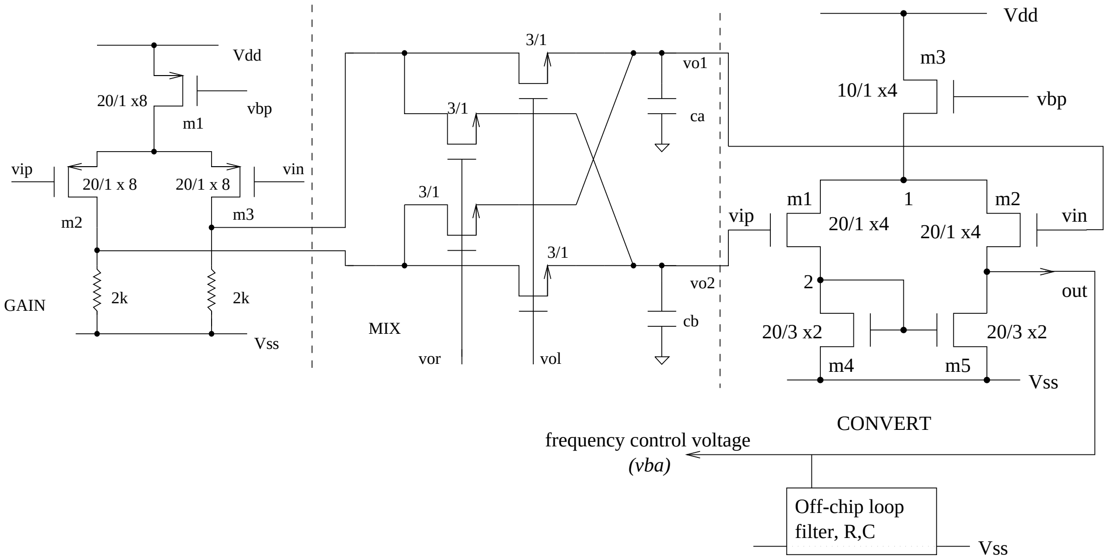


Figure 4.7: Frequency control block

4.4 Amplitude Control Loop

From Chapter 2, the designed OTA has two control voltages vcp and vba to control the output impedance R_o and the transconductance G_m respectively. A control loop is required to tune vcp of the OTAs to provide high impedance. That is, we use feedback to control the dissipation (of the integrators) to be as small as possible, so that the g_m stage will not be loaded by the output impedance.

For the circuit to oscillate at ω_o in Fig. 4.5, its frequency response $H(j\omega_o) = 1$ for each integrator. Each one must have a phase shift of 90^o, and the output impedance is maximum as the poles are on the imaginary axis.

Fig. 4.5b shows the structure of the amplitude-control-loop. There are two squarers and one adder, the summing signal then compares to the reference signal and provides the control voltage vcp to all the OTAs to provide higher output impedance.

Figs. 4.8a shows the amplitude detector and 4.8b shows the amplitude-control circuit. Instead of summing the voltages from the VCO, we sum currents and make use of the square-law behavior of the MOS transistors to produce currents with amplitudes are proportional to the square of the input signals. Currents is chosen because they are easier to be manipulated. The current sum is in node *sum* at Fig. 4.8b. The VCO signals are two quadrature sine waves: $a \sin \vartheta t$ and $a \cos \vartheta t$. If each squarer has each VCO signal as the input, the amplitude of the current through $M11$ [3] will be proportional to a^2. *Appendix* E shows how the amplitude detector works.

Consider Fig 4.8b, the transistors $M8$,$M9$ and the $1K$ resister provide a reference voltage at node 8, which is controlled by vdn. With $M10$ and $M13$, two reference current sources are implemented. This configuration is similar to the am-

[3] $\sin^2 x + \cos^2 x = 1$

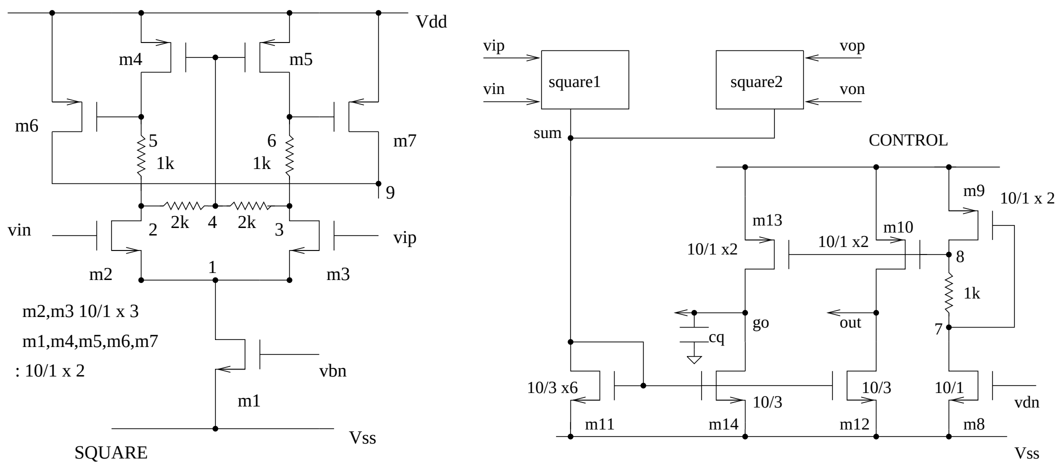


Figure 4.8: (a) Amplitude Detector and (b) Amplitude control circuit

plitude detector to achieve a direct relationship of the summed current and the reference current.

The current through $M11$ is mirrored and scaled to $M12$ and $M14$, which then provide the control voltages at go and out. The out signal is then fed back to the OTAs of the VCO without the LPF for fast response to initialize the oscillation. The signal go will be sent to the vcp of the OTAs in the slave filter and go to the pad for measurement. An off-chip loop filter or an external capacitor cq and a 2-nd order RC compensation eliminates the higher frequency components at the point go, and provides a smooth control signal to the slave filter. The amplitude of the VCO signals can be controlled by voltage vdn, which is provided by the bias circuit and same as vbn.

4.5 Q-factor of the Filter

The Q-factor of the biquad is the square root of the ratio of C_1 and C_2 (Eqn. 3.2). Since we have accounted for the parasitic capacitances, and implemented the capacitors by an array of unity capacitors, the Q factor of the filter should be accurate. The control voltages vba and vcp are mainly for frequency control of the filter and the high impedance control of the OTAs respectively.

However, it doesn't mean that there is no way to control the Q of the filter. We can make use of the finite output impedance of the OTAs to tune the Q. That is, we can tune *vcp* by forcing voltage to that pin off-chip if the testing result shows that the Q factor is not the design value. The detail will be discussed in *Appendix* D.

4.6 Reference Frequency

One of the factors that limit the dynamic range of this continuous-time filter is the reference signal feed-through, and the choice of reference frequency plays an important part in the amount of feed-through. The choices are grouped based on the location of the reference frequency with respect to the frequency response of the slave.

- If the reference frequency is in the stopband, the feed-through will be minimum because the filter tends to filter out this frequency, at least for the parasitic feed-through paths to the input of the filter. However, this frequency may be quite far away from the unity-gain frequencies of the integrators in the slave. Thus, this choice may suffer from poor master-slave matching.

- If the reference frequency is located at the passband edge, it is close to the unity-gain frequency of the slave which gives this choice very good master-slave matching characteristics. But it suffers from severe reference frequency feed-through problems. This is because at the passband edge, high-gain paths exist from internal nodes which will lead to a large feed-through.

In fact, there is already a clock signal generated by another PLL at the front-end of the receiver, and we can make use of this frequency as the reference clock signal. The frequency of the clock is $38.69MHz$. Although it is far away from the passband edge, it provides the best immunity to reference frequency feed-through.

For the purpose of testing, we provide different frequencies as reference to test the performance of the PLL, e.g. the lock-in/capture frequency range, phase noise.

4.7 Bias Circuit

Having outlined the general sub-circuits for the filter, we will briefly discuss the biasing circuit as shown in Fig. 4.9. It needs to provide bias voltages to

- *vbn* of the squarers, it controls the total current consumed by each squarer;
- *vbp* of the gain buffer, it controls the gain;
- *vdn* of the amplitude control sub-circuit, it is connected to *vbn* to control the amplitude of the VCO signals;
- *vbp* of the differential inputs single-ended output amplifier, it controls the amount of current passing through it;

The bias signals are also shown in Fig. 4.10. The resistor here is off-chip. From this biasing circuit structure [17, P.196], the transconductances can be stabilized over temperature, creating a net stabilization of integrator excess phase.

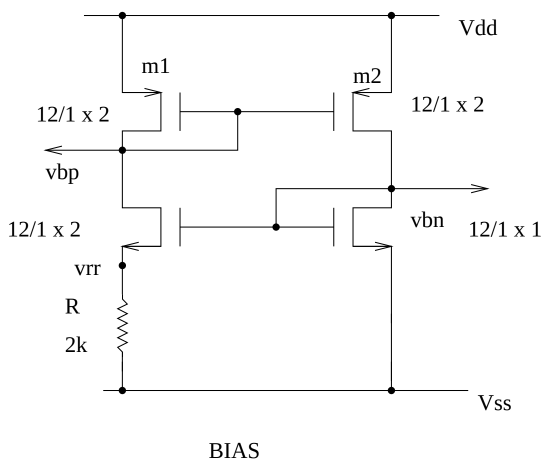


Figure 4.9: The biasing circuit

4.8 Summary of the Filter Circuit Design

After discussing the various subcells of the tuning circuits throughout the chapter, we will briefly review the overall architecture of the automatic tuning by Fig. 4.10.

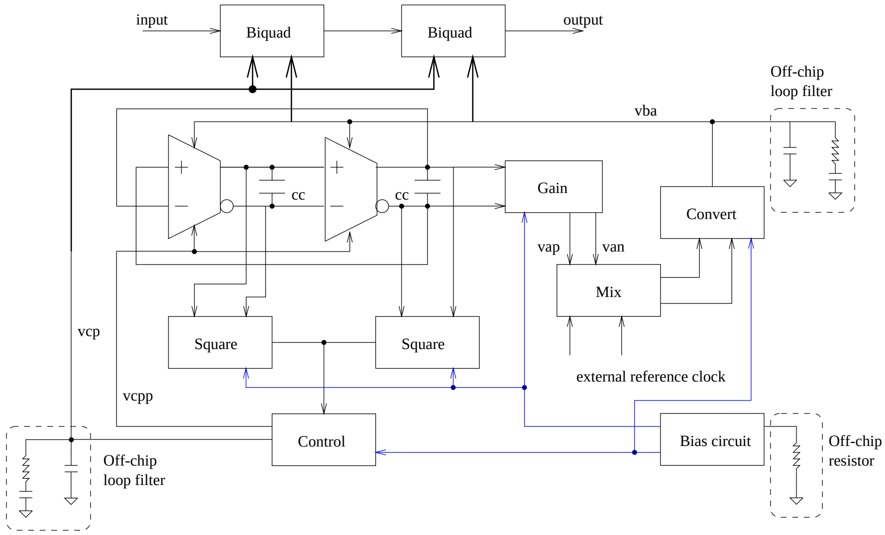


Figure 4.10: The whole automatic tuning circuits

During simulation, an addition constraint is to verify the PLL stability under random derivation which can be due to component process and temperature variation.

4.9 Simulation Results of the Control Circuit

With a reference sinusoid signal with frequency of $38.69MHz$, the phase-lock loop also generates sinusoidal signals with the same frequency as shown in Fig. 4.11. The corresponding frequency control signal vba and amplitude control signal vcp

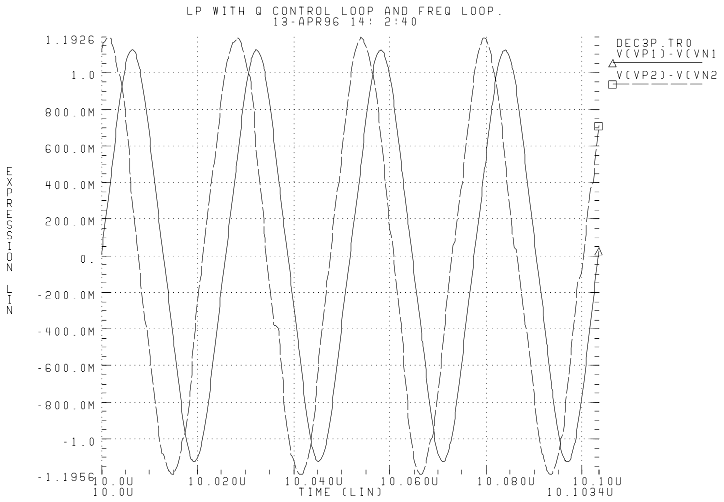
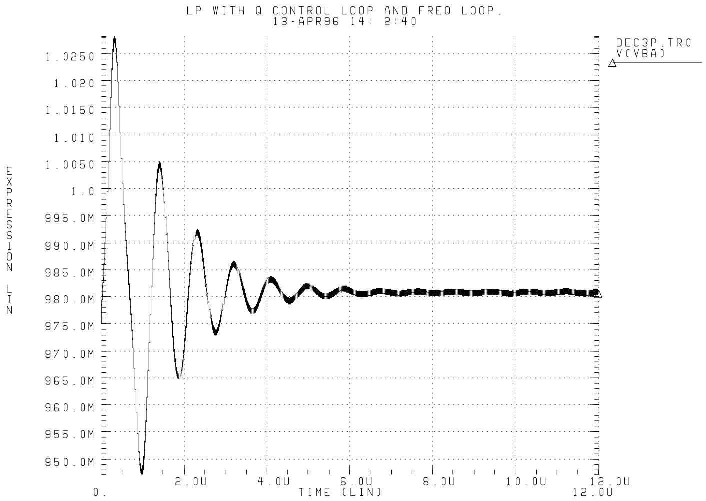


Figure 4.11: The VCO signals

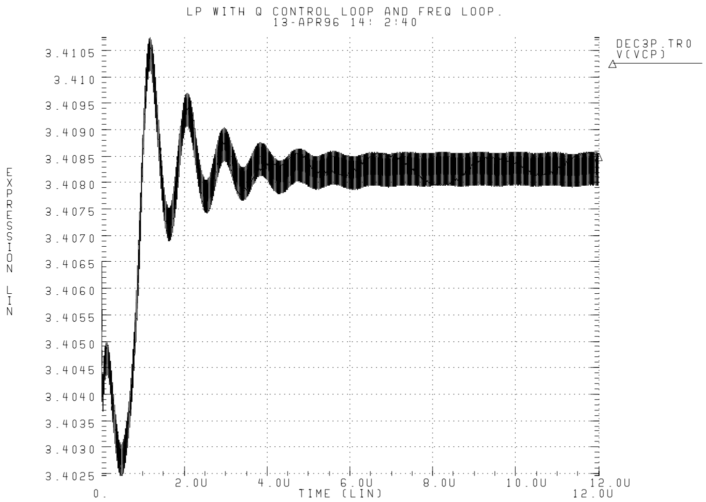
are shown in Fig. 4.12. The above simulation results are simulated at $70\,^{\circ}C$. The PLL also works properly under the simulations with temperature between $25-90\,^{\circ}C$.

Simulations with 4 process corners (FF, FS, SS and SF) show that only at SS corner, the PLL cannot start-up as the amplitude control circuit doesn't work. The ratio M of the current mirror in the amplitude-control need to change from $6:1$ to $5:1$. The modified version is shown in Fig. 4.13. That is, we can either connect $G1$ to $G2$ or connect $G1$ to Vss.

The automatic tuning system can maintain the cut-off frequency and the Q - factor of the filter response for $\pm 30\%$ variation of the capacitance of the unity capacitors or $\pm 30\%$ variation of the sheet resistance of poly-silicon in the simulations.



(a) Frequency control signal *vba*



(b) Amplitude control signal *vcp*

Figure 4.12: Control signals of tuning circuit

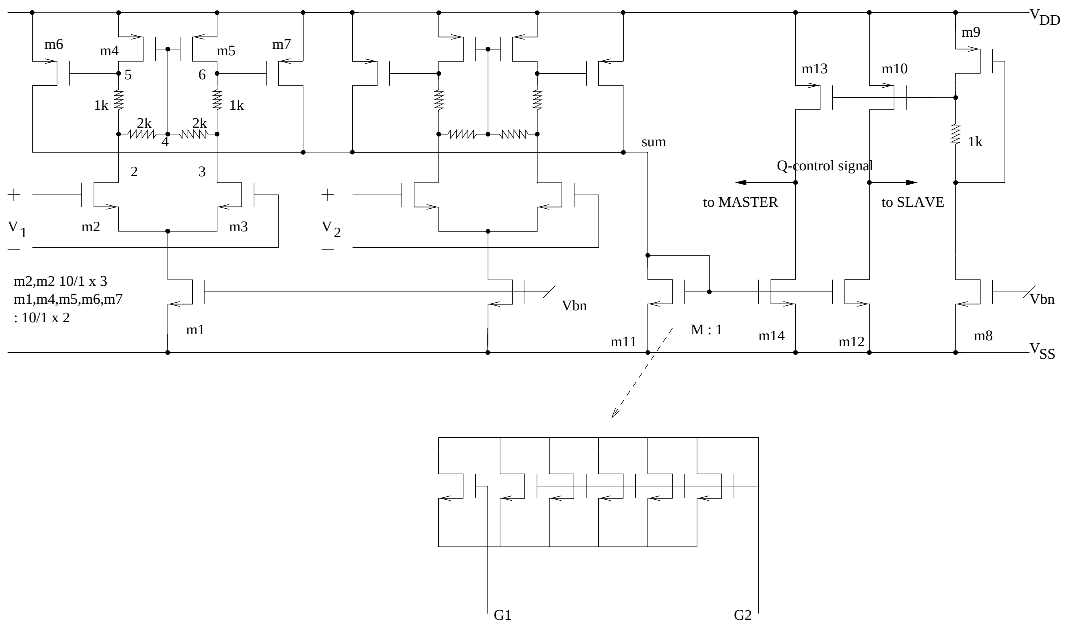


Figure 4.13: Modified amplitude control circuit

Chapter 5

Layout Considerations

5.1 Introduction

In the testing chip, we use the HP CMOS26 process 0.8μm technology to implement the prototype low-pass filter. Before going into specific details, it is worthwhile to remember that the layout of a digital circuit is completely different from the layout of an analog circuit.

A digital circuit is made by interconnecting simple blocks. The layout of the basic blocks is performed manually or with automatic tools to build up a library of basic cells. The major task is then to place the cells and route between them. The designer can perform these two steps with the help of powerful CAD tools, especially when very large networks must be created. The layout of a digital circuit is generated and intended to minimize area and signal-delay. This involves looking at the interconnections among blocks and not so much at the individual transistors.

By contrast, the layout of an analog circuit contains networks with limited complexity. A given analog integrated circuit uses the same cells a limited number of times and different designs very rarely reuse specific cells. Therefore, the layout of analog circuits mainly involves optimizing transistor layouts with much less concern for interconnections. Important design criteria influenced by the layout are accuracy and noise immunity.

It is essential that we first understand the potential impact of layout on circuit performance. The performance and function of an analog circuit often relies heavily on the precision of its components values. The unavoidable parasitic effects associated with device placement and routing can easily upset this critical precision, making analog circuits considerably more sensitive to layout induced performance degradation than the digital circuits of comparable size.

There is a taxonomy of the most commonly considered layout effects and the methods used by expert designers to minimize them. The effects can be grouped roughly as to whether they introduce problems of *circuit loading, signal coupling, or matching deficiencies.* We also pay particular attention to the device placement and routing implications of these effects [32] in the layout.

5.2 Components

This section presents layout techniques of basic elements including resistors and capacitors. Other elements can be found in [28, 32, 33].

5.2.1 Resistor

Resistors are important elements in CMOS analog integrated circuits. They are used in basic blocks such as op-amps and comparators, but much more frequently in analog systems like data converters and filters.

For high linear performance, the integrated resistor is fabricated by poly-silicon sheets. The absolute accuracy of integrated resistors is less than 30% and they exhibit poor temperature and voltage coefficients. Matching between resistors is

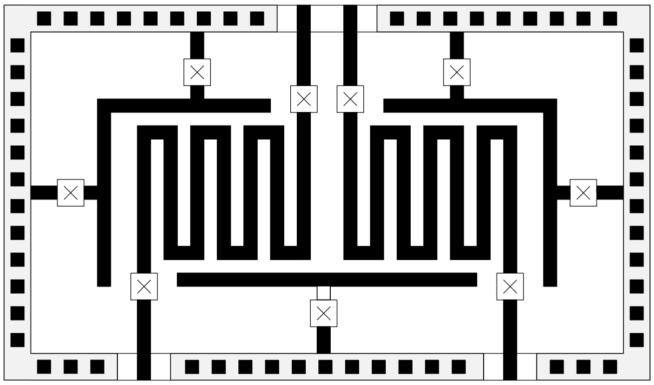


Figure 5.1: Layout of an integrated resistor

much better and can be kept, with careful layout, below 0.1% mismatch. The typical structure of the integrated resistors in this design is shown in Fig. 5.1. There are two resistors with the same resistance. A substrate bias surrounding the wells constitutes the resistor and ensures better insulation thus avoiding lateral stray resistance. Dummy strips placed around the resistors define the same boundary and help to improve resistor value control.

5.2.2 Capacitor

The capacitor is a basic building block of the OTA-C filter. To provide high linear performance and minimize the chip area consumed, we use the four layers, Metal 3, Metal 2, Metal 1 and Poly-silicon layers to fabricate the capacitors in this chip.

The nominal voltage independent capacitances of the layers are shown in Table 5.1.

It is recommended [28] to realize the bigger capacitor as the parallel connection of a number of small capacitor elements, as shown in Fig. 5.2. It is an array of 3 $\times$ 2 unity capacitors. The area-perimeter ratio is automatically kept constant.

unit area capacitance by 4 layers	0.1374 $fF/\mu m^2$
fringing capacitance by 4 layers	0.09435 $fF/\mu m$
unit area capacitance from poly to substrate	0.0575 $fF\mu m^2$
fringing capacitance from poly to substrate	0.0226 $fF\mu m$

Table 5.1: Nominal Voltage Independent Capacitances

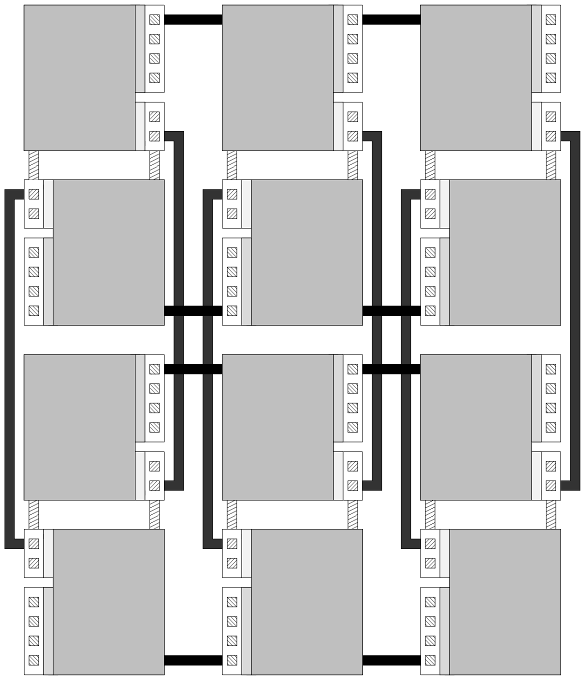


Figure 5.2: An array of 3×2 unity capacitors

Fig. 5.3a and b show the layout and the schematic of the unit-sized capacitor. Since the configuration of the biquad filter is balanced, the structure of the capacitor should also be balanced. However in Fig. 5.3c, there is a capacitor between poly-silicon layer (terminal A) and the substrate layer, (assuming the capacitances between metal layers to the substrate layer can be neglected) resulting in an unbalanced configuration. This effect will greatly degrade the performance of the filter.

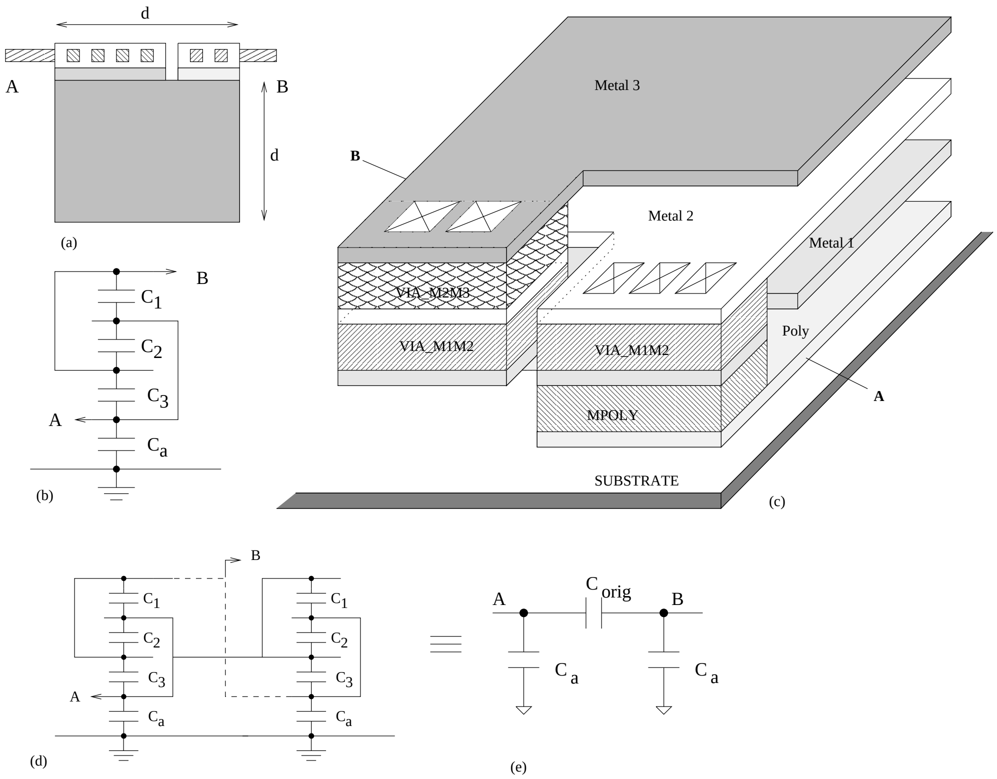


Figure 5.3: The structure of the capacitor

Two unity capacitors are connected together as shown in Fig. 5.3d to get the balanced structure. The equivalent schematic is shown in Fig. 5.3e. The capacitors C_a are absorbed into the capacitor C_{orig}. The total capacitance of Fig. 5.3d is

$$C_{eqiv} = C_{orig} + \frac{C_a}{2}$$

Table 5.2 shows the dimensions and the sizes of the unity capacitors for the loads of the 2 biquads.[1]

[1]the effect of output buffers, will be discussed in section 6.1.

	No. of row	No. of column	No. of unity cap.	size of unity cap.
capa	4	3	12	40.8 μ
capb	4	2	7	40.8 μ
capc	3	1	3	42.4 μ
capd	3	4	12	45.2 μ
cvco	2	1	2	41.0 μ

Table 5.2: Capacitors in the filter

5.2.3 Pads

Since the circuit of the filter is analog based, the pads do not require the buffer as that in digital circuits. The pads are connected in a dual ring structure. The schematic and the layout of a input/output pad, with two protection diodes is shown below.

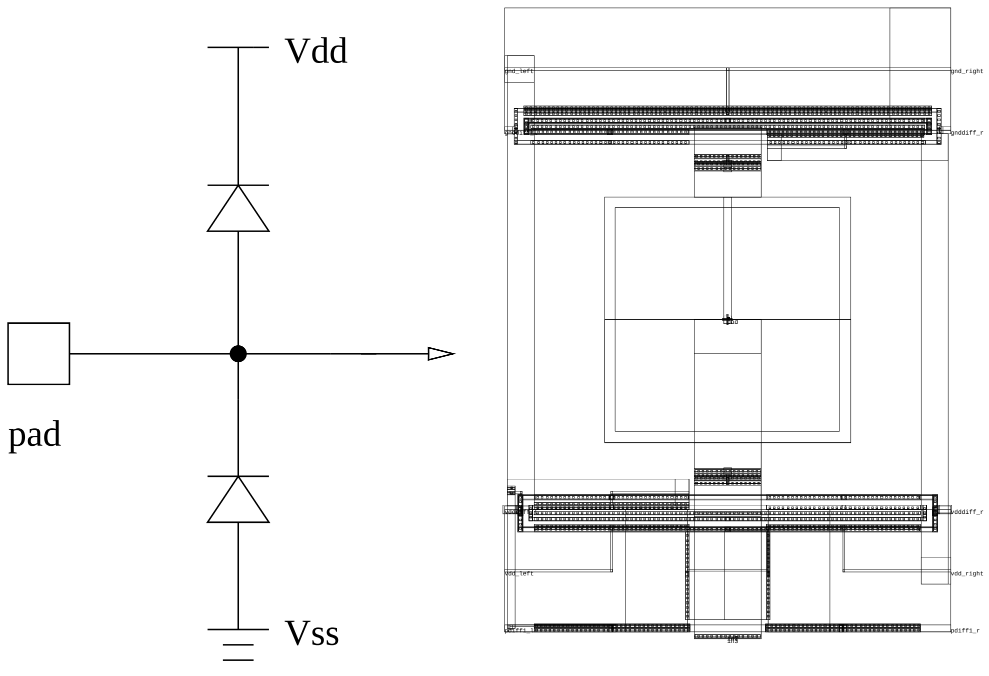


Figure 5.4: The schematic and layout of an input/output pad

5.3 Placement

During the layout stage, care was taken to place the various elements of the system in such a way as to accomplish proper matching between the filter components and also between the "master" and the "slave". Thus, all the transconductors were laid out in the same blocks with the same orientation. The tuning circuit was placed on the other side of the placement of the biquads, to minimize the noise coupled from the tuning circuit into the signal paths. The floor plan is shown below.

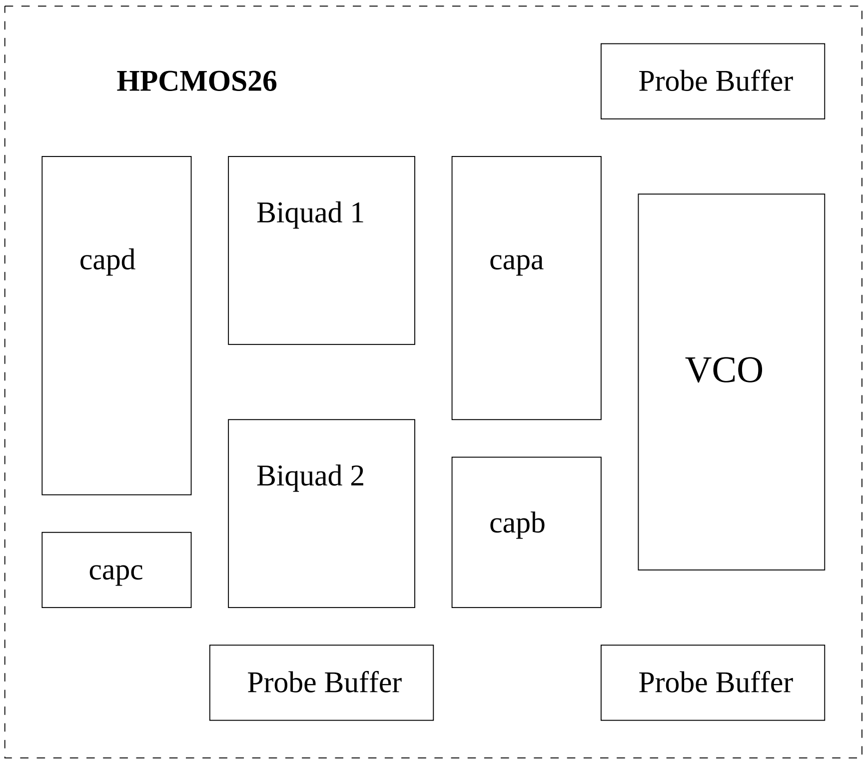


Figure 5.5: The floorplan of the testing chip

5.4 Mask Layout Issues

The mask layout of this prototype chip was performed by GDT Designer tool, which features a design database and a technology database. These databases capture the design connectivity and technology information needed in the design and verification of the integrated circuit. The final layout was throughly checked for DRC errors by the program *Checkmate* which extracts all circuit devices from the primitive mask geometries. The extracted circuits were re-simulated in HSPICE as a final verification of layout correctness.

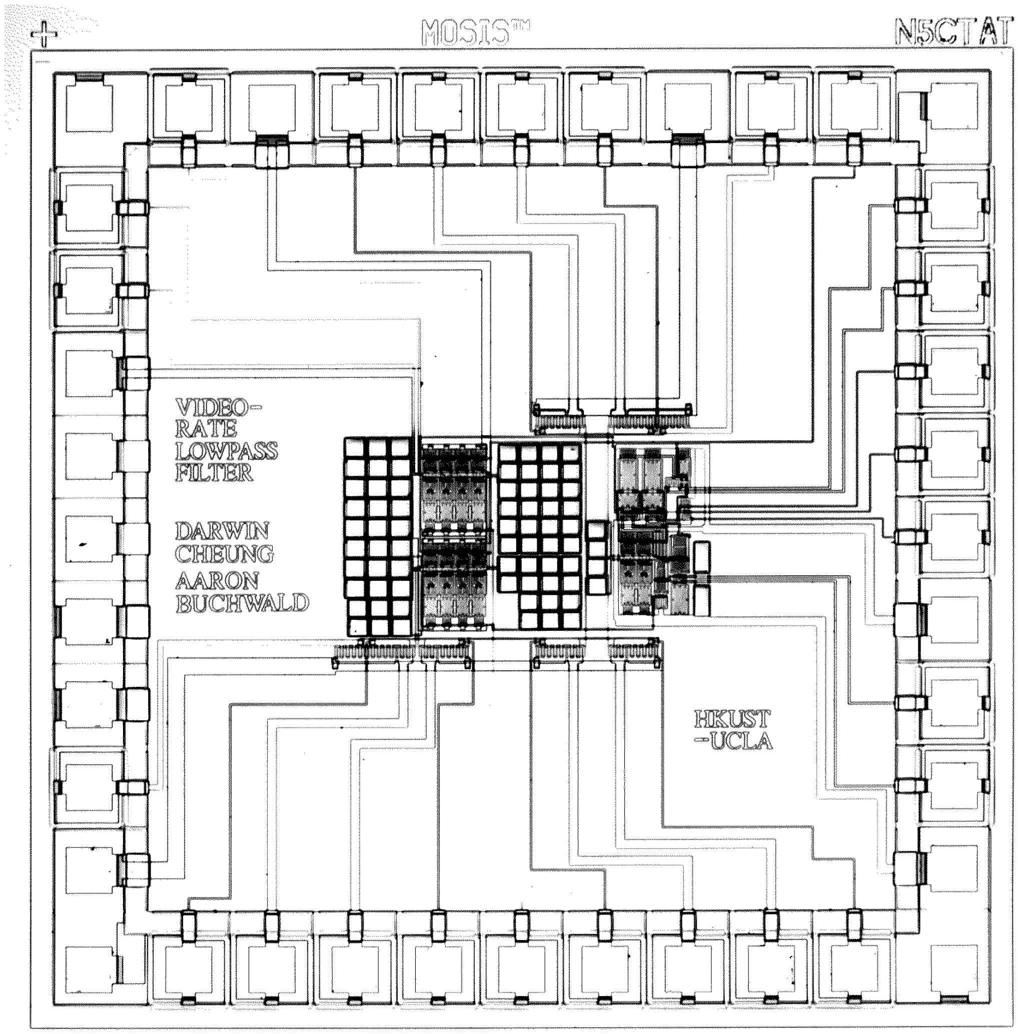


Figure 5.6: Photograph of a Low-pass filter chip

Shown in Fig. 5.6, is the chip layout of the lowpass filter. The chip was fabricated through MOSIS in a 0.8μm CMOS process. The core area consumes $0.914\text{mm} \times 0.65\text{mm} = 0.5941\text{mm}^2$ and the entire chip area occupies $2.36\text{mm} \times 2.36\text{mm}$. The testing chips were mounted in 40-pin ceramic DIP packages.

Chapter 6

Testing of a Prototype Low Distortion Video Filter and Proposed Improvements

6.1 Output Buffer

This low-pass filter is used in the front-end receiver of the CATV, but for prototype-testing purpose, the two outputs of the last biquad section are buffered and brought out of the chip for measurement. A output buffer as shown in Fig. 6.1 is cascaded to the outputs. Taking the input capacitance of the buffer into account, the value of capacitance C_d is changed to compensate the effect to have the same cut-off frequency. There is 4.8 mA across each transistor in the buffer.

Similarly, to probe out the sinusoidal waveform of the VCO, we decrease the capacitor value C_{vco} for the addition of the buffers.

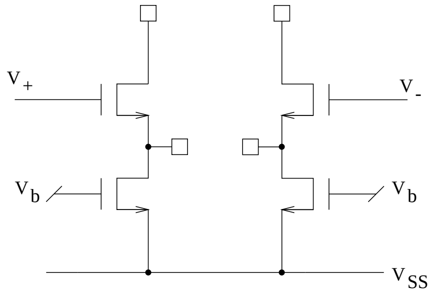


Figure 6.1: Voltage follower as the buffer

6.2 Updated simulation model

A data sheet of the parameters of the wafer is included with the 25 testing chips from MOSIS. We found that the sheet resistance of the poly-layer is 60% smaller than the value we expected, and the simulation result with this BSIM model is like the pre-simulation result in Slow-Slow process.

As discussed in section 4.9, $G1$ should be connected to V_{ss} for testing. Since the sheet resistance of the poly-layer decreases, we need to decrease the bias voltage vbn to change the current of the *amplitude detector* by force biasing externally. It makes the amplitude control loop work properly in the post-simulation.

When the value of vbn decreases a lot and the oscillation frequency increases, the loop gain of the PLL drops, the oscillation amplitude diminishes, and the circuit eventually fails to oscillate.

6.3 Prototype Circuit Testing and Measurements

The testing chip was fabricated by MOSIS in their HP CMOS26B process. In this section, we present test results from the fabricated chips.

6.3.1 Instruments

The primary measurements of interest for this IC are spectral and were handled well by Hewlett-Packard 3588A spectrum analyzer. The transfer characteristics are measured by HP8752 network analyzer. Data from the analyzers were downloaded to work-station HP382 via an IEEE-488 interface for analysis and plotting. Other measurements of interest were readily taken with good quality oscilloscopes and digital voltmeters.

6.3.2 Testing board

A circuit board was built for this IC, providing input-output support circuits, clean power distribution, and bias reference elements. Several power splitters were used for the conversions between two differential signals to a singled-ended signal.

6.3.3 Frequency Response

Nominal Performance The frequency response of the lowpass filter was measured and plotted in Fig. 6.2. The cross marks the -3dB cut-off frequency. One may observe that the cut-off frequency is around 16MHz. The derivation maybe due to

- the over-estimation of the input parasitic capacitances of the buffer and the input/output parasitic capacitances of the OTAs, or
- the Q-control voltage being too high, leading to a small peak at the passband edge and an increase of the cut-off frequency. (See Appendix D.)

The attenuation degrades somewhat at high frequencies due to parasitic signal feed-through. Figs. 6.3 and 6.4 show the corresponding phase and the group delay responses. The group delay within 800kHz to 20MHz is around 60 ± 30ns.

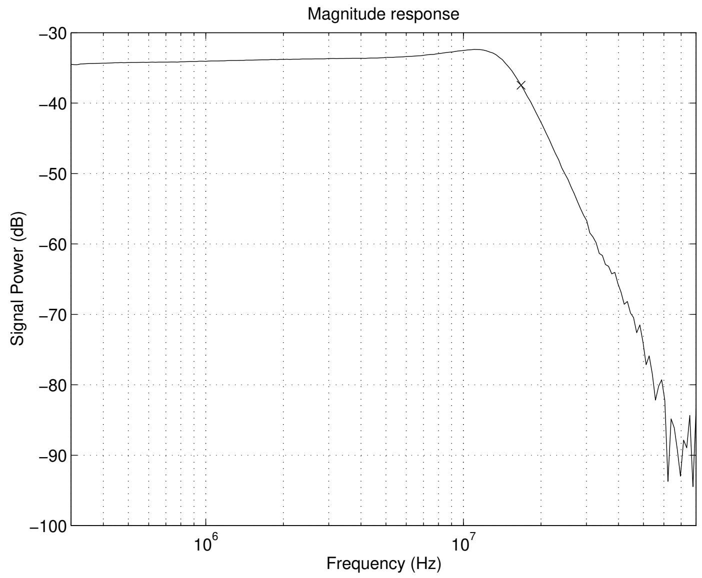


Figure 6.2: Measured frequency response of the 4th-degree Butterworth filter

Tuning Fig. 6.5 demonstrates tuning of the filter's cut-off frequency via a single rheostat adjustment from 0.9V to 1.2V. Fig. 6.6 shows Q-factor tuning via a single resistor trim. The control voltages are tuned to produce an expected frequency response with 10MHz cut-off frequency in Fig. 6.7.

Summary The frequency response measurements of this prototype filter confirm our expectations based on simulated performance of the two cascaded biquad sections. The derivations of the cut-off frequency and the quality-factor (Q) are due to automatic tuning (PLL).

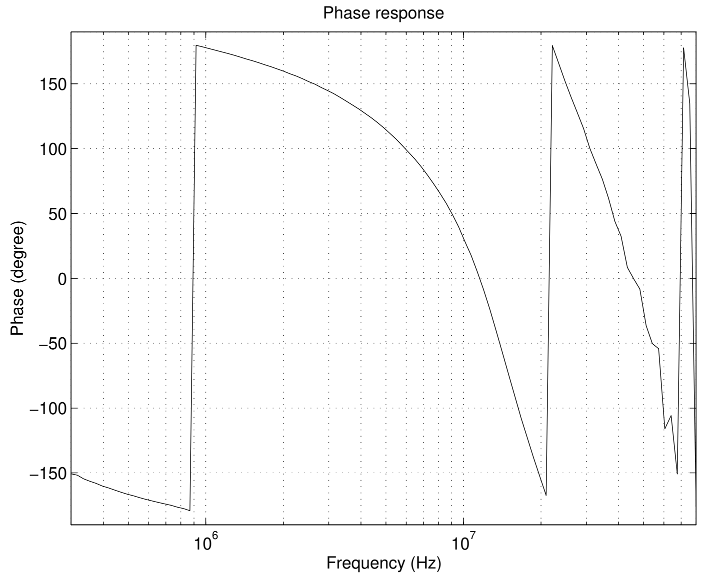


Figure 6.3: Measured phase response of the 4th-degree Butterworth filter

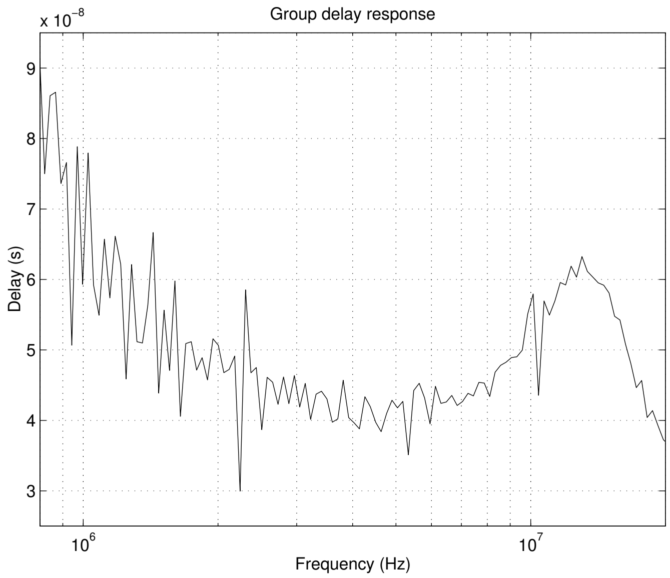


Figure 6.4: Measured group delay of the 4th-degree Butterworth filter

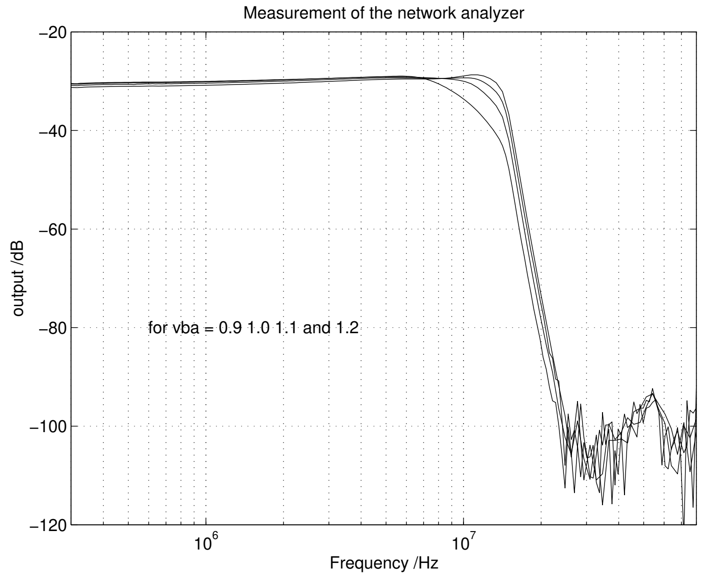


Figure 6.5: Frequency responses of the lowpass filter as *vba* is varied from 0.9 - 1.2V

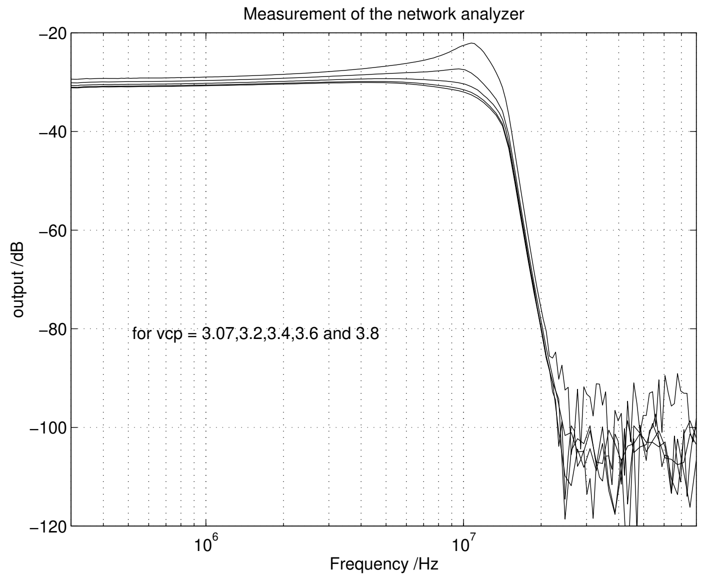


Figure 6.6: Frequency responses of the lowpass filter as *vcp* is varied from 3.07-3.8V

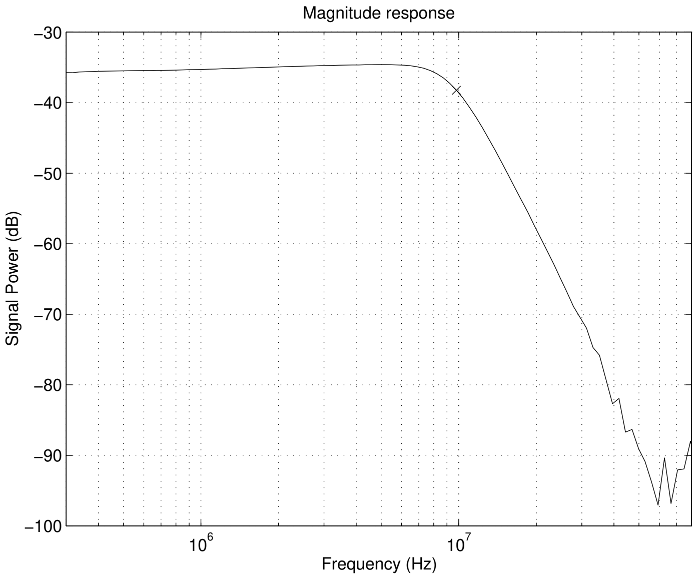


Figure 6.7: Frequency responses of the lowpass filter with tuned *vba* and *vcp*

6.3.4 Distortion

Harmonic Distortion Fig. 6.8 shows the measured harmonic distortion of the 4th-degree filter when driven by a 325mV_{pp} sinusoid at 2MHz. For this stimulus, THD is measured at better than -61dBc. The harmonic distortion at half the filter bandwidth, 8MHz, with the nominal signal level of 432mV_{pp} is shown in Fig. 6.9. Tuning the biasing voltage vbn to move the oscillating frequency of the VCO towards the passband, Fig. 6.10 shows the THD at better than -60dBc and the reference signal feed-through better than -63dBc with nominal signal level of 338mV_{pp} at 10MHz.

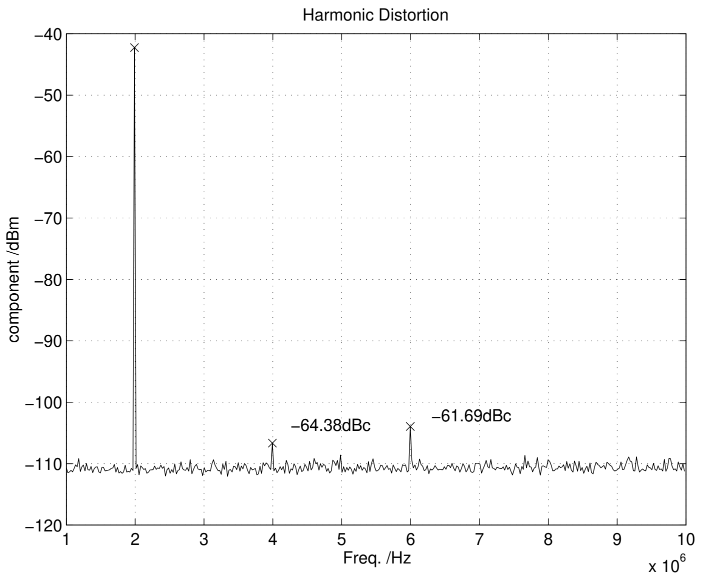


Figure 6.8: The total harmonic distortion measurement with 2MHz input

Intermodulation Distortion Intermodulation distortion in the filter for 378mV_{pp} signals near 7MHz is shown in Fig. 6.11.[1] We observed distortion performance, with third-order distortion products less than -57dBc. We set the control voltages such that the filter has a cut-off frequency of 11MHz, as shown in Fig. 6.12a. The IMD

[1] In these measurements, two sinusoidal signals of equal amplitude are summed and applied to the filter input. The stated amplitude is the combined amplitude of the composite input; each sinusoid has half that amplitude.

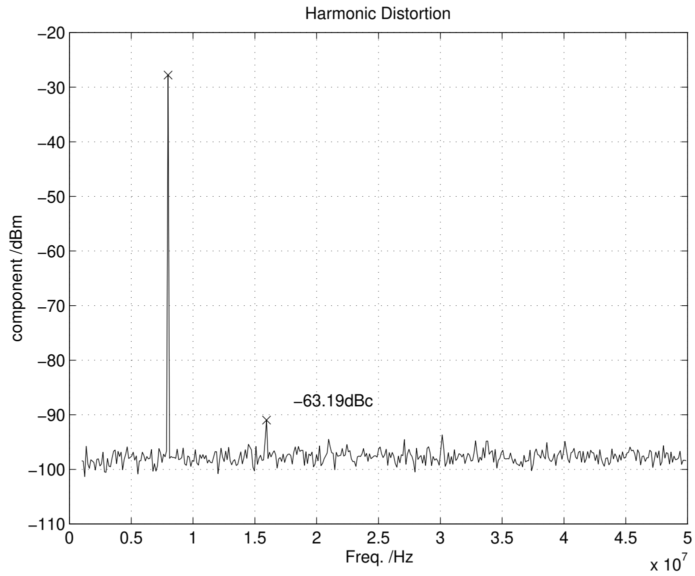


Figure 6.9: The total harmonic distortion measurement with 8MHz input

for 270mV_{pp} input signals near the passband edge shows the distortion is just better than -51dBc, as shown in Fig. 6.12b. This is reasonable as the transconductance of the integrators is small for smaller cut-off frequency. Again, we tune the filter response to have a 16MHz cut-off frequency, as shown in Fig. 6.13a. With the same input amplitude as before, we observe excellent distortion performance, with IMD less than -57dBc in Fig. 6.13b.

Summary Measured distortion performance of the prototype filter is excellent, quite comparable with the performance of all video-frequency CMOS IC filters reported to date. Some improvements should be gained in a filter with proper dynamic-range-scaling. Besides, the performance depends on the transconductance of the integrators and the qualify-factor. The automatic tuning part should be redesigned for improvement.

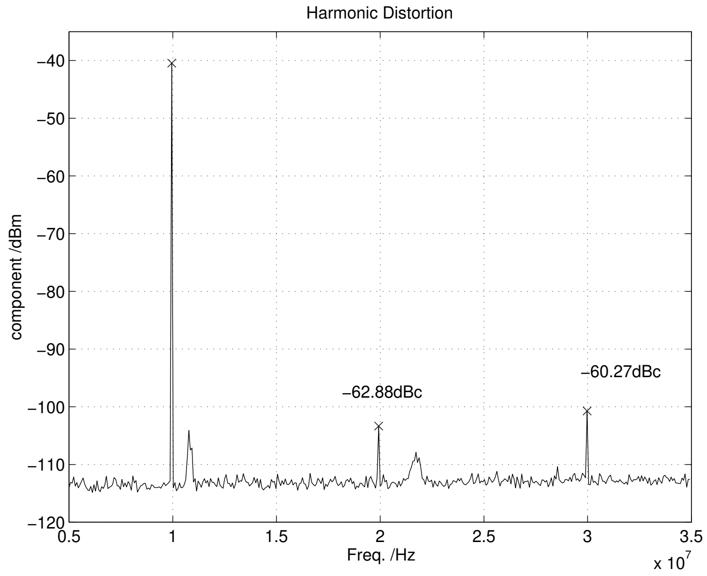


Figure 6.10: The total harmonic distortion measurement with 10MHz input

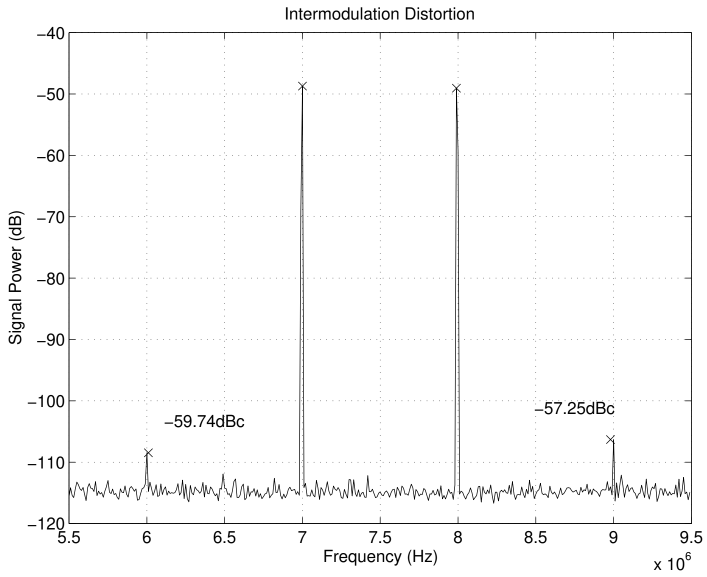
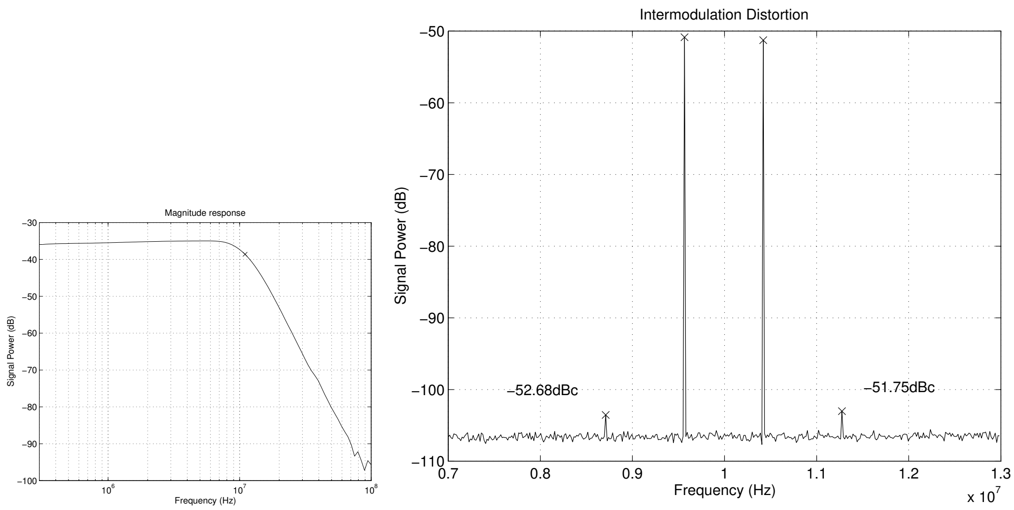


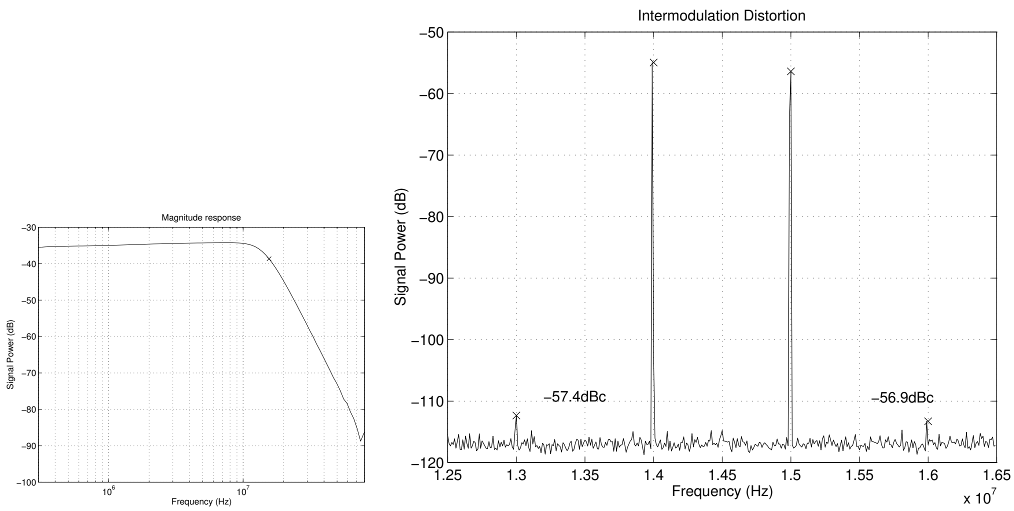
Figure 6.11: The inter-modulation distortion measurement with 6 and 7MHz inputs



(a) Frequency response with cut-off frequency of 11Mhz

(b) IMD

Figure 6.12: The inter-modulation distortion measurement with 9.5 and 10.5 MHz inputs



(a) Frequency response with cut-off frequency of 16Mhz

(b) IMD

Figure 6.13: The inter-modulation distortion measurement with 14 and 15 MHz inputs

6.3.5 Automatic Tuning

Phase Lock Loop The measured free-running frequency of the VCO is around 35.4MHz. Fig. 6.14 shows the spectrums of the VCO oscillating signal at two reference frequencies. We observe that the shape of the spectrum looks like a saddle with the locked component at the center. It is mainly due to the negative phase provided by the on-board second order RC loop filters. The characteristic of the PLL with

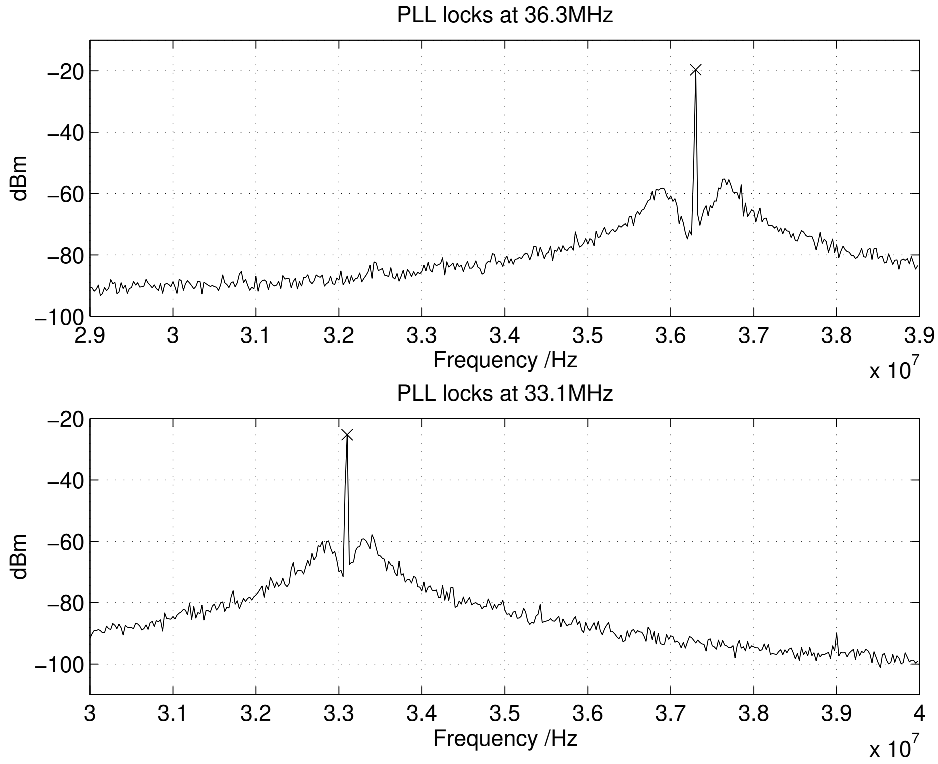


Figure 6.14: The spectrum of the VCO waveforms at 2 different reference frequencies

respect to the control voltages and the amplitude of the VCO signals is shown in Fig. 6.15. It demonstrates that the frequency control loop is not independent of the amplitude loop since the amplitude of the VCO signals varies with *vba*. This may be due to the absence of loop filter for another copy of the amplitude control signal directly back to PLL: *out* (see section 4.4).

Increasing the reference frequency from 32.5 MHz to 36.5 MHz, and then vice-versa. We can measure the frequency lock-in range and the capture range of to PLL

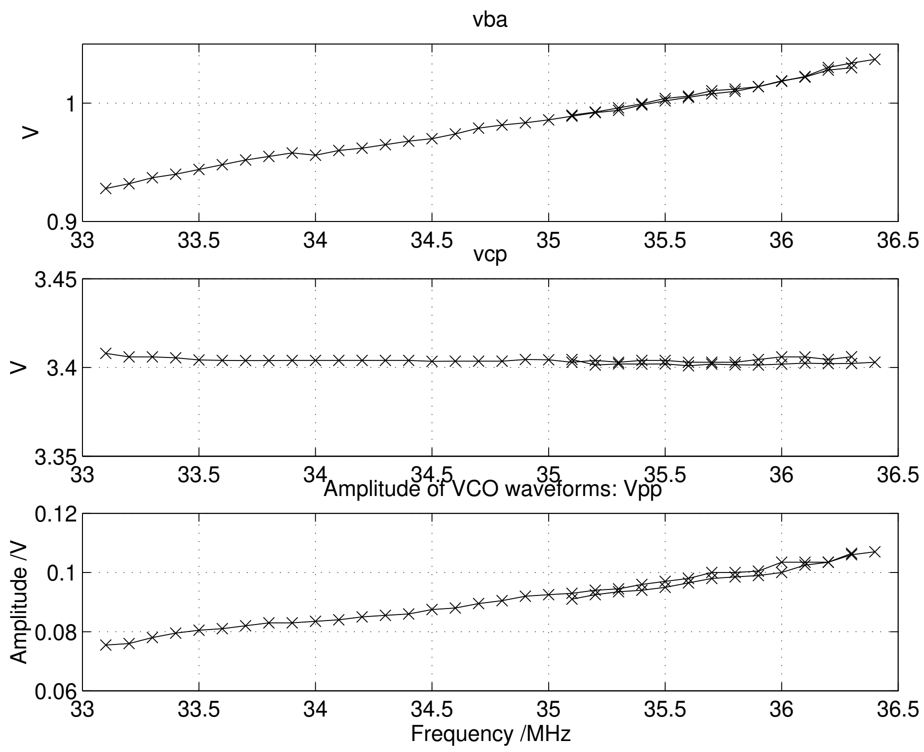


Figure 6.15: The characteristic of the PLL

as shown in Fig. 6.16. The lock-in range is about 1.3MHz and the capture range is around 3.2MHz. The range is so narrow mostly due to the small open loop gain of the PLL.

Summary The performance of the PLL is critical to that of the filter as it provides the frequency-control and amplitude-control voltages. The poor performance is mainly due to the the incorrect information of the poly-silicon sheet resistance, resulting in improper running of the amplitude detectors. Besides, the amplitude-control voltages for the VCO and the filter are separated. There may be an offset between these two, since they are outputs of high-gain circuits. Also, the absence of the loop filter for the amplitude-control voltage for the VCO may lead to the stability problem of the VCO.

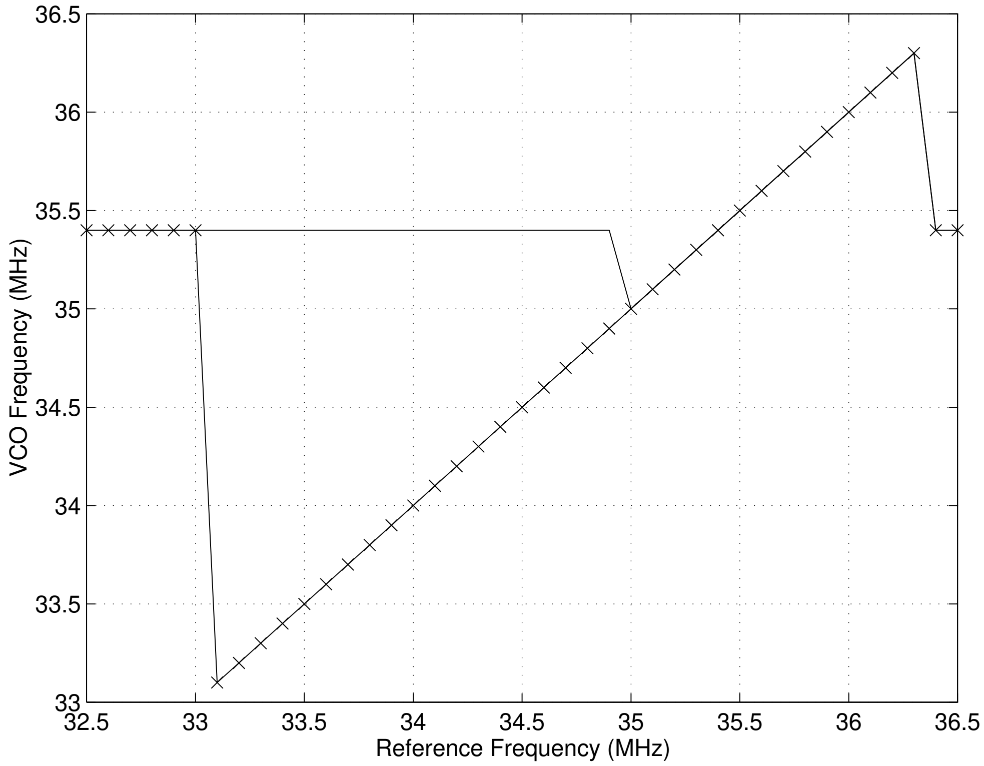


Figure 6.16: The lock-in range and capture range of PLL

6.3.6 Noise

The measured noise spectral density at the filter output shows that the noise of the spectrum analyzer is dominated, as shown in Fig. 6.17. It does not make sense to calculate the integrated RMS noise at the input with this measured noise. Since the noise analysis of the HSPICE is accurate, we use the simulated data to calculate the signal to noise ratio of this prototype chip. Fig. 6.18 shows the total equivalent input noise of the filter. The noise within 16MHz is about $130\mu V_{rms}$. For nominal signal level of 337.5mV_{pp} (120mV_{rms}), the signal to noise ratio (SNR) is about 59.26-dB. The corresponding dynamic range (SNDR) with -57-dB IMD near passband edge is 55-dB ($\sim$ 9.1 bits).

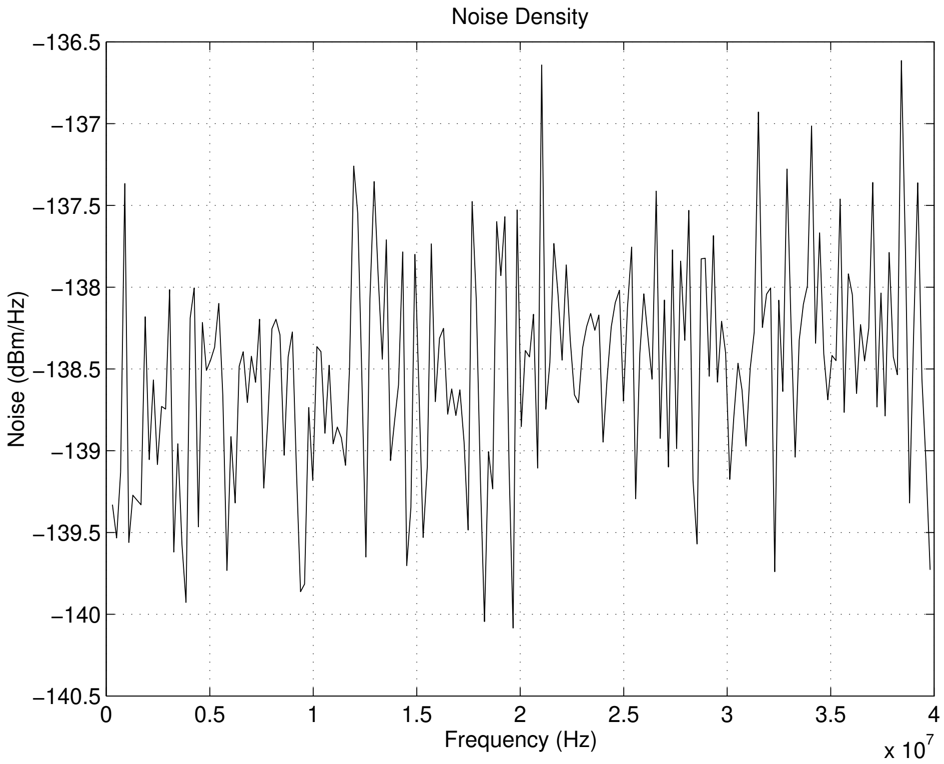


Figure 6.17: Measured noise spectral density at the output of the filter

6.3.7 Summary

The measured performance of the prototype filter is summarized in Table 6.1. With global bias of the control voltages, the filter shows good performance. The main weakness of this prototype is the automatic tuning part.

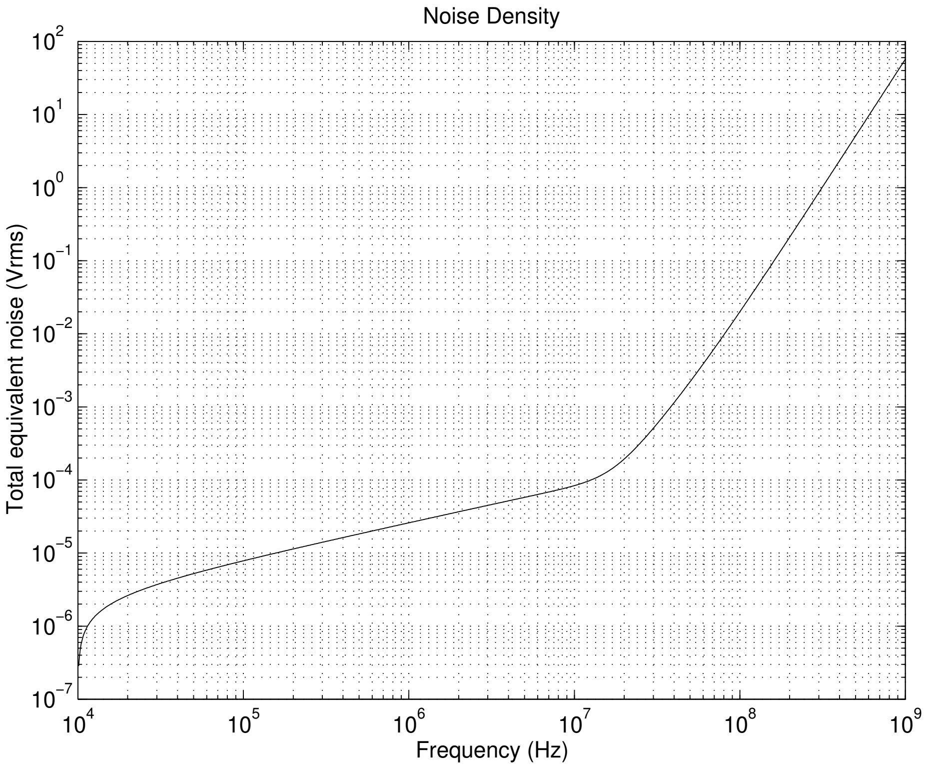


Figure 6.18: Simulated total equivalent input noise

Technology	0.8μm HP CMOS26
Filter type	Fourth-order Butter-worth
Cutoff Frequency	15 MHz
Tunable Range	1.4 MHz - 16 MHz
Group Delay	60 $\pm$ 30 ns
THD (338mV_{pp}, 10MHz input) :	-60 dB
SNR	59.26 dB
SNDR	55.00 dB
Power supply	5 V
Power Consumption	32 mW
Active Die Area	0.6 mm^2

Table 6.1: Summary of Measured Performance

6.3.8 Further Research

The measured performance of the prototype filter presented in the previous sections provides evidence of the success of this research in meeting the principal goals of this thesis.

The main directions for design improvements are motivated by observed weakness in the present design. Two types of low-pass filter with some improvements were redesigned and were fabricated by TSMC 0.5μm process. The measurement results will be published soon.

6.3.9 Lowpass filter with digital switches

Instead of applying the master-slave configuration to provide the automatic tuning to compensate the effect due to process variations, we simply use the digital switches to tune the capacitances of the filter. It can get rid of the reference signal feed-through, and consumes less area and power dissipation for the automatic tuning part.

Fig. 6.19 shows the schematic of the capacitor. The capacitances of $c3$, $c2$, $c1$ and $c0$ are in binary ratio. They can turn on or off individually by switches $b[3..0]$. The tuning can be done automatically by the digital part circuitry. For example, applying a $10MHz$ sinusoid wave to the input, and turning on and off the switches $b[3..0]$ by some digital control circuits until the output signal is about 3 dB less than the input.

The structure of the OTA is the same as before with different sizes of the transistors. Each OTA consumes more power as before in order to have a large transconductance.

Since the ratio of the capacitances of a biquad is not an integer, a number of unit-sized capacitors, *unitcap* and an additional capacitor between 1 and 2 are connected in parallel. The equivalent capacitance of a *unitcap* and the number of

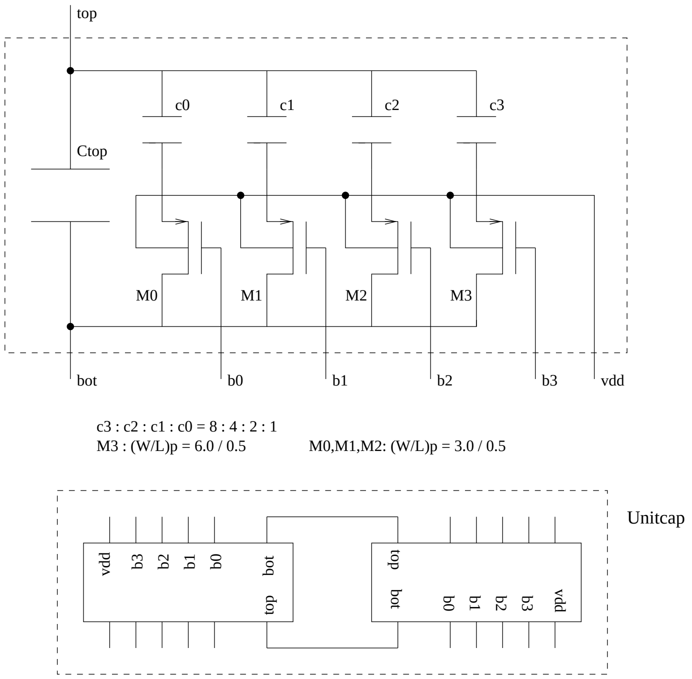


Figure 6.19: Capacitors with digital switches

unitcaps of the filter are shown in Table 6.2. The combination of $b[3..0]$ can be compensated for $\pm 40\%$ of the capacitance process variation.

For testing prototype, we can apply a constant voltage to vcp to set the quality-factor of the filter and turn on the switches manually to change the cut-off frequency of the filter.

Capacitor	equivalent capacitance
Ctop	0.24pF
c3	0.1024pF
c2	51.2fF
c1	25.6fF
c0	12.8fF

Capacitor	No. of unitcap
$capa$	$6 + 1.11$
$capb$	$3 + 1.35$
$capc$	$1 + 1.36$
$capd$	$10 + 1.07$

Table 6.2: i. Equivalent capacitance of a unitcap, ii. No. of unitcaps of a filter

Table 6.3 shows the simulations result from the Testing chip.

	Simulation Result
Input common mode :	3.5V
Input signal swing :	200mV
Output common mode :	3.305V
Output signal swing :	200mV
Power dissipation : [a]	27.6mW
Cut-off frequency :	8MHz (-1 dB)
Linearity/THD :	
1 tone (@2MHz)	-65.2dB
1 tone (@8MHz)	-72.2dB
2 tones (@$3, 4MHz$)	-67.5dB
Total Output Noise :	
1MHz	29$\mu Vrms$
10MHz	90$\mu Vrms$
100MHz	108$\mu Vrms$
1GHz	108$\mu Vrms$

[a] without the probe buffers

Table 6.3: Specifications of the improved filter I

6.3.10 Lowpass filter with improved amplitude-control loop

From the simulation results shown in the HP CMOS process, the PLL works alright, but the amplitude loop is maxed out, and the VCO amplitude is at maximum. The transistors of OTAs in the oscillator go to triode region easily. From the measurement results, we can see that the amplitude control is not working well. Some work needs to be done on the compensation for both loops.

The performance of the amplitude control loop can be improved by changing the resistor values in the SQUARE subcircuit in Fig. 4.8 from $2k\Omega$ and $1k\Omega$ to $5k\Omega$ for both. This increases the proportion of squared (amplitude-detected) signal to standing current and unrectified signal. It results in a cleaner feedback for the amplitude loop.

The two amplitude-control voltages for the VCO and the filter are combined to get rid of any offset.

Besides, a replica of SQUARE block could be used in the CONTROL block to generate the gate drive for the two top current sources. This would make the control signal for the amplitude loop to have a more direct relationship to the desired amplitude. The corresponding circuit is shown in Fig. 6.20.

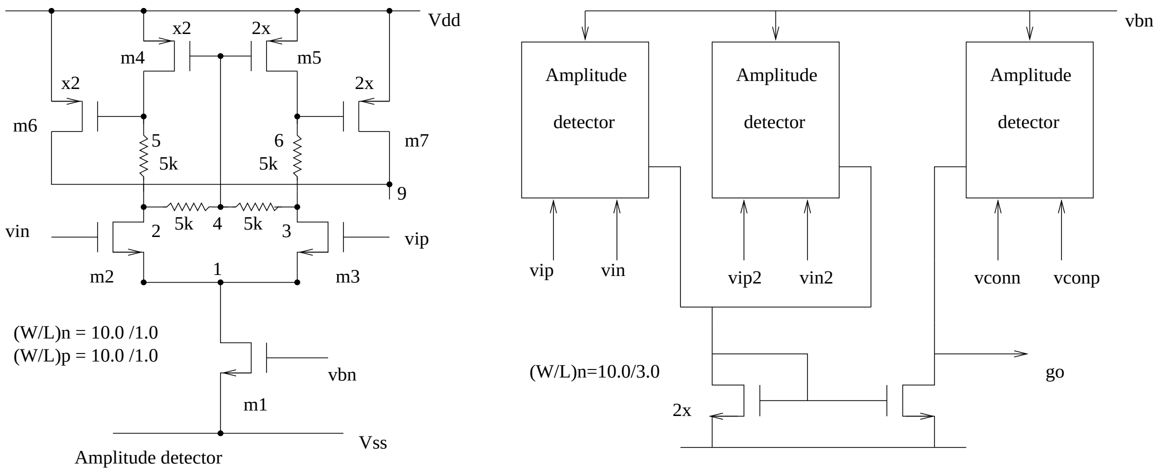


Figure 6.20: Improved amplitude control circuit

Table 6.4 shows the simulations result from the Testing chip.

	Simulation Result
Input common mode :	3.5V
Input signal swing :	200mV
Output common mode :	3.738V
Output signal swing :	200mV
Power dissipation : [a]	16.0mW
Cut-off frequency :	8MHz (-1 dB)
Linearity/THD :	
1 tone (@$2MHz$)	-45.5dB
1 tone (@$8MHz$)	-57.6dB
2 tones (@$3,4MHz$)	-53.4dB
Total Output Noise :	
1MHz	$30\mu Vrms$
10MHz	$90\mu Vrms$
100MHz	$108\mu Vrms$
1GHz	$110\mu Vrms$

[a]without the probe buffers

Table 6.4: Specifications of the improved filter II

Chapter 7

Conclusions

A 4th-order Butterworth lowpass filter is implemented by transconductance-C integrators. Two biquadratic sections are cascaded together to realize a 4th-order filter.

A differential transconductor (OTA) comprising a source-coupled pair with poly-silicon degeneration resistor and a cross-coupled high-impedance load is designed. With this transconductor, tunable integrators for very-high-frequency integrated filters can be realized. Good high-speed properties stem from the absence of internal nodes, which pushes non-dominant poles to the gigahertz range.

Dual feedback loops stabilize circuit performance against temperature- and process-variations. The resonant frequency of a master VCO, comprising back-to-back integrators, tracks the frequency of a stable reference clock by virtue of an on-chip PLL. The VCO control voltage is broadcast to all matched transconductors, thus accurately controlling natural frequencies of the filter. A separate Q-tuning loop controls the dissipation of the integrator, thus insuring a 90-degree phase shift at the resonant frequency.

Experimental results shows that 10-MHz 55-dB Dynamic Range (SNDR) 4th-order Butterworth lowpass filter is achieved.

Appendix A

Noise in MOSFETS: Brief Review

Noise is a signal with random amplitude versus time. It is generated by all passive and active devices. Its average value over a given period of time is zero and therefore its power is measured by the noise voltage squared and averaged over that time period.

There are three common distinct sources of noise in solid-state devices: shot noise, thermal noise, and flicker noise.

Shot noise Since electric currents are carried by randomly propagating individual charge carriers superimposed on the nominal current I, there is always a random variation i_{ns}. This is due to the fluctuation in the number of carriers crossing a given surface in the conductor in any time interval. It can be shown that the mean square of i_{ns} is given by

$$\overline{i_{ns}^2} = 2qI\triangle f \tag{A.1}$$

where $\triangle f$ is the bandwidth. Eqn. A.1 holds if the density of the charge carriers is so low, and the external electric field is so high, that the interactions between the carriers is negligible. Otherwise, the randomness of their density and velocity is reduced due to the correlation introduced by the repulsion of their charge. Hence, the noise current is smaller than predicted.

In a conducting MOSFET channel, the charge density is usually high and the electric field is low. Therefore, (A.1) does not hold. The noise current due to random carrier motions is hence better described as thermal noise.

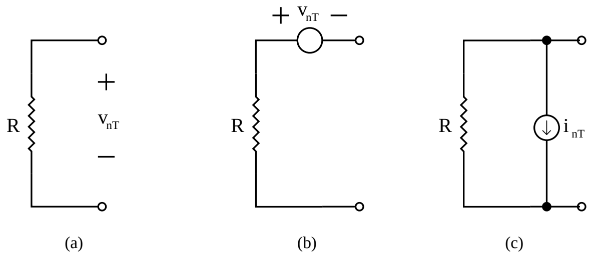


Figure A.1: Thermal noise of a resistor: (a) noisy resistor; (b) and (c) equivalent circuits.

Thermal Noise In a real resistor R, the electrons are in random thermal motion. As a result, a fluctuating voltage v_{nT} appears across the resistor even in the absence of a current from an external circuit (Fig. A.1a). Thus, the Thèvenin model of the real (noisy) resistor is shown in Fig. A.1b. Clearly, the higher the absolute temperature T of the resistor, the larger v_{nT} will be. It can be shown that the mean square of v_{nT} is given by

$$\overline{v_{nT}^2} = 4kTR\triangle f \tag{A.2}$$

where $\triangle f$ is the bandwidth in which the noise is measured in Hz. For high frequencies ($\approx 10^{13}Hz$), other physical phenomena dominate, which cause $\overline{v_n^2}$ to decrease with increasing frequency, so that the overall noise energy is finite. The average value of the thermal noise is zero. Since its spectral density $\overline{v_{nT}^2}/\triangle f$ is independent of frequency (for lower frequencies), it is a "white noise". Redraw Fig. A.1(b) in the form of Norton equivalent, that is a noiseless resistor R in parallel with a noise current source i_{nT}, the value is

$$\overline{i_{nT}^2} = 4kT\frac{1}{R}\triangle f \tag{A.3}$$

Since the channel of a MOSFET in conduction contains free carriers, it is subject to thermal noise. With R given by the incremental channel resistance, the noise can then be modeled by a current source (Fig. A.2). If the device is in saturation, its channel tapers off, and the $R \simeq \frac{3}{2g_m}$. In most circuits, it is convenient to

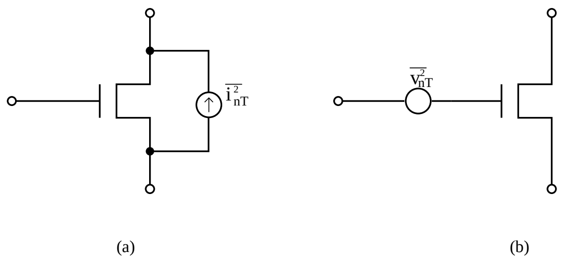


Figure A.2: Equivalent models for the thermal noise in a MOSFET

pretend that i_{nT} is caused by a voltage source connected to the gate of an noiseless MOSFET. This "gate referred" noise voltage source is then given by

$$\overline{v_{nT}^2} \simeq \overline{(i_{nT}/g_m)^2} = \frac{8}{3}\frac{kT}{g_m}\triangle f \tag{A.4}$$

Both i_{nT} and v_{nT} depend on the dimensions, bias conditions, and temperature of the device.

If the device is switched off, then R becomes very high, and the equivalent noise circuit will be a current source with a value given by Eqn. (A.3) . As $\overline{v_{nT}^2}$ is very small, the MOSFET can be regarded as a noiseless open circuit for usual external impedance level.

However [27] shows that this noise model does not accurately predict the thermal noise of MOSFET's operating in the triode region.

Flicker Noise In an MOS transistor, extra electron energy states exist at the boundary between the Si and SiO_2. these can trap and release electrons from the channel, and hence introduce noise. Since the process is relatively slow, most of the noise energy will be at low frequencies. A possible model of this noise phenomenon is a current source in parallel with the channel resistance. The dc component of the noise current is zero. Its mean-square value increases with temperature and the density of the surface states; it decreases with the gate area $W \times L$ and the gate oxide capacitance per unit area C_{ox}. For devices fabricated with a "clean" process, the gate-referred noise voltage is nearly independent of the bias conditions and is given by the approximating equation:

$$\overline{v_{nf}^2} = \frac{K}{C_{ox}WL}\frac{\triangle f}{f} \tag{A.5}$$

The noise process is called flicker noise or $1/f$ noise. It is the dominant noise mechanism in a MOSFET at low frequencies.

Appendix B

Review of Distortion

Distortion can be considered to be any change in signal waveform caused by circuit operation. Since all transistor circuits are non-linear, the voltage or current signals in such circuits are not only proportional to other signals, but are also proportional to the products, squares, and cubes, etc of the other signals. Besides, waveform alterations due to noise, interference, or even the band-limiting of a linear filter might be considered as distortion. We usually use dynamic range to indicate the level of the distortion of a circuit.

Dynamic range is the ratio of the maximum usable output voltage to the minimum usable output voltage. The maximum usable output voltage will be limited by slew rate and ultimately V_{max}. The amount of distortion tolerated for a given application is specified in terms of total-harmonic-distortion (THD). The minimum signal is limited by the internally generated noise voltages. If the signal level is less than the noise level, the noise obscures the useful signal. The amount by which the signal must exceed the noise to constitute a useful signal is specified in terms of the minimum signal-to-noise ratio (SNR).

B.1 Harmonic Distortion

In this section, we consider the signal distortion due to circuit non-linearities. In linear systems, the input can be decomposed into the sum of a set of sinusoids. The response of the system to each sinusoid is separately determined and the sum of these responses yield the system response to the original input. However, this procedure fails for non-linear systems. The response of a non-linear system to a simple sinusoidal input can contain components at multiples of the input frequency. These phenomena will complicate the analysis of the non-linear systems and circuits in the case of multiple-sinusoid input: The output may contain frequency components not produced by any input sinusoid alone.

For a circuit designed to approximate a linear system, the spurious harmonic and intermodulation products may be considered to be small aberrations in the circuit's ideal response, where we assume its input-output transfer function to be continuous and smooth.

We begin with the consideration of the simple system shown in Fig. B.1 considered at "low" frequencies where the reactive elements in the circuits composing the system are neglected.

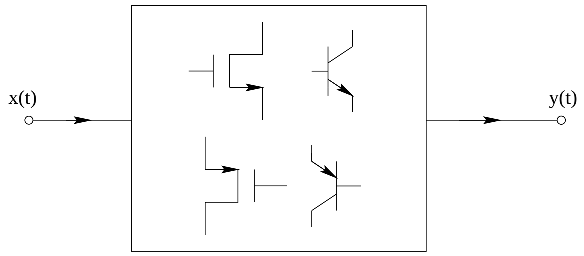


Figure B.1: A Nonlinear system

The output of the system above can be expressed as a power-series expansion around the quiescent operating point (x_o, y_o):

$$y - y_o = a_1(x - x_o) + a_2(x - x_o)^2 + a_3(x - x_o)^3 + \cdots \tag{B.1}$$

The coefficient a_1 is the familiar incremental gain of the system and the higher-order coefficients, a_2,$a_3, \ldots$, characterize its non-linear distortion. Applying a simple cosine signal, $x = x_o + \rho_x \cos \omega t$, to the system and collecting corresponding cosine terms, we get

$$\begin{aligned} y - y_o =&(\frac{1}{2}a_2\rho_x^2 + \ldots) + \ (a_1 + \frac{3}{4}a_3\rho_x^2 + \ldots)\rho_x \cos \omega t \\ &+ (\frac{1}{2}a_2 + \ldots)\rho_x^2 \cos 2\omega t + \ (\frac{1}{4}a_3 + \ldots)\rho_x^3 \cos 3\omega t \\ &+ \ldots \end{aligned} \tag{B.2}$$

The resulting system output contains terms at frequencies that are integer multiples of the input frequency – harmonics. For quasi-linear systems, the power-series terms converge rapidly and the coefficients above a_3 can be ignored, in which case (B.2) becomes

$$\begin{aligned} y - y_o \approx& \frac{1}{2}a_2\rho_x^2 + (a_1 + \frac{3}{4}a_3\rho_x^2)\ \rho_x \cos \omega t \\ &+ \frac{1}{2}a_2\rho_x^2 \cos 2\omega t + \frac{1}{4}a_3\rho_x^3 \cos\ 3\omega t \end{aligned} \tag{B.3}$$

For small inputs where $\frac{3}{4}a_3\rho_x^2 \ll a_1$, the system is said to be in its "mild-distortion" regime for which

$$y - y_o \approx a_1\rho_x \cos \omega t + \frac{1}{2}a_2\rho_x^2 \cos 2\omega t + \frac{1}{4}a_3\rho_x^3 \cos 3\omega t \tag{B.4}$$

The system's harmonic distortion is defined as the ratio of output signal amplitudes at frequencies 2ω, 3ω,$\cdots$ to the amplitude at ω :

$$\begin{aligned} \mathrm{HD}_2 &\triangleq \frac{\text{Signal amplitude at } 2\omega}{\text{Signal amplitude at } \omega} \approx \frac{1}{2}\frac{a_2}{a_1}\rho_x \\ \mathrm{HD}_3 &\triangleq \frac{\text{Signal amplitude at } 3\omega}{\text{Signal amplitude at } \omega} \approx \frac{1}{4}\frac{a_3}{a_1}\rho_x^2 \end{aligned} \tag{B.5}$$

Higher-order terms are defined similarly. The total-harmonic-distortion (THD) of a system is specified as the root-mean-square (RMS) sum of all harmonic distortion components. From (B.5), we see that given a power series expansion of the non-linear system's transfer function, the distortion products at the output for a prescribed sinusoidal input can be estimated. For signals of very small amplitude, the distortion of the system can be negligible until the signal levels are increased, with 3rd order distortion proportional to ρ_x^2.

B.2 Harmonic Pre-Distortion

Harmonic distortion is defined in terms of the output distortion products produced when a circuit is driven by a pure sinusoidal signal at its input. But sometimes we cannot express the relation directly because we cannot find a simple closed-form equation for the output in terms of the input. Hence, one might ask what input signal is required to produce a purely sinusoidal output. This is called the harmonic pre-distortion (HP), which is an analogy to harmonic distortion (HD). To visualize this, consider the input of the system in Fig. B.1 expanding in a power-series in the output variable:

$$x - x_o = b_1(y - y_o) + b_2(y - y_o)^2 + b_3(y - y_o)^3 + \dots \tag{B.6}$$

Similarly, we get

$$\begin{aligned} \mathrm{HP}_2 &\approx \frac{1}{2}\frac{b_2}{b_1}\rho_y \\ \mathrm{HP}_3 &\approx \frac{1}{4}\frac{b_3}{b_1}\rho_y^2 \end{aligned} \tag{B.7}$$

where the output of the system is $y = y_o + \rho_y \cos \omega t$.

To obtain the relations between harmonic distortion and pre-distortion, we assume an incremental input $\triangle x = x - x_o$ for which the output is $\triangle y = y - y_o$. Correspondingly, we have the following expressions

$$\triangle y = a_1 \triangle x + a_2 \triangle x^2 + a_3 \triangle x^3 + \cdots \quad \text{and} \tag{B.8a}$$

$$\triangle x = a_1 \triangle y + a_2 \triangle y^2 + a_3 \triangle y^3 + \cdots \tag{B.8b}$$

Assume the expansions in (B.8) apply around a fixed operating point, and $\triangle x = f(\triangle y)$ is monotonic , analytic, and revertable. By direct substitution and comparison of the coefficients, we solve the equations to yield

$$\begin{aligned} a_1 &= \frac{1}{b_1}, \\ a_2 &= -\frac{b_2}{b_1^3}, \\ a_3 &= \frac{2b_2^2 - b_1 b_3}{b_1^5}, \text{etc.} \end{aligned} \tag{B.9}$$

As a result, the a_i coefficients are easily determined from the b_i. Equations symmetric with those in (B.9) give the reverse relations. Substituting (B.9) into the definitions of HD and HP, we obtain the relations

$$\begin{aligned} \mathrm{HD}_2 &= \begin{cases} \mathrm{HP}_2, & \text{if } b_1 < 0 \\ \text{-}\mathrm{HP}_2, & \text{if } b_1 > 0 \end{cases} \\ \mathrm{HD}_3 &= 2\mathrm{HP}_2^2 - \mathrm{HP}_3. \end{aligned} \tag{B.10}$$

These simple relations make it easy to relate harmonic distortion directly to harmonic pre-distortion. The discussion above will be useful to later sections.

Appendix C

Output Impedance of the Cross-coupled pair

Consider the output stage shown in Fig. C.1

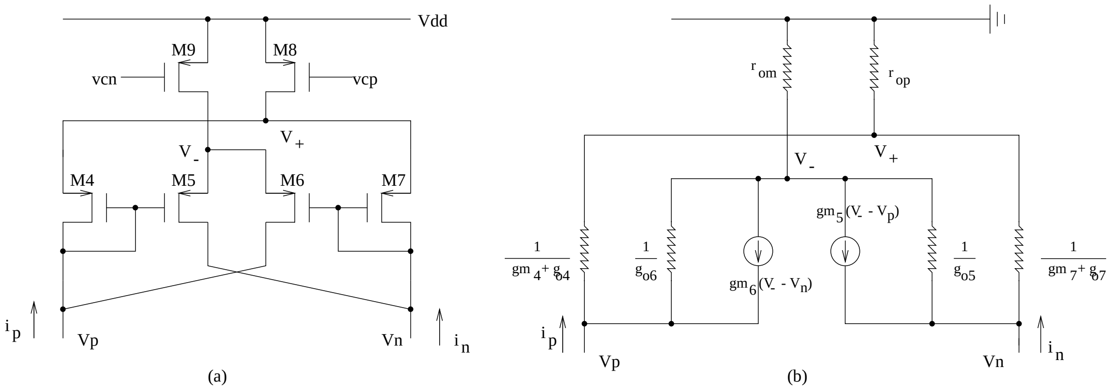


Figure C.1: Cross-coupled pairs and 2 triode transistors

To calculate the output impedance of this configuration, suppose an ideal voltage source is connected between V_p and V_n. At low frequencies,

$$i_p = (gm_4 + g_{o4})(V_p - V_+) + g_{o6}(V_p - V_-) - gm_6(V_- - V_n), \tag{C.1a}$$

$$i_n = (gm_7 + g_{o7})(V_n - V_+) + g_{o5}(V_n - V_-) - gm_5(V_- - V_p), \tag{C.1b}$$

and

$$g_{op}V_+ = (gm_4 + g_{o4})(V_p - V_+) + (gm_7 + g_{o7})(V_n - V_+), \tag{C.1c}$$

$$g_{om}V_{-} = g_{o6}(V_p - V_{-}) - gm_6(V_{-} - V_n) + g_{o5}(V_n - V_{-}) - gm_5(V_{-} - V_p) \tag{C.1d}$$

From (C.1c) and (C.1d), we get

$$V_{+} = \frac{(gm_4 + g_{o4})V_p + (gm_7 + g_{o7})V_n}{g_{op} + gm_4 + gm_7 + g_{o4} + g_{o7}}, \tag{C.1e}$$

$$V_{-} = \frac{(g_{o6} + gm_5)V_p + (g_{o5} + gm_6)V_n}{g_{om} + gm_5 + gm_6 + g_{o5} + g_{o6}} \tag{C.1f}$$

Substitute (C.1e) and (C.1f) into (C.1a), (C.1b),

$$\begin{aligned} i_p - i_n =& \frac{1}{(g_{op} + gm_4 + gm_7)(g_{om} + gm_5 + gm_6)} \times \\ & \Big\{(gm_4 - gm_5 + g_{o4} + g_{o6})V_p - (gm_7 - gm_6 + g_{o5} + g_{o7})V_n \\ & + (gm_7 - gm_4 + g_{o7} - g_{o4})\frac{(gm_4 + g_{o4})V_p + (gm_7 + g_{o7})V_n}{g_{op} + gm_4 + g_{o4} + gm_7 + g_{o7}} \\ & + (gm_5 - gm_6 + g_{o5} - g_{o6})\frac{(gm_5 + g_{o6})V_p + (gm_6 + g_{o5})V_n}{g_{om} + gm_5 + g_{o5} + gm_6 + g_{o6}}\Big\}, \end{aligned} \tag{C.1g}$$

$$\begin{aligned} \approx& \frac{1}{(g_{op} + gm_4 + gm_7)(g_{om} + gm_5 + gm_6)} \times \\ & \Big\{(gm_4 - gm_5 + g_{o4} + g_{o6})V_p - (gm_7 - gm_6 + g_{o5} + g_{o7})V_n \\ & + (gm_7 - gm_4 + g_{o7} - g_{o4})\frac{gm_4V_p + gm_7V_n}{g_{op} + gm_4 + gm_7} \\ & + (gm_5 - gm_6 + g_{o5} - g_{o6})\frac{gm_5V_p + gm_6V_n}{g_{om} + gm_5 + gm_6}\Big\}, \end{aligned} \tag{C.1h}$$

Set $V_p = \frac{\triangle V}{2}, \quad V_n = -\frac{\triangle V}{2}$,

$$
\begin{aligned}
\triangle i &= i_p - i_n \\
&= \frac{\triangle V}{2} \times \frac{1}{(g_{op} + gm_4 + gm_7)(g_{om} + gm_5 + gm_6)} \times \\
&\quad \Bigg\{ g_{op} \Bigg[(g_{om} + gm_5 + gm_6)(gm_4 - gm_5 + gm_7 - gm_6 \\
&\quad + g_{o4} + g_{o5} + g_{o6} + g_{o7}) + (gm_5 - gm_6)(gm_5 - gm_6 + g_{o5} - g_{o6}) \Bigg] \\
&\quad + (gm_4 + gm_7)(g_{om} + gm_5 + gm_6)(gm_4 - gm_5 + gm_7 - gm_6 + \sum_{i=4}^{7} g_{oi}) \\
&\quad + (gm_4 + gm_7)(gm_5 - gm_6)(gm_5 - gm_6 + g_{o5} - g_{o6}) \\
&\quad + (gm_4 - gm_7)(g_{om} + gm_5 + gm_6)(gm_7 - gm_4 + g_{o7} - g_{o4}) \Bigg\} \\
&\rightarrow 0 \quad \text{for some } vcp \text{ and } vcn
\end{aligned}
\tag{C.1i}
$$

From the symmetry of the cross-couple pairs, $gm_4 \approx gm_7$ and $gm_5 \approx gm_6$. But with different values of vcp and vcn, V_+ and V_- are not the same and transistors (M4, M7) and (M5, M6) are operated at different operating points. With the large signal and low frequency operation, the drain-current relation for PMOS transistor is :

$$
\begin{aligned}
i_D &= \mu_p C_{ox} \frac{W}{L} (v_{GS} - V_T - \frac{v_{DS}}{2}) v_{DS} \\
\frac{\partial i}{\partial v_{DS}} &= g_o = \frac{1}{\mu_p C_{ox} \frac{W}{L} (v_{GS} - V_T - v_{DS})}
\end{aligned}
$$

For fixed vcn, we can tune vcp and correspondingly changing g_{op}, to minimize the value in the right bracket of (C.1i). Then we can obtain a very high output impedance. This configuration can act as the ideal current sources for OTAs. Here, the expression of g_{op} at maximum output impedance is not shown because it is lengthy and messy.

Appendix D

Q-factor Control

Consider each OTA has a output impedance of R across the output terminals.

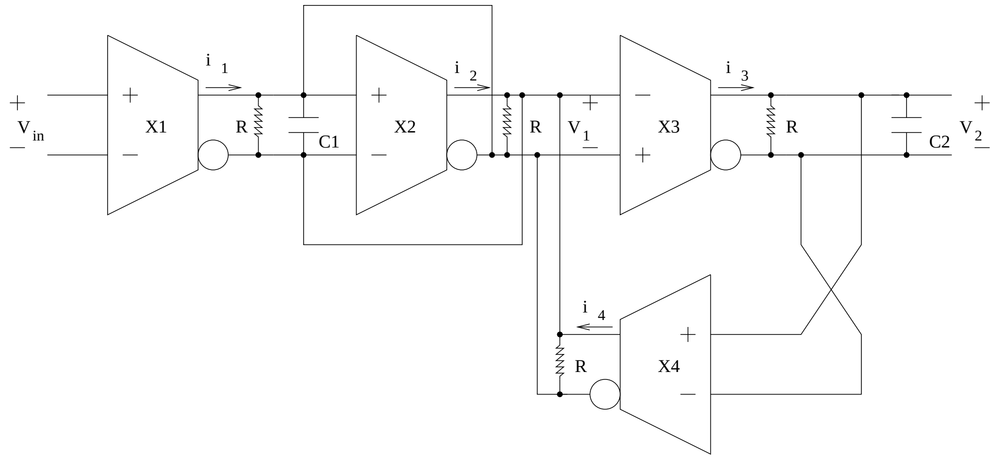


Figure D.1: 2nd order biquad section

$$\begin{aligned} i_1 &= gm_1 V_{in}, \\ i_2 &= -gm_2 V_1, \\ i_3 &= -gm_3 V_1, \\ i_4 &= gm_4 V_2. \end{aligned} \tag{D.1a}$$

and

$$-V_1 = (i_1 - i_2 - i_4)\left(\frac{1}{sC_1} \parallel \frac{R}{3}\right) \tag{D.1b}$$

$$V_2 = i_3(\frac{1}{sC_2} \parallel R) \tag{D.1c}$$

Substitute Eqn. D.1a to Eqn. D.1b, we have

$$\begin{aligned} -V_1 &= (gm_1V_{in} + gm_2V_1 - gm_4V_2)\frac{R}{3 + sC_1R} \\ \Rightarrow (gm_4V_2 - gm_1V_{in})\frac{R}{3 + sC_1R} &= (1 + \frac{gm_2R}{3 + sC_1R})V_1 \\ \Rightarrow V_1 &= \frac{\frac{R}{3+sC_1R}}{1 + \frac{gm_2R}{3+sC_1R}}(gm_4V_2 - gm_1V_{in}) \end{aligned} \tag{D.1d}$$

Then substitute Eqn. D.1d into Eqn. D.1c,

$$\begin{aligned} V_2 &= -gm_3\frac{R}{1 + sC_2R} \bullet \frac{\frac{R}{3+sC_1R}}{1 + \frac{gm_2R}{3+sC_1R}}(gm_4V_2 - gm_1V_{in}) \\ &= \frac{R}{1 + sC_2R} \bullet \frac{-gm_3R}{3 + sC_1R + gm_2R}(gm_4V_2 - gm_1V_{in}) \\ \Rightarrow &[(1 + sC_2R)(3 + sC_1R + gm_2R)]V_2 = -gm_3R^2(gm_4V_2 - gm_1V_{in}) \\ \Rightarrow V_2 &= \frac{gm_1gm_3R^2}{s^2C_1C_2R^2 + s[3c_2R + C_1R + gm_2C_2r^2] + 3 + gm_3gm_4R^2}V_{in} \\ &= \frac{\frac{gm_1gm_3}{C_1C_2}}{s^2 + s[\frac{3}{C_1R} + \frac{1}{C_2R} + \frac{gm_2}{C_1}] + \frac{gm_3gm_4}{C_1C_2} + \frac{3}{C_1C_2R^2}}V_{in} \end{aligned} \tag{D.1e}$$

Let $\omega_o^2 = \frac{gm_3gm_4}{C_1C_2}$,

$$\frac{V_2}{V_{in}} = \frac{\frac{gm_1}{gm_4}\omega_o^2}{s^2 + s\omega_o[\frac{1}{\sqrt{gm_3gm_4}}(\sqrt{\frac{C_2}{C_1}}\frac{1}{R/3} + \sqrt{\frac{C_1}{C_2}}\frac{1}{R}) + \frac{gm_2}{sqrtgm_3gm_4}\sqrt{\frac{C_2}{C_1}}] + \omega_o^2(1 + \frac{1}{gm_3gm_4R(\frac{R}{3})})} \tag{D.1f}$$

If all OTAs have the same transconductance gm,

$$\frac{V_2}{V_{in}} = \frac{\omega_o^2}{s^2 + s\omega_o[\frac{1}{gm}(\sqrt{\frac{C_2}{C_1}}\frac{1}{R/3} + \sqrt{\frac{C_1}{C_2}}\frac{1}{R}) + \sqrt{\frac{C_2}{C_1}}] + \omega_o^2(1 + \frac{1}{gm^2R(\frac{R}{3})})} \tag{D.1g}$$

If $R \to \infty$,

$$\begin{aligned} \frac{V_2}{V_{in}} &= \frac{\omega_o^2}{s^2 + s\omega\sqrt{\frac{C_2}{C_1}} + \omega_o^2} \\ \text{where } Q_o &= \sqrt{\frac{C_1}{C_2}} \quad \text{and } \omega_o^2 = \frac{gm^2}{C_1C_2} \end{aligned} \tag{D.1h}$$

Express Eqn. D.1g in terms of Q_o,

$$\frac{V_2}{V_{in}} = \frac{\omega_o^2}{s^2 + s\omega_o[\frac{1}{gm}(\frac{1}{Q_o}\frac{1}{R/3} + \frac{Q_o}{R}) + \frac{1}{Q_o}] + \omega_o^2(1 + \frac{1}{gm^2R(\frac{R}{3})})} \tag{D.1i}$$

Let $\omega_o'^2 = \omega_o^2(1 + \frac{1}{gm^2 R(\frac{R}{3})})$,

$$\frac{V_2}{V_{in}} = \frac{\omega_o'^2 \frac{1}{1+\frac{1}{gm^2 R(\frac{R}{3})}}}{s^2 + s\omega_o' \frac{1}{\sqrt{1+\frac{1}{gm^2 R(\frac{R}{3})}}}[\frac{1}{gm}(\frac{1}{Q_o}\frac{1}{R/3} + \frac{Q_o}{R}) + \frac{1}{Q_o}] + \omega_o'^2} \tag{D.1j}$$

Compared to Eqn. D.1h, the gain factor is

$$gain = \frac{1}{1 + \frac{1}{gm^2 R^2/3}} < 1 \tag{D.1k}$$

and the new central frequency ω_o' is

$$\begin{aligned} \omega_o'^2 &= \omega_o^2(1 + \frac{1}{gm^2 R^2/3}) \\ \Rightarrow \omega_o' &= \omega_o \sqrt{1 + \frac{1}{gm^2 R^2/3}} > \omega_o \end{aligned} \tag{D.1l}$$

and the Q factor is

$$Q = \frac{\sqrt{1 + \frac{1}{gm^2 R^2/3}}}{\frac{1}{Q_o} + \frac{1}{gmR}(\frac{1}{3Q_o} + Q_o)} \tag{D.1m}$$

Hence, Q can be either increased or decreased by R. But the cost is the gain loss and the increase of the central frequency ω_o'.

Appendix E

Amplitude Control Circuit

Consider the amplitude detector as shown in Fig. E.1, the voltage between nodes 2 and 3 is proportional to the input voltage. Resistors $R1$ and $R2$ limit the voltage swing at these nodes. Resistors $R3$ and $R4$ provide a level shift of the these nodes to reduce the current comsumed at $M6$ and $M7$. Besides, transistors $M4$, $M5$ and $R1, R2, R3, R4$ form the negative-feedback loops to act as a CMFB circuit.

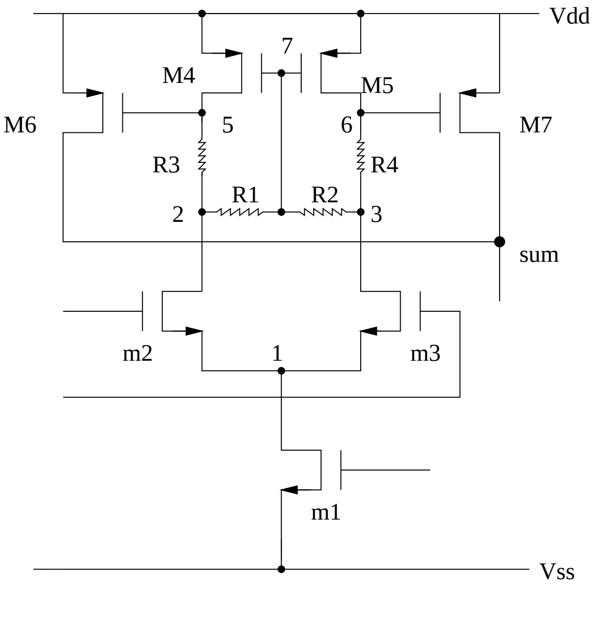


Figure E.1: Amplitude Detector

The current drawn by $M6$ ($M7$) is proportional to the square of voltage node 5 (6). Both currents are summed at node *sum*. As a result, the current at *sum* is proportional to the square of the input voltage.

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