A CMOS 10-Mbaud 20-mW PAM/QPSK Modulator Using a Digital-to-Analog Current-Division Square-Root-Cosine Waveshaping Converter

A thesis submitted
in partial satisfaction of the requirements for
the Degree of Master of Philosophy in
Electrical and Electronic Engineering

by

Kenneth Ka Lun Choi
Department of Electrical and Electronic Engineering
The Hong Kong University of Science and Technology
Hong Kong, 1996

A CMOS 10-Mbaud 20-mW PAM/QPSK Modulator Using a Digital-to-Analog Current-Division Square-Root-Cosine Waveshaping Converter

by

Kenneth Ka Lun Choi

Approved by:

____

Dr. Howard Luong , Thesis Co-supervisor

____

Prof. K.C.Smith , Thesis Examination Committee Chairman

____

Dr. Wing-Hung Ki , Research Committee Member

____

Dr. Philip Chan , Acting Head of the Department

Department of Electrical and Electronic Engineering
The Hong Kong University of Science and Technology

To

My parents

CONTENTS

LIST OF FIGURES iii

1 OVERVIEW OF QAM TRANSMISSION SYSTEMS 1
- 1.1 Introduction 1
- 1.2 General Aspects of QAM Systems 3
- 1.3 Waveshaping and Intersymbol Interference (ISI) 5
- 1.4 Comparison of QAM Modulators 6

2 FILTER DESIGN CONSIDERATIONS 11
- 2.1 All Digital QAM Modulator 11
- 2.2 Transmission Filter Characteristics 13
- 2.3 Matched Filter 14
- 2.4 sin(x)/x Compensation 15
- 2.5 Filter Design 15
- 2.6 Sample Functions and Eye-Diagrams 18
- 2.7 Summary 22

3 ARCHITECTURAL SIMPLIFICATION 25
- 3.1 Interpolation 25
- 3.2 Constraining the IF center frequency 26
- 3.3 Summary 28

4 CIRCUIT DESIGN 31
- 4.1 Current Division Technique 31
- 4.2 Architecture for Multiplication 33
- 4.3 Current-Division Waveshaping Converter 34

5 VLSI IMPLEMENTATION 37
5.1 Floor Plan 37
5.2 Layout Compiler 38
5.3 Actual Layout 39

6 SIMULATION AND TEST RESULTS 41
6.1 Simulation Results 41
6.2 Test Results 43
6.3 Problems and Future Research 48
6.4 Conclusions 50

A MATLAB PROGRAMS 53
A.1 Matlab Simulation Programs 53

REFERENCES 61

LIST OF FIGURES

Chapter 1

1.1	General QAM modulation system.	3
1.2	Frequency spectrum of square data pulses.	6
1.3	All analog QAM transmission system.	7
1.4	Transmission system using table-look-up method.	8
1.5	Digital QAM waveshaping with dual baseband DACs.	8
1.6	QAM waveshaping with a merged DAC and digital filter	9

Chapter 2

2.1	Digital QAM Modulator.	11
2.2	16-QAM and QPSK constellation plane.	12
2.3	Impulse response of a Nyquist filter.	13
2.4	Frequency response of a raised-cosine Nyquist filter.	14
2.5	Impulse response of transmit filter, $t(t)$.	17
2.6	Frequency response of transmit filter $T(f)$.	17
2.7	Frequency response of $T(f)Z(f)$.	18
2.8	Impulse response of $T(f)Z(f)R(f)$.	18
2.9	Frequency response of $T(f)Z(f)R(f)$.	19
2.10	(a) Input data to be transmitted; (b) frequency spectrum of the input data.	20
2.11	Frequency spectrum of the (a) transmitted and (b) received signal.	20
2.12	The waveform of the (a) transmitted and (b) received signal.	21
2.13	Eye diagram of the (a) transmitted and (b) received signal.	21
2.14	The IF QPSK modulated signal.	22

Chapter 3

3.1 Interpolation. 26
3.2 Baseline QPSK modulator. 27
3.3 Polyphase decomposition of QPSK modulator. 28

Chapter 4

4.1 The basic principle of current division. 32
4.2 Multiplier based on CDT. 33
4.3 Digital-to-analog current-division waveshaping converter. 35
4.4 Polyphase implementation of a QPSK modulator, using the digital-to-analog current-division waveshaping converter. 36
4.5 Timing diagram of different clock signals. 36

Chapter 5

5.1 Layout floor plan of the PAM/QPSK modulator 37
5.2 Layout hierarchy of the QPSK modulator. 38
5.3 Layout of the QPSK modulator. 40

Chapter 6

6.1 Simulated impulse responses of the modulator. 42
6.2 Simulated output spectrum of the modulator at (a) baseband (b) IF 42
6.3 Die photo of the PAM/QPSK modulator. 43
6.4 Measured impulse response of the modulator. 44
6.5 Measured eye-diagram of the I or Q channel at f_s=2-Mhz. 45
6.6 Measured eye-diagram of the I or Q channel at f_s=40-Mhz. 45
6.7 Measured output spectrum of the I or Q channel at f_s=2-Mhz. 46
6.8 Measured output spectrum of the I or Q channel at f_s=40-Mhz. 46
6.9 Measured output spectrum of the modulator at fs=2Mhz. 47
6.10 Measured output spectrum of the modulator at fs=40Mhz. 47
6.11 Alternative multiplier for QPSK modulator. 48

Appendix A

ACKNOWLEDGMENTS

I would like to express my gratitude to my MPhil project advisor, Dr. Aaron Buchwald for his technical guidance and suggestions for my masters thesis.

I also wish to thank my colleagues and friends in the Analog Integrated Circuits Research Laboratory at the Hong Kong University of Science & Technology for their invaluable support and encouragement; especially to my labmates, Darwin, Felix and Leonardo. I would like to thank the staff of Broadcom Corporation for their help in using the *Mentor Graphics GDT CAD* system and in testing of the prototype modulator circuit; in particular, thanks to Sam Liu, Agnes Woo, Dr. Loke Tan, Ken Kindsfater and Dr. Robin Joshi, with special thanks to Dr. Tom Kwan for his revision of this thesis.

Finally, I would like to thank my mother. She is the most important person in my life.

Kenneth Ka Lun Choi

Hong Kong, November 1996

ABSTRACT

The purpose of this research is to design and implement a low-power, high-speed, high-accuracy QPSK modulator using a novel digital-to-analog current-division technique, which efficiently merges the FIR filtering operation and the DAC functions into the same circuitry.

Design techniques and measured results of a prototype CMOS modulator for broadband PAM and QPSK data formats are presented. The circuit is based on a poly-phase implementation of a traditional all-digital architecture. Reduction in area and power is accomplished by using a digital-to-analog current-division square-root-cosine waveshaping converter. Digital data is applied at the input and a filtered analog waveform is produced at the output, without the need for a standard D/A converter at the back-end. The circuit has been fabricated in a 0.8-μm CMOS process (MOSIS HPCMOS26G), occupies an area of 1.2-mm$\times$1.213-mm, and dissipates 30-mW from a single 5V supply. The maximum baud-rate of the modulator is 10-Mbaud at a sample-rate of 40-MHz. The 33-tap FIR waveshaping filter insures out-of-band ripples are suppressed by more than 32-dB. This modulator is applicable to broadband digital communication such as wireless telephony, wireless modems, digital video, and digital subsriber line systems.

As far as the laws of mathematics refer to reality, they are not certain, and as far as they are certain, they do not refer to reality.

— Albert Einstein

1

OVERVIEW OF QAM TRANSMISSION SYSTEMS

1.1 INTRODUCTION

Quadrature Amplitude Modulation (QAM) has become the dominant data-format for broadband digital communication systems. Commercial deployments of QAM technology include such applications as digital cable TV, cable modems and voiceband modems. Recently, telecommunications companies are considering QAM solutions for DSL (Digital Subscriber Line) and are moving away from Discrete Multi-Tone (DMT) systems, which result in very expensive VLSI realizations. QAM is also the predominant modulation technique used in high-data-rate digital microwave radios with data rates of several hundred megabits-per-second. In addition, digital Direct Broadcast Satellite (DBS) systems exclusively employ QPSK modulation (4-QAM) worldwide.

Broadband QAM systems for the commercial market require efficient and inexpensive transceivers. Therefore, a high-degree of integration is desirable. A series of digital implementations of QAM systems has recently been developed which takes advantage of the rapid improvements in CMOS technology [1]. However, a complete transceiver cannot be totally digital, but requires a Digital-to-Analog Converter (DAC) at the transmitter, and an Analog-to-Digital Converter (ADC) at the receiver. These data conversion operations often limit the performance of the overall system, especially for high data rates and large constellations such as 64-QAM or 256-QAM.

Previous design approaches have separated the digital transceiver function from the data converters. Although this is a logical partition, the ultimate system performance is left in the hands of the data-converter designer and is taken away from the receiver designer. To move to the next level of integration, the data-converters must be considered as an integral part of the overall system. However, as yet, high-speed low-power solutions based on a hybrid digital-analog techniques for QAM transmission system have not been thoroughly explored.

In this thesis, the focus is on developing a high-speed-monolithic solution for a QPSK (4-QAM) transmitter. A systems-level approach to the design of the transmission filter and the DAC is taken. Significant reductions in complexity are possible due to the fact that a general purpose DAC is not required; only a DAC which performs waveshaping for a well-defined set of inputs is needed [2]. Given this knowledge, the waveshaping FIR filtering function can be merged with the DAC, resulting in a very low-power area-efficient modulator which produces a direct IF analog output.

This chapter will briefly review quadrature amplitude modulation. An overview of a general QAM system will be presented. Various implementations of a QAM modulator will then be compared to the proposed approach.

1.2 GENERAL ASPECTS OF QAM SYSTEMS

Phase/Frequency modulation is widely used to translate a baseband signal to a higher frequency where it is more suitable for transmission through a channel. In passband modulation schemes, QAM has been proven to be highly bandwidth- and power-efficient [3]. A typical QAM transmission scheme is shown in Fig. 1.1. The transmitted IF signal consists of the sum of two independent signals, $I(t)$, and $Q(t)$, modulated by carriers of the same frequency, but separated by a 90° phase-shift.

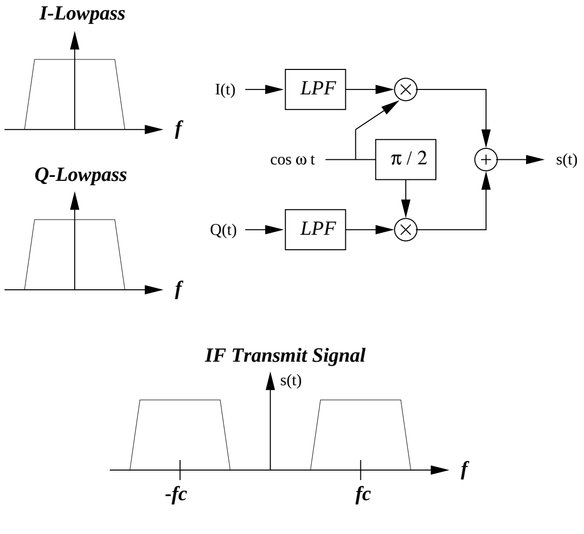

Figure 1.1 General QAM modulation system.

$$s(t) = I(t) \cdot \cos \omega_c t - Q(t) \cdot \sin \omega_c t \tag{1.1}$$

In the frequency domain, I and Q represent two bandlimited signals which are mixed up to the intermediate frequency (IF), f_c.

A significant advantage of QAM is that both the *In-Phase*, $I(t)$, and *Quadrature*, $Q(t)$, signals occupy the same bandwidth, thereby allowing twice the data transmission for a given spectrum allocation. It is possible to separate the I and Q channels at the receiver because the carriers ($\cos \omega_c t$ and $\sin \omega_c t$) are orthogonal, meaning that the integral of their product over an integer number of periods goes to zero;

$$\int_0^{NT_c} \cos \omega_c t \cdot \sin \omega_c t \; dt \equiv 0 \tag{1.2}$$

Provided that the carrier-phase can be recovered at the receiver (*coherent detection*), the two baseband data channels can be extracted as in a Fourier series,

$$I(t) = \frac{2}{NT_c} \int_0^{NT_c} s(t) \cos \omega_c t \; dt \tag{1.3}$$

$$Q(t) = -\frac{2}{NT_c} \int_0^{NT_c} s(t) \sin \omega_c t \; dt \tag{1.4}$$

Bandwidth efficiency is defined as the ratio of the bit-rate of the modulator to the bandwidth of the signal occupied. As stated, QAM has twice the bandwidth efficiency of a similar Pulse-Amplitude Modulation (PAM) system. However, A PAM system can approach the bandwidth efficiency of a QAM system by using Single-Sideband (SSB) modulation, where the spectral redundancy in the negative frequencies are suppressed using specialized filters.

However, the filters required for SSB transmission are complex and difficult to implement in VLSI [4] and they can only approximate true SSB operation.[1]

Power efficiency can be characterized by the probability of making an error at the receiver as a function of the signal-to-noise ratio (SNR). For QAM systems, the bit-error-rate (BER) is low with respect to a fixed signal-to-noise ratio as compared to other non-coherent systems such as Frequency Shift Keying (FSK).

1.3 WAVESHAPING AND INTERSYMBOL INTERFERENCE (ISI)

In most digital communication channels, significant degradation of the pulse waveform can result if the bandwidth of the transmitted signal is not limited. If square data pulses are transmitted, the zero-crossings will be distorted by the channel and excess energy from the sharp edge transitions can leak into adjacent channels. Square pulses have a wide energy spectrum with an envelope of $\mathrm{sinc}(f/f_b)$ [5] as illustrated in Fig. 1.2.

In order to limit the bandwidth of the data signal, filtering of the transmitted pulses is necessary. However, severe ISI could occur if the filtering is not properly performed. Therefore, a special type of filter, known as a *Nyquist filter* has to be designed for shaping the transmitted pulses. For a QAM transmission system, the goal is to design an efficient way to do waveshaping with minimum

[1] In practice the redundant negative spectrum can not be completely suppressed; a *vestige* of the spectrum is left behind. This technique is, therefore, known as Vestigial Sideband (VSB) modulation.

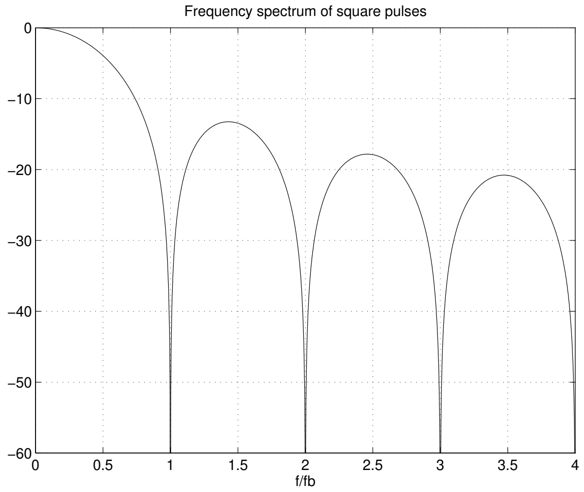

Figure 1.2 Frequency spectrum of square data pulses.

ISI. In the next section, several implementations of this waveshaping operation will be presented and their advantages and disadvantages will be discussed.

1.4 COMPARISON OF QAM MODULATORS

Analog Filters: Several high-bit-rate digital transmission systems use analog hardware (Fig. 1.3) to do the baseband signal processing. For instance, in [6], a 400-Mb/s 256-QAM modem is discussed which uses analog circuits for most of the signal processing functions. The waveshaping filters are continuous-time Bessel filters, which approximate a linear-phase transfer function. Phase-linearity is important to maintain control over ISI. However, because of the diverse technologies employed, these systems are relatively costly and difficult to manufacture. Some of them also require trimming and calibration.

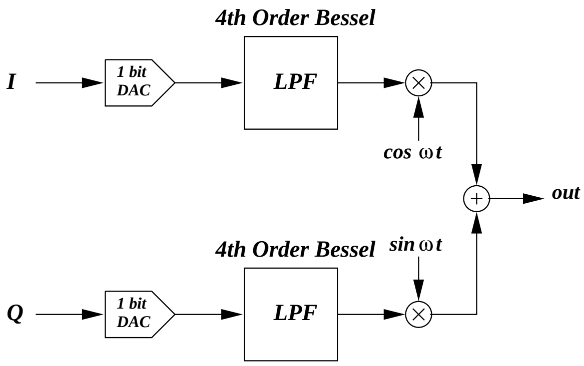

Figure 1.3 All analog QAM transmission system.

Look-Up Tables: To avoid the disadvantage of the high-sensitivity of analog waveshaping filters, digital baseband processing can be used to generate the waveforms; DACs then convert these digital waveforms to analog signals. A simple approach uses a table-look-up method as shown in Fig. 1.4. The modulator maps the input bit-stream to the corresponding waveshaping patterns from a look-up table, which is usually implemented by a read only memory (ROM). Dual baseband DACs could be used with the resulting pair of analog signals being mixed to IF, or, if a high-resolution, high-speed DAC is available, all-digital modulation is possible and a single IF DAC can generate the transmitted analog signal.

The disadvantage of this approach is that the ROM must store all the possible waveshapes and grows exponentially as the number of filter taps (number of data symbols overlapped by one waveform) expands, the oversampling ratio grows, or the number of QAM levels increases. Therefore, for all but simple cases (5-taps, 4x-oversampled, 16-QAM), the ROM quickly expands to the point where this method becomes very inefficient.

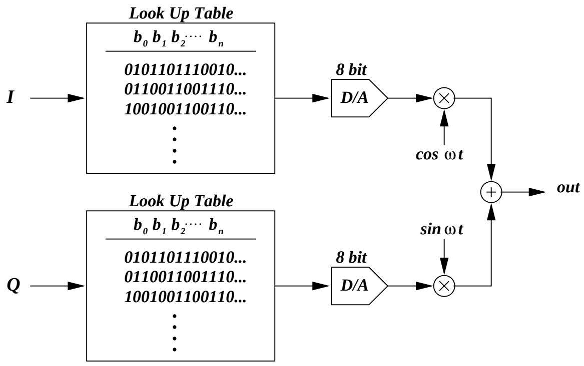

Figure 1.4 Transmission system using table-look-up method.

Digital Filters Another approach that has been widely utilized is the employment of digital FIR transmission filters. Because FIR filters can be designed to have a linear phase-response, are inherently stable and can easily be implemented to meet the Nyquist-criterion, they are a natural choice to implement the waveshaping function. A block diagram of this approach using dual baseband DACs is shown in Fig. 1.5. An alternative implementation using digital

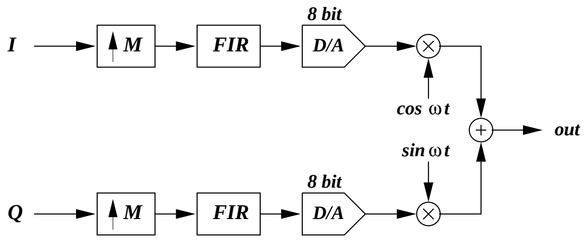

Figure 1.5 Digital QAM waveshaping with dual baseband DACs.

mixing and a single IF DAC is shown in Fig. 2.1. A disadvantage of this method is that the speed of the digital waveshaping filter is limited by the critical path of the multiplier in the FIR architecture. This slows down the overall speed of the modulator [7]. Besides, as with the look-up-table method, a DAC is required which can limit the performance of the overall system, especially for high data rates.

Digital Filter Merged with DAC In this thesis, a digital-input-analog-output PAM/QPSK transmission filter is developed. The architecture, shown in Fig. 1.6, incorporates the advantages of a digital FIR filter while using an analog multiplier which eliminates the critical path in digital circuits. The modulator produces a direct analog output so there is no need for a general-purpose DAC. This implementation is very efficient since all computations are

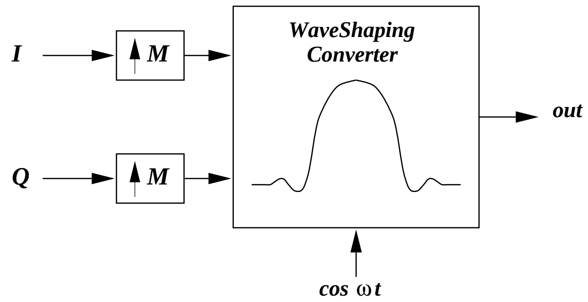

Figure 1.6 QAM waveshaping with a merged DAC and digital filter

performed in the analog current domain. The analog multiplier employs a current division technique which is very suitable for implementation in a digital CMOS process. Coefficient tap-weights are in digital form and can be easily modified. Summation is performed by connecting all current outputs to a common node. This technique results in a modulator and DAC combination that requires less silicon area and less power than other realizations.

Since the modulator developed in this thesis is based on the all digital QAM Modulator architecture [7], a detailed discussion of the all digital architecture is presented in the following chapter and design criteria of the waveshaping function will be established. Details of the design and measured results of the circuit are presented in subsequent chapters.

2

DESIGN CONSIDERATIONS FOR DIGITAL QAM FILTERS

As the modulator described in this thesis is based on digital methods, important design considerations for a digital system will be introduced in this chapter, such as the choice of coefficients for the waveshaping filter and $\sin(x)/x$ compensation. Matched filter design for optimal performance in white Gaussian noise will also be discussed. Finally, some sample modulated waveforms and their associated eye-diagrams will be presented, which aid in visualizing system operation.

2.1 ALL DIGITAL QAM MODULATOR

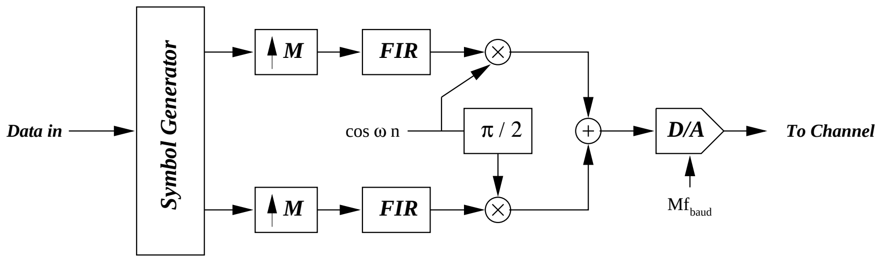

Figure 2.1 Digital QAM Modulator.

A digital QAM modulator is shown in Fig. 2.1. The basic function of the modulator is to convert a serial input bit stream into a bandlimited IF analog output waveform. The operations performed can be described briefly as follows.

First, an input binary bit-stream is formatted into in-phase and quadrature data streams. The serial input bit stream with bit-rate R is converted into a lower rate digital symbol stream with a symbol rate $1/T$, where $R = \log_2(M \times 1/T)$ for an M-QAM transmission format. The in-phase, $I(t)$, and quadrature, $Q(t)$, parts of the symbol are derived from the input bit-stream by mapping bits into two multi-level data streams. For an M-QAM system, $\log_2 M$ bits from the input bit stream are mapped into $\sqrt{M}$ discrete level I and Q data streams. Each pair of I and Q symbols represents a location in the QAM constellation plane. A 16-QAM and a QPSK constellation plane are shown in Fig. 2.2. After the formatter, the I and Q streams pass through

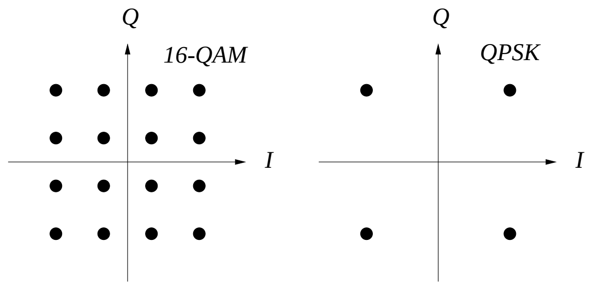

Figure 2.2 16-QAM and QPSK constellation plane.

the Nyquist lowpass filter to match the channel requirement according to the allowable bandwidth and the out-of-band emissions. The lowpass filtered I, Q streams are then mixed up to the desired IF frequency. These modulated signal waveforms are finally summed and converted to an analog signal through a DAC before being transmitted.

2.2 TRANSMISSION FILTER CHARACTERISTICS

Digital modulations produce significant out-of-band energy because of the high frequency content of square pulses. Therefore lowpass filtering is necessary to limit the bandwidth and out-of-band energy before the signal is transmitted through the channel.

The transmission filter characteristic has to be carefully chosen in order that the intersymbol interference (ISI) is minimized during transmission. It has been shown that a transmission filter impulse response can be designed to eliminate ISI. A Nyquist filter is one such candidate since its impulse response has uniformly spaced zero-crossings at every $T = 1/f_b$ seconds as shown in Fig. 2.3. However, an ideal Nyquist filter cannot be physically realized because

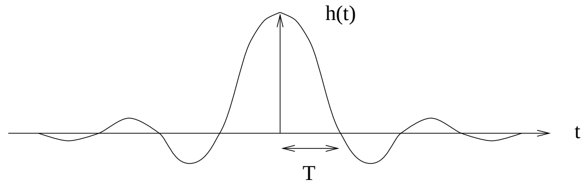

Figure 2.3 Impulse response of a Nyquist filter.

it has an infinite impulse response. In practice, a filter with a raised-cosine characteristic has been widely used. The impulse response can be described by the following expression,

$$g(t) = \frac{\sin \frac{\pi t}{T}}{\frac{\pi t}{T}} \frac{\cos \frac{\alpha \pi t}{T}}{1 - (\frac{2\alpha t}{T})^2} \tag{2.1}$$

This gives rise to a frequency response given by

$$G(\omega) = \left(\begin{array}{cc} T & 0 \leq \omega \leq \frac{\pi}{T}(1-\alpha) \\ \frac{T}{2}(1 - \sin(\frac{T}{2\alpha}(\omega - \frac{\pi}{T}))) & \frac{\pi}{T}(1-\alpha) \leq \omega \leq \frac{\pi}{T}(1+\alpha) \end{array} \right) \tag{2.2}$$

The parameter α is the excess bandwidth of the Nyquist frequency response as shown in Fig. 2.4.

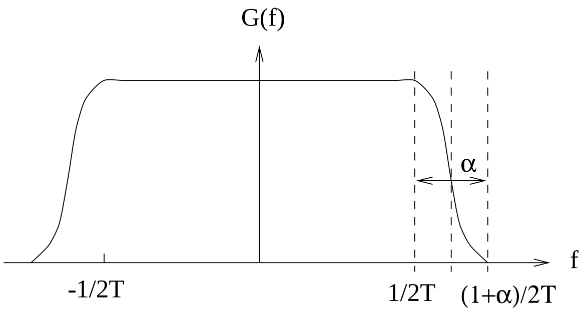

Figure 2.4 Frequency response of a raised-cosine Nyquist filter.

2.3 MATCHED FILTER

In practice, transmission filters for QAM systems are typically designed to *match* the receive filter in order to maximize the signal-to-noise ratio (SNR) of the received signal in the presence of channel noise. For the case of Additive White Gaussian Noise (AWGN), the matching criterion is,

$$H_R(\omega) = H_T^*(\omega) \tag{2.3}$$

Therefore, the lowpass filter design criteria for a QAM system splits the wave-shaping filter into two parts such that,

- The receive filter is the complex conjugate of the transmit filter.
- The cascade of the transmit and receive filters is a Nyquist filter.

2.4 SIN(X)/X COMPENSATION

Because a digital-to-analog converter is usually followed by an ideal zeroth-order hold, it introduces an inherent $\sin(x)/x$ amplitude distortion into the spectrum of the signal being converted. A typical zeroth-order hold spectrum is given by

$$H_{DAC}(f) = \frac{\sin(\pi f/f_s)}{\pi f} e^{-j\pi(f/f_s)} \tag{2.4}$$

To eliminate this effect, a predistortion compensation is usually employed by introducing some peaking into the frequency response of the lowpass filter.

2.5 FILTER DESIGN

With the above constraints, a square-root raised-cosine filter, $h_{sqr}(n)$, is chosen as the waveshape which satisfies

$$H_R(\omega) = H_{sqr}(\omega) * H^*_{sqr}(\omega) \tag{2.5}$$

The final design procedure for the transmit filter is summarized below.

1. Compute the raised-cosine coefficients of the filter, $h_r(n)$ from Eqn. 2.1 with an excess bandwidth factor α determined by system specifications.
2. Obtain the square-root raised-cosine filter coefficients, $h_{sqr}(n)$ by spectral factorization, such as the method as described on Page 57 of [8].

3. Convolve $h_{sqr}(n)$ with $h_{comp}(n)$ where $H_{comp}(\omega) = \frac{\omega/2}{\sin(\omega/2)} e^{j\omega/2}, \ |\omega| < \pi$ to predistort for the zeroth-order hold function.

4. Quantize the filter coefficients to obtain $h_t(n)$, our final transmission filter coefficients.

Filter Coefficients: The filter for this project is designed for transmission of QPSK modulation in a cable modem application with 30-dB out-of-band suppression, and $\alpha = 0.35$. The resulting filter requires 33 taps. The coefficients of the QPSK modulator have been determined in the manner prescribed above and are listed in Table 2.1.

Tap no.	Coefficient
1,33	0.001953125
2,32	0.001953125
3,31	-0.00390625
4,30	-0.0078125
5,29	-0.0078125
6,28	0
7,27	0.013671875
8,26	0.01953125
9,25	0.01171875
10,24	-0.01171875
11,23	-0.0390625
12,22	-0.046875
13,21	-0.017578125
14,20	0.0546875
15,19	0.140625
16,18	0.21875

Table 2.1 Table of transmission filter coefficients

Impulse and Frequency Response: The impulse and frequency responses of the transmit filter, T, are shown in Fig. 2.5 and Fig. 2.6 respectively.

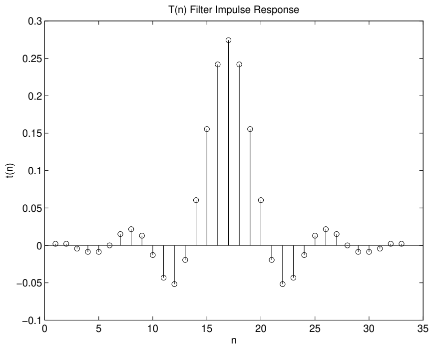

Figure 2.5 Impulse response of transmit filter, $t(t)$.

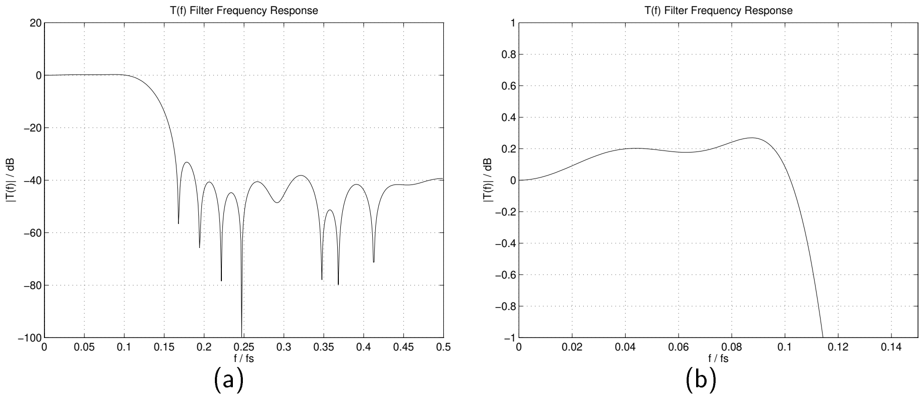

Figure 2.6 Frequency response of transmit filter $T(f)$.

The passband of Fig. 2.6(b) clearly shows the $x/\sin(x)$ predistortion peaking. After combining $T(f)$ with the zeroth-order-hold action of the DAC, $Z(f)$, the frequency response of the output becomes flattened, as shown in Fig. 2.7. After the transmitted signal passes through the receive filter, the data pulses are the raised-cosine Nyquist shapes of Fig. 2.8, which has a frequency spectrum shown in Fig. 2.9.

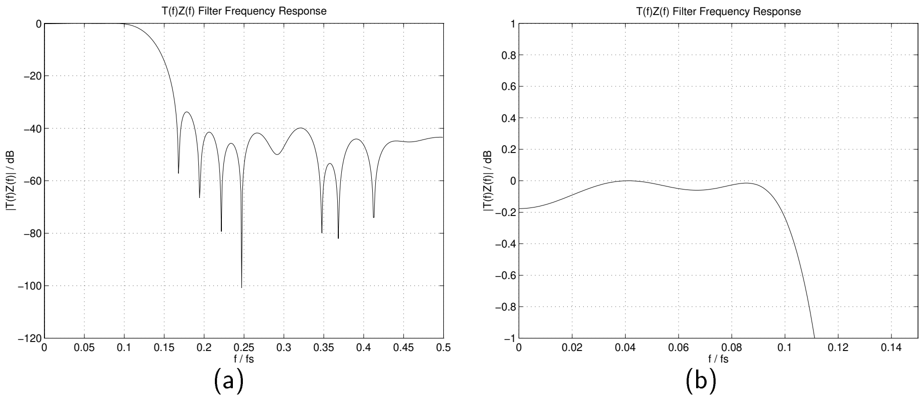

Figure 2.7 Frequency response of $T(f)Z(f)$.

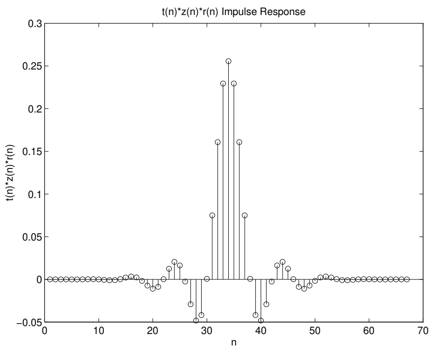

Figure 2.8 Impulse response of $T(f)Z(f)R(f)$.

2.6 SAMPLE FUNCTIONS AND EYE-DIAGRAMS

The impulse responses and frequency spectrums of previous Figs. 2.5–2.9 are adequate to describe the system. However, some key performance aspects are not easily seen from these plots. For example, when the signal is being transmitted through the channel, there is ISI which contaminates the data sample. This occurs because the transmit filter does not have precise zero-

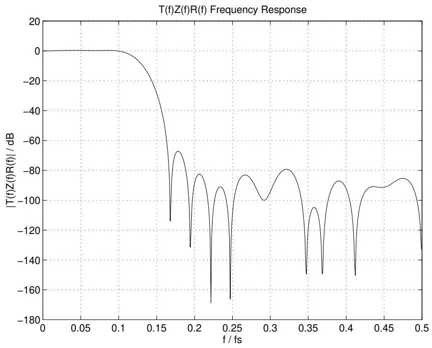

Figure 2.9 Frequency response of $T(f)Z(f)R(f)$.

crossing. Only after passing through the receive filter are the zero-crossings properly re-aligned for zero intersymbol interference.

An *eye-diagram* can be used to illustrate these points more clearly. Random data is applied to the modulator. The data is 4x-oversampled so that $f_s = 4f_b$. The raw non-return-to-zero (NRZ) square pulses are shown in Fig. 2.10(a) and the characteristic $\text{sinc}(f/f_b)$ spectrum of these pulses is plotted in Fig. 2.10(b). This frequency spectrum can be compared to the spectrums of the transmitted and received signal of Figs. 2.11(a) and (b) respectively. It can be seen that the waveshaping filter is essential for reducing the out-of-band energy.

The time domain waveform obtained after the raw data passes through the transmit filter is illustrated in Fig. 2.12(a). The eye-diagram for this data is shown in Fig. 2.13(a), where it can be clearly seen that ISI reduces the maximum eye opening.

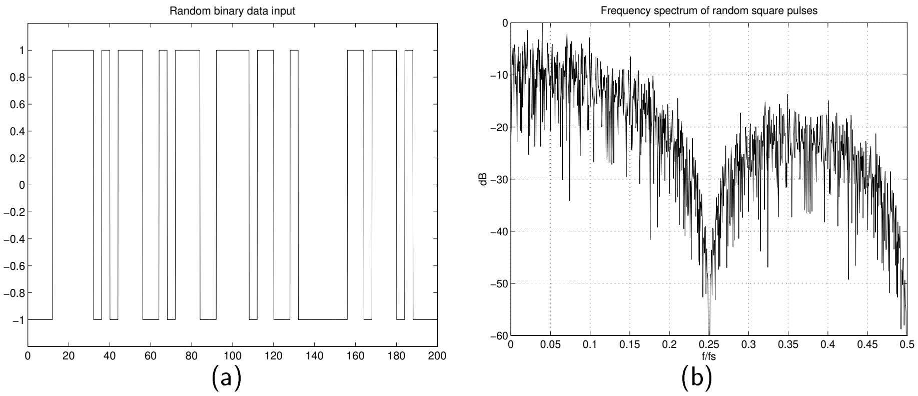

Figure 2.10 (a) Input data to be transmitted; (b) frequency spectrum of the input data.

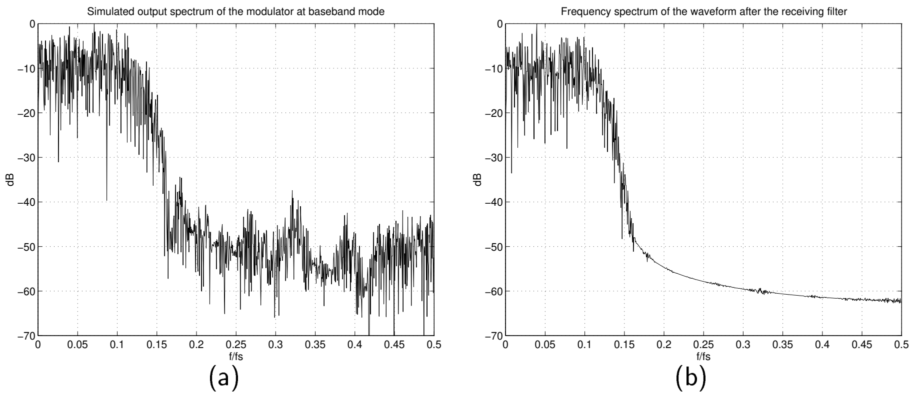

Figure 2.11 Frequency spectrum of the (a) transmitted and (b) received signal.

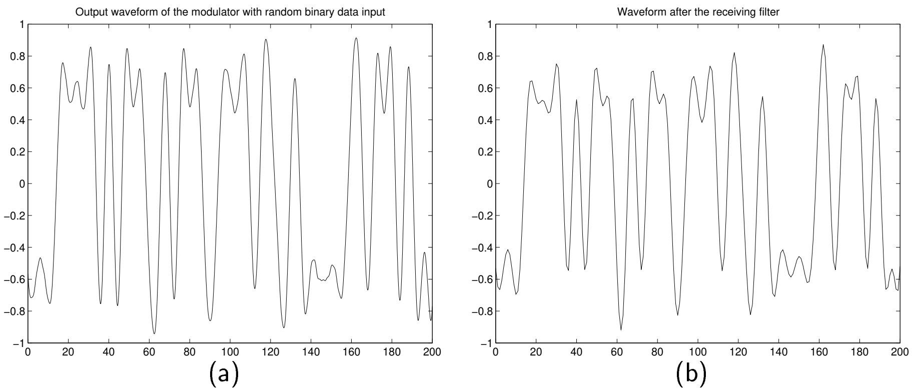

Figure 2.12 The waveform of the (a) transmitted and (b) received signal.

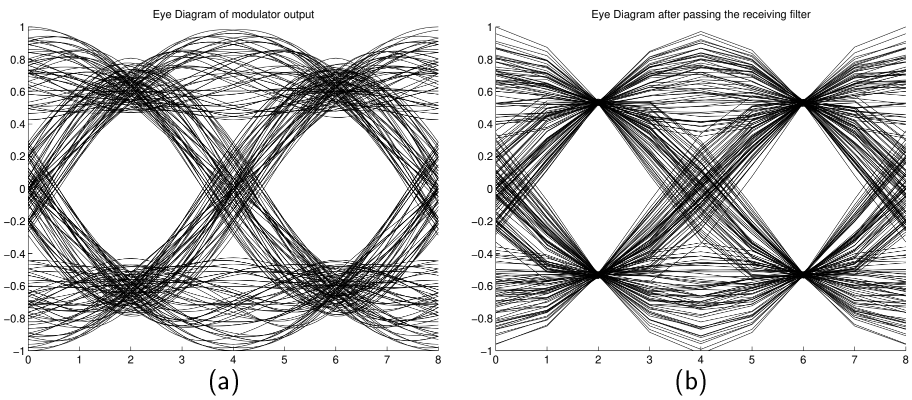

Figure 2.13 Eye diagram of the (a) transmitted and (b) received signal.

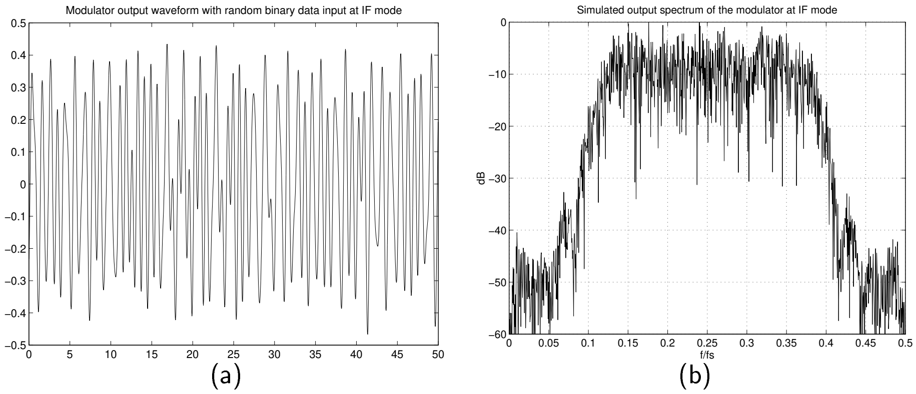

Figure 2.14 The IF QPSK modulated signal.

The data is then passed through the receive filter, where the resulting time domain waveform and eye-diagram are shown in Figs. 2.12(b) and 2.13(b) respectively. The cascade of the transmit and receive filter produces zero crossing that are aligned to the symbol-rate grid so that no ISI corruption occurs at the sample point.

Intermediate Frequency Spectrum: The baseband I and Q waveforms of Figs. 2.12 and 2.13 are eventually modulated to an intermediate frequency. The IF QPSK modulated signal is shown in Fig. 2.14. This example shows the IF center frequency is equal to the baud rate, $f_c = f_b$, which is equal to $f_s/4$ in a 4x-oversampled system.

2.7 SUMMARY

The basic elements of a QAM IF modulator have been described. A straightforward realization of these building blocks will result in a reasonably sized integrated circuit. However, a significant hardware simplification can be achieved by employing various digital techniques. For instance, the choice of a 4x-oversampled system, which centers the IF spectrum at the baud-rate, allows several architectural simplifications to be made. The next chapter will be devoted to discussing this aspect of the design.

3

ARCHITECTURAL SIMPLIFICATION

In this chapter, the architectural simplification of the QPSK modulator is addressed. The system architecture of the QPSK modulator is based on a polyphase decomposition which also involves interpolation with an IF frequency constraint. Without any simplification, the in-phase and quadrature channels in a QPSK modulator requires two 33-tap FIR filters. After simplification, there will be four sub-filters with the total number of taps equivalent to one 33-tap FIR filter.

3.1 INTERPOLATION

Interpolation is the process in which the data rate is increased by inserting a constant number of zeros between each input data. This process is illustrated in Fig. 3.1.

Depending on the application, the interpolation ratio is chosen accordingly. In our QPSK modulator, interpolation by four is chosen which will be explained in the next section. It is obvious that there will be a lot of zeros

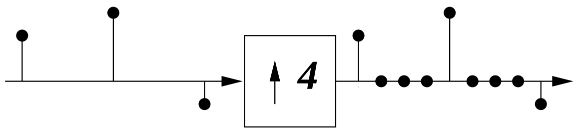

Figure 3.1 Interpolation.

in the data stream after the interpolation. The output of the 33-tap filter is only determined by the input data samples which are non-zero. Therefore, the 33-tap filter can be broken down into four sub-filters by simply multiplexing the outputs of each sub-filters sequentially.

Mathematically, it can be described as,

$$\begin{aligned}
\hat{x}(n) &= \begin{cases} x(n/4) & : (n \bmod 4) = 0 \\ 0 & : \text{otherwise} \end{cases} \\
y(n) &= \hat{x}(n) \odot h(n) \\
&= \begin{cases} x(n/4) \odot h(4n) & : (n \bmod 4) = 0 \\ x((n-1)/4) \odot h(4n+1) & : (n \bmod 4) = 1 \\ x((n-2)/4) \odot h(4n+2) & : (n \bmod 4) = 2 \\ x((n-3)/4) \odot h(4n+3) & : (n \bmod 4) = 3 \end{cases}
\end{aligned} \tag{3.1}$$

where $\odot$ represents discrete domain convolution.

Power dissipation is lower because each sub-filter is clocked at one-fourth of the output frequency. Also, the length of the filters is shortened which simplifies the clock distribution.

3.2 CONSTRAINING THE IF CENTER FREQUENCY

The IF center frequency can be chosen in such a way that the hardware implementation can be further simplified. If we choose the IF center frequency to be four times the baseband signal frequency, the mixing cosine and sine functions $\cos\omega_c n$, $\sin\omega_c n$ become $\cos\pi n/2$, $\sin\pi n/2$ which are periodic sequences $\{1, 0, -1, 0\}$ and $\{0, 1, 0, -1\}$ respectively. This leads to the architecture as shown in Fig. 3.2.

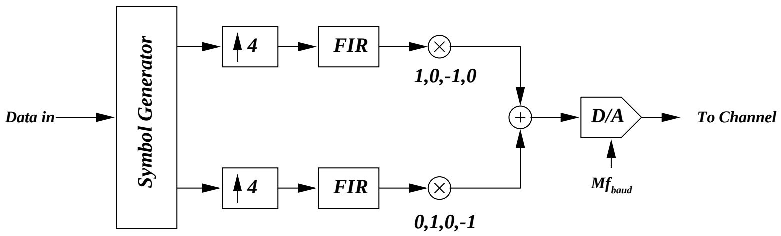

Figure 3.2 Baseline QPSK modulator.

First, the system up-samples the input bit stream by four. Then, the data goes through a square-root raised-cosine FIR filter. After that, the in-phase (I) and quadrature-phase (Q) data streams are multiplied by the $\{1, 0, -1, 0\}$ and $\{0, 1, 0, -1\}$ sequences respectively. Because the output depends only on non-zero elements of the sequences, the polyphase architecture can be further simplified as shown in Fig. 3.3.

There is no reason to calculate baseband signal values that will be later set to zero by the IF mixer. If this information is utilized initially, half the samples of both the I and Q channels can be ignored. The architecture involves four sub-filters. Suppose the original filter response is h_n with order N. The complete modulator can be implemented as shown in Fig. 3.3, where

$$y(n) = \begin{cases} h_{4k} \odot I(k) & \text{if } (n \bmod 4) = 0 \\ h_{4k+1} \odot Q(k) & \text{if } (n \bmod 4) = 1 \\ -h_{4k+2} \odot I(k) & \text{if } (n \bmod 4) = 2 \\ -h_{4k+3} \odot Q(k) & \text{if } (n \bmod 4) = 3 \end{cases} \text{, where } k = (n \text{ div } 4). \quad (3.2)$$

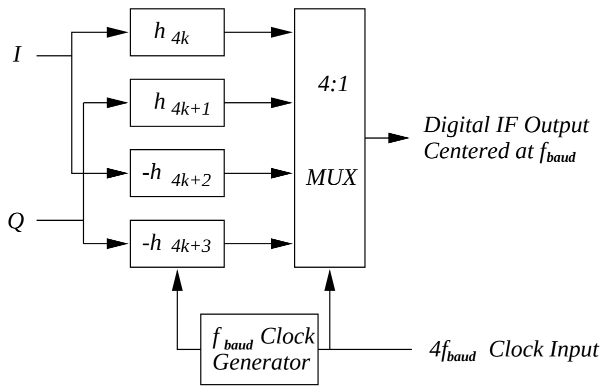

Figure 3.3 Polyphase decomposition of QPSK modulator.

With some manipulation this expression can be shown to equal,

$$y(n) = (h_n \odot \hat{I}(n)) * \cos \pi n/2 + (h_n \odot \hat{Q}(n)) * \sin \pi n/2 \tag{3.3}$$

which is the desired function, where $\hat{I}(n)$, $\hat{Q}(n)$ are up-sampled by 4 versions of $I(n)$ and $Q(n)$ respectively. Eqn. 3.3 shows that the system in Fig. 3.3 is equivalent to the one in Fig. 3.2.

3.3 SUMMARY

A straightforward realization of a QAM modulator would require two independent 33-tap filters, a mixer and a general-purpose DAC. Using interpolation by four and centering the IF spectrum at the baud-rate, $f_b = f_s/4$, several simplifications in the digital FIR/mixer combination can be made. This results in a structure consisting of four sub-filters, which have a total tap length of 33, cascaded with a 4:1 mux. In addition this structure can be implemented as a combined digital/analog circuit, which generates a direct analog IF output, eliminating the need for the DAC.

Now that the QAM system aspects and modulator architecture have been described, the remainder of the thesis will concentrate on the circuit-level implementation, physical realization and test results.

I seem to have been only like a boy playing on the seashore, and diverting myself in now and then finding a smoother pebble or a prettier shell than ordinary, whilst the great ocean of truth lay all undiscovered before me.

— Sir Iassc Newton

4

CIRCUIT DESIGN

In this chapter, circuit design aspects of the project will be discussed. Since a key element of the QPSK modulator is the waveshaping filter, a detailed discussion of how the current-division technique [9] can be used to implement a digital FIR filter architecture will be presented. First, the current division technique is reviewed briefly. Next, a multiplication circuit using the current-division technique with a digital input and an analog output will be described. Finally, we show how the above techniques are used to implement a waveshaping converter.

4.1 CURRENT DIVISION TECHNIQUE

It can be shown that current can be divided in an inherently linear manner by using a current division technique in CMOS technology [9]. This technique can be illustrated with the aid of Fig. 4.1. A common voltage is applied to the gates of the two MOS transistors (with respect to the substrate). V_a and V_b are two fixed dc voltages which can have any value as long as the

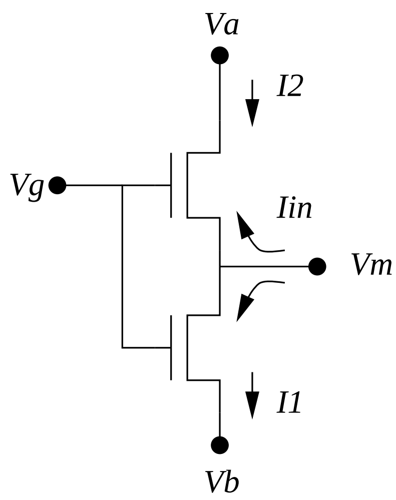

Figure 4.1 The basic principle of current division.

transistors are in the on-state (saturation or weak-inversion). I_{in} is the current flowing into, or out of, the circuit, which will be divided into two parts. One part of the current flows into the node connected to V_a and the other part flows into the node connected to V_b. It can be shown that the fraction of this input current flowing to one side is:

- constant and independent of I_{in} (implying low distortion),
- independent of the values of V_a and V_b,
- independent of whether one or both devices are saturated or nonsaturated,
- and also independent of whether one or both devices operate in strong or weak inversion.

In [9], the ratio of the two currents is shown to be equal to the ratio of the two aspect-ratios W/L of the transistors. These conditions make the current division technique independent of other process variations besides mismatches of the W/L ratios of transistors. Mismatches in threshold voltages V_t are insignificant if the effective gate voltage V_{gt} is large enough ($\sim$ 2V).

4.2 ARCHITECTURE FOR MULTIPLICATION

Multiplication of an analog signal with a digital coefficient can be performed by the circuit shown in Fig. 4.2, which acts like a multiplying DAC. The

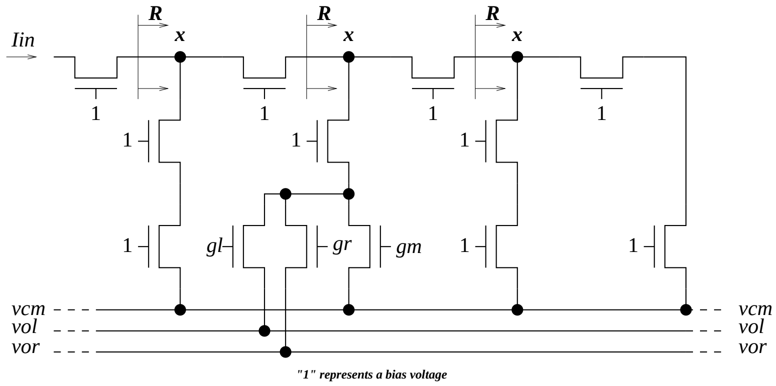

Figure 4.2 Multiplier based on CDT.

architecture is based on an R-2R ladder structure with the resistors replaced by MOS transistors. Suppose the resistance of an MOS transistor is R. The equivalent resistance at nodes marked with an "X" towards the right side of the circuit is always R. According to the current division principle, the current will be divided equally when it passes nodes marked with an "X". This produces a set of binary weighted currents. By summing the currents of desired branches, we get a multiplication effect. Mathematically, the current-division multiplier can be described as,

$$\begin{aligned} I(Vol, Vor) &= b_{N-1} \cdot \frac{I_{in}}{2} + b_{N-2} \cdot \frac{I_{in}}{2^2} + \ldots + b_0 \cdot \frac{I_i n}{2^{N-1}} \\ &= \left(\frac{b_{N-1}}{2} + \frac{b_{N-2}}{2^2} + \frac{b_0}{2^{N-1}}\right) \cdot I_{in} \\ &= C \cdot I_{in} \end{aligned} \tag{4.1}$$

where the C is the multiplier coefficient.

With this circuit, any power of two multiplier can be obtained. Negative coefficients can be implemented by swapping the connection of Vol and Vor.

4.3 DIGITAL-TO-ANALOG CURRENT-DIVISION WAVESHAPING CONVERTER

Basically, a digital-to-analog current-division waveshaping converter is a device which converts digital signals to analog signals with a waveshaping action. It can be accomplished by implementing the digital FIR filter architecture presented earlier, while using the multiplier described in the previous section. A BPSK waveshaper, based on this approach is shown in Fig. 4.3. The input I/Q digital bit streams run into a delay chain. Control signals switch the current-division multipliers either on or off. The coefficient of each 33-tap multiplier is the FIR filter coefficient. The reference current of each multipliers is fixed because the modulator is designed for a BPSK signal which requires only two output levels; therefore binary switching is adequate for level generation. If a multi-level QAM signal is desired, the circuit can be modified by multiplying the reference current by the appropriate level. The current outputs of

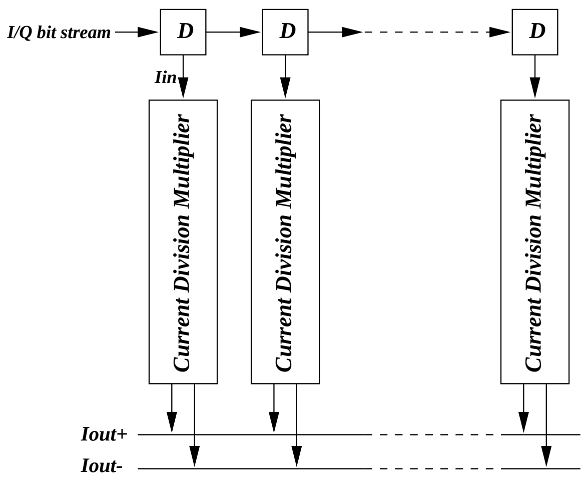

Figure 4.3 Digital-to-analog current-division waveshaping converter.

each multiplier are summed differentially at I_{out+} and I_{out-} to produce the filtered waveform. Since the coefficients of the multipliers comprise a square-root raised-cosine impulse response, the output of this architecture is equivalent to an FIR filter cascaded with a DAC.

Combining the current-division multipliers with the polyphase decomposition architecture discussed in Chapter 3, a QPSK modulator can be built using this Current-Division Waveshaping Converter (CDWC), as shown in Fig. 4.4. The complete modulator is built with four sub-filters, while constraining the IF center frequency to be four times the Nyquist rate of the baseband signal. The four phase clock generator is used to multiplex the output of the sub-filters by switching on each sub-filters one at a time. The timing diagram of the control signals is shown in Fig. 4.5. In the next chapter the physical layout of the circuit will be discussed.

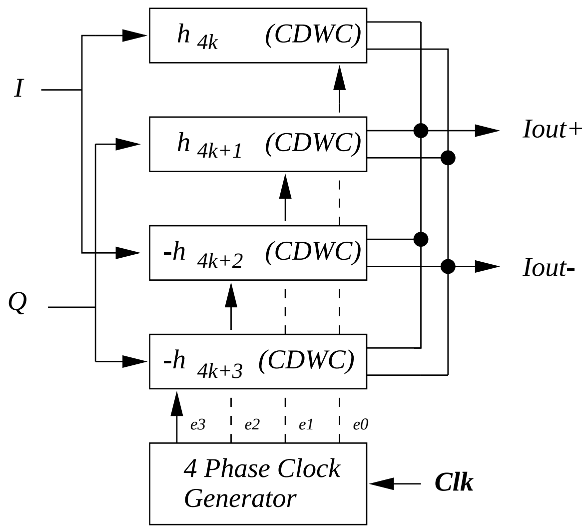

Figure 4.4 Polyphase implementation of a QPSK modulator, using the digital-to-analog current-division waveshaping converter.

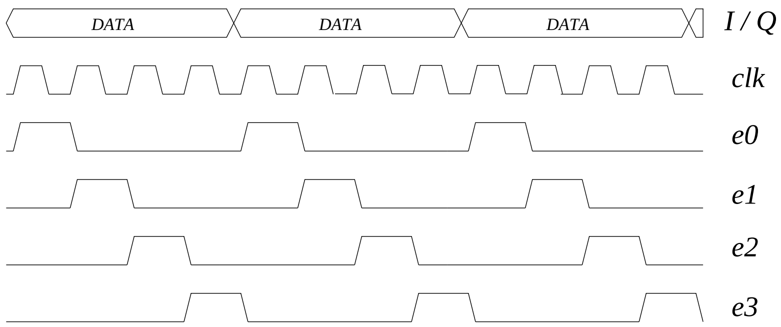

Figure 4.5 Timing diagram of different clock signals.

5

VLSI IMPLEMENTATION

5.1 FLOOR PLAN

The layout floor plan of the PAM/QPSK modulator is shown in Fig. 5.1. Because of the polyphase decomposition, the layout is sub-divided into four

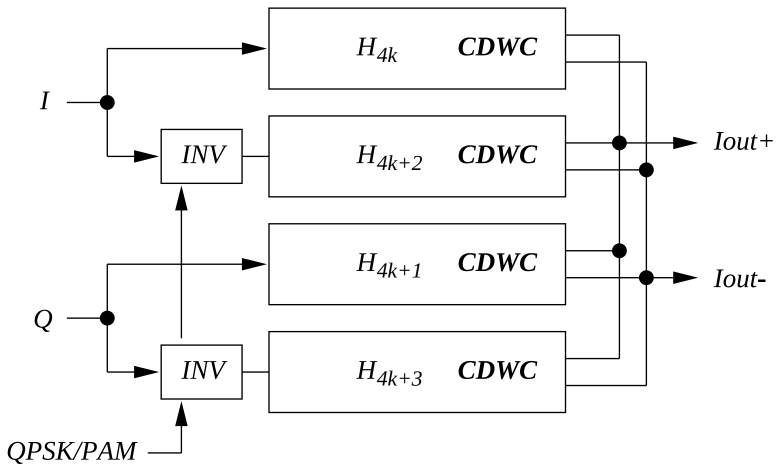

Figure 5.1 Layout floor plan of the PAM/QPSK modulator

sub-filter blocks. The in-phase and quadrature phase sub-filters are grouped separately. The inverter (INV) is used to select the mode of operations, either

PAM or QPSK because their difference relies only on the sign of the sub-filter coefficients h_{4k+2} and h_{4k+3}. Since I and Q are binary bit streams, we can simply invert the bit to get the effect of switching the sign of the coefficients of the impulse response.

5.2 LAYOUT COMPILER

The entire layout was designed using the *Mentor Graphics GDT* layout editor. The goal of the layout design is to make the filter coefficient programmable during layout compilation. Therefore, a generator approach based on *Mentor Graphics GDT* is employed. The methodology of the layout compiler for this project can be illustrated in Fig. 5.2. The main portion of the

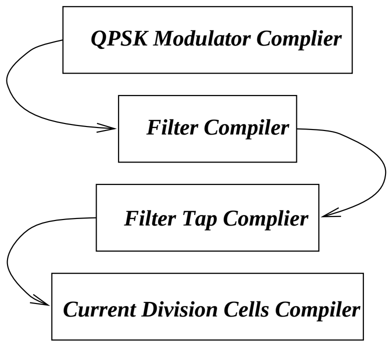

Figure 5.2 Layout hierarchy of the QPSK modulator.

layout generator is the Current-Division Waveshaping Converter (CDWC) compiler. It accepts different power of two coefficients as inputs, and generates the sub-filter cells accordingly.

An example of the input files of the compiler is given below.

```
# Filter order
order 9
# Filter maximum bit accuracy
bit 9
# tap : tap | no. | coef | no. | physical value
tap 0  1   2 (2 0) (1 1)
tap 4  -4  2 (4 1) (3 0)
tap 8  6   2 (4 0) (2 1)
tap 12 -9  4 (4 1) (3 1) (2 0) (1 0)
tap 16 127 2 (8 0) (1 1)
tap 20 -9  4 (4 1) (3 1) (2 0) (1 0)
tap 24 6   2 (4 0) (2 1)
tap 28 -4  2 (4 1) (3 0)
tap 32 1   2 (2 0) (1 1)
```

Using the *Mentor Graphics GDT* layout editor, the compiler is designed to be technology independent which means a new layout can be quickly recompiled and automatically generated given process parameters and a *technology file*.

5.3 ACTUAL LAYOUT

The layout of the QPSK modulator occupies 1mm$\times$1.213mm and is shown in Fig. 5.3. Each of the four sub-filters can be recognized as one of the four rows in the structure. The clock generator is shown in the left-most column and the bias current mirrors occupy the lower right corner.

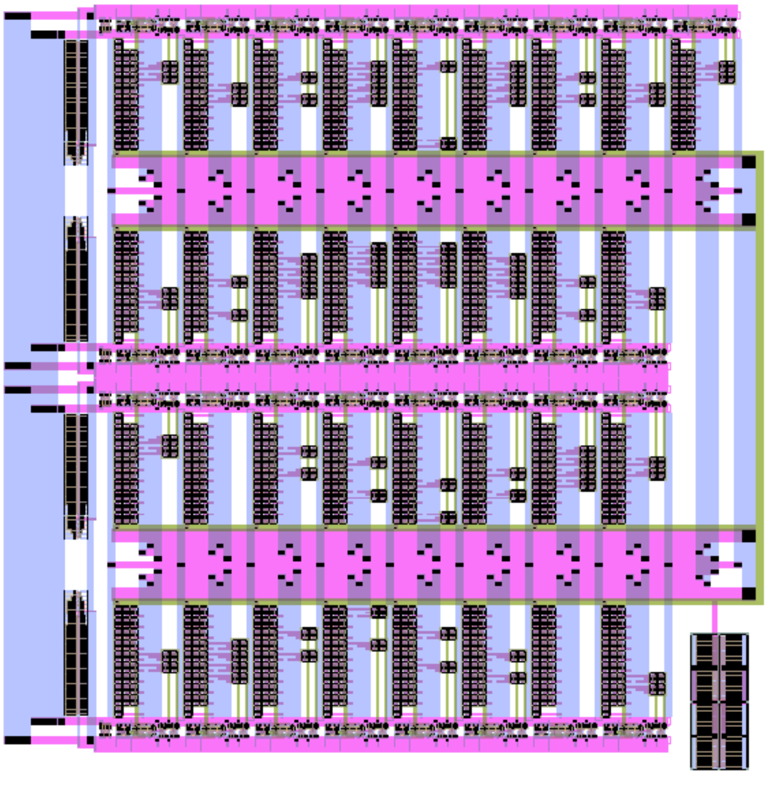

Figure 5.3 Layout of the QPSK modulator.

6

SIMULATION AND TEST RESULTS

6.1 SIMULATION RESULTS

The layout of the PAM/QPSK modulator was extracted and simulated using *Hspice*. A BSIM level-28 model for a 0.8μm MOSIS HPCMOS26G process was used in simulation. By applying a single pulse input to the circuit, the impulse response of the Nyquist filter of the modulator can be observed. The simulated impulse responses are shown in Fig. 6.1, where out_0 is the modulated output, and out_1 is the lowpass version obtained by filtering out_0 with a 5-th order butterworth filter with the cut-off frequency of 20-Mhz. The input impulse sequence is $\{\cdots -1, -1, -1, 1, -1, -1, -1\cdots\}$, where no zero is applied because of the simplified architecture of the modulator. In this simulation, the sampling frequency is 40-Mhz.

In order to look at the output spectrum of the modulator, a random input bit stream is applied. To shorten the simulation time, this analysis is performed in *Matlab*. The output spectrum is shown in Fig. 6.2; spectrums at

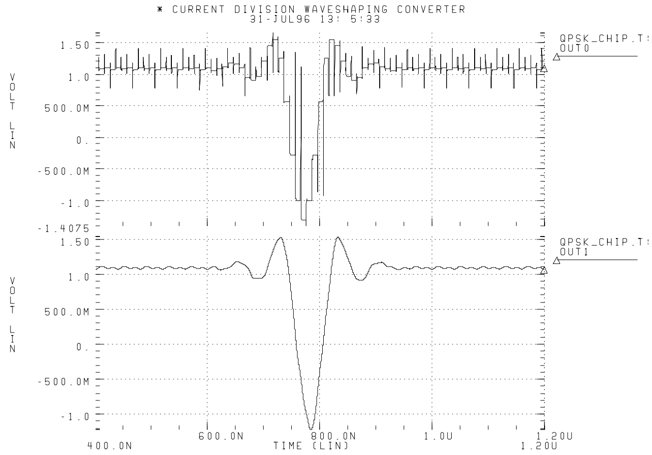

Figure 6.1 Simulated impulse responses of the modulator.

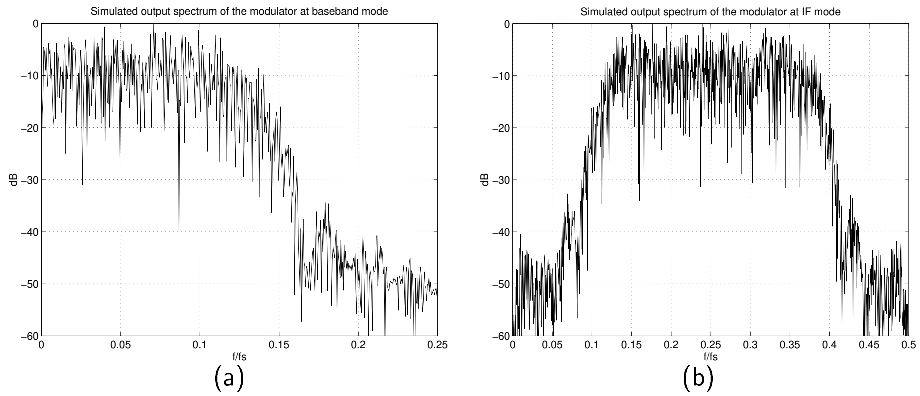

Figure 6.2 Simulated output spectrum of the modulator at (a) baseband (b) IF

baseband and IF are shown. The out-of-band ripples are at least 30-dB down from the passband, which matches the specification of the intended application.

6.2 TEST RESULTS

The modulator has been fabricated in a 0.8μm MOSIS HPCMOS26G process. The chip occupies an area of 1.45mm^2, (1.2mm$\times$1.21mm). The die photo is shown in Fig. 6.3.

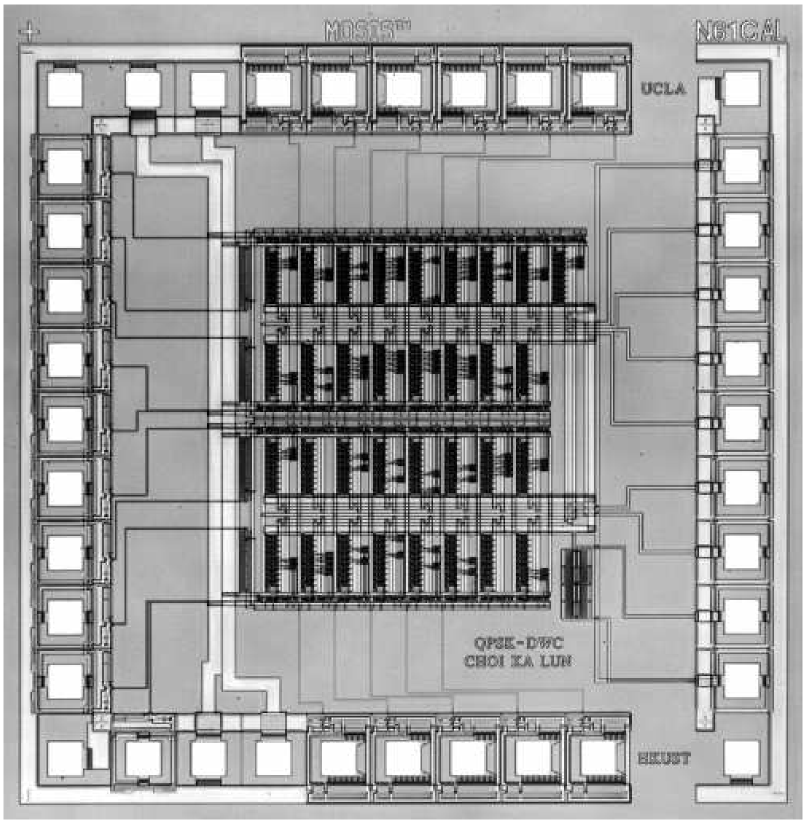

Figure 6.3 Die photo of the PAM/QPSK modulator.

Impulse Response: First, the circuit is tested by applying a periodic impulse to both the I and Q channels. The measured output impulse response taken from a sampling oscilloscope is shown in Fig. 6.4. The measured response matches the simulated response of Fig. 6.1. Eye-diagrams of either the

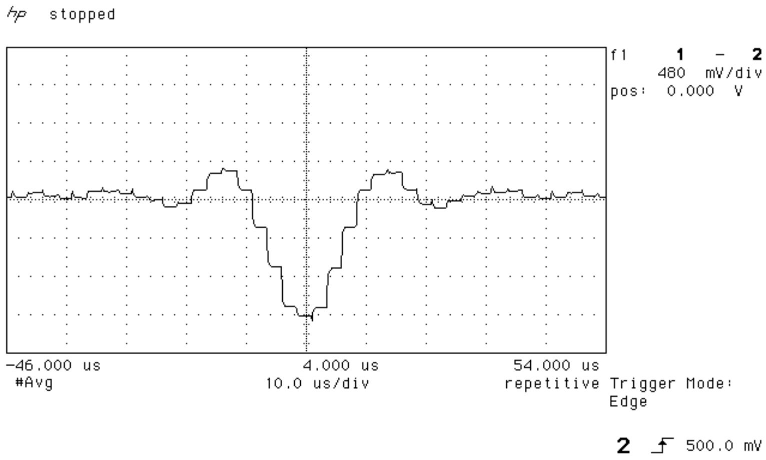

Figure 6.4 Measured impulse response of the modulator.

I or Q channel are shown in Fig. 6.5 for f_s=2-Mhz. This plot is typical of a square-root-cosine waveshaping filter and can be compared to the ideal case of Fig. 2.13. The eye-diagram for f_s=40-Mhz is shown in Fig. 6.6. This plot shows some distortion of the eye opening. However, this is due to ringing in the off-chip buffer amplifier, which can be corrected by designing a new test board.

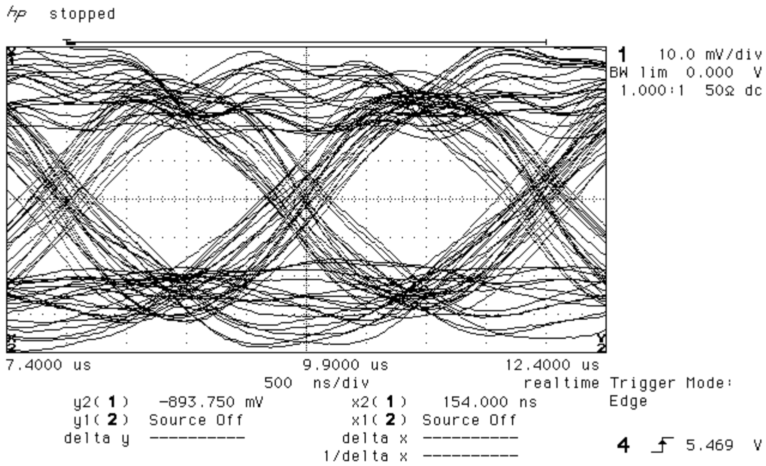

Figure 6.5 Measured eye-diagram of the I or Q channel at f_s=2-Mhz.

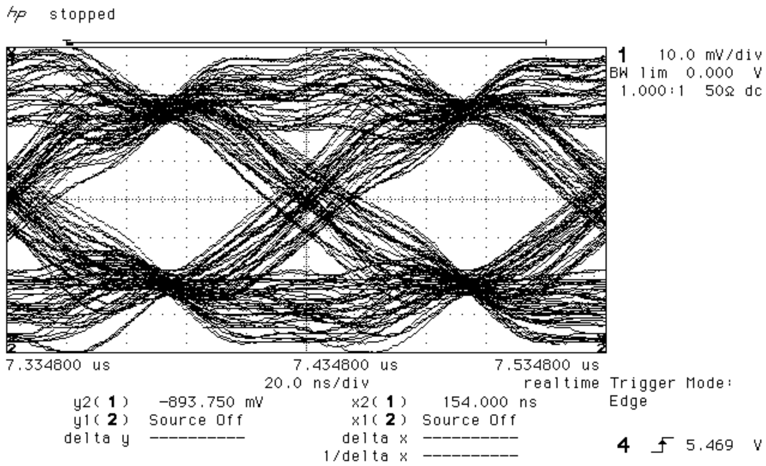

Figure 6.6 Measured eye-diagram of the I or Q channel at f_s=40-Mhz.

Frequency Response at Baseband: The circuit has also been tested by applying a pseudo random binary sequence to the I and Q channels. The measured output spectrums of either the I or Q channel of the modulator are shown in Fig. 6.7 for f_s=2-Mhz and Fig. 6.8 for f_s=40-Mhz.

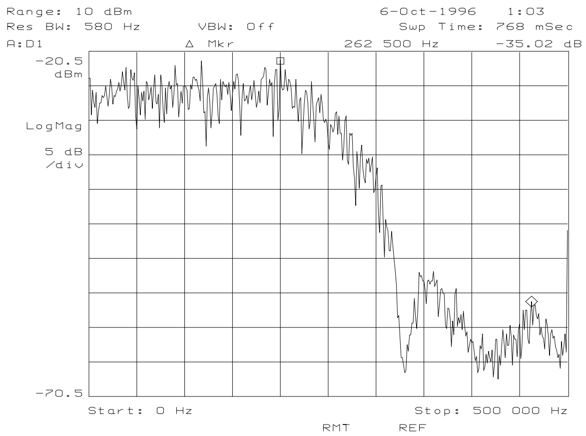

Figure 6.7 Measured output spectrum of the I or Q channel at f_s=2-Mhz.

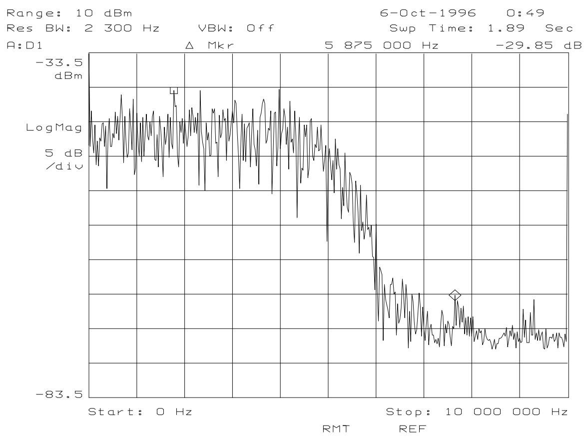

Figure 6.8 Measured output spectrum of the I or Q channel at f_s=40-Mhz.

Frequency Response at IF: In the same manner, the measured output spectrums of the QPSK modulator in IF mode are shown in Fig. 6.9 and Fig. 6.10. The IF carrier frequency is centered at one quarter of the output sampling rate.

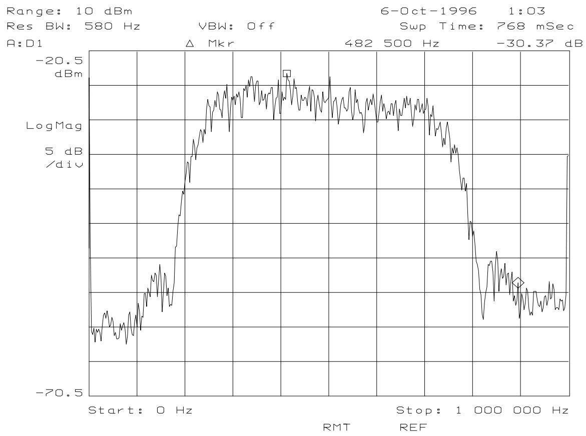

Figure 6.9 Measured output spectrum of the modulator at fs=2Mhz.

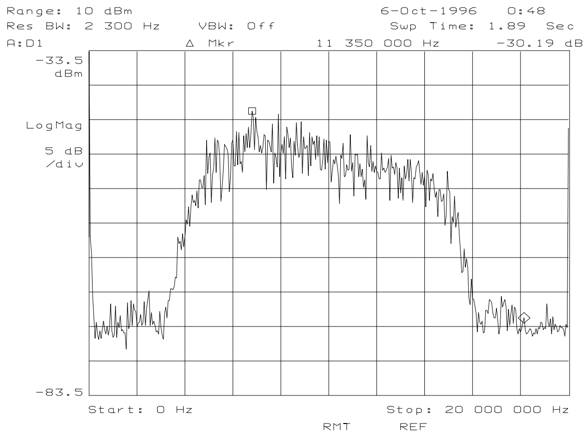

Figure 6.10 Measured output spectrum of the modulator at fs=40Mhz.

6.3 PROBLEMS AND FUTURE RESEARCH

The speed of the present modulator design is mainly limited by the external feedback amplifier which provides a low impedance current summing junction for the multiplier. Also, depending on the application, an output power amplifier is necessary for driving low impedance lines (50Ω). That means a higher output current is necessary for such applications. However, in the present design, the multiplication function is done by a current-division technique which dumps a high percentage of current to the dump line when the value of coefficient is small. This makes much of the bias current is unusable. For higher output power applications, it becomes impractical, unless a separate power amplifier is also integrated.

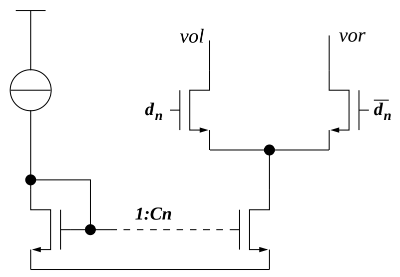

Figure 6.11 Alternative multiplier for QPSK modulator.

For future research, several suggestions are given as follows.

- Design a high bandwidth on-chip amplifier as the low impedance current summing junction. This will allow higher speed operation.

- Find an alternative FIR implementation. One suggestion is to use a differential pair with binary weighted tail current sources as an analog multiplier as shown in Fig. 6.11. In this architecture, no low impedance summing junction is required. $I(vol, vor) = C_n \cdot Iref \cdot d_n$, where C_n is the coefficients of h_n and a higher output power can be achieved because all the current is being transfered to the output.

6.4 CONCLUSIONS

A low-power, high-speed QPSK modulator has been developed using a novel current-division square-root raised-cosine waveshaping converter. The modulator can be used to generate either a single PAM in-phase or quadrature baseband signal, or it can generate a QPSK signal at an IF center frequency equal to the baud-rate. Merging of the FIR filter coefficients into the DAC makes the combined FIR/DAC function very efficient.

A prototype chip was developed in a 0.8μm CMOS process, occupies an area of 1.45mm^2 (1.2mm$\times$1.21mm), and dissipates 20-mW at 10-Mbaud. Also, a layout compiler has been written for the QPSK modulator. The compiler can automatically synthesize a layout with different filter coefficients and for different CMOS technologies. This modulator will find application in broadband communication systems where a high-degree of integration is desired with a minimal power budget, such as battery-powered wireless telephony, and wireless modems. The small chip area also makes the circuit atractive for commerical applications were cost is critical, such as modems for cable TV and, fast computer networking, and digital subscriber line systems.

There are many paths to the top of the mountain,
but the view is always the same.

— Chinese Proverb

A

MATLAB PROGRAMS

A.1 MATLAB SIMULATION PROGRAMS

A.1.1 qpsk_chip.m

```
function u = qpsk_chip(I,I_mode,Q,Q_mode,OR)

h = [
 0.001953125
 0.001953125
-0.00390625
-0.0078125
-0.0078125
 0
 0.013671875
 0.01953125
 0.01171875
-0.01171875
-0.0390625
-0.046875
-0.017578125
 0.0546875
 0.140625
 0.21875
 0.248046875
 0.21875
 0.140625
 0.0546875
-0.017578125
-0.046875
-0.0390625
-0.01171875
 0.01171875
 0.01953125
 0.013671875
 0
-0.0078125
-0.0078125
-0.00390625
```

```
 0.001953125
 0.001953125
];

O = 33;

h0 = h(1:4:O);
h1 = h(2:4:O);
h2 = h(3:4:O);
h3 = h(4:4:O);

L = size(I,2);

p0 = [];
p1 = [];
p2 = [];
p3 = [];

r0 = zeros(1,9);
I0 = I;
if I_mode == 1,
   r2 = ones(1,8);
   I1 = -I;
else
   r2 = zeros(1,8);
   I1 = I;
end
r1 = zeros(1,8);
Q0 = Q;
if Q_mode == 1,
   r3 = ones(1,8);
   Q1 = -Q;
else
   r3 = zeros(1,8);
   Q1 = Q;
end

for i=1:L,
   r0 = [I0(i) r0(1:8)];
   r1 = [Q0(i) r1(1:7)];
   r2 = [I1(i) r2(1:7)];
   r3 = [Q1(i) r3(1:7)];

   d0 = sum(h0'.*r0);
   d1 = sum(h1'.*r1);
   d2 = sum(h2'.*r2);
   d3 = sum(h3'.*r3);

   p0 = [p0 d0];
   p1 = [p1 d1];
   p2 = [p2 d2];
   p3 = [p3 d3];
end;

p0 = p0(9:L);
p1 = p1(9:L);
p2 = p2(9:L);
```

```
p3 = p3(9:L);

L = L-8;
y = zeros(1,L*4);
y(1:4:L*4-1) = p0;
y(2:4:L*4-1) = p1;
y(3:4:L*4-1) = p2;
y(4:4:L*4) = p3;

N = size(y,2);
u = zeros(1,N*OR);
for i=1:OR,
   u(i:OR:(N-1)*OR+i) = y;
end

end
```

A.1.2 run_random.m

```
N = 512;

I = 2*((rand(1,N)>0.5) - 0.5);
I_mode = 0;
Q = I;
Q_mode = 0;

u = qpsk_chip(I,I_mode,Q,Q_mode,1);

figure(1);
freq(u,1,1,0.25,1,1);
axis([0 0.25 -60 0]);
title('Simulated output spectrum of the modulator at baseband mode');
print -deps graph/spectrum_basep.eps;

OR = 8;
y = resample(u,OR,1);

figure(2);
x = (0:8*OR)/OR;
y = y./max(y);
eye_diagram(x,y,2*OR+1,8*OR);
axis([0 8 -1 1]);
title('Eye Diagram of modulator output');
print -deps graph/eye_transmit.eps;

figure(3);
f=(1:1600)/1600*4;
l=sinc(f);
plot(f,20*log10(l));
grid on;
xlabel('f/fb');
axis([0 4 -60 0]);
title('Frequency spectrum of square pulses');
```

```
print -deps graph/square.eps;

figure(4);
k = zeros(1,1600);
for i = 1:32,
   k(i:32:1600) = I(14:63);
end
x = (1:1600)/(OR);
k = k./max(k);
plot(x,k);
title('Random binary data input');
axis([0 200 -1.2 1.2]);
print -deps graph/random_input.eps;

figure(5);
k = zeros(1,N*32);
for i = 1:32,
   k(i:32:N*32) = I;
end
freq(k,0,1,0.5,OR,1);
axis([0 0.5 -60 0]);
title('Frequency spectrum of random square pulses');
print -deps graph/random_spectrum.eps;

figure(6);
x = (0:1600)/(OR);
y = y./max(y);
plot(x,y(256:1856));
axis([0 200 -1 1]);
title('Output waveform of the modulator with random binary data input');
print -deps graph/transmit_wf.eps;

figure(7);
freq(u,1,1,0.5,1,1);
axis([0 0.5 -70 0]);
title('Simulated output spectrum of the modulator at baseband mode');
print -deps graph/transmit_spectrum.eps;

figure(8);
v = rec_filter(u);
x = (0:8);
v = v./max(v);
eye_diagram(x,v,3,8);
axis([0 8 -1 1]);
title('Eye Diagram after passing the receiving filter');
print -deps graph/eye_receive.eps;

figure(9);
x = (0:200);
v = v./max(v);
plot(x,v(1:201));
axis([0 200 -1 1]);
title('Waveform after the receiving filter');
print -deps graph/receive_wf.eps;
```

```
figure(10);
freq(v,1,1,0.5,1,1);
axis([0 0.5 -70 0]);
title('Frequency spectrum of the waveform after the receiving filter');
print -deps graph/receive_spectrum.eps;
```

A.1.3 run_iq.m

```
N = 512;

I = 2*((rand(1,N)>0.5) - 0.5);
I_mode = 1;
Q = 2*((rand(1,N)>0.5) - 0.5);
Q_mode = 1;

OR = 1;
u = qpsk_chip(I,I_mode,Q,Q_mode,OR);

figure(1);
freq(u,1,1,0.5,1,1);
axis([0 0.5 -60 0]);
title('Simulated output spectrum of the modulator at IF mode');
print -deps graph/spectrum_iqp.eps;

OR = 8;
y = resample(u,OR,1);

figure(2);
x = (0:1599)/(OR*4);
plot(x,y(1:1600));
title('Modulator output waveform with random binary data input at IF mode');
print -deps graph/transmit_wfiq.eps;
```

A.1.4 verify.m

```
h = [
 0.001953125
 0.001953125
-0.00390625
-0.0078125
-0.0078125
 0
 0.013671875
 0.01953125
 0.01171875
-0.01171875
-0.0390625
-0.046875
-0.017578125
 0.0546875
 0.140625
 0.21875
```

```
 0.248046875
 0.21875
 0.140625
 0.0546875
-0.017578125
-0.046875
-0.0390625
-0.01171875
 0.01171875
 0.01953125
 0.013671875
 0
-0.0078125
-0.0078125
-0.00390625
 0.001953125
 0.001953125
];

n = -16:16;

N = size(h,1);

h = h/sum(h);
[H,w] = freqz(h);
Y = H.*sinc(w/2/pi).*exp(-j*w/2);
Y = Y./max(abs(Y));
y = invfreqz(Y,w,33,0);
ht = conv(y,y);

y = y/sum(y);
ht = ht/sum(ht);

figure(1);
stem(h);
title('T(n) Filter Impulse Response');
ylabel('t(n)');
xlabel('n');
print -deps graph/impulse_tt.eps;

figure(2);
plot(w/pi/2,20*log10(abs(H)));
grid on;
title('T(f) Filter Frequency Response');
ylabel('|T(f)| / dB');
xlabel('f / fs');
print -deps graph/impulse_tf.eps;

figure(3);
plot(w/pi/2,20*log10(abs(H)));
grid on;
title('T(f) Filter Frequency Response');
ylabel('|T(f)| / dB');
xlabel('f / fs');
axis([0 0.15 -1 1]);
print -deps graph/impulse_tom.eps;
```

```
figure(4);
plot(w/pi/2,20*log10(abs(Y)));
grid on;
title('T(f)Z(f) Filter Frequency Response');
ylabel('|T(f)Z(f)| / dB');
xlabel('f / fs');
print -deps graph/impulse_tzf.eps;

figure(5);
plot(w/pi/2,20*log10(abs(Y)));
grid on;
title('T(f)Z(f) Filter Frequency Response');
ylabel('|T(f)Z(f)| / dB');
xlabel('f / fs');
axis([0 0.15 -1 1]);
print -deps graph/impulse_tzom.eps;

figure(6);
[H,w]=freqz(ht);
stem(ht);
title('t(n)*z(n)*r(n) Impulse Response');
ylabel('t(n)*z(n)*r(n)');
xlabel('n');
print -deps graph/impulse_tzrt.eps;

figure(7);
plot(w/pi/2,20*log10(abs(H)));
grid on;
title('T(f)Z(f)R(f) Frequency Response');
ylabel('|T(f)Z(f)R(f)| / dB');
xlabel('f / fs');
print -deps graph/impulse_tzrf.eps;
```

REFERENCES

[1] Loke Kun Tan. *High Performance Architectures and Circuits for QAM Transceivers.* PhD. Dissertation, UCLA, Los Angeles, 1995.

[2] David K. Su and Bruce A. Wooley. A CMOS oversampling D/A converter with a current-mode semidigital reconstruction filter. *IEEE J. Solid-State Circuits*, 28(12):1224–1233, December 1993.

[3] Leon W. Couch II. *Digital and analog communication systems.* Macmillan Publishing Company, New York, fourth edition, 1993.

[4] Henry Samueli, Leo Montreuil, and Woo H. Paik. QAM modem technology for digital cable TV. *CED*, December 1994.

[5] Aaron Buchwald and Kenneth W. Martin. *Integrated fiber-optic receivers.* Kluwer Academic Publishers, Boston/London/Dordrecht, 1995.

[6] Y. Nakamura, Y. Saito, and S. Aikawa. 256-QAM modem for multicarrier 400-Mbit/s digital radio. *IEEE J. Select Areas Commun.*, SAC-5:329–335, April 1987.

[7] Bennett C. Wong and Henry Samueli. A 200-MHz all-digital QAM modulator and demodulator in 1.2-μ m CMOS for digital radio applications. *IEEE J. Solid-State Circuits*, 26(12):1970–1980, December 1991.

[8] P.P. Vaidyanathan. *Multirate systems and filter banks.* Prentice Hall, first edition, 1993.

[9] Klaas Bult and Govert J. G. M. Geelen. An inherently linear and compact MOST-only current division technique. *IEEE J. Solid-State Circuits*, 27(12):1730–1735, December 1992.