A 1-V CMOS Power Amplifier for Bluetooth Applications

by

Ho Ka Wai

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ABSTRACT

With recent advance in CMOS processes, many essential building blocks for wireless transceivers, such as low-noise amplifier (LNA), mixer, frequency synthesizer, channel selection filter and digital-to-analog converter, have been demonstrated using CMOS technology. However, not much work has been done or reported a CMOS power amplifier, in particular at low supply voltage. As supply voltage is reduced to 1V, the performance of the power amplifier, such as the output power and the efficiency are degraded.

In this thesis, the design considerations of a RF CMOS power amplifier under low supply voltage are detailed. A two-stage power amplifier operated at 2.4GHz and 1-V supply has been designed and fabricated for Bluetooth applications in a standard 0.35μm CMOS technology. A common-gate Class E output stage, which operates under low supply voltage without degrading the efficiency, is proposed. A pre-amplifier with positive feedback configuration is employed to drive the common-gate output stage. To achieve high efficiency and high output power,

bondwires are used as inductors for the power amplifier because of their high quality factor.

Measurement results show that the amplifier delivers 18dBm output power with 33% power-added efficiency (PAE) under a 1V supply voltage. With a 1.2V supply, the amplifier delivers 20dBm output power with 35 % PAE and can be integrated for class 1 Bluetooth application. The measured output spectrum falls within the Bluetooth spectrum mask when a modulated signal is input to the power amplifier. The adjacent-channel power rejection (ACPR) at 550kHz offset is –21.4 dBc under 1V and –23.5 dBc with 1.2V supply voltage.

CHAPTER 1

INTRODUCTION

1.1 Motivation

Wireless communications have shown remarkable growth in the last decade. For example, more and more people have their own mobile phones. Some of them have already owned several mobile phones in the past few years and are eager to buy new phones with better performance. Manufacturers have to develop smaller mobile phones with longer lifetimes and lower cost so as to keep competitive. Therefore, experts in wireless communications put significant efforts to further improve the performance and reduce the cost of the mobile phone.

Nowadays, the dominant technologies used for the radio frequency (RF) front-end circuits of a mobile phone are Gallium Arsenide (GaAs), BiCMOS and silicon bipolar. These technologies offer higher breakdown voltage, lower substrate loss and higher quality of monolithic inductors and capacitors compared with CMOS

technology. However, they are much more expensive. CMOS technology is exclusively used on the digital signal-processing unit. The realization of the RF front-end circuits using CMOS technology can provide single-chip solution which greatly reduces the cost. Moreover, the advance in CMOS process has made it more possible to realize CMOS RF circuits with performance comparable to that using GaAs, BiCMOS and silicon bipolar. Most of the essential building blocks of a receiver, such as low noise amplifier (LNA), mixer, frequency synthesizer and intermediate frequency (IF) filter, have been realized by CMOS processes [1][2].

Recently, short distance wireless communications, such as wireless local area network (WLAN) and Bluetooth, have drawn the attention of researchers due to the rapidly growth in personal communication systems. CMOS RF front-end circuits are capable to meet the specifications so that the whole system can be integrated into one chipset [3].

Although CMOS technology provides single chip solution, it also suffers from a poor quality factor of monolithic passive components, low breakdown voltage of the transistors and large process variation. Also, the scaling of the CMOS technology forces the supply voltage to a lower level which results in degradation of the performance of the transceiver.

Among all the building blocks of a transceiver, the power amplifier contributes the most in terms of power consumption of the whole transceiver. The efficiency of the power amplifier becomes one of the crucial parameters to be optimized for power saving. However, the efficiency of the power amplifier is degraded by reducing supply voltage.

This dissertation will focus on the design considerations and implementation of a CMOS power amplifier for Bluetooth applications under low supply voltage.

1.2 Specifications

In this section, the specification of Bluetooth will be described. Also, the requirement of power amplifier for Bluetooth applications will be detailed.

As the last building block of the transmitter, a RF power amplifier has to amplify the RF signal before a RF signal is transmitted at the antenna. Because there are losses in the channel, the signal power should be large enough so that the signal is still readable at the receiver. Therefore, the output power of the power amplifier defines the transmission distance of a communication standard.

Bluetooth is a short distance wireless communication standard which operates from 2400MHz to 2483.5MHz Industrial Scientific Medicine (ISM) band. Based on the

signal transmission distance, the required transmitter power level for Class 1, Class 2 and Class 3 are 20dBm, 4dBm and 0dBm, respectively. The modulation scheme employed is Gaussian Frequency Shift Keying (GFSK) which is a constant envelope modulation scheme [4]. Table 1.1 shows the requirement of the transmitted power at certain frequency offset.

Table 1.1 Transmit spectrum mask

Frequency Offset	Transmit Power
± 550 kHz	-20 dBc
|M-N| = 2	-20 dBm
|M-N| ≥ 3	-20 dBm

According to table 1.1, the output spectrum of the power amplifier for Class-1 Bluetooth should be under the profile as shown below.

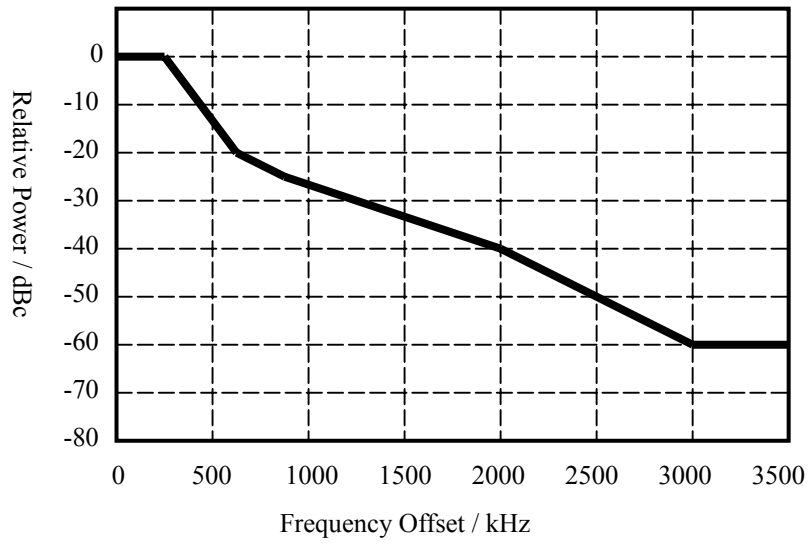

Figure 1.1 Output spectrum mask for class 1 Bluetooth

Since the specification on linearity of the power amplifier is quite relaxed, non-linear power amplifiers can be used to achieve high efficiency. The trade off between linearity and efficiency will be detailed in chapter 2.

With the advance in process, the supply voltage is scaled down. The new market trend is to build a single supply system with low operating voltage. Our research group, the Analog Research Group, have demonstrated the use of 1-V supply voltage in many essential building blocks such as low noise amplifier (LNA), mixer and voltage-controlled oscillator (VCO) [5]. Therefore, the power amplifier will be designed under 1-V supply voltage in order to fully integrate the whole transceiver. The output power is targeted at 20dBm for Class 1 Bluetooth application.

1.3 Thesis Outline

In this thesis, there are 7 chapters. Some of the basics of power amplifier will be detailed in chapter 2 to provide background information for the readers. Chapter 3 will discuss the design considerations of the power amplifier used for Bluetooth applications. The inductor is one of the essential components in power amplifier circuit. The modeling of the bondwire inductor will be described in chapter 4. In chapter 5, both circuit and printed circuit board (PCB) layout considerations will be presented. The measurement results of bondwire and the power amplifier will be

shown in chapter 6. The thesis ends with a conclusion in chapter 7 and talks about the potential improvement of the circuit and the future work.

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CHAPTER 2

BASICS OF POWER AMPLIFIER

2.1 Introduction

Wherever there are wireless communications, there are transmitters. When there are transmitters, there must be RF power amplifiers. People rate the performance of an RF power amplifier in terms of the power gain, the efficiency and the linearity. Also, the basic underlying principles of operations of different power amplifier modes should be thoroughly understood before an improved circuit topology can be designed. Therefore, understanding the language used in the world of power amplifiers and the basic operating principle of different modes of power amplifier is required.

In this chapter, the merits and the terminologies used to characterize a power amplifier will be reviewed. Also, different classes of power amplifier and their corresponding features will be described.

2.2 Figure Of Merits

Whenever an RF power amplifier is discussed, people are interested in its power gain, power-added efficiency (PAE), the drain efficiency (DE) and the linearity.

The power gain of a power amplifier is defined as follows:

$$\text{Power Gain} = \frac{\text{Power delivered to the load}}{\text{Power avaliable at the input port}} = \frac{P_{out}}{P_{in}} \tag{2.1}$$

The RF power amplifier consumes most of the power inside a transceiver. To preserve the battery lifetime, the power amplifier should be effective in converting DC power to RF power. PAE and DE are the parameters to characterize the effectiveness of power conversion. They are defined as:

$$DE = \frac{P_{out}}{P_{DC}} \tag{2.2}$$

$$PAE = \frac{P_{out} - P_{in}}{P_{DC}} \tag{2.3}$$

where P_{out} is the output power at the desired frequency, P_{DC} is the DC supply power and P_{in} is the input power at the frequency of interest. PAE includes information on the driving power for a power amplifier, so PAE is commonly used instead of DE.

It is observed that the PAE is approximately equal to the DE if the power gain is

large enough. It also means that the power amplifier is more efficient.

Traditionally, linearity is measured with third order intermodulation intercept (IP3) and 1dB compression point (P_{1dB}). Figure 2.1 shows the graphic representations of IP3 and P_{1dB}.

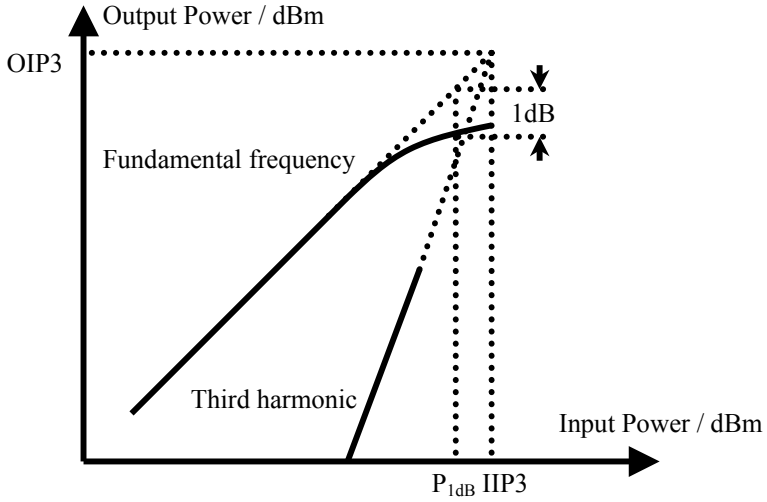

Figure 2.1 Definitions of IP3 and P_{1dB}

Those parameters can be obtained using a two-tone test [1] as pictured in Fig. 2.2.

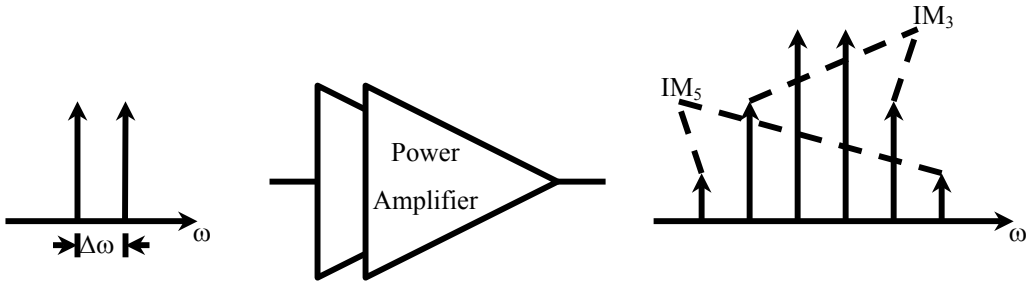

Figure 2.2 Two-tone test of a power amplifier

By applying two single-tone signals with equal amplitude but with slightly different frequencies circuit, the intermodulation products of the power amplifier are then measured at the output.

However, IP3 and P_{1dB} are not accurate enough and can only provide a rough measure of linearity of a power amplifier. This is because most power amplifiers operate near the 1dB compression point in order to achieve the highest efficiency, and the nonlinear effects of higher order distortion should be taken into account. Therefore, the adjacent-channel power rejection (ACPR) is used to assess the linearity of a power amplifier instead of IP3 and P_{1dB}. Figure 2.3 shows the definition of ACPR.

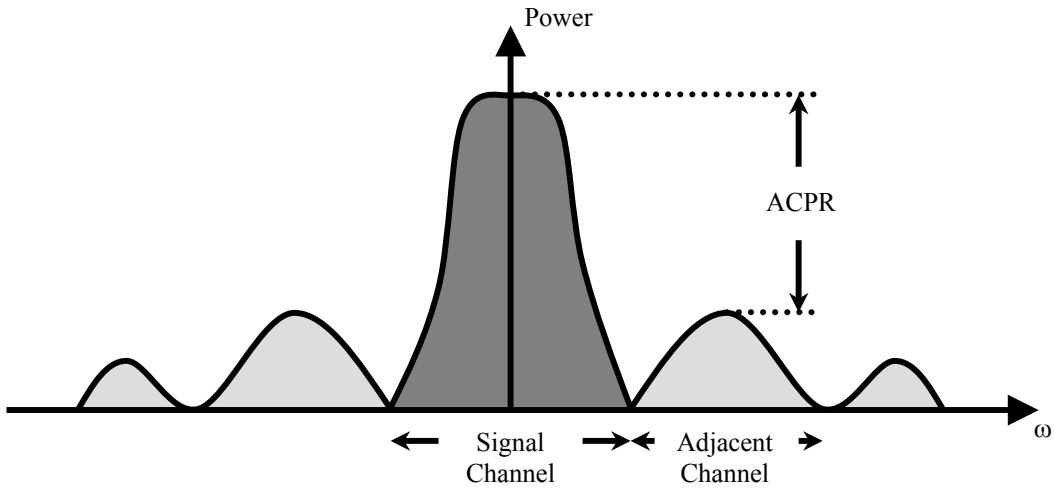

Figure 2.3 Definition of ACPR

When a modulated signal is applied to the power amplifier, the output of the power amplifier consists of the amplified signal channel and the adjacent channel signal

resulted from intermodulation. Since the input used in testing the ACPR is a modulated signal, higher order distortions are also included. Therefore, it is more accurate to measure the linearity of a power amplifier using ACPR instead of a two-tone test.

2.3 Classification Of Power Amplifiers

Digital modulation offers superior performance, such as noise insensitiveness and integration of low cost CMOS process over analog modulation, and is widely used in wireless systems. To facilitate discussion on the tradeoff between power efficiency and spectral efficiency in digital modulation, literature classifies power amplifiers as either linear power amplifiers or nonlinear power amplifiers [2].

2.3.1 Linear Power Amplifiers

When a linear power amplifier is used to amplify a signal, there is linear relationship between the input signal and the output signal. This is important for the non-constant envelope modulation scheme because the signal information, which is embedded in the envelope, will be lost if the power amplifier is not linear enough. Among all classes of power amplifiers, only class-A, class-AB and class-B can be viewed as a linear power amplifier.

2.3.1.1 Class A

A class-A power amplifier is the simplest power amplifier. It can be viewed as a small-signal amplifier except the signal level is a substantial fraction of the bias level. A typical circuit topology is shown in Fig. 2.4.

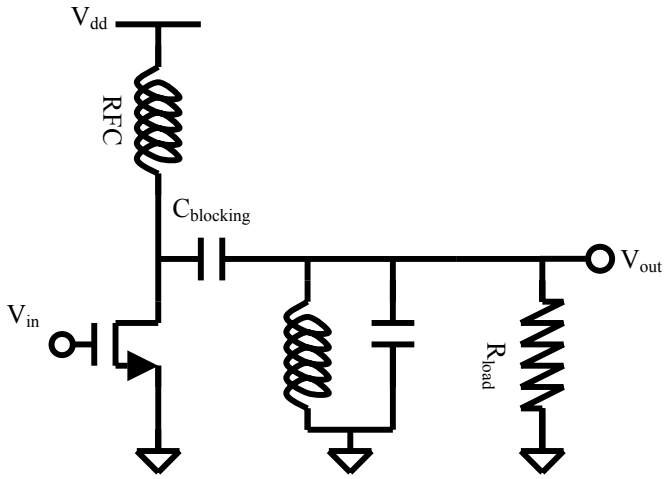

Figure 2.4 Typical configuration of a class-A power amplifier

It consists of an RF choke, a DC blocking capacitor, a parallel LC tank and a transistor. An RF choke (RFC) is used to feed DC power to the drain and provide a constant current to the transistor. Also, the use of inductive load doubles the voltage swing at the drain of the transistor which lowers the supply voltage by a factor of two [3]. The DC blocking capacitor prevents current flow to the output loading in order to eliminate DC power consumption. Due to the non-linearity of the transistor, the parallel LC tank filters the out-of-band emission so that only a

single tone sine wave is observed across the output loading.

The NMOS transistor shown in Fig. 2.4 is operated in the saturation region or pinch-off region for the whole input cycle. The transistor is biased to V_{dd} so that it operates in the saturation region for the entire period. Since both the transconductance (g_m) and the output resistance (R_{out}) of the transistor remain the same throughout the entire input cycle, the gain, g_mR_{out}, is approximately the same throughout the period and the linearity is the best among the other classes of power amplifier. Figure 2.5 shows the waveforms of a class-A power amplifier.

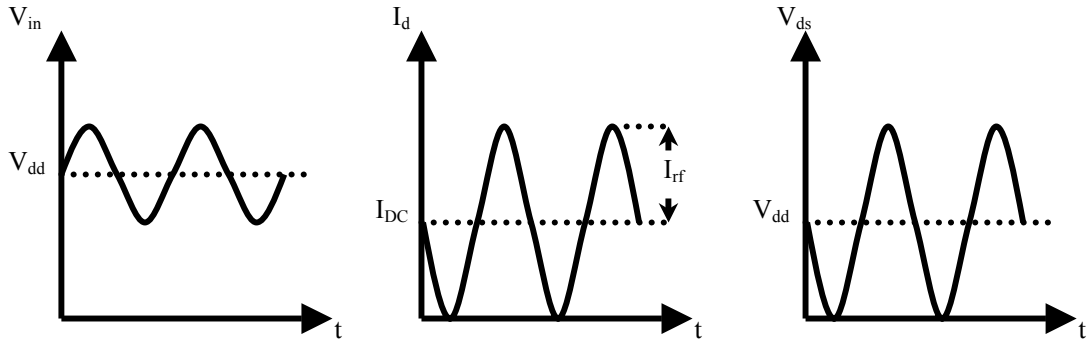

Figure 2.5 Voltage and current waveforms of an ideal class-A power amplifier

However, due to the 100% duty cycle or 360° conduction angle, the transistor always draws current during the period and the voltage across the transistor is always larger than zero. In other words, the transistor dissipates power constantly throughout the cycle. High linearity is achieved with the price of poor efficiency in a class-A

power amplifier.

The efficiency can be derived with the fact that the transistor is biased at V_{dd} and the amplitude of the output voltage swing is as large as V_{dd}. Also, the DC supply current, I_{DC} is the same as the RF current, I_{rf}. Therefore, the DE of a class-A power amplifier is:

$$DE = \frac{P_{rf}}{P_{DC}} = \frac{\frac{1}{2} I_{rf} V_{dd}}{I_{DC} V_{dd}} = \frac{1}{2}$$

The inherent DE of a class-A power amplifier is limited to 50%. Any non-ideal effects, such as losses associated with the parasitics will further reduce the efficiency. Therefore, the class-A power amplifier is chosen only when the requirement of linearity is stringent.

2.3.1.2 Class B

It is noticed that the efficiency can be improved if the transistor does not conduct current for the entire cycle, but only draws current at a certain period of time. For example, if the transistor conducts half of the cycle, it is categorized as class-B power amplifier. Because the transistor has a 180° conduction angle, the transistor is biased at the threshold voltage and the transistor is in cut off region during half period of time, as shown in Fig. 2.6.

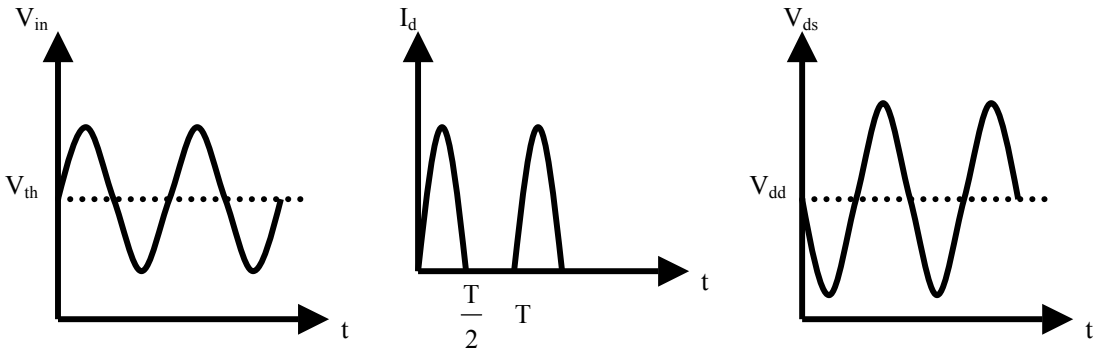

Figure 2.6 Voltage and current waveforms of an ideal class-B power amplifier

In practice, a class-B power amplifier is usually realized in push-pull configuration, as shown in Fig. 2.7, to maximize efficiency.

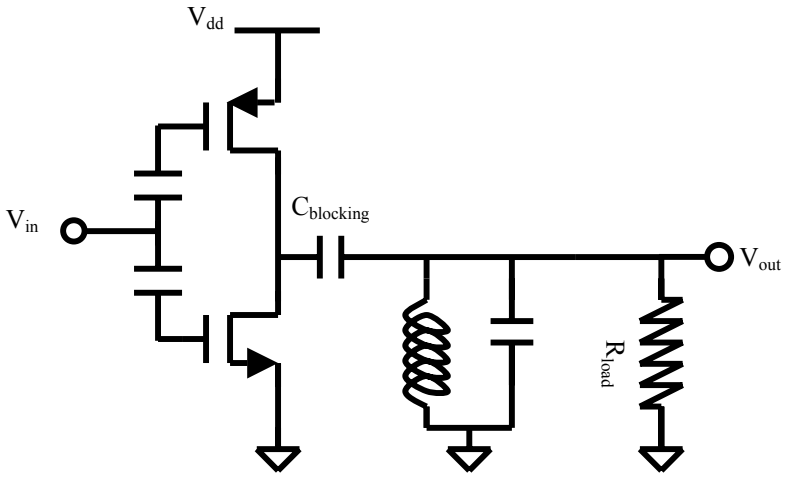

Figure 2.7 Complementary class-B power amplifier

On the first half of the cycle, the current is 'pushed' to the output loading through the PMOS transistor. On the other half cycle, the current is 'pulled' from the load to NMOS transistor. However, due to the absent of high speed PMOS device, this

configuration is seldom used for RF applications.

As shown in Fig. 2.8, a transformer-coupled class-B power amplifier utilizes two NMOS transistors.

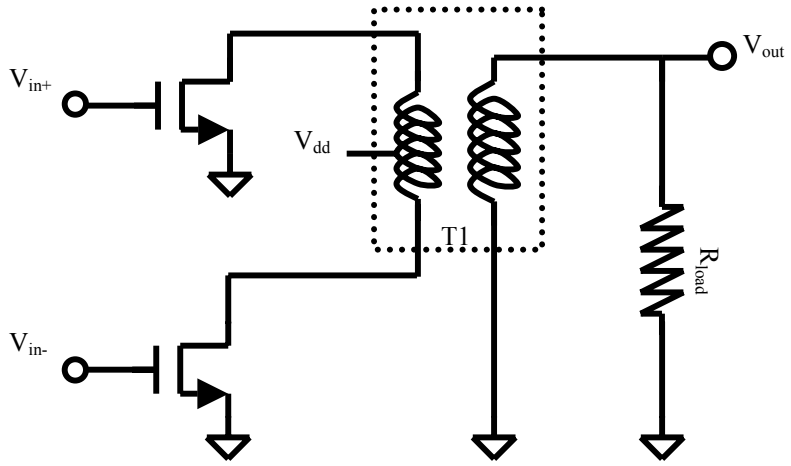

Figure 2.8 A transformer coupled class-B power amplifier

Since two NMOS transistors are used, it is more suitable for high-speed applications. The transformer is used to combine the differential-ended drain current into a single-ended current.

With a 50% duty cycle, the DE can achieve 78% [3]. However, the linearity is inevitably degraded due to the switching between the cut-off region and the pinch-off region of the transistors. In practice, a class-B power amplifier is difficult to implement because the two transistors may have different threshold voltages and they may be ON or OFF at the same time.

2.3.1.3 Class AB

When the transistors are ON at the same time for some instant, the amplifier is defined as a class-AB power amplifier. The corresponding waveforms are shown in Fig. 2.9.

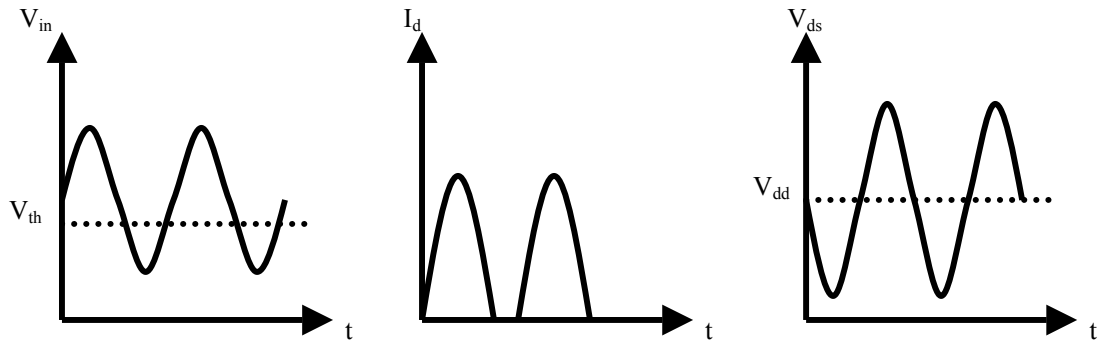

Figure 2.9 Voltage and current waveforms of an ideal class-AB power amplifier

As its name implies, all parameters associated with a class-AB power amplifier lie between class-A and class-B. For example, the efficiency is between 50% and 78%. The performance of linearity is somewhere between class-A and class-B. Since the duty cycle of the transistors is ranged from 100% to 50%, the transistors are biased above the threshold voltage.

The circuit topologies of a class-AB power amplifier can be either a simple transistor configuration as class-A or a push-pull configuration as class-B. Class-AB power amplifiers are widely used in a system with a non-constant envelope modulation

scheme [4] since it can provide better linearity with acceptable efficiency.

2.3.2 Non-Linear Power Amplifiers

When a system employs constant envelope modulation scheme, the linearity of a power amplifier is not critical. A non-linear power amplifier can be used so as to obtain higher efficiency. Class-C, class-E and class-F are examples of non-linear power amplifiers with high efficiency.

2.3.2.1 Class C

The efficiency of a power amplifier is increased from 50% for a class-A power amplifier to 78% for a class-B power amplifier with the condition angle decreased from 360° to 180°. It is observed that efficiency greater than 78% can be achieved if the condition angle is further reduced to a level smaller than 180°. The resultant power amplifier is categorized as class-C. In fact, the circuit topologies can be the same for class-A, class-AB, class-B and class-C. The transistor in a class-A, class-AB, class-B and class-C power amplifiers is operated as a current source. The major difference associated with these four types of power amplifier is the biasing condition. With the reduction in condition angle, the efficiency is traded-off with the linearity from class-A to class-C. The price of achieving high efficiency is the poor linearity performance. Moreover, although the efficiency can approach 100%

with conduction angle trends to zero, the output power will be zero since there is no drain current at all. Figure 2.10 shows the current and voltage waveforms of a class-C power amplifier.

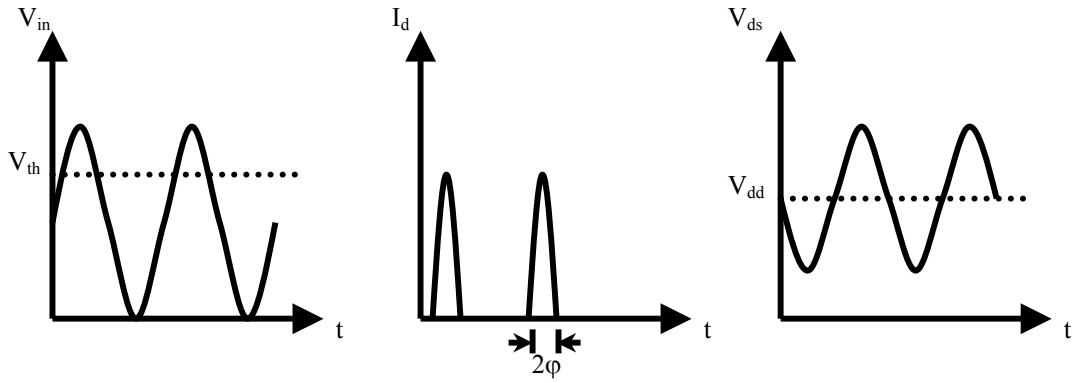

Figure 2.10 Voltage and current waveforms of an ideal class-C power amplifier

From [5], the DE can be expressed in terms of φ where 2φ is the conduction angle (in radian) for the class-C power amplifier:

$$DE = \frac{\varphi - \sin\varphi}{4\left[\sin\left(\frac{\varphi}{2}\right) - \frac{\varphi}{2}\cos\left(\frac{\varphi}{2}\right)\right]} \tag{2.4}$$

Equation 2.4 can also be applied to class-A with $2\varphi = 2\pi$, class B with $2\varphi = \pi$ and class-AB with $\pi < 2\varphi < 2\pi$.

When the conduction angle is reduced, the input driving power has to be increased in order to maintain the device in the pinch-off regions which is essential to retain the output power level. Among all of the conventional power amplifiers, the

input-driving requirement of a class-C power amplifier is the largest. Therefore, a class-C power amplifier is only suitable for a system with constant envelope modulation scheme and low output power. For a system with high output power and a constant envelope modulation scheme, switch mode power amplifier is used which have both high output power and superior efficiency.

2.3.2.2 Class E

The class-E power amplifier was first invented by Sokal in 1975 [6]. Several criteria have to be fulfilled for a power amplifier to be categorized as class-E. First of all, voltage across the switch remains low when the switch turns off. When the switch turns on, voltage across the switch should be zero. Finally, the first derivative of the drain voltage with respect to time is zero, $\frac{dV_{ds}}{dt} = 0$, when the switch turns on. The first two conditions suggest that the power consumption by the switch is zero. The last condition, $\frac{dV_{ds}}{dt} = 0$, ensures that the voltage-current product is minimized even if the switch has a finite switch on time. Figure 2.11 shows a typical configuration of a class-E power amplifier. L_1 acts as either an RF choke or a finite DC-feed inductance [7]. C_2 and L_2 are designed to be a series LC resonator plus an excess inductance L_x at the frequency of interest. C_1 and L_x are designed so that the conditions for a class-E power amplifier operation are met.

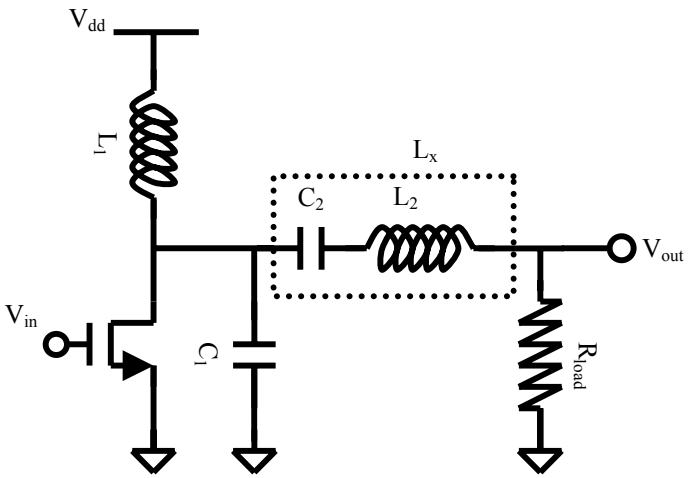

Figure 2.11 A typical configuration of a class-E power amplifier

Figure 2.12 shows the waveforms of a class-E power amplifier.

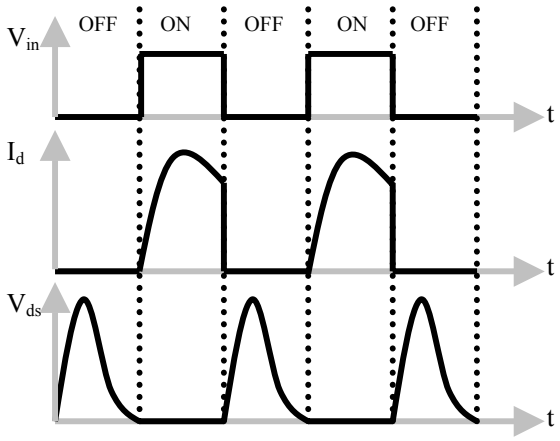

Figure 2.12 Voltage and current waveforms of an ideal class-E power amplifier

It was observed that there is no overlapping between the voltage and the current waveforms. Class-E power amplifiers achieve 100% efficiency theoretically in the expense of poor linearity performance. However, the peak drain voltage is approximately $3.6V_{dd}$ which increases the stress on the device especially for low

breakdown CMOS process.

2.3.2.3 Class F

The idea of a class-F power amplifier is to exploit the harmonic contents so that the drain voltage and current waveforms are shaped to achieve higher efficiency. A sharper edge of the drain voltage will lower the loss of the switch. Therefore, a square wave is desired at the drain. A parallel LC tank tuned to the third harmonic is included to obtain the third harmonic component and add to the fundamental component to approximate a square wave at the drain of the transistor. The circuit configuration of a class-F power amplifier is shown in Fig. 2.13.

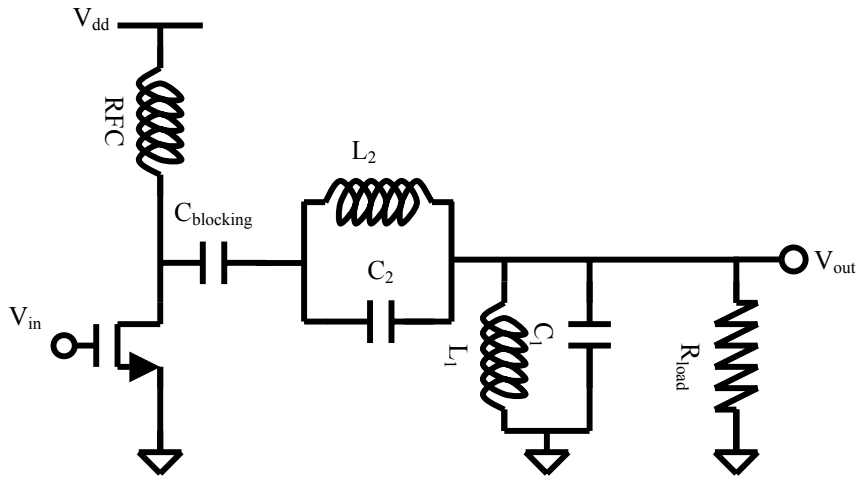

Figure 2.13 A simple configuration of a class-F power amplifier

L_1 and C_1 are tuned to resonate at the fundamental frequency while L_2 and C_2 are tuned to present non-zero load impedance at the third harmonic frequency to make

up the second terms in the Fourier series expansion of a square wave. Figure 2.13 shows only the simplest class-F power amplifier with one LC tank tuned to the third harmonic. Additional LC tanks can be added to resonate at other odd harmonic frequencies to obtain a better square wave. The voltage and the current waveforms shown in Fig. 2.14 will be observed.

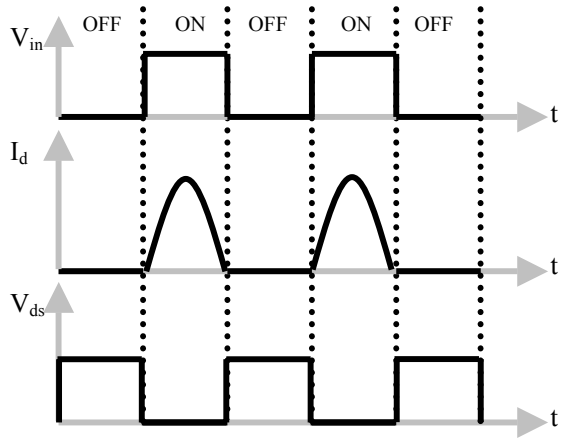

Figure 2.14 Voltage and current waveforms of an ideal class-F power amplifier

A class-F power amplifier can achieve 100% efficiency ideally. However, the disadvantage, in addition to the highly non-linear performance, is the complicated circuit topology for scaling of 3rd harmonic.

2.4 Summary

This chapter provides background for the designer to choose a suitable power amplifier. Efficiency and linearity are the major considerations when a class of

power amplifier is to be selected. It is very important to understand the specifications of the power amplifier in advance because different applications will result in different choices of power amplifiers. A table of summary is shown of the performance of all the classes discussed.

Table 2.1 Performance summaries of different classes of power amplifiers

	Ideal Efficiency	Linearity	Practical efficiency	Process
Class A	50%	Good	35%	SOI 0.5μm CMOS [8]
Class AB	50% - 78.5%	Good	45%	0.35μm CMOS [9]
Class B	78.5%	Moderate	49%	PHEMT [10]
Class C	78.5% - 100%	Poor	55%	0.6μm CMOS [11]
Class E	100%	Poor	62%	0.35μm CMOS [12]
Class F	100%	Poor	80%	PHEMT [10]

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CHAPTER 3

DESIGN OF POWER AMPLIFIER

3.1 Introduction

Recall that the research goal is to design a CMOS power amplifier for Bluetooth applications. Therefore, the corresponding specifications should be studied before the design of the power amplifier.

As stated in chapter 1, the output power of the power amplifier is set to be 20dBm for class-1 Bluetooth application under 1V supply voltage. Since the modulation scheme employed by Bluetooth is GFSK, which is a constant envelope modulation scheme, a non-linear power amplifier can be used to achieve high efficiency. Among all classes of non-linear power amplifiers, the class-E power amplifier is the most attractive candidate in terms of circuit simplicity and high efficiency performance.

In this chapter, the circuit technique used for the power amplifier to work under low

supply voltage will be detailed in this chapter. Also, the design considerations of a class-E power amplifier will be discussed. Both the calculated and the simulated results will be presented. Finally, the characteristics of one of the crucial components, the inductors, will be investigated.

3.2 Design of Power Amplifier

3.2.1 Differential Topology

Differential configuration will be adopted because of its numerous advantages. First of all, the common-mode noise is minimized which reduces the disturbance of substrate coupling to other circuits. Since the current is discharged to the ground twice per cycle, interference to the desired signal is reduced.

A large output voltage swing is needed for a power amplifier so as to provide moderate output power. However, the breakdown voltage of the devices in CMOS process is too low to withstand a large voltage swing. With the process scaling, the situation is even worse. Fortunately, the most pronounced advantage of differential configuration, gain boosting, relaxes the stringent requirement on device breakdown voltage. The same circuit topology with differential configuration gives double output power compared with the single-ended configuration. Also, the size of the

transistor can be smaller because the current flow through the transistor is reduced for the same supply voltage and the same output power.

3.2.2 Class-E Power Amplifier

The circuit topology of a class-E power amplifier is reprinted in Fig. 3.1.

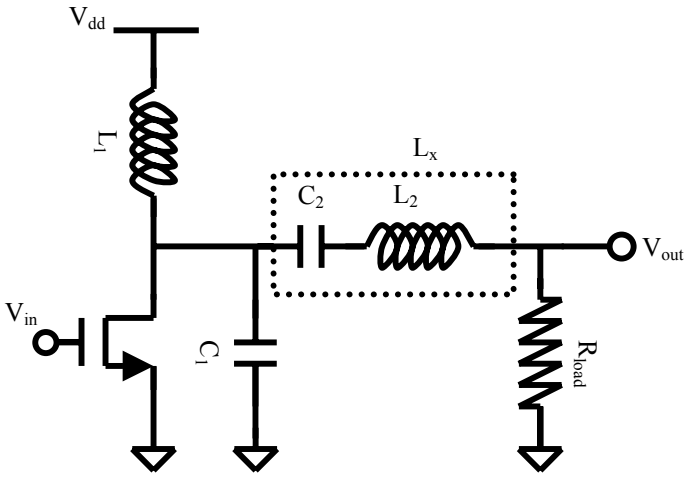

Figure 3.1 Configuration of a class E power amplifier

The component values can be calculated using the following equations [1]:

$$L_X = \frac{\pi V_{dd}^{\,2}\left(\pi^2 - 4\right)}{2\omega P_{out}\left(\pi^2 + 4\right)} \tag{3.1}$$

$$C_1 = \frac{P_{out}}{\pi\omega V_{dd}^{\,2}} \tag{3.2}$$

$$R_{load} = 0.577\frac{V_{dd}^{\,2}}{P_{out}} \tag{3.3}$$

These equations can be derived by the fact that the switch is either turned on or off. Therefore, two state equations can be obtained. For a power amplifier to be categorized as class-E, several criteria, as stated in chapter two, have to be fulfilled. These criteria are the boundary conditions to be applied and the state equations can be solved.

It should be noted that the above equations are only valid for class-E power amplifiers and R_{load} is not necessary the same for all classes of power amplifier [2]. R_{load} is usually called optimum load (R_{opt}) and is defined as a loading presented to the power amplifier for a desired output power with the highest efficiency. The optimum load is designed according to the specification on output power and the supply voltage.

In the above analysis, L_1 is assumed to be an RFC. The rule of thumbs for an inductor to be an RFC is that the reactance of L_1 is larger than ten times the reactance of C_1:

$$X_{L_1} > 10X_{C_1} \tag{3.4}$$

In fact, L_1 acts as either a RF choke (RFC) or a finite DC-feed inductance. However, it is advantageous to choose L_1 as a finite DC-feed inductor because the serial resistance of the inductor is reduced with a smaller inductance value which

provides higher efficiency than an RFC with the same output power and the same supply voltage [3]. The operating frequency can be pushed higher with a finite DC-feed inductor since the parasitic capacitors associated with the transistors are resonated out by the inductor. In practice, the capacitor used to fulfill the class-E operation, C_1, can be implemented by the parasitic capacitance of the transistor. Therefore, L_1 can be calculated by the resonant equation of a LC tank.

$$L_1 = \frac{1}{\omega^2 C} = \frac{1}{\omega^2 \left(C_p - C_1 \right)} \tag{3.5}$$

In the above equation, C is the total capacitance at the drain of the transistors, C_p, minus the required parasitic capacitor, C_1, in fulfilling the operating condition of a class-E power amplifier.

3.2.3 Output Matching Network

The output power will be low if the power amplifier is directly connected to the antenna, which has a 50Ω loading. For example, if R_{opt} = 50Ω and V_{dd} is 1V, then

$$P_{out} = 0.577 \frac{V_{dd}^{\ 2}}{R_{opt}} = 11.54\text{mW}$$

As a result, the optimum load is typically about several ohms and can be obtained with the supply voltage (V_{dd}) and the output power (P_{out}) fixed according to the

specification of a wireless standard.

In order to match the 50Ω loading, an up-conversion matching network is implemented to transform the optimum load to a 50Ω load. L-matching network is chosen because of its circuit simplicity. Also, the excess inductance (L_x) in a class-E power amplifier can be combined with the inductor used in the matching network if a low-pass L matching network is used. Therefore, the schematic of a class-E power amplifier is modified as Fig. 3.2.

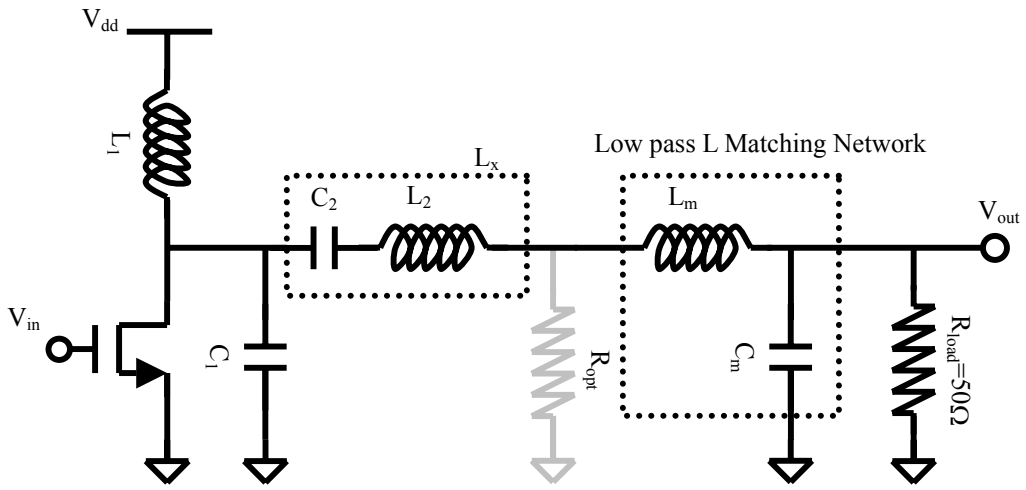

Figure 3.2 Complete schematic of a class E power amplifier

The values of L_m and C_m can be calculated using the following equations [4]:

$$L_m = \frac{\sqrt{R_{opt}\left(R_L - R_{opt}\right)}}{\omega} \tag{3.6}$$

$$C_m = \frac{\sqrt{\left(R_L - R_{opt}\right)/R_{opt}}}{\omega R_L} \quad (3.7)$$

3.2.4 Design Of Output Stage

Since the power amplifier is designed for class-1 Bluetooth application, the output power is 20dBm, 100mW. The use of differential topology is to relax the output power from 100mW to 50mW. The target output power is designed to be 60mW to provide margin for some losses due to parasitics and the supply voltage of the power amplifier is set to 1V. Therefore, the optimum load can be calculated using equation 3.1.

$$R_{opt} = \frac{V_{dd}^{\ 2}}{P_{out}}\left(\frac{8}{\pi^2 + 4}\right) = \frac{1}{60m}(0.577) = 9.6\Omega$$

Also, the values of parameters, L_x and C_1 can be calculated using equation 3.2 and 3.3 to meet the requirements of a class-E power amplifier.

$$L_X = \frac{\pi V_{dd}^{\ 2}\left(\pi^2 - 4\right)}{2\omega P_{out}\left(\pi^2 + 4\right)} = 0.735\text{nH}$$

$$C_1 = \frac{P_{out}}{\pi\omega V_{dd}^{\ 2}} = 1.27\text{pF}$$

With R_{opt} = 9.6Ω, the parameters of a L-matching network can be calculated using

equation 3.6 and 3.7.

$$L_m = \frac{\sqrt{R_{opt}\left(50 - R_{opt}\right)}}{\omega} = 1.31\text{nH}$$

$$C_m = \frac{\frac{\sqrt{\left(50 - R_{opt}\right)/R_{opt}}}{50}}{\omega} = 2.72\text{pF}$$

The parasitic capacitance associated with the transistor should be known before the calculation of L_1. As a result, the size of the transistor should be designed first in order to find out the value of L_1. However, the empirical equation to calculate the transistor sizing is absent due to the *apriori* designability of the class E power amplifier, the size of the transistor can only be estimated by the their maximum allowable current flow.

Because the output power is set to 60mW and the supply voltage is 1V, the average current flow through the transistor is about 60mA. Since the switch will conduct current for only half of the period, the peak current should be at least 120mA. With $V_{gs} = V_{ds} = 1V$, $V_{th} = 0.6V$ and $\mu C_{ox} = 140\mu A/V^2$, the size of the transistor can be calculated by the current equation:

$$I_d = \frac{\mu C_{ox}}{2}\frac{W}{L}\left(V_{gs} - V_t\right)^2 \qquad (3.8)$$

Because TSMC 0.35-μm CMOS will be used, the W/L of the transistor is found to be approximately equal to 4500μ/0.4μ, which gives 4.2pF parasitic capacitors. Therefore, L_1 can be calculated by equation 3.5:

$$L_1 = \frac{1}{\omega^2 C} = \frac{1}{\omega^2\left(C_p - C_1\right)} = 1.6\text{nH}$$

3.2.5 Common-Gate Class E Power Amplifier

In the above analysis, all the components are assumed to be ideal. However, it is not the case in practice. For example, the passive components, inductor and capacitor, consist of parasitic serial resistances. Also, the switch has finite on-resistance and finite transition times. As a result, the efficiency of a class-E power amplifier is much degraded from theoretical 100% to the highest achievable PAE of 63% in CMOS process [5]. Those non-ideal effects push RF circuit designers to develop new circuit techniques to support low voltage design.

In a class-E power amplifier, the transistor acts as a switch instead of a current source. The switch can be implemented by either common-source or common-gate configuration. Usually, the switch is implemented using a common-source configuration. For a common-source switch, the input signal is applied at the gate of the transistor. The voltage across the transistor, V_{ds} is fixed by the supply

voltage.

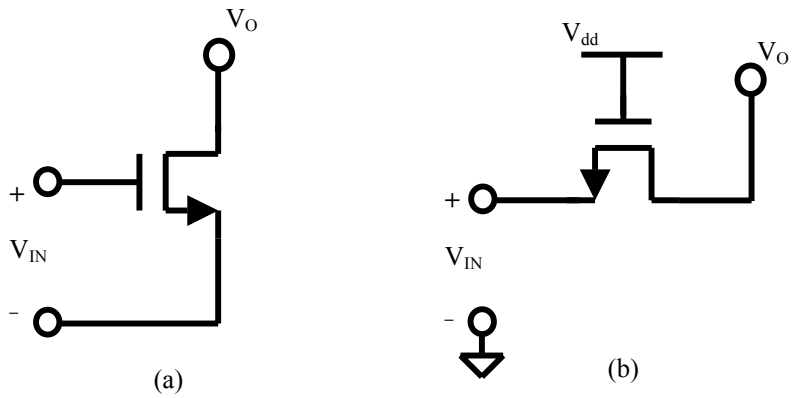

Figure 3.3 A switch using (a) common-source (b) common-gate configuration

When the supply voltage is scaled down, the voltage dropped across the on-resistance of the transistor is compatible to the supply voltage. The effective supply voltage will decrease the power capability and hence degrade the efficiency.

$$V_{effective} = V_{dd} - V_{R_{on}} \tag{3.9}$$

The situation is even worse if an RFC is used instead of a finite DC feed inductor. Therefore, a finite DC feed inductor is preferred because the voltage drop across the inductor is minimized and the effect on the effective supply voltage is neglected.

[6] proposed a common-gate class-E power amplifier to relax the device stress. The corresponding schematic is shown in Fig. 3.4. The common-gate class-E power amplifier is connected in cascode with a large transistor to avoid the loading effect to the input stage. However, the cascode transistor unfortunately reduces the voltage

headroom across the switch.

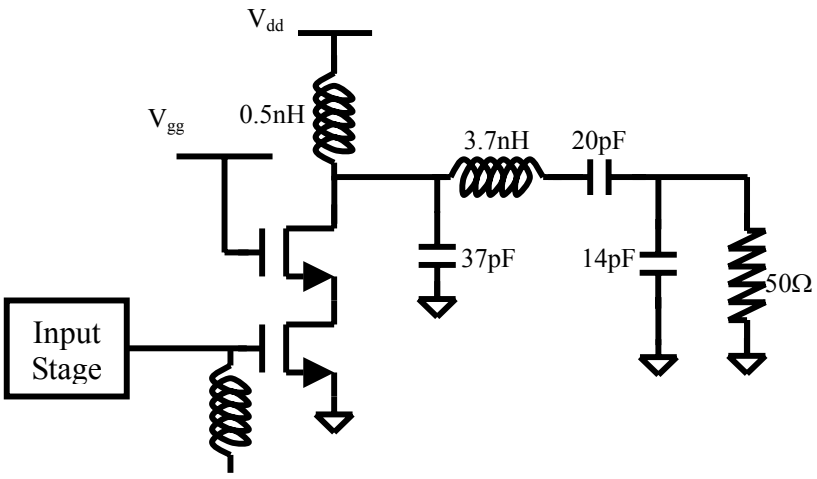

Figure 3.4 Schematic of the published common-gate class-E power amplifier

To overcome the voltage drop across the switch, a common-gate switch without connecting in cascode is proposed and the schematic of the proposed common-gate class-E power amplifier is shown in Fig. 3.5.

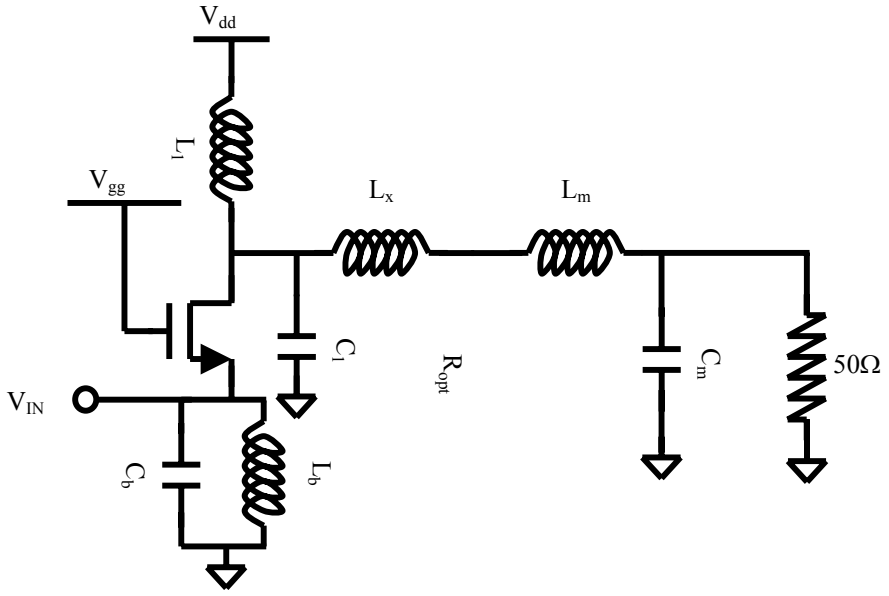

Figure 3.5 Schematic of the proposed common-gate class-E power amplifier

For a common-gate switch, the input signal is directly applied to the source. By proper biasing, the effective supply voltage can be increased from $V_{dd} - V_{Ron}$ (in the common-source case) to $V_{dd} - V_{Ron} + V_{signal}$ where V_{signal} is the amplitude of the input signal. Figure 3.6 shows the corresponding current and voltage waveforms of the proposed common-gate class E power amplifier.

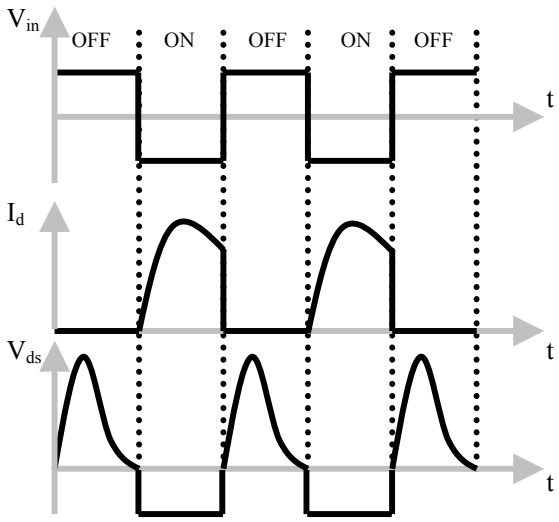

Figure 3.6 Voltage and current waveforms of a common-gate class E power amplifier

The idea utilizes the fact that the voltage at the source is in phase with the voltage at the drain. If the source is biased at ground and the gate is tied to V_{dd}, the switch is turned on when the voltage of the source is negative. Since the input signal is applied to the source, the amplitude of the signal increases the voltage across the switch. As a result, the supply voltage is raised effectively. The effect of V_{Ron} can be compensated by the amplitude of the applied signal in the common-gate

configuration, and the supply voltage can be lower with compatible efficiency. The problem of low impedance of the input of the common-gate switch without cascode can be solved with the inclusion of a driver stage with positive feedback before the class-E amplifier.

3.2.6 Drive Stage Using Positive Feedback

The pre-amplifier of the power amplifier is a very important element since the efficiency and the output power can be very low if the driving signal to the output stage is not optimum. Under low supply voltage, the pre-amplifier is very hard to design mainly because the size of the output stage transistors needs to be in millimeter range, which introduces a large capacitive loading.

Because differential configuration is employed, the problem can be solved by utilizing a cross-coupled pair to form a positive feedback as the pre-amplifier. Several publications demonstrated the use of the positive feedback in power amplifiers [5][7]. Also, a pre-amplifier with positive feedback provides a large swing to the input of the output stage which maintains high efficiency.

3.2.7 Proposed Architecture

The overall schematic of the proposed power amplifier is shown in Fig. 3.7.

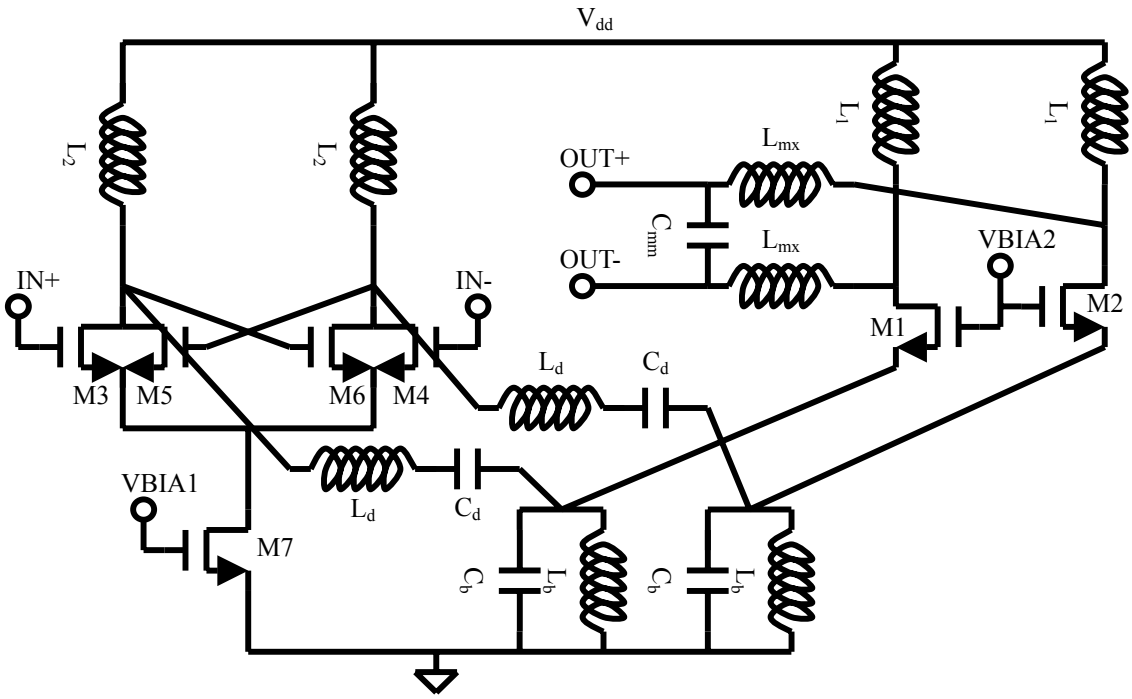

Figure 3.7 Schematic of the proposed power amplifier

The design of the proposed power amplifier starts by specifying the required power gain and the output power. First of all, the output power is assumed to be 120mW, 20.8dBm. The power gain of the output stage is set to 7dB. Therefore, the required input power for the output stage is 13.8dBm. In other words, the output power of the driver stage should be at least 13.8dBm. The input power to a power amplifier utilizing positive feedback input stage is around 3dBm [5][7]. As a result, the power gain of the driver stage is equal to 10.8dBm. It is always the case that the power gain of the input stage is higher than the output stage because the input stage is focused on high power gain while the output stage is targeted to achieve high efficiency.

Since the DC biasing points for the drain of the driver stage and the source of the output stage are different, an interstage-matching network with a DC blocking capacitor, C_d, is implemented to connect the driver stage and the output stage.

Another function of the interstage-matching network is to present an optimum load to the driver stage while transfer the maximum power to the input of the output stage. Since the driver stage using positive feedback works as a class-E power amplifier, the values of the components of the driver stage can be calculated using the same agreement as the output stage.

$$R_{opt}(\text{preamp}) = \frac{V_{dd}^{\,2}}{P_O(\text{preamp})}\left(\frac{8}{\pi^2+4}\right) = \frac{1}{12\text{m}}(0.577) = 48\Omega$$

$$L_X(\text{preamp}) = \frac{\pi V_{dd}^{\,2}\left(\pi^2-4\right)}{2\omega P_o(\text{preamp})\left(\pi^2+4\right)} = 2\text{nH}$$

$$C_1(\text{preamp}) = \frac{P_o(\text{preamp})}{\pi\omega V_{dd}^{\,2}} = 0.253\text{pF}$$

$$L_2 = \frac{1}{\omega^2 C} = \frac{1}{\omega^2\left(C_p - C_2\right)} = 2.4\text{nH}$$

The impedance looking from the source of the output stage to the 50Ω load is calculated as shown below:

$$Z = \frac{1}{g_{m1}} + \frac{\omega^2 L_1 L_{mx} + j\omega L_1 R_L \left(\omega^2 L_{mx} C_m - 1\right)}{R_L \left\{\omega^2 \left[L_1 \left(C_m + C_p\right) + L_{mx} C_m \left(1 - \omega^2 L_1 C_p\right)\right] - 1\right\} + j\omega \left[L_{mx}\left(\omega^2 C_p L_1 - 1\right) - L_1\right]}$$

Since all the parameters have been designed, the impedance Z is found to be:

$$Z=18.36+j13.15$$

The biasing LC tank L_b and C_b is to bias the source of the output stage to ground and can be separated into two parts: a LC tank resonates at the frequency of interest and a matching network, L_y and C_d, for matching the impedance Z and Ropt(*preamp*). Figure 3.8 shows the equivalent schematic of the interstage-matching network.

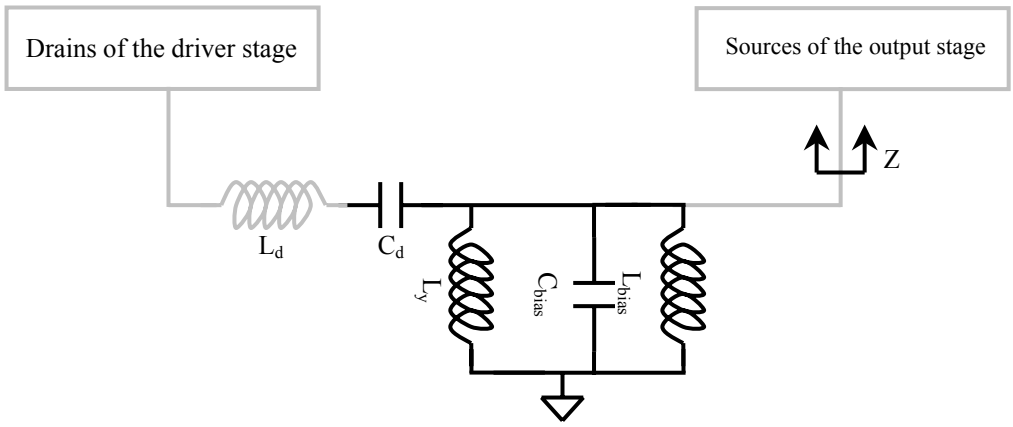

Figure 3.8 Equivalent schematic of the interstage-matching network

Since the capacitor C_{bias} will be implemented by the parastics capacitance of C_d which will be detailed in Chapter 5, C_{bias} is chosen to be one fifth of C_d and the inductor L_{bias} can be calculated using the resonant equation:

$$L_{bias} = \frac{1}{\omega^2 C_{bias}}$$

Table 3.1 summarizes the values of the passive components used in the power amplifier.

Table 3.1 Summary of the values of the passive components

L_1	L_2	L_m	C_m	L_b	C_b	L_d	C_d
1.6nH	2.4nH	2nH	1.36pF	1.9nH	0.55pF	2nH	4.2pF

Table 3.2 summarized the sizing of the transistors used in the proposed power amplifier. The corresponding parasitic drain capacitances, C_p, are also shown and the capacitances are used to calculate the finite DC feed inductors, L_1 and L_2.

Table 3.2 Summary of the transistors sizing

	M1	M2	M3	M4	M5	M6	M7
W	4500μm	4500μm	600μm	600μm	1200μm	1200μm	12000μm
L	0.4μm	0.4μm	0.4μm	0.4μm	0.4μm	0.4μm	0.4μm
C_p	4.2pF	4.2pF	0.78pF	0.78pF	1.35pF	1.35pF	17pF

3.2.7 Pre-simulation Results

The proposed power amplifier is simulated using Hspice. Level 49 BSIM3 model for TSMC 0.35-μm double-polysilicon 4-metal layer process is used throughout the

simulation. The performance of the proposed power amplifier is summarized in Table 3.3.

Table 3.3 Performance of the proposed power amplifier

	Frequency	Supply Voltage	Input Power	Output Power	Power Gain	DE	PAE
Calculated	2.4GHz	1V	-	120mW	17.8dB	100%	-
Simulated	2.4GHz	1V	3dBm	116.7mW	17.6dB	65.1%	63.8%

The DE is only 65.1% because the transistors have a finite transition time which introduced overlapping of the voltage and the current waveforms. In addition to the power dissipation due to the finite transition time, the on-resistor of the switch degrades the efficiency.

Figure 3.9 shows the waveforms of the drain of the driver stage (V_{di}), the drain of the output stage (V_{do}) and the source of the output stage (V_s).

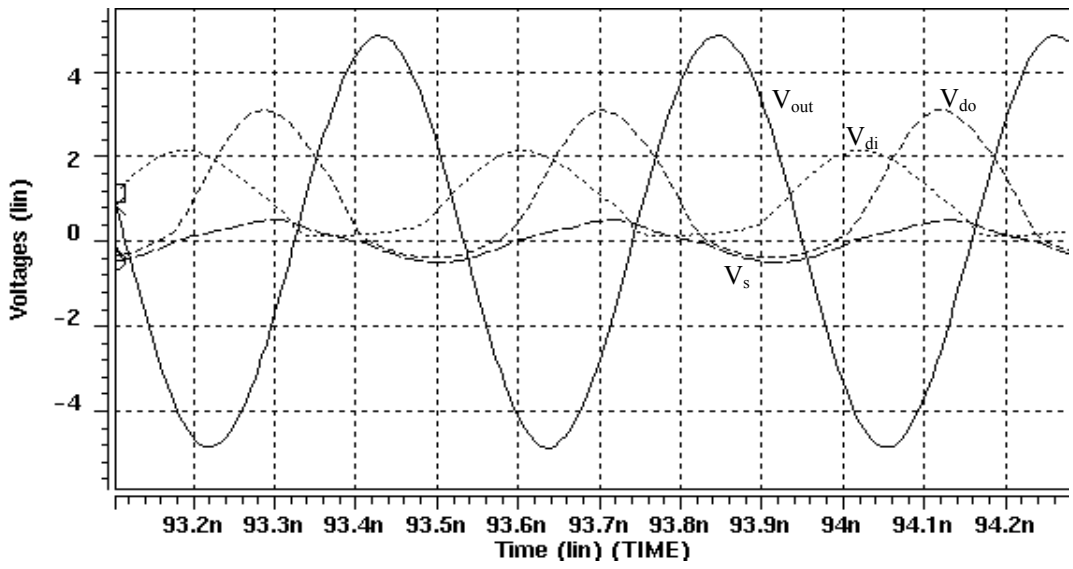

Figure 3.9 Transient response of the proposed power amplifier

It can be seen that the voltage at the source of the output stage swings to a negative value which increases the effective supply voltage.

3.2.8 Inductor Realization

In the pre-simulation, all the passive components are ideal. The parasitic serial resistance of both the capacitor and the inductor are assumed to be zero. In practice, the efficiency depends highly on the quality of the passive components especially the inductors. The quality of an inductor can be justified by quality factor (Q):

$$Q = \frac{\omega L}{R} \tag{3.10}$$

To investigate the effect on the inductor Q, PAE of the proposed power amplifier is plotted against Q in Fig. 3.10.

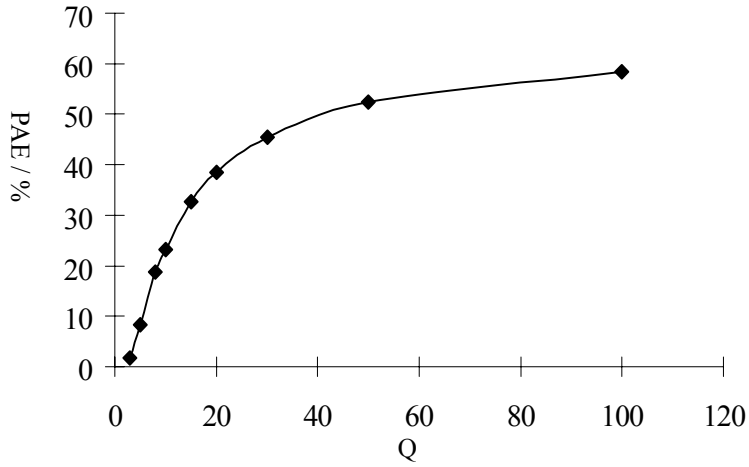

Figure 3.10 PAE versus inductor Q

It is observed that the PAE drops rapidly when the Q is below 20. Therefore, the

inductor Q should be kept at a level higher than 20 for acceptable PAE.

CMOS monolithic inductors are well known for its low quality factor (Q) due to high substrate loss and high parasitics. Monolithic inductors are widely used in RF applications even when the Q of monolithic inductors ranges from 3 to 6 in the CMOS process. Many building blocks, such as LNA and VCO, use monolithic inductors with Q-compensation circuitry [8]. These methods of Q compensation of on-chip inductors, however, are not feasible in power amplifiers because the power consumed in compensating the inductor losses would significantly lower the efficiency. Therefore, bondwire inductors are used to implement high-Q inductors to obtain a higher PAE.

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CHAPTER 4

BONDWIRE MODELING

4.1 Introduction

In chapter 3, the design of the proposed power amplifier and the pre-simulation results were presented. However, it is possible that measurement results cannot match the simulation results if the modeling of the components used is not accurately done. Although the model of the transistors (the level 49 BSIM3 model) is accurate enough, the model of another essential component, inductor, is still inaccurate in RF applications.

In the design of the power amplifier, all the inductors are realized using bondwire. Because of the high quality factor offered by bondwire which reduces resistive power losses, a higher PAE can be obtained. Although bondwire inductors provide a high quality factor, predetermination of bondwire inductance is difficult. Since the inductance is sensitive to bonding geometry, bondwires need to be modeled

accurately before they can be used as inductors in a power amplifier.

In this chapter, the model used for bondwire inductor will be introduced and the quantitative analysis of the inductance will be presented. The analytical solution will provide a rough estimation of the relationship between the inductance and the physical length of the bondwire which facilitates both the circuit layout and the PCB layout. Finally, the simulation of the bondwire inductance and the quality factor will be done using HP's ADS.

4.2 Inductor Model

In order to have an accurate model, all the elements used in the inductor model have to be well defined according to the electromagnetic theory and the physical structure. Figure 4.1 shows a lumped element model for the bondwire inductor.

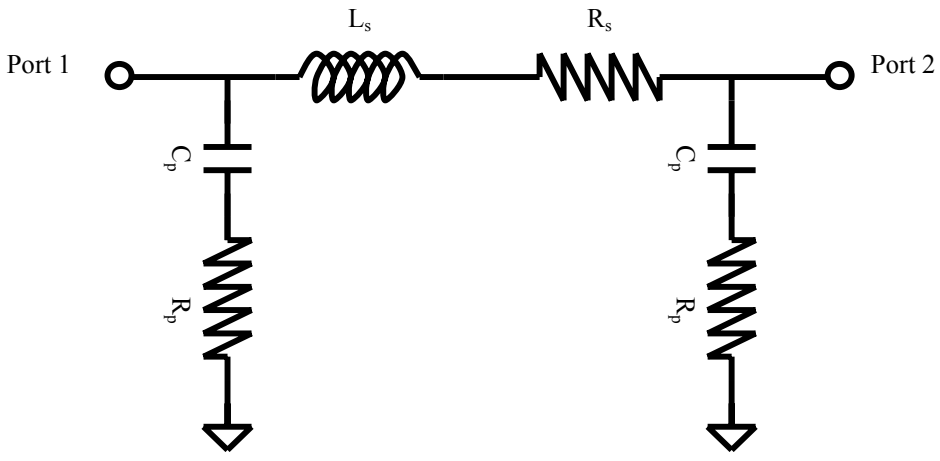


Figure 4.1 Lumped-element model for a bondwire inductor

L_s is the inductance of the bondwire, R_s models the serial resistor, C_p accounts for the overlap capacitance between the inductor and the ground plate and R_p models the substrate loss. This model will be used to do the empirical fit of the measurement results in chapter 6.

4.3 Analytical Solution Of Bondwire Inductance

The inductance of a wire can be calculated by equation 4.1 [1]:

$$L = \frac{\mu_o l}{2\pi}\left\{\ln\left[\left(\left(\frac{2l}{d}\right)+\left(1+\frac{2l}{d}\right)^2\right)^{\frac{1}{2}}\right]+\frac{d}{2l}-\left(1+\left(\frac{d}{2l}\right)^2\right)^{\frac{1}{2}}+\mu_r\delta\right\} \quad (4.1)$$

$$\delta = 0.25\tanh\left(\frac{4d_s}{d}\right) \quad (4.2)$$

$$d_S = \sqrt{\frac{\rho}{\pi f \mu_o \mu_r}} \quad (4.3)$$

where l is the length of the wire, d is the diameter of the wire, ρ is the resistivity of the material of the wire, d_s is the skin depth and μ_o, μ_r are the absolute permeability and the relative permeability of the wire respectively.

The inductance of the wire will be decreased if the wire close to the ground plate. The negative mutual inductance caused by the ground plate is give by [1]:

$$M(2h) = \frac{\mu_o l}{2\pi}\left\{\ln\left[\left(\left(\frac{l}{2h}\right)+\left(1+\left(\frac{l}{2h}\right)^2\right)\right)^{\frac{1}{2}}\right]+\frac{2h}{l}-\left(1+\left(\frac{2h}{l}\right)^2\right)^{\frac{1}{2}}\right\} \qquad (4.4)$$

where h is the distance between the ground plate and the inductor. As a result, the total inductance of the wire is reduced to $L_{total} = L - M(2h)$.

Since aluminum bondwire with 1.25-mil diameter will be used, $\rho = 1.75\times10^{-8}\Omega m$, $\mu_r = 1.00002$, $\mu_o = 4\pi\times10^{-7}\,Hm^{-1}$ and $d = 31.75\mu m$. Also, $2h = 2mm$ because the bondwire is typically 1mm above the ground plate. The theoretical total inductance of the wire is plotted against the length of the wire in Fig. 4.2.

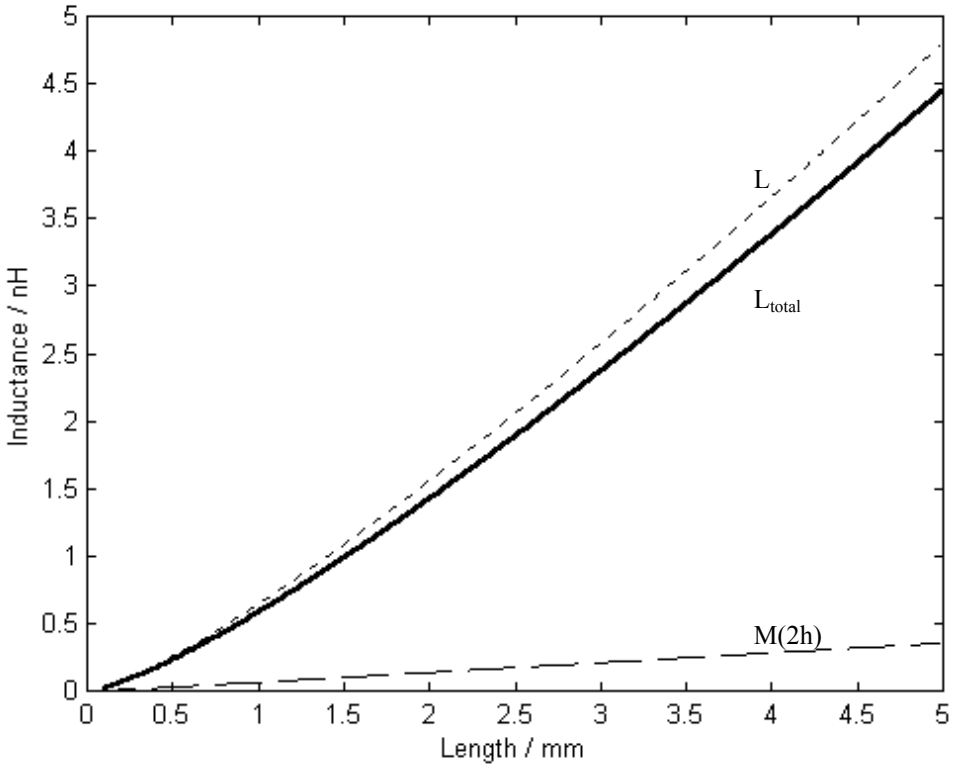


Figure 4.2 Theoretical total inductance (L_{total}) against the length of the wire

Several inductance values will be used in the proposed power amplifier. For example, the RFC of the input stage and the output stage are 2.3nH and 1.6nH respectively. Also, 2nH inductors are used in the output of the power amplifier and the interstage matching. Their corresponding lengths can be found in Fig. 4.2.

The resistance of the bondwire can be estimated using the following equation

$$R_S = \rho \frac{l}{A} \tag{4.5}$$

where l is the length of the wire, A is the effective area of the wire, ρ is the resistivity of the material of the wire. Because of the skin effect [2], the effective area of the wire is reduced from $\pi\left(\frac{d}{2}\right)^2$ to $\pi\left[\left(\frac{d}{2}\right)^2 - \left(\frac{d-2d_s}{2}\right)^2\right]$.

For example, the serial resistance, R_S, of inductance with 2nH can be calculated by equation 4.5 with $l = 2.65\text{mm}$, $\rho = 1.75\times10^{-8}\Omega\text{m}$ and $d = 31.75\mu\text{m}$:

$$R_S(2\text{nH}) = \rho\frac{l}{A} = 1.75\times10^{-8}\frac{2.65\times10^{-3}}{\pi\left[\left(\frac{31.75\mu}{2}\right)^2 - \left(\frac{31.75\mu - 2.718\mu}{2}\right)^2\right]} = 0.357\Omega$$

Therefore, the quality factor of the bondwire inductor with 2nH inductance is:

$$Q = \frac{\omega L}{R_S} = 84.5$$

4.4 Simulation Results of Bondwire Inductance

The analytical equations, however, do not accurately provide information on the quality factor of an inductor. Fortunately, commercial software, HP's ADS, contains a function to simulate the bondwire inductance and the quality factor as long as the physical parameters are provided. For example, the length of the bondwire, the height of the bondwire to the ground plate and conductivity of the material used. Since aluminum bondwire with 1.25-mil diameter will be used, the same parameters, $\rho = 1.75\times10^{-8}\Omega m$, $\mu_r = 1.00002$, $\mu_o = 4\pi\times10^{-7} Hm^{-1}$, 2h = 2mm and $d = 31.75\mu m$, are inputted. The relationships of the length with both the inductance and the quality factor are shown in Fig. 4.3 with the frequency fixed to 2.4GHz.

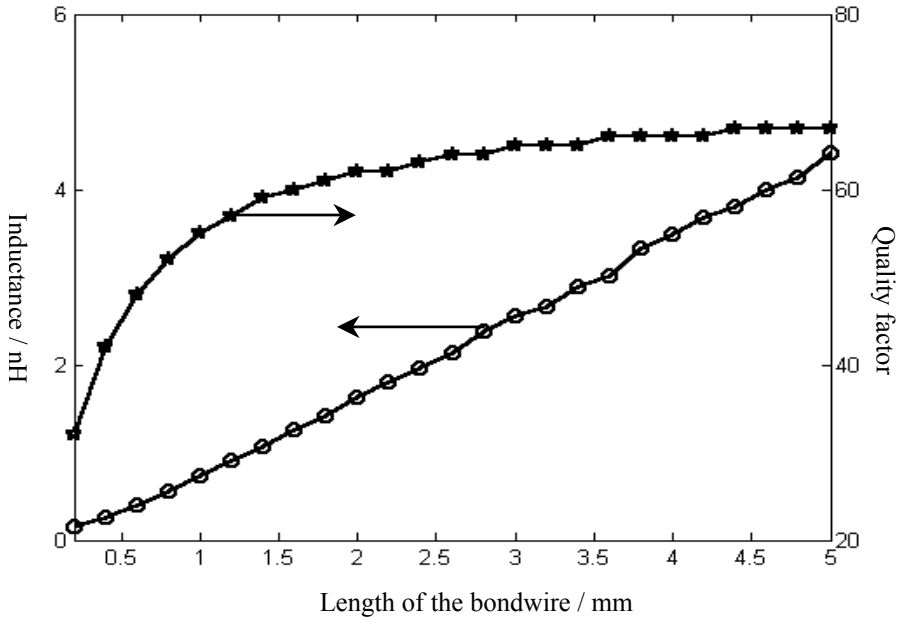


Figure 4.3 Simulated Inductance (asterisk marked) and quality factor (circle marked) against the length of the bondwire

The inductance and the quality factor are found by the Y-parameters [3]. It is observed that the quality factor increases with the length of the bondwire. This is because when the bondwire is longer, the eddy current induced by the ground plate will decrease, which results in smaller losses. The quality factor remains constant when the effect of the ground plate is neglected. From the simulation, the quality factor is at least 30 and can be used in the power amplifier without severely degrading the PAE.

Reference

[1] A. M. Niknejad, R. G. Meyer, "*Design, Simulation and Applications of Inductors and Transformers for Si RFICS*", 2000.

[2] Pieter L. D. Abrie, "*The Design of Impedance-matching Networks for Radio-Frequecny and Microwave Amplifiers*", 1985.

[3] R. L. Bunch, D. I. Sanderson, S. Raman, "Quality Factor and Inductance in Differential IC Implementations," *IEEE Microwave Magazine*, pp. 82-92, June 2002.

CHAPTER 5

LAYOUT CONSIDERATIONS

5.1 Introduction

Due to the enormous current flow in a power amplifier compared to other building blocks, a 100 mV reduction in the output voltage swings will result when there is only 0.2Ω parasitic resistor. Therefore, the layouts of the power amplifier have to be carefully designed so that the performance of the circuit will not be degraded.

In this chapter, some layouts of the components will be detailed. For example, the layouts of the capacitor and the interconnection wire will be discussed. Because bondwire will be used as the inductors, the floorplan and the layout of the overall circuit as well as the PCB will be presented. Finally, the post-simulation results will be given.

5.2 Capacitors Layout

There are numerous approaches used when drawing the layout of capacitors, metal-metal capacitors, polysilicon-polysilicon capacitors and substrate-well capacitors. Among all the layout techniques, the capacitor using polysilicon-polysilicon provides the highest capacitance density. However, some of the process does not offer double polysilicon layers for capacitors realization. Fortunately, the TSMC 0.35-μm process offers double polysilicon layers, so the layout of the capacitors will be drawn using double polysilicon layers.

Two important issues have to be considered for the layout of the capacitors.

First of all, the serial resistance of the capacitors layout should be minimized especially when the capacitor is in the signal path of the circuit. The resistivity of polysilicon is larger compared with the resistivity of metal. The large resistivity of polysilicon contributes the most to the serial resistance of the capacitor. Therefore, the dimension of the polysilicon should be small enough to minimize the serial resistance and large capacitance can be realized using fingers. Also, the interconnection should use metal as the media instead of polysilicon.

Contacts are used to connect the polysilicon to the metal. Since a contact contributes 6.9Ω resistance, many contacts have to be present to minimize the serial

resistance. As a result, the layout of a polysilicon-polysilicon capacitor should be similar to the one shown in Fig. 5.1.

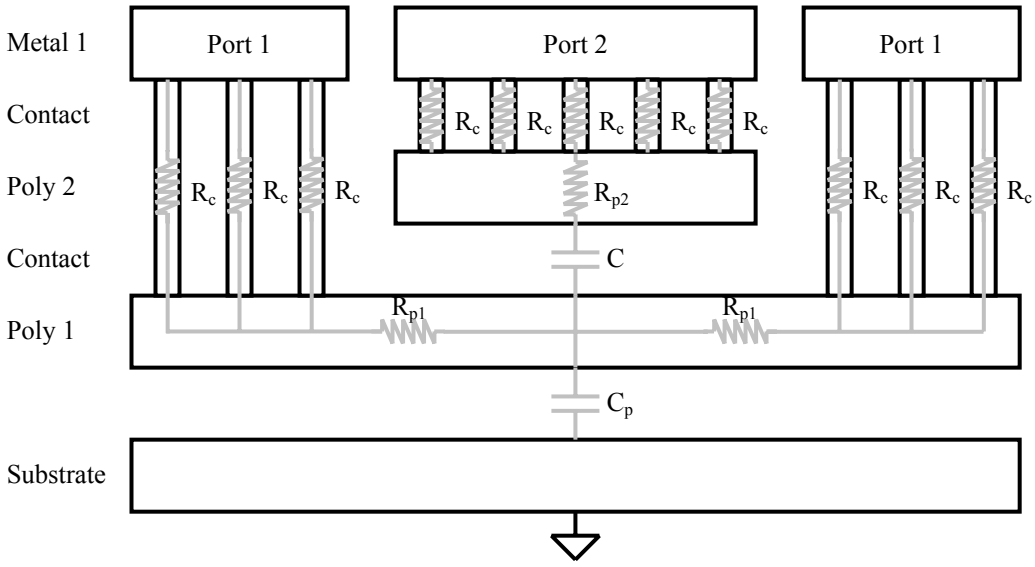


Figure 5.1 Polysilicon-polysilicon capacitor with parasitics

Secondly, the parasitic capacitance introduced by the capacitor itself should be taken into account. A parasitic capacitor (C_p) is formed between the lower polysilicon layer and the substrate. This parasitic capacitor is accompanied with the wanted polysilicon-polysilicon capacitor (C) where C is about 5 times C_p. Therefore, the ports should be assigned carefully depending on the circuit. For example, port 2 should be assigned to a node which is more sensitive to the parasitics while the parasitic should have negligible effect for the node connected to port 1.

Figure 5.2 extracts the part of the schematic of the proposed power amplifier containing the capacitors.

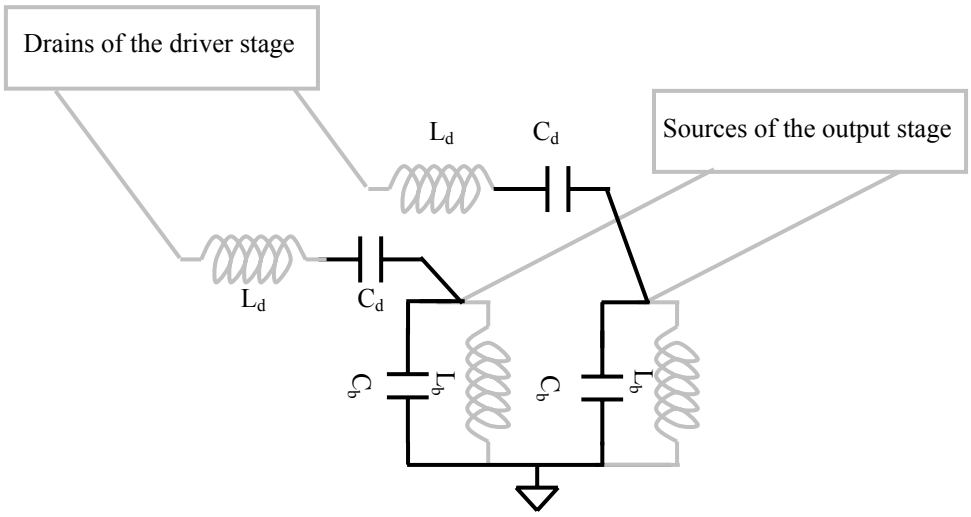


Figure 5.2 Capacitors inside the proposed power amplifier

It is observed that the capacitor C_d can be implemented by the polysilicon-polysilicon capacitor while the parasitic capacitor as discussed is utilized as the capacitor C_b. Therefore, the area of the capacitors layout can be reduced and the parasitic effect can be eliminated.

5.3 Wire Layout

Due to the finite current density of the metal layers, even the simplest component, the interconnecting wire, has to be designed carefully so that the width is large enough to allow a large current to flow without burning the wire.

By rule of thumb, a metal slab with thickness of 1-μm is capable of handling 1mA of current. Since there are approximately 40mA of current flow in the driver stage and 100mA of current drawn from the output stage, the corresponding widths of the

metal are 40μm and 100μm. Although metal 4, which is about 1.4 times thicker than other metal layers, reduces the width to 29μm and 72μm, respectively, these wide metals introduce an undesirably large parasitic capacitor with the substrate. Therefore, two or three metal layers are connected in parallel so as to minimize the parasitic capacitor. In order to eliminate the capacitor formed between the metals, a large number of via are added to reduce the potential difference.

5.4 Floorplan

Figure 5.3 shows the block diagram of the overall layout.

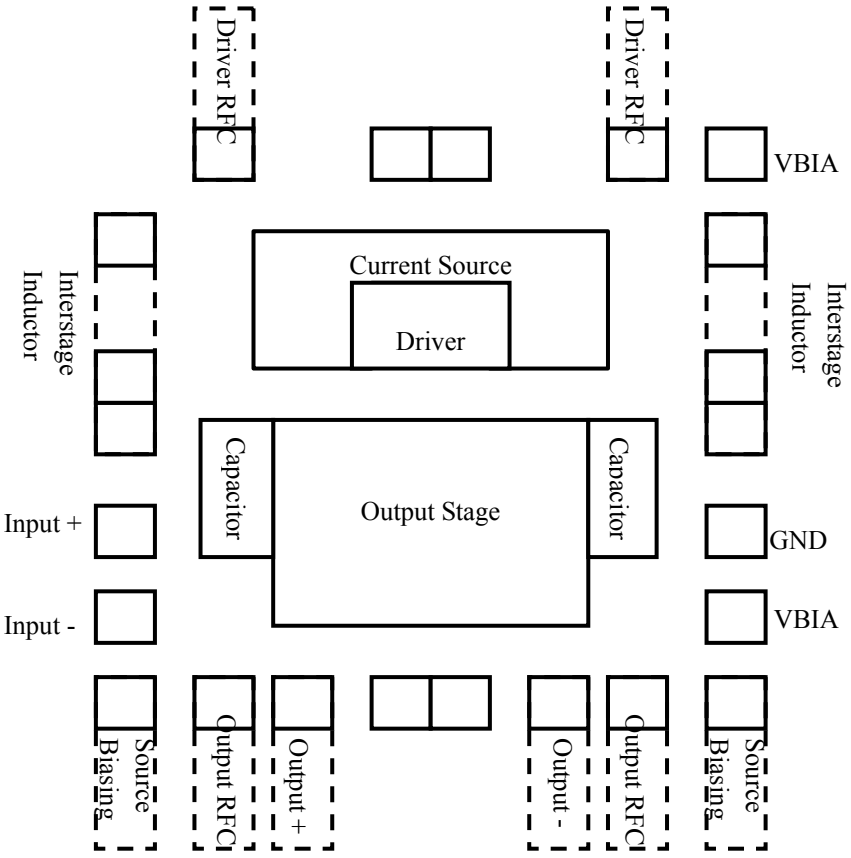


Figure 5.3 Floorplan of the overall circuit

Since all the inductors are realized by bondwires, the layouts of the pads as well as the circuits are placed to facilities bonding of the bondwires.

Figure 5.4 shows the final layout of the proposed power amplifier. The area of the chip is 0.9 x 0.8 mm^2.

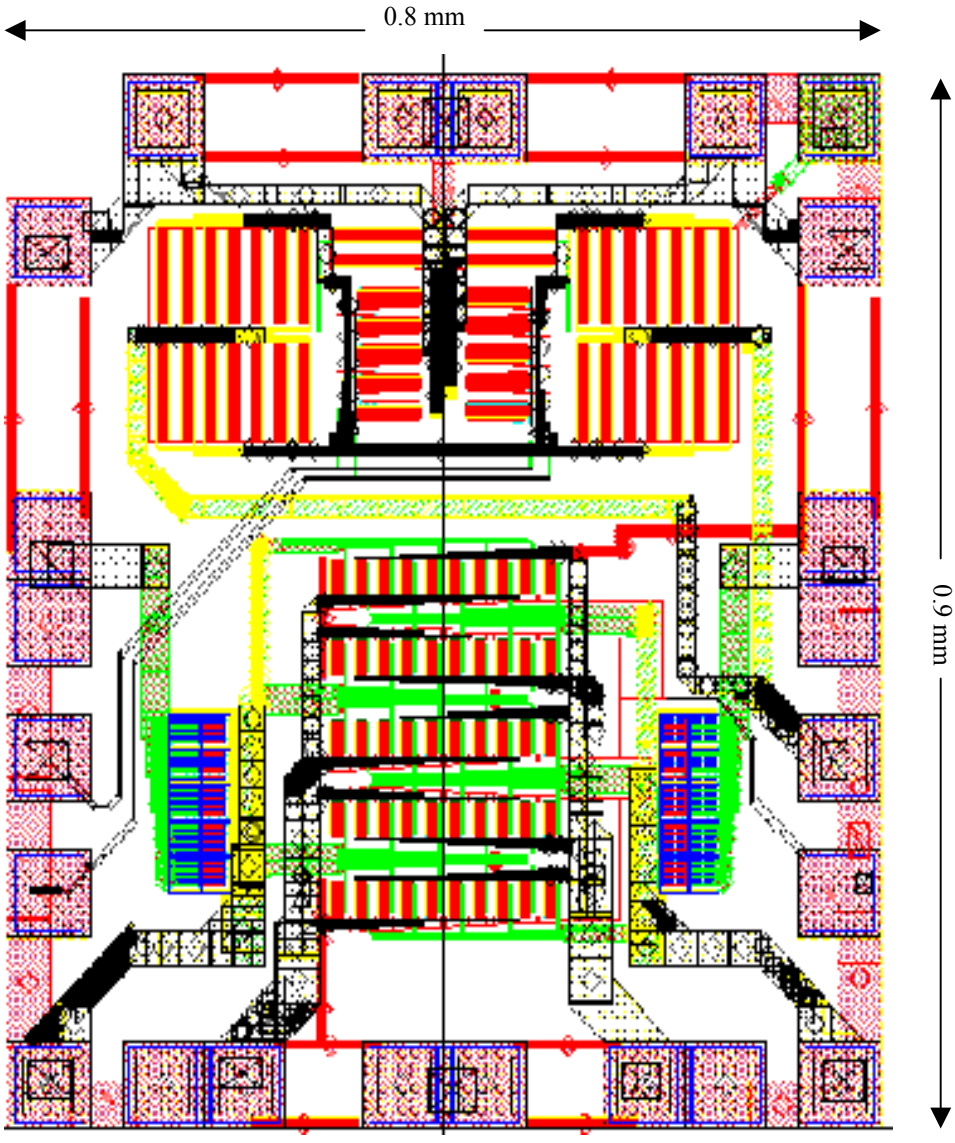


Figure 5.4 Circuit layout of the proposed power amplifier

5.5 Post-Layout Simulation Results

Due to the parasitics introduced by the circuit layout, some of the values of the inductors are reduced to optimize the performance of the overall circuit. The modified inductances are shown in Table 5.1.

Table 5.1 Modified parameters for post-layout simulation

L_1	L_2	L_m	C_m	L_b	C_b	L_d	C_d
0.9nH	2nH	1.8nH	1.5pF	1.2nH	0.8pF	1.8nH	4.5pF

Figure 5.5 shows the waveforms of the drain of the driver stage (V_{di}), the drain of the output stage (V_{do}) and the source of the output stage (V_s).

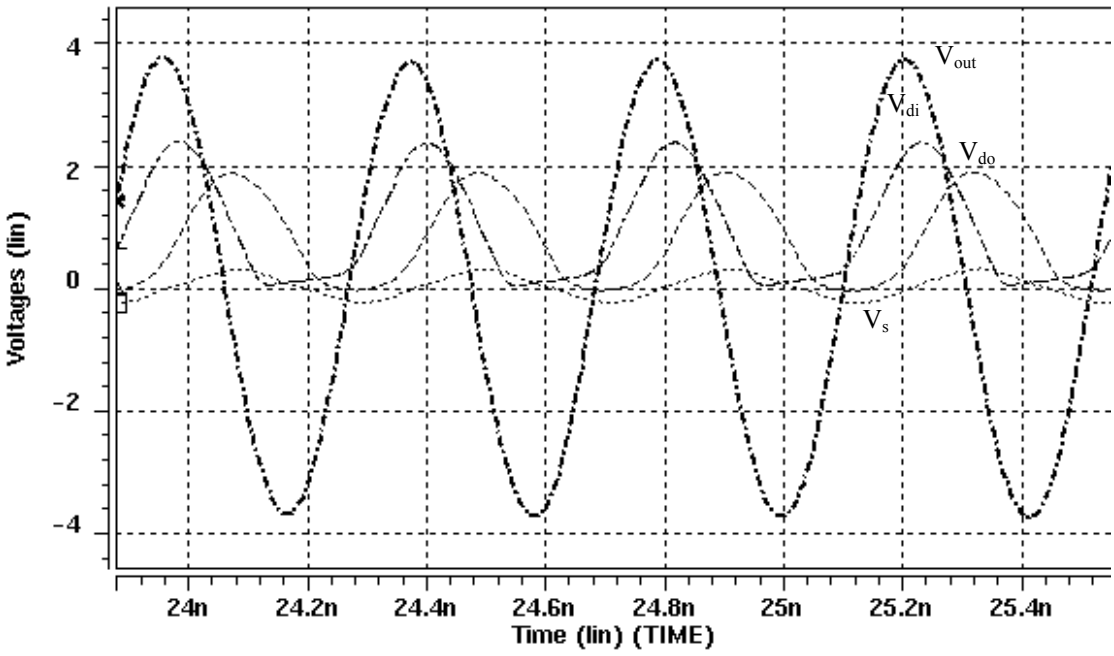


Figure 5.5 Post-simulation on the transient response of the proposed power amplifier

Apart from the changes made to the inductances, the quality factors of the inductors are also included in the post simulation.

Both the calculated result and the pre-simulated result are reprinted for comparison. The performance of the power amplifier is summarized in Table 5.2. The output power is 19dBm with 35% PAE. The degradation of the performance is mainly due to the inclusion of the quality factors of the inductors. All the inductors assume a quality factor of 30.

Table 5.2 Performance of the power amplifier

	Frequency	Supply Voltage	Input Power	Output Power	Power Gain	DE	PAE
Calculated	2.4GHz	1V	-	120mW	17.8dB	100%	-
Pre-sim	2.4GHz	1V	3dBm	116.7mW	17.6dB	65.1%	63.8%
Post-sim	2.4GHz	1V	3dBm	78mW	15.8dB	37%	35%

CHAPTER 6

MEASUREMENT RESULTS

6.1 Introduction

In this chapter, both the testing setups and the measurement results for the bondwire and the power amplifier will be presented. The calibration for bondwire modeling and the inductor model will be detailed. Moreover, the procedure for measuring the power amplifier will be illustrated and the measurement results of the power amplifier will be given out.

6.2 Bondwire Measurement

6.2.1 Testing Setup

Figure 6.1 shows the testing setup for bondwire measurement. The setup is targeted on 1-port measurement of the bondwire inductance. It consists of a SMA connector, a microstrip line with 50Ω characteristic impedance and a 1mm gap for bonding the wire.

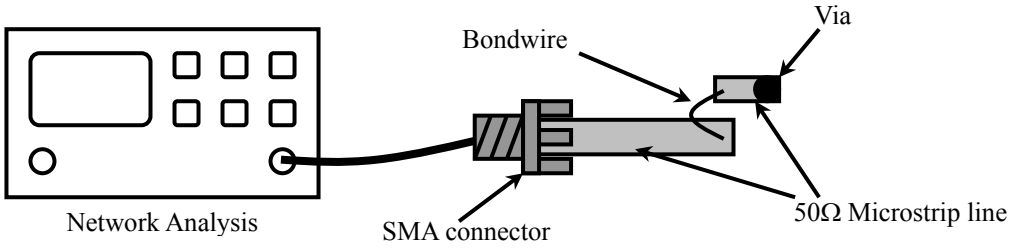


Figure 6.1 Testing setup for bondwire inductance

6.2.2 Measurement Results

Before the bondwire inductance is measured, the effects on SMA connector and the microstrip line should be calibrated out. Figure 6.2 shows the simulation result and the measurement result of the SMA connector and the microstrip line.

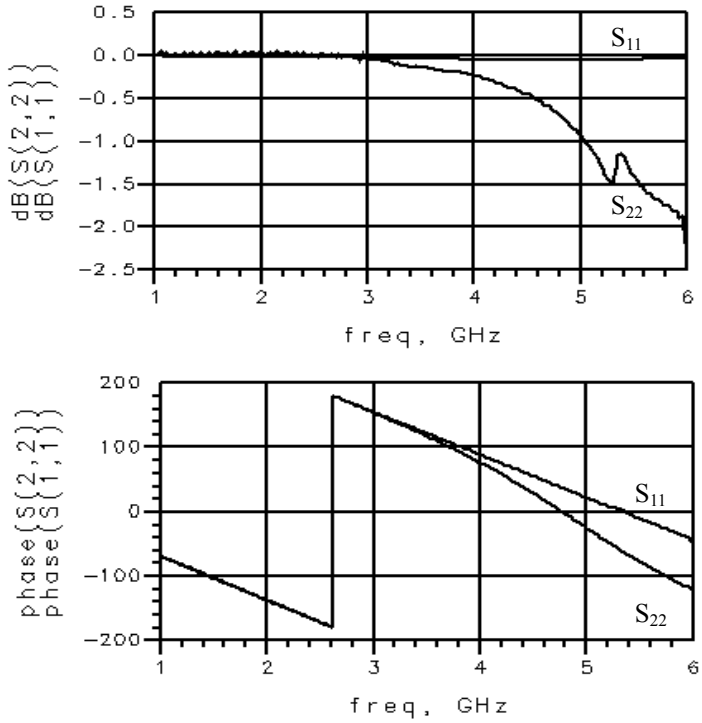


Figure 6.2 Simulated (S_{11}) and measured (S_{22}) S-parameter of open-pad testing setup

The calibration setup of the SMA connector is the same as shown in Fig. 6.1 except that the bondwire is removed. It is observed that the SMA model fit the measurement results from 1GHz to 3GHz and the frequency range for Bluetooth application, 2.4GHz to 2.48GHz, is covered.

A bondwire is bonded across the gap and the setup is then measured again. The model described in chapter 4 is used to fit the measured result. Figure 6.3 shows the simulated (S_{11}) and the measured (S_{22}) S-parameters.

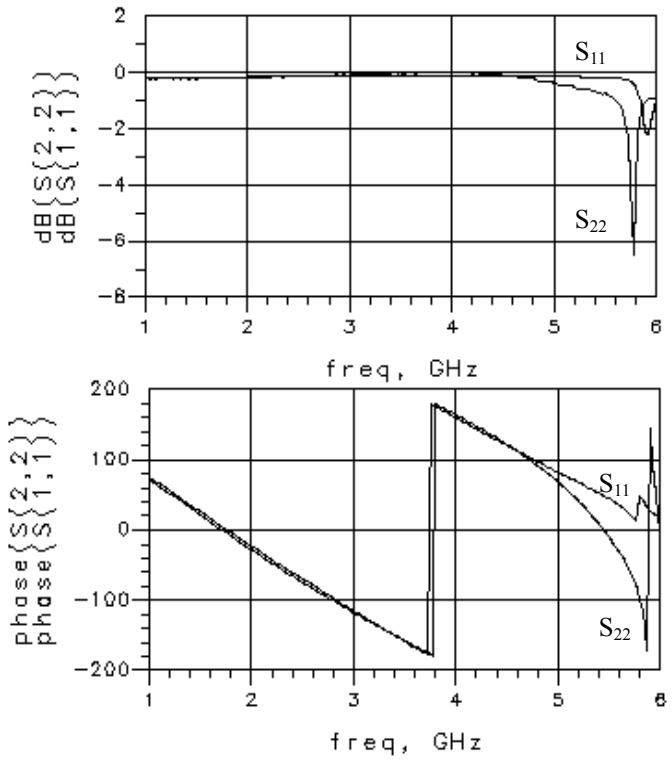


Figure 6.3 Simulated (S_{11}) and measured (S_{22}) S-parameter of bondwire measurement

The simulation results of the overall model, including the SMA connector and the bondwire inductor, also fit the measurement results from 1GHz to 3GHz. By

varying the loop of the bonding machine, the lengths of the bondwire are changed accordingly. Several models are used to fit the measured results with the same procedures described above. Figure 6.4 shows an example of the bondwire models which gives 1.2nH with the quality factor equals 27 at 2.4GHz.

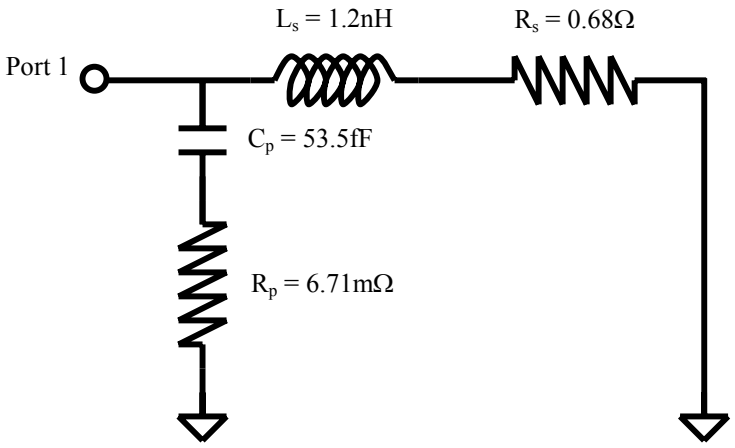


Figure 6.4 A 1.2nH bondwire model

Several inductors with different inductances will be used for the proposed power amplifier. Table 6.1 shows the parameters of the inductors used.

Table 6.1 Parameters for different inductors

	L_s	R_s	C_p	R_p	Q
Biasing Inductor	1.2nH	0.68Ω	53.5fF	6.71mΩ	27
Output RFC	0.97nH	0.54Ω	58.8fF	136mΩ	27
Input RFC Output Matching Interstage Matching	1.94nH	0.47Ω	87.3fF	35mΩ	62

6.3 The Power Amplifier Measurement

6.3.1 Die Photo of the Power Amplifier

Figure 6.5 shows the photograph of the power amplifier fabricated in a 0.35-μm 4M2P standard CMOS process with the threshold voltage of NMOS transistor equals 0.65V (V_{TN} = 0.65V). The chip area, which including bonding pad, is 0.8 mm x 0.9 mm.

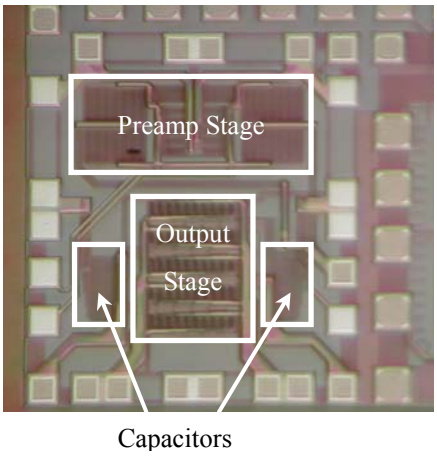


Figure 6.5 Photograph of the chip

6.3.2 Testing Setup

A commercial power splitter, AMPS H-183-4, is used to provide a differential input signal. A commercial power combiner (AMPS H-183-4) is used at the output to convert the differential output to the single-ended output. There are

5.1dB loss associated with the coaxial cables and the splitter. The signal generator used provide functions on generating a GFSK output signal for Bluetooth, so the ACPR can be measured with the same testing setup by changing the generated signal from single-tone sine wave to GFSK modulated signal.

Figure 6.6 shows the testing setup for the proposed power amplifier.

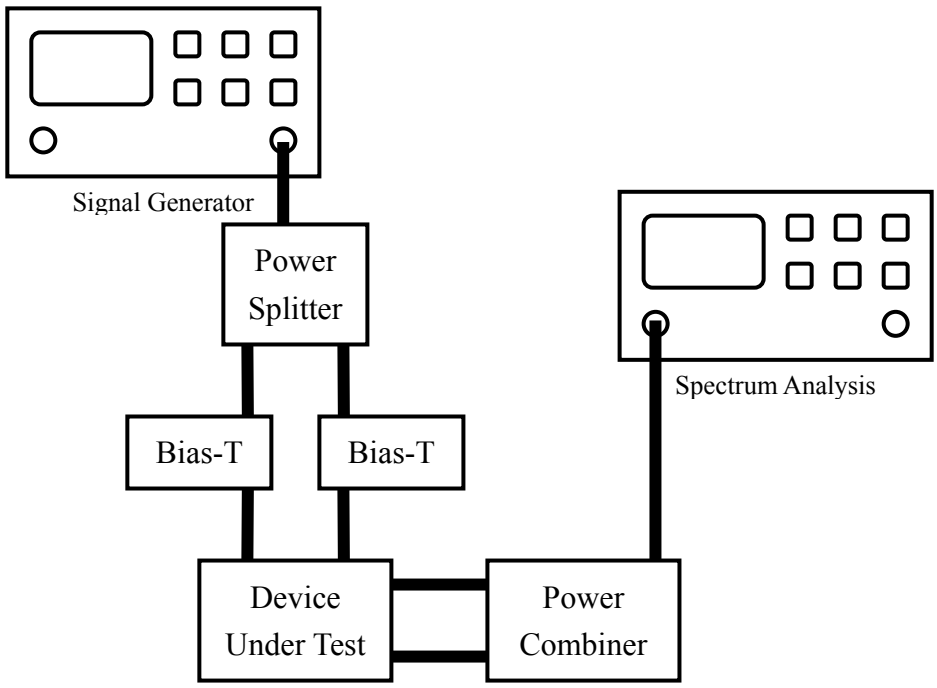


Figure 6.6 Testing setup for the proposed power amplifier

The bare die is directly attached to the PCB ground plate. Due to the unavailable of conductive epoxy, silver paint is used to fix the die to the PCB. All the inductors are realized using 1.25-mil aluminum bondwire. Since the bondwire inductance is highly dependent on the bonding geometry, the PCB is carefully designed to

facilitate wire bonding especially for the interstage inductors. The interstage inductors are implemented by bonding the wire from the die to the PCB and then bonded back from the PCB to the die. Also, since the inductors used in biasing the common-gate switch is directly connected to the ground plate of the PCB, the inductance can be very small.

As the input impedance is not 50Ω, an L-matching network is designed using equations 3.6 and 3.7 to allow maximum power transfer from the signal generator to the input of the power amplifier. The actual input power applied to the power amplifier is measured at the input pad of the bare die using high impedance probe so that the losses associated with the input matching network is calibrated out. Another important issue is the calibration of the high impedance probe. As long as the calibration of the high impedance is accuracy, the power measured provides accuracy information on the input power at the input of the power amplifier. The calibration of the high impedance probe is done by probing an open pad using a high-speed probe, which have a 50Ω impedance and the power is measured by the high impedance probe. Since the power is well defined for the high-speed probe, the power loss associated with the high impedance probe can be calibrated out. The degree of accuracy of the calibration will be dependent on how well the actual input impedance of the power amplifier is matched to the impedance of the calibration set

up, which is the impedance of the open pad in parallel with the impedance of the high-speed probe.

The experimental prototype is shown in Fig. 6.7.

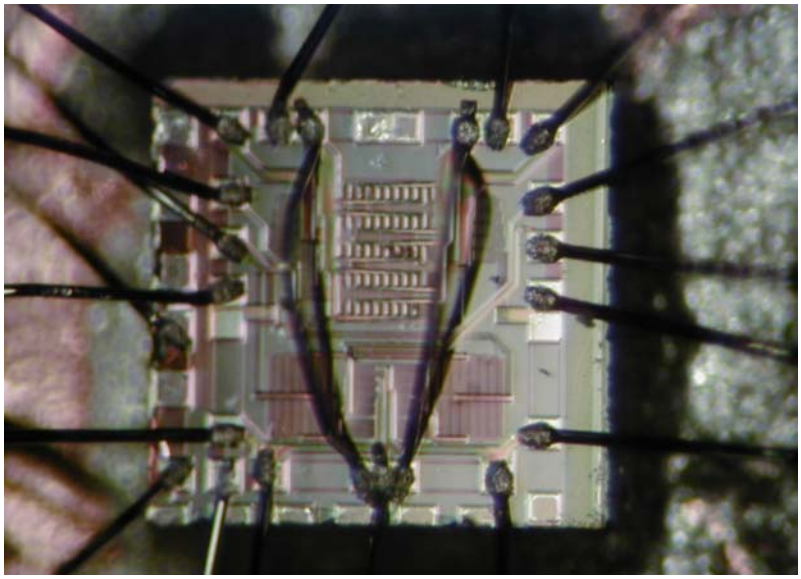


Figure 6.7 Experimental prototype of the power amplifier

6.3.3 Measurement Results

Figure 6.8 shows the measured output power and the measured PAE against the supply voltage.

It is observed that the dependence of the output power is approximately proportional to V_{dd}^2. The simulation results are also presented for comparison. The measured output power shows agreement with the simulated output power. At 1V, the power amplifier delivers 68mW with 33% PAE. When the supply voltage is increased to

1.2V, the PAE raised to 35% with 102mW output power.

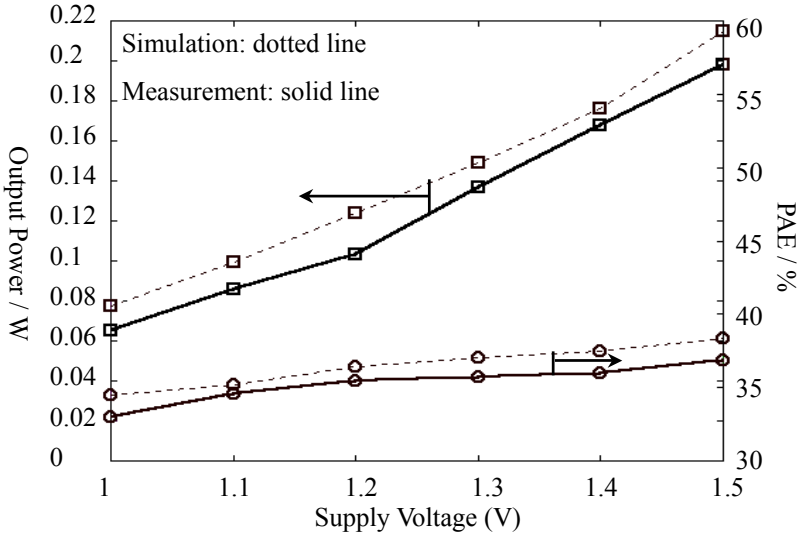


Figure 6.8 Output power and PAE versus supply voltage

Both the simulated results and the measurement results shown that the PAE do not have significant improvement when the supply voltage is increased. It is because the voltage drop across turn-on resistor is neglected when the supply voltage is increased. The effective supply voltage defined in equation 3.9 will approximately equal to the supply voltage. Since the DC biasing currents of the transistors are remaining unchanged when the supply voltage is increased, the total power dissipation and the output power is larger at the same time which resulted in a constant PAE.

Figure 6.9 shows the measured output power and the PAE versus the frequency range of the Bluetooth specification with 1V and 1.2V supply voltage.

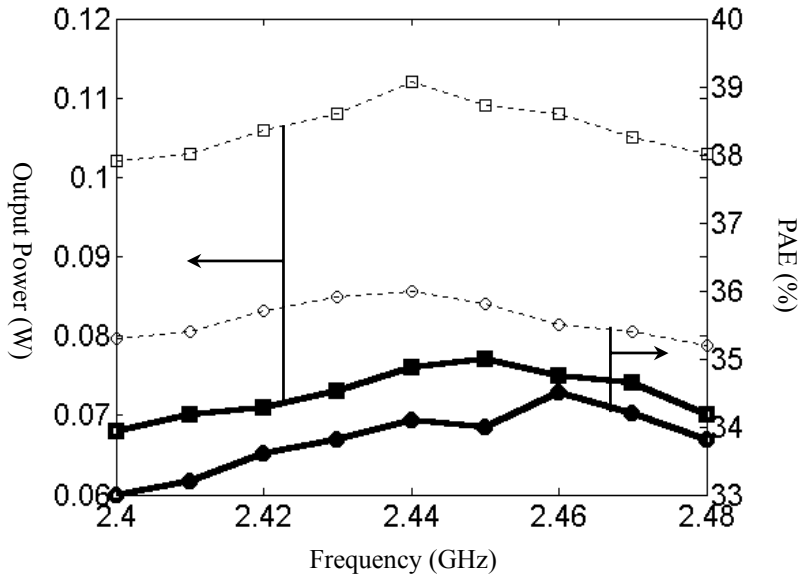
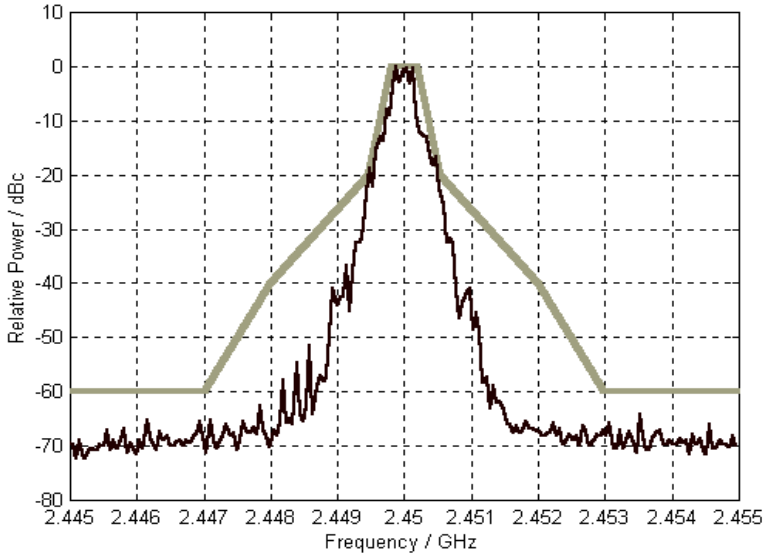


Figure 6.9 Output power and PAE versus frequency with 1V (shown in solid line) and 1.2V supply voltage (shown in dotted line)

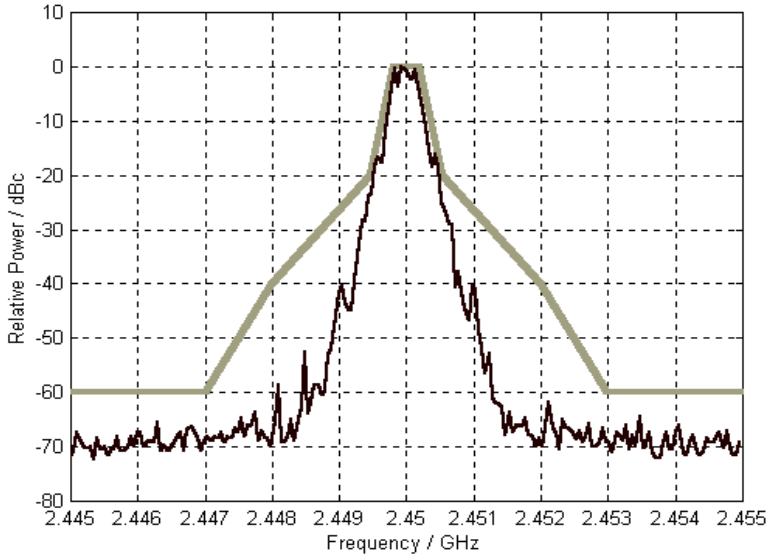
The power amplifier achieves 34.5% PAE and gives 77mW output power at 2.45GHz under 1V supply. The PAE maintain at least 33% over the frequency range from 2.4GHz to 2.48GHz. At 1.2V supply voltage, the amplifier gives 20dBm output power with at least 35% PAE which can be integrated for Class-1 Bluetooth application.

In order to verify the operation with the bluetooth specification, a GFSK modulated signal with BT equals 0.5 is applied to the power amplifier.

Figure 6.10 shows the measured ACPR under 1V and 1.2V supply voltage and the measurements are made using a 100 kHz resolution bandwidth and a 30 kHz video bandwidth.



(a)



(b)

Figure 6.10 The measured ACPR under (a) 1V and (b) 1.2V supply voltage

Both the measured output spectrums of the proposed power amplifier with 1V and 1.2V fall within the spectrum mask of the Bluetooth specifications. For 1V, the ACPR at 550kHz frequency offset is –21.4-dBc while 23.5-dBc is measured for 1.2V supply voltage.

6.4 Performance Summary

Table 6.2 summarizes the performance of the proposed power amplifier. The existing literature of the power amplifier is also shown for comparison. This work is the first power amplifier targeted on 1V supply voltage.

Table 6.2 Summary of performance of the power amplifiers

	[1]	[2]	[3]	This Work	
Process	0.25μm CMOS	0.35μm CMOS	0.25μm CMOS	0.35μm CMOS	
Supply Voltage	1.8V	2V	2.5V	1V	1.2V
Frequency	900MHz	1.9GHz	2.4GHz	2.4GHz	2.4GHz
PAE	41%	48%	48%	33%	35%
Output Power	0.9W	1W	0.23W	77W	120mW
ACPR @ ± 550 kHz	-	-	-	-21.4dBc	-23.5dBc

Reference

[1] C. Yoo and Q. Huang, "A common-gate switch 0.9-W class-E power amplifier with 41% PAE in 0.25μm CMOS". *IEEE J. Solid-State Circuits*, vol. 36, No. 5, pp. 823-830, May 2001.

[2] K. C. Tsai and P. R. Gray, "1.9-GHz 1-W CMOS RF power amplifier for wireless communication". *IEEE J. Solid-State Circuits*, vol. 34, pp. 962-970, July 1999.

[3] Vathulya V. R., Sowlati T. and Leenaerts D. "Class 1 Bluetooth Power Amplifier with 24dBm Output Power and 48% PAE at 2.4GHz in 0.25μm CMOS". *European Solid State Circuits Conference*, Villach, Austria, September 2001.

CHAPTER 7

CONCLUSION

7.1 Conclusion

This thesis attempted to build a low voltage RF power amplifier prototype for Bluetooth applications. Different classes of power amplifiers are reviewed and the design considerations for power amplifiers were investigated.

The power amplifier was implemented in a differential configuration in order to minimize the amount of substrate current injected at the signal frequency. A two-stage power amplifier operated at 2.4GHz with 20.8dBm output power with 1V supply voltage and 63.8% PAE is designed and simulated. The common-gate class E output stage is implemented to compensate the effect on scaling of the supply by proper biasing the common-gate switch. The pre-amplifier stage utilized the positive feedback configuration to drive the low impedance common-gate switch.

One of the most essential components, an inductor, was realized using bonding wire

because of its high quality factor compared with on-chip spiral inductor. The modeling of the bondwire inductor is also done. The quality factor of the bondwire is measured to be at least 26, which is high enough for power amplifier application.

The bare die was assembled on the PCB with all necessary DC supply and the output-matching network of the power amplifier. The PCB was designed to facilitate the wire bonding. The measurement results showed that the power amplifier had achieved 34.5% PAE and gave 77mW output power at 2.45GHz under 1V supply. At 1.2V supply voltage, the amplifier gave 20dBm output power with 35% PAE which can be integrated for Class 1 Bluetooth application.

With the trend of decreasing supply voltage of the whole system, a power amplifier with low operating voltage is desired for realizing a single chip, single supply transceiver. The proposed power amplifier can be integrated with others building blocks to provide a low cost fully CMOS transceiver in the future.

7.2 Potential Improvement

Although the proposed power amplifier can work at supply voltage as low as 1V, the PAE of the power amplifier still have room to be improved. First of all, the margin for the power losses of the power amplifier should be set larger in the design phase so that the output power can be higher at 1V supply voltage. Therefore, the size of

the output stage should be bigger to allow larger current to obtain higher output power. However, there is limitation on increasing the transistor size. Since the parasitics associated with the transistor will also increase when the size of the transistor is larger, the finite DC feed inductance will be too small to be implemented in practice and it is proved that the quality factor of the bondwire inductor will decrease for smaller inductance. Moreover, when the finite DC feed inductance is too small, the feed inductance does not allow constant input current and the voltage swing at the drain of the output stage will decrease. As a result, both the output power and efficiency will be degraded. Once the circuit is fabricated, the only way to have larger output power is to increase the supply voltage which is not desired if a single low supply voltage system is wanted.

Secondly, although bondwires offer quality factor as high as 62, the variation of bondwire inductance is about 10% which will degrade the performance of the power amplifier especially at high frequency operation. The precision of the bondwire inductance is limited by the bonding machine. The situation will be improved if an automatic bonding machine with the function of inductance estimation is available. In fact, the most desired solution is to have a monolithic inductor with high quality factor. However, 0.35μm CMOS process can only provide on chip spiral inductor with highest quality factor of 4 and is not suitable for the power amplifier circuitry.

Moreover, the ratio of the size of the input device to the size of the positive feedback device can be designed to optimize the performance of the proposed power amplifier. To investigate the relationship of the transistor size between the input device and the positive feedback device, the ratio of the transistor size is varied and the details of the simulation is summarized in Table 7.1.

Table 7.1 Summary of the simulation on the ratio of the size of the input device to the positive feedback device

Ratio	W_I	L_I	W_P	L_P	$g_{mI} + g_{mP}$	Output Power	Total Drain Capacitance
0.4	50μm	0.4μm	125μm	0.4μm	189m A/V	0.118mW	1.71pF
0.5	600μm	0.4μm	1200μm	0.4μm	190m A/V	0.121mW	1.72pF
0.6	680μm	0.4μm	1130μm	0.4μm	190.6m A/V	0.120mW	1.72pF

In the simulation, the proposed power amplifier shown in Fig. 3.7 is simulated and the ratio of the size of the input device to the positive feedback device is varied. The output power, the total transconductance and the total drain capacitance of the input stage are kept unchanged to compare the effect of the ratio of the transistor on both the input power and the supply voltage. Since the total transconductance and the total drain capacitance vary with supply voltage, Table 7.1 only shows the condition at 1V supply voltage. The conditions under other supply voltage can be easily found with the given parameters.

Fig. 7.1 shows the plot of the input power of the power amplifier and the supply

voltage against the ratio of the transistor size between the input device and the positive feedback device.

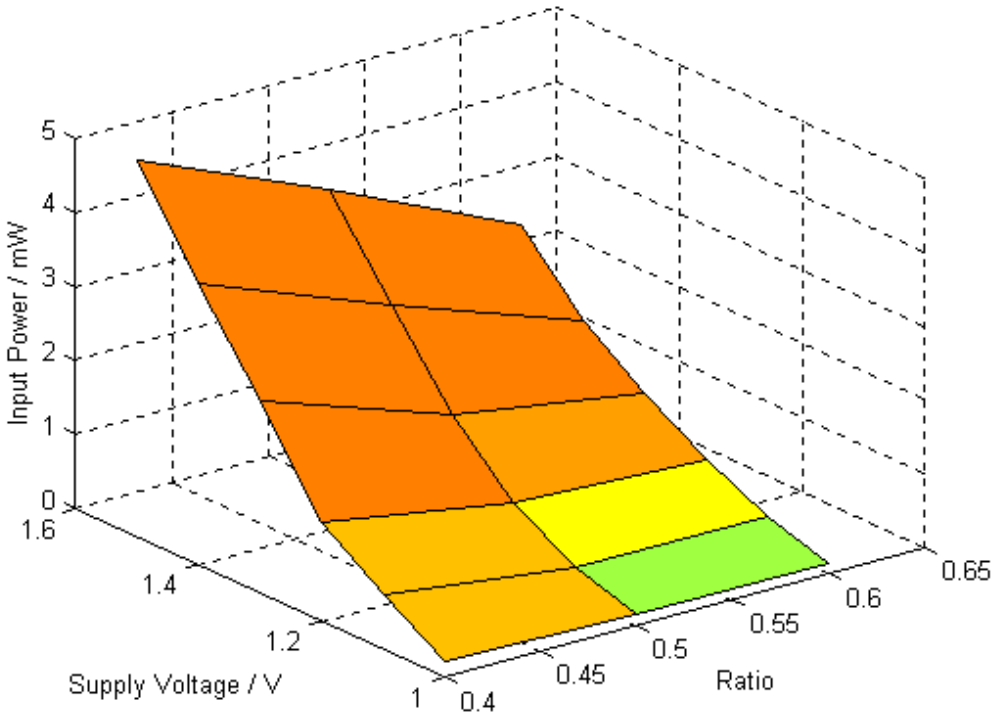


Figure 7.1 Input power and supply voltage against the ratio of the input device size to the size of the positive feedback device

Intuitively, the size of the input device should be smaller so that the previous stage of the power amplifier, such as the up-conversion mixer, can drive the preamp stage of the power amplifier. However, it is observed that the required input power for locking the drain voltage of the input stage have to be larger when the ratio of the input device size to the positive feedback device size is small. It is because the current flow through the input device is not large enough to lock the drain voltage of the input stage. Since the drain voltage of a class-E power amplifier can be as high

as 3.56 x V_{dd}, the input power has to be larger when the supply voltage is increased. As a result, an additional buffer stage has to be added which resulted in larger power dissipation of the whole system. Therefore, the ratio of the size of the input device to the positive feedback device should be chosen to be the same to minimize the driving input power.

With the advance in CMOS process, 0.18μm CMOS process provide options such as thick metal layer to design on chip spiral inductor with quality factor as high as 10. Also, since the feature size of the device is decreased, the finite turn-on and turn-off time becomes smaller and the power losses associated with the transistors is decreased with the same operating frequency. The power amplifier can be fully integrated with trade-off on the performance of the efficiency.

7.3 Future Work

CMOS power amplifier for WLAN application is another potential research topic. However, there are several problems needed to be solved. First of all, the operating frequency for WLAN application is 5GHz, the modeling of bondwire inductor in 5GHz is still absent. The method described in chapter 4 to model the bondwire inductor is not applicable because the SMA model is only applied to frequency up to 3GHz. A novel methodology has to be developed to model the bondwire inductor if

bondwire inductor has to be used. Another approach to realize an inductor is to use on chip inductor. Although 0.18μm CMOS process should be used for frequency as high as 5GHz, the quality factor of CMOS monolithic inductor is still limited to around 10. Moreover, the linearity requirement is –20dBc at 11MHz frequency offset with the signal bandwidth limited to 9MHz frequency offset for the specification of 802.11a. Since the degree of non-linearity of the active device increased with frequency, linear power amplifier has to be used or linearization techniques such as pre-distortion [1], feed-forward [2] and feedback [3] have to be applied to the non-linear power amplifier which resulted in degradation of efficiency performance. Therefore, in order to design a power amplifier for WLAN application with low supply voltage, the linearity has to be traded-off with the efficiency unless some novel circuit technique is developed for high frequency application.

Reference

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[2] Y. Y. Woo, Y. Yang, J. Yi, J. Nam, J. H. Cha, B. Kim, “Feedforward amplifier for WCDMA base stations with a new adaptive control method”. *IEEE MTT-S International Microwave Symposium*, vol. 2, pp. 769-772, 2002.

[3] J. S. Chang, H. G. Bah, S. L. Yong, T. T. Meng, “A novel low-power low-voltage Class D amplifier with feedback for improving THD, power efficiency and gain linearity”. *IEEE International Symposium on Circuits and Systems*, vol. 1, pp. 635-638, 2001.

APPENDIX A

INPUT IMPEDANCE OF THE OUTPUT STAGE

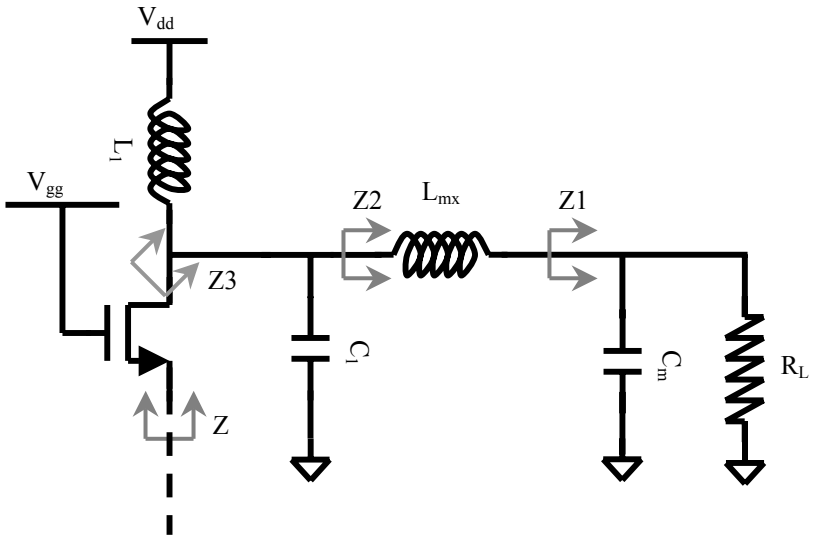

Figure A1 Schematic of the output stage

$$Z1 = X_{C_m} \left\| R_L = \frac{R_L}{1 + j\omega C_m R_L} \right.$$

$$Z2 = X_{L_{mx}} + Z1 = j\omega L_{mx} + \frac{R_L}{1 + j\omega C_m R_L}$$

$$Z2 = \frac{R_L\left(1 - \omega^2 L_{mx} C_m\right) + j\omega L_{mx}}{1 + j\omega C_m R_L}$$

$$Z3 = L_1 \left\| Z2 \right\| C_1 = \frac{j\omega L_1 Z2}{Z2 + j\omega L_1} \left\| C_1 \right.$$

$$Z3 = \frac{j\omega L_1 R_L\left(1-\omega^2 L_{mx}C_m\right)-\omega^2 L_1 L_{mx}}{R_L\left[1-\omega^2\left(L_1+L_{mx}\right)C_m\right]+j\omega\left(L_1+L_{mx}\right)}\Big\| C_1$$

$$Z3 = \left\{\frac{j\omega L_1 R_L\left(1-\omega^2 L_{mx}C_m\right)-\omega^2 L_1 L_{mx}}{R_L\left[1-\omega^2\left(L_1+L_{mx}\right)C_m\right]+j\omega\left(L_1+L_{mx}\right)}+j\omega C_1\right\}^{-1}$$

$$Z3 = \frac{\omega^2 L_{mx}L_1 + j\omega L_1 R_L\left(\omega^2 L_{mx}C_m-1\right)}{R_L\left\{\omega^2\left[L1\left(C_m+C_1\right)+L_{mx}C_m\left(1-\omega^2 L_1 C_1\right)\right]-1\right\}+j\omega\left[L_{mx}\left(\omega_2 L_1 C_1-1\right)-L_1\right]}$$

$$Z = \frac{1}{g_{m1}} + Z3$$

$$Z = \frac{1}{g_{m1}} + \frac{\omega^2 L_1 L_{mx} + j\omega L_1 R_L\left(\omega^2 L_{mx}C_m-1\right)}{R_L\left\{\omega^2\left[L_1\left(C_m+C_p\right)+L_{mx}C_m\left(1-\omega^2 L_1 C_p\right)\right]-1\right\}+j\omega\left[L_{mx}\left(\omega^2 C_p L_1-1\right)-L_1\right]}$$