A 70 MHz CMOS Band-pass Sigma-Delta Analog-to-Digital Converter for Wireless Receivers

A thesis submitted to
The Hong Kong University of Science and Technology
in partial fulfillment of the requirements for
the Degree of Master of Philosophy in
Electrical and Electronic Engineering

by

Hsu Kuan Chun Issac

Department of Electrical and Electronic Engineering

B.Eng. (Hons), HKUST

August 1999

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Approved by:

_____
Dr. Howard Cam Luong
Thesis Supervisor

_____
Dr. Mansun Chan
Thesis Examination Committee Member (Chairman)

_____
Dr. Wing-Hung Ki
Thesis Examination Committee Member

_____
Prof. Philip C.H. Chan
Head of Department

Department of Electrical and Electronic Engineering
The Hong Kong University of Science and Technology

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ABSTRACT

Analog-to-digital converters play an essential role in modern RF receiver design. Conventional Nyquist converters require analog components that are precise and highly immune to noise and interference. In contrast, oversampling converters can be implemented using simple and high-tolerance analog components. Moreover, sampling at high frequency eliminates the need for abrupt cutoffs in the analog anti-aliasing filters. A technique of noise shaping is used in ΣΔ converters in addition to oversampling to achieve a high-resolution conversion. A significant advantage of the method is that analog signals are converted using simple and high-tolerance analog circuits, usually a 1-bit comparator, and analog signal processing circuits having a precision that is usually much less than the resolution of the overall converter.

In this thesis, a technique to design the ΣΔ converters for 70 MHz will be described. Impulse-invariant-transformation is used to transform a discrete-time (z-domain) loop-filter transfer function into continuous-time (s-domain). The continuous-time loop-filter is then implemented using a transconductor-capacitor filter. A latched-type

comparator and a TSPC D Flip-flop are being used as the quantizer of the ΣΔ converter. Two second-order band-pass ΣΔ converters have been implemented in a MOSIS HP 0.8μm CMOS technology and a MOSIS HP 0.5μm CMOS technology respectively.

For the first converter, at supply voltage of 3 V, the maximum signal-to-noise-and-distortion-ratio (SNDR) is measured to be 35.14 dB, which corresponds to a resolution of 5.9 bits, at an input voltage being 0.17 V. The total current supply at 70 MHz is around 10 mA. For the second converter, at both supply voltages of 2.5 V and 3 V, the maximum SNDR is measured to be 42.0 dB, which corresponds to a resolution of 7 bits, at an input voltage being around 0.2V. The total current supply at 70 MHz is 15.5 mA.

Acknowledgements

I would like to take this opportunity to express my sincere gratitude to many individuals who have given me a lot of supports during my two-year master program in the HKUST. Without them, my research would not have been successfully completed on time.

Firstly, I am indebted to my supervisor, Dr. Howard Luong, for his patience, valuable guidance and encouragement throughout the entire research. He has taught me a lot, given me his best support and shown his enthusiasm in helping me to solve technical problems. He has also created an indispensable environment for me to conduct my research work.

I would also like to thank Dr. Yueming Cai, for his technical advice and support in ΣΔ theory. He gave me a chance to know more about the ΣΔ system design and considerations.

I would like to thank Frederick Kwok, Jack Chan, S.F. Luk, Joe Lai and Allen Ng for their important technical supports in measurement setups and CAD tools.

I would also be very grateful to my friends, S.T. Yan, Chi-Wa Lo, David Leung, Vincent Cheung, Toby Kan, Thomas Choi and Ronny Hui, in analog research laboratory. They have shared their fun and experience with me from time to time. I would also like to thank them for their technical discussions.

I would like to thank my parents for their love, support and patience.

Finally, I would like to thank Dr. Mansun Chan and Dr. W.H. Ki for being my thesis examination committee.

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Chapter 1 Introduction

1.1 Analog-to-digital conversion

Data converter is a key component in any electronic system. Real world signals are inherently analog; however, the digital form of analog signals can be processed using robust, flexible and reliable digital-signal-processing (DSP). Therefore, analog-to-digital conversion becomes critical. Data converter is also a very critical component in wireless receivers. Different radio-frequency (RF) receiver architectures have different specifications on their analog-to-digital-converters (ADCs). In Section 1.2, conventional RF receiver architectures will be described. In Section 1.3, proposed architecture using continuous-time band-pass ΣΔ ADC will be discussed. In Section 1.4, the specification of the ADC will be given. Finally, in Section 1.5, the organization of the thesis will be described.

1.2 Conventional RF receiver architectures

There are two RF receiver architectures that are commonly used to implement a wireless receiver: superheterodyne and direct-conversion. The superheterodyne system requires mixers to translate the RF input to a intermediate-frequency (IF). Major amplifications and filtering will be done at the IF stage. Block diagrams of a superheterodyne receiver and a direct-conversion receiver are shown in Figure 1.1 and Figure 1.2 respectively.

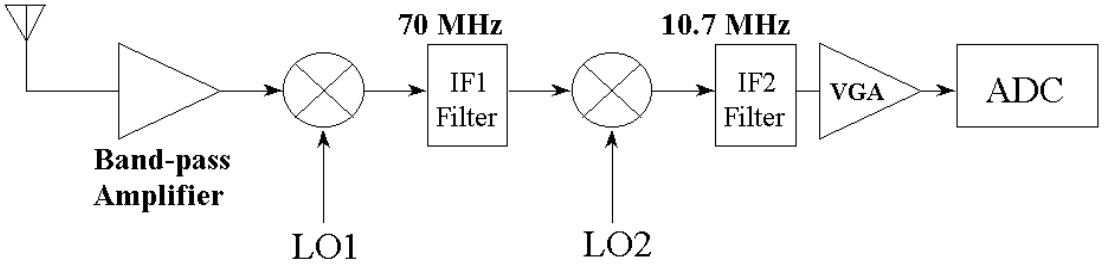


Figure 1.1—Block diagram of a superheterodyne receiver.

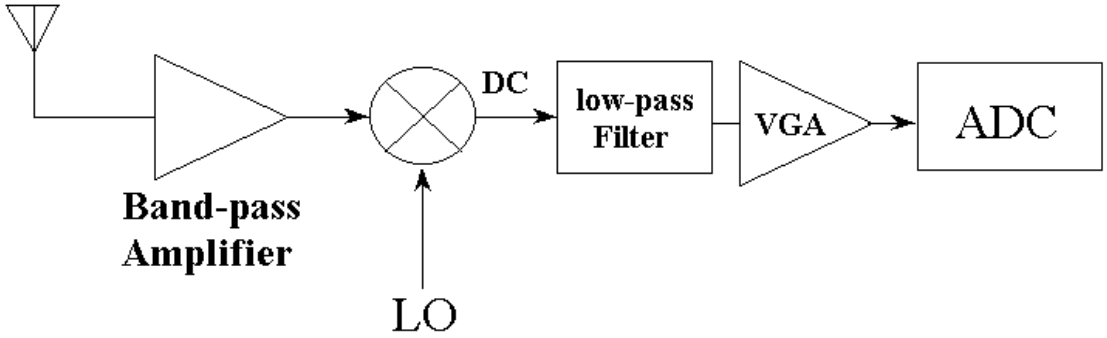


Figure 1.2—Block diagram of direct-conversion receiver.

Superheterodyne receivers down-convert the input signal from RF to two different IFs. It is easier to have the main amplification and filtering of the signal at a lower frequency range. However, it includes two stages of down mixing and two IF band-pass filters and hence increases the power consumption of the system. In contrast, direct-conversion receivers translate the RF signal directly to the baseband in one step (IF=0). The main amplification and filtering of the signal would then be done by a low-pass filter after the mixer. Therefore, direct-conversion receivers consume less power than superheterodyne receivers do. However, this receiver architecture has a severe DC offset problem that will affect the circuit biasing conditions. Therefore, in the next section, a proposed single high-IF receiver architecture will be considered.

1.3 Proposed single high-IF receiver architecture

Figure 1.3 shows the block diagram of the proposed single high-IF receiver architecture.

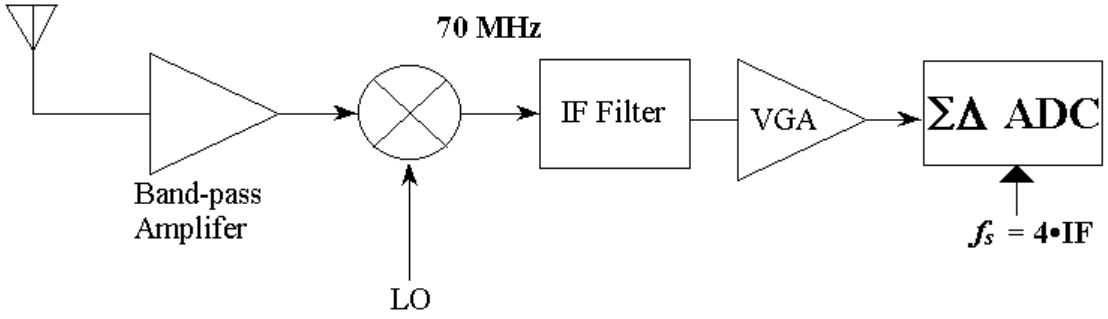


Figure 1.3—Block diagram of the proposed receiver architecture.

The difference between the proposed architecture and the superheterodyne receivers is that the proposed architecture uses only one stage of down mixing and one IF filter instead of two in the superheterodyne system. The power consumption of the proposed architecture will be lower than that of the superheterodyne system. On the other hand, the difference between the proposed architecture and the direct-conversion system is that the proposed architecture uses single high-IF at 70 MHz rather than at DC in the direct-conversion. The advantage of using high-IF is that the image-rejection requirement is not so stringent than using low-IF. Another advantage of using high-IF is that the DC offset problem will not exist as in the case of direct-conversion receivers. However, the ADC used in the proposed architecture as shown in Figure 1.3 must be different from the one used in the conventional systems as discussed in the next section.

1.4 Specification of the ADC

Conventional receiver systems down-convert the input signal from RF to baseband. The required ADC then converts the analog signal into digital code. A Nyquist-rate ADC can perform well enough in converting the baseband signal from the analog form into the digital form. However, as discussed in the last section, the proposed architecture converts the input signal from RF to high-IF at 70 MHz. Since the signal itself is a very narrow-band signal, i.e. with a bandwidth of 200 kHz, it would be wasteful and much more noisier to convert the whole 70 MHz bandwidth into the digital form. The most optimal converter for such a narrow-band signal at 70 MHz with high resolution is a band-pass ΣΔ ADC. For the GSM wireless receiver, the converter should have eight bits of resolution, equivalently 48 dB signal-to-noise-and-distortion-ratio (SNDR) for a 200 kHz bandwidth. For supply voltages from 2.5 V to 3 V, the current supply is desired to be less than 20 mA. Table 1.1 summarizes the target specification of the ΣΔ ADC.

Parameter	Target Specification
Operating frequency	70 MHz (200 kHz bandwidth)
Sampling frequency	280 MHz
SNDR	48 dB (8 bits of resolution)
Maximum total current supply	20 mA

Table 1.1—Target specification of the ΣΔ ADC.

Two continuous-time band-pass ΣΔ ADCs have been designed and tested in this project. The first design is implemented using HP 0.8μm CMOS technology, with zero-delay continuous-time ΣΔ modulator design. Source-degeneration Gm-cells, which will be discussed in Chapter 4, are being used to implement the loop-filter.

However, as the loop delay in the modulator is non-zero and the linearity of the Gm-cells is not good enough, the performance of the ΣΔ modulator is not satisfactory. Therefore, another design that is implemented using HP 0.5μm CMOS technology, with one-delay continuous-time ΣΔ modulator design. Triode-region Gm-cells, which will also be discussed in Chapter 4, are being used to implement the loop-filter. Both simulations and measurements show that the second design has a better performance than the first design has.

1.5 Organization of the thesis

In Chapter 2, the fundamental knowledge of the ΣΔ ADC will be introduced. The discrete-time low-pass ΣΔ ADC, the discrete-time band-pass ΣΔ ADC and the continuous-time band-pass ΣΔ ADC will be described. The method to transform the discrete-time transfer function of the loop-filter into the continuous-time transfer function will also be presented. System level loop-filter design and different system simulations on continuous-time band-pass ΣΔ ADC will then be described in Chapter 3.

As a Gm-C loop-filter is needed, the design and simulation of linear transconductor cells (Gm-cells) is presented in Chapter 4.

In Chapter 5, design and simulation for all the building blocks of the quantizer, including a comparator, a D flip-flop, and a DAC, are described. The integration of the quantizer is discussed.

Finally, in Chapter 6, the ΣΔ ADC prototype will be presented. Circuit level simulations and testing results will be presented. Some future work and a conclusion will be drawn.

Chapter 2 ΣΔ fundamentals

2.1 Introduction [1],[2]

It is often desirable to convert analog signals into the digital domain using an analog-to-digital converter (ADC). In this chapter the main properties of ΣΔ techniques that are useful for converting signals between analog and digital formats are reviewed. ΣΔ modulation has become popular for achieving high resolution. A significant advantage of the method is that analog signals are converted using not only simple and high-tolerance analog circuits but also analog signal processing circuits having a precision that is usually much less than the resolution of the overall converter.

Conventional converters, as illustrated in Figure 2.1, are often difficult to implement in fine-line VLSI technology with reasonably low power consumption. These difficulties arise because conventional methods need analog components that are precise and highly immune to noise and interference. However, the conversion rate of conventional converters is Nyquist rate, i.e. sampling frequency is twice the signal bandwidth. That is why conventional converters are usually referred to as Nyquist converters.

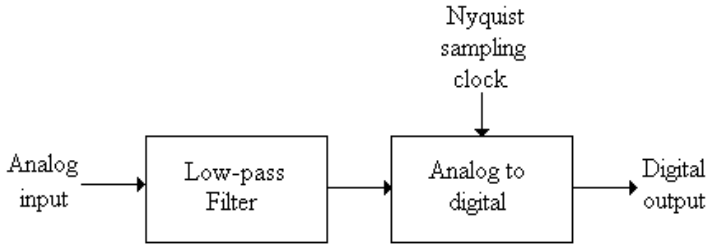


Figure 2.1–Conventional Nyquist-rate ADC blocks [1].

The low-pass filter at the input to the encoder in Figure 2.1 attenuates high-frequency noise and out-of-band signals to prevent them from aliasing into the desired signal when sampled. The analog-to-digital circuit can take a number of different forms such as flash converters for fast operation, successive-approximation converters for moderate rates, and ramp converters for high resolution.

Oversampling converters can use simple and high-tolerance analog components for implementation, but they require fast and complex DSP stages. The use of high-frequency modulation can eliminate the need for abrupt cutoffs in the analog anti-aliasing filters at the input to the ADCs. ΣΔ converters use the technique of noise shaping in addition to oversampling to allow high-resolution conversion of relatively low bandwidth signals.

This chapter is organized into five main sections. In Section 2.2, some basic properties of the quantization noise are described. General oversampling ADC and ΣΔ modulator will be described in Section 2.3. Discrete-time low-pass ΣΔ modulation as a technique for shaping the spectrum of quantization noise is introduced in Section 2.4. In Section 2.5 discrete-time band-pass ΣΔ modulation is explained, and in Section 2.6, the continuous-time design and implementation of band-pass ΣΔ modulator are described.

2.2 Quantization noise [1],[2]

Quantization in amplitude and sampling in time are the two main functions of all digital modulators. Once sampled, the signal samples must also be quantized in amplitude to a finite set of output values. The typical transfer characteristic of

quantizers or ADCs with an input signal sample *x* and an output *y* is shown in Figure 2.2.

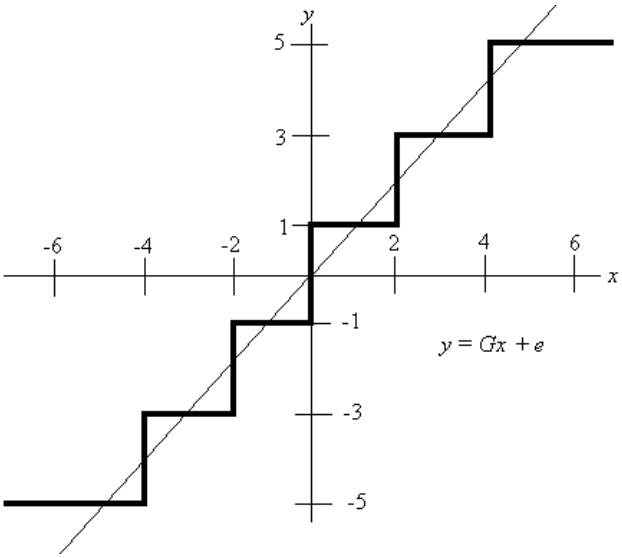


Figure 2.2–An example of a uniform multilevel quantization characteristic that is represented by linear gain G and an error e [1].

The quantizer, embedded in any ADC is a non-linear system, is difficult to analyze. To make the analysis tractable, it is useful to represent the quantized signal *y[n]* by a linear function *Gx[n]* with an error *e[n]*: that is, *y[n]=Gx[n]+e[n]*. The gain *G* is the slope of the straight line passing through the center of the quantization characteristic. In Figure 2.2, the level spacing Δ is 2. So, the quantizer does not get saturated when $-6 \le x[n] \le 6$ and the error is bounded by $\pm\Delta/2$. This consideration remains applicable to a two-level (single-bit) quantizer but, in this case, the choice of gain *G* is arbitrary.

To further simplify the analysis of the noise from the quantizer, the following assumptions about the noise process and its statistics are traditionally made [3]:

1. The error sequence e[n] is a sample sequence of a stationary random process,
2. The error sequence is uncorrelated with the sequence x[n],

3. The random variables of the error process are uncorrelated; i.e. the error is a white-noise process,
4. The probability distribution of the error process is uniform over the range of quantization error.

For a zero mean *e[n]*, its variance σ_e^2 or power is:

$$\sigma_e^2 = \frac{1}{\Delta}\int_{-\frac{\Delta}{2}}^{\frac{\Delta}{2}} e^2 de = \frac{\Delta^2}{12} \qquad (2.1)$$

When a quantized signal is sampled at frequency f_s=1/T, all of its power folds into the frequency band $0 \le f < f_s$. Then, if the quantization noise is white, the spectral density of the sampled noise is given by:

$$E(f) = \sqrt{\frac{\sigma_e^2}{f_s/2}} = \sigma_e\sqrt{\frac{2}{f_s}} \qquad (2.2)$$

We can use this result to analyze oversampling modulators. Consider a signal lying in the frequency band $0 \le f \le f_B$. The oversampling ratio (OSR), defined as the ratio of the sampling frequency f_s to the Nyquist frequency $2f_B$, is given by the integer:

$$OSR = \frac{f_s}{2f_B} \qquad (2.3)$$

Hence, the in-band quantization noise will be given by:

$$n_o^2 = \int_0^{f_B} E^2(f)df = \sigma_e^2 \cdot \frac{2f_B}{f_s} = \frac{\sigma_e^2}{OSR} \qquad (2.4)$$

Thus, we have the well-known result that oversampling reduces the in-band quantization noise from ordinary quantization by the square root of the oversampling ratio. Therefore, each doubling of the sampling frequency decreases the in-band noise by 3 dB and thus increases the resolution by half a bit.

Figure 2.3 shows the power spectral density, *E(f)*, of the quantization noise for Nyquist rate sampling with rate f_{s1} and oversampling rate f_{s2}. For Nyquist rate sampling where the signal band, $f_B=f_{s1}/2$, all the quantization noise power, represented by the area of the tall shaded rectangle, occurs across the signal bandwidth. In the oversampled case, the same noise power, represented by the area of the unshaded rectangle has been spread over a bandwidth equal to the sampling frequency, f_{s2}, which is much greater than the signal bandwidth, f_B. Only a relatively small fraction of the total noise power falls in the band $[-f_B,f_B]$, and the noise power outside the signal band can be greatly attenuated with a digital low-pass filter following the ADC.

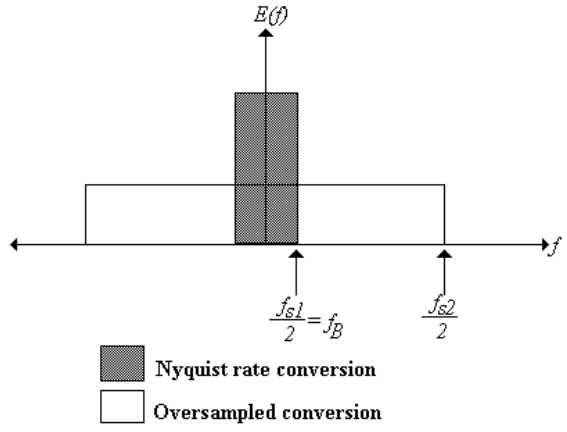


Figure 2.3–Quantization noise power spectral density for Nyquist rate and oversampled conversion [2].

2.3 Oversampling ADC and ΣΔ modulator [1],[2]

A general way of writing the discrete-time domain output of an ADC is given as $Y(z)=X(z)H_x(z)+E(z)H_e(z)$, where H_x is the signal transfer function (STF) and H_e is

the noise transfer function (NTF). For oversampled conversion, we have $H_x(z)=H_e(z)=1$. In fact, oversampled ADCs can be designed to incorporate noise shaping, where H_x usually leaves the signal undisturbed but H_e shapes the noise to allow a high resolution output. Oversampling reduces the quantization noise power in the signal band by spreading the fixed quantization noise power over a bandwidth much larger than the signal band as discussed in the last section. Noise shaping further attenuates this noise in the signal band and amplifies it outside the signal band. Consequently, this process of noise shaping by the ΣΔ modulator can be viewed as pushing quantization noise power from the signal band to higher frequencies. The modulator output could then be filtered to attenuate the out-of-band quantization noise.

A block diagram of a ΣΔ modulator is shown in Figure 2.4. The modulator consists of a loop-filter that has a transfer function *H(z)*, a quantizer and a digital-to-analog converter (DAC) in the feedback path. The quantizer can be linearized and modelled as an additive error as shown in Figure 2.5.

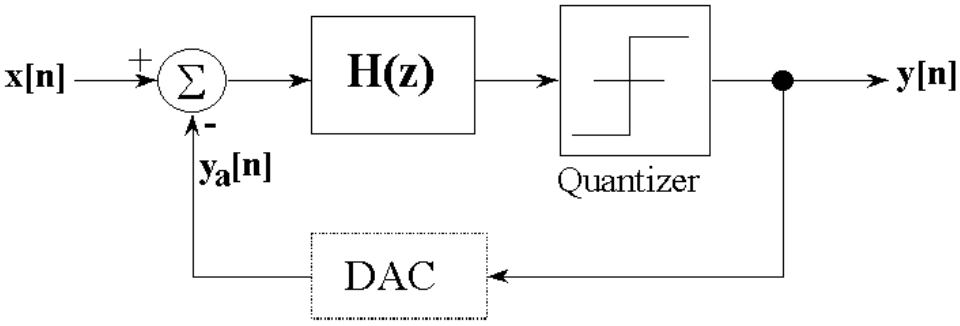
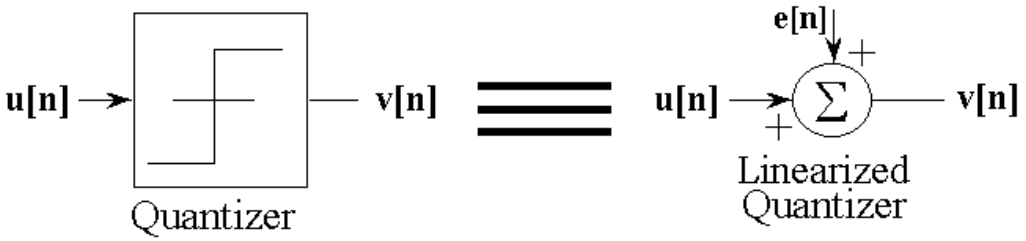


Figure 2.4—Block diagram of a ΣΔ modulator.



$$v[n] = u[n] + e[n]$$

Figure 2.5—Linearized model of the quantizer.

2.4 Discrete-Time Low-pass ΣΔ modulation [1],[2]

A block diagram of a first-order ΣΔ modulator is shown in Figure 2.6 and a linearized version of the block diagram is shown in Figure 2.7.

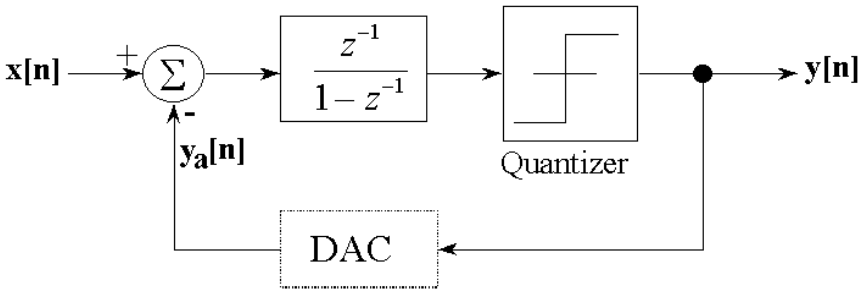


Figure 2.6–Block diagram of a first-order ΣΔ modulator.

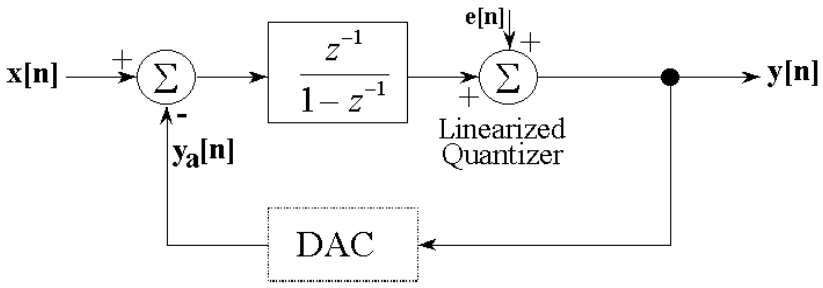


Figure 2.7—Linearized model block diagram of a first-order ΣΔ modulator.

The signal that is being quantized is a filtered version of the difference between the input *x[n]* and an analog representation, $y_a[n]$, of the quantized output,

y[n]. The loop-filter is a discrete-time integrator whose transfer function is $H(z) = z^{-1}/(1-z^{-1})$. If the DAC is ideal, it is replaced by a unity gain transfer function. The modulator output $Y(z)$ in the frequency domain is then given by:

$$Y(z) = X(z) \cdot z^{-1} + E(z) \cdot (1 - z^{-1}) \qquad (2.5)$$

so that the STF $H_x(z)$ is z^{-1} and the NTF $H_e(z)$ is $1-z^{-1}$. The output is just a delayed version of the signal plus a quantization noise shaped by a first-order differentiator (or high-pass filter). Note that a zero gain is provided by the NTF at DC frequency. The magnitude spectrum of a first-order ΣΔ noise transfer function (NTF) is plotted in Figure 2.8. The frequency axis has been normalized with respect to the sampling frequency, f_s.

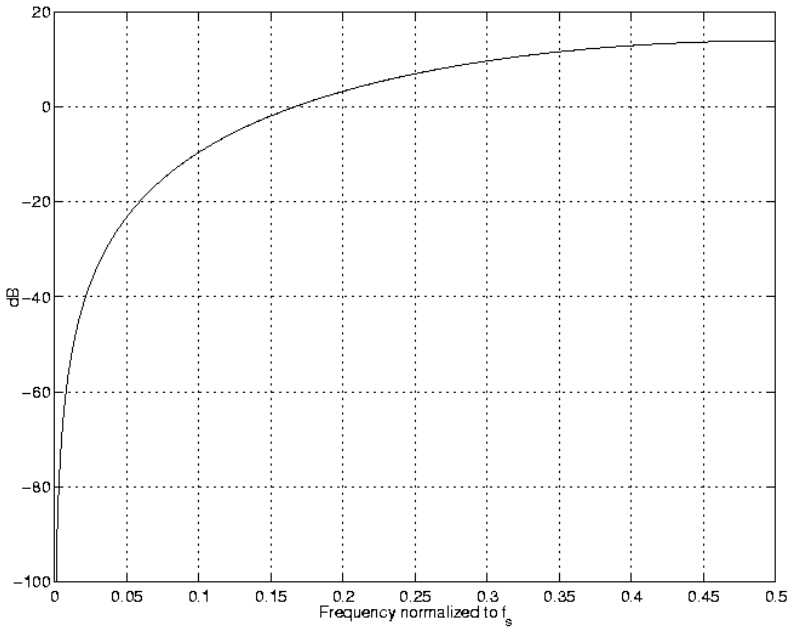


Figure 2.8–First-order Noise Transfer Function (NTF) magnitude spectrum in dB.

The in-band quantization noise after the noise-shaping will be given by:

$$
\begin{aligned}
n_o^{\,2} &= \int_0^{f_B} E^2(f)\cdot\left|1-z^{-1}\right|^2 df \\
&= \int_0^{f_B} \frac{\sigma_e^{\,2}}{f_s/2}\cdot\left|1-z^{-1}\right|^2 df \\
&= \frac{2\sigma_e^{\,2}}{f_s}\cdot\int_0^{f_B}(2-2\cos\frac{2\pi f}{f_s})df \\
&= \frac{4\sigma_e^{\,2}}{f_s}\cdot\int_0^{f_B} 2\sin\frac{\pi f}{f_s}df \\
&\approx \frac{8\sigma_e^{\,2}}{f_s}\cdot\int_0^{f_B}(\frac{\pi f}{f_s})^2 df \qquad (f_B << f_s) \\
&= \frac{\sigma_e^{\,2}\cdot\pi^2}{3}\cdot(\frac{2f_B}{f_s})^3 \\
&= \frac{\sigma_e^{\,2}\cdot\pi^2}{3}\cdot(\frac{1}{OSR})^3
\end{aligned}
\qquad (2.6)
$$

Therefore, each doubling of the sampling frequency decreases the in-band noise by 9 dB and, thus, increases the resolution by one and a half bits. Figure 2.9 shows the quantization noise spectrum before and after noise shaping.

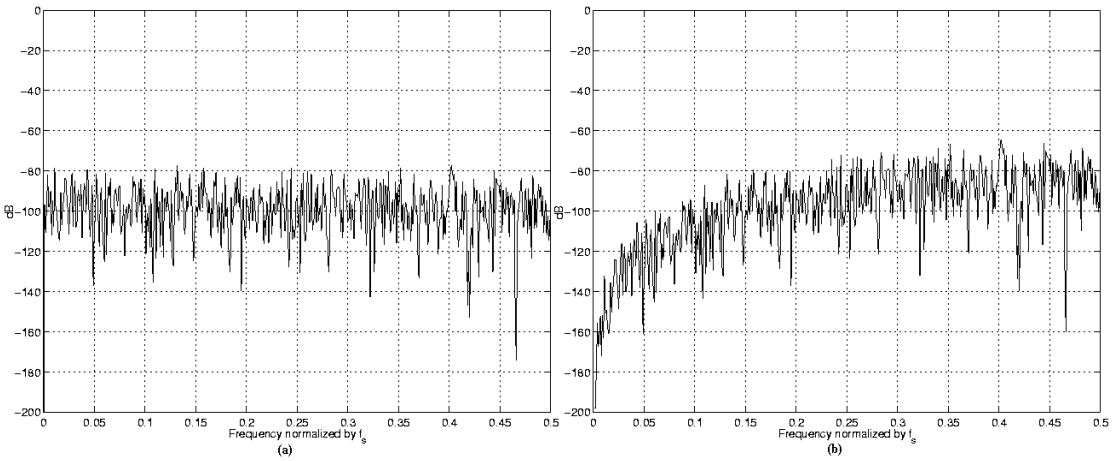


Figure 2.9–Quantization Noise Spectrum. (a) Before first-order low-pass ΣΔ noise-shaping, (b) After first-order low-pass ΣΔ noise-shaping.

2.5 Discrete-Time Band-pass ΣΔ modulation [1],[2]

We have assumed that the sampling frequency, f_s, is much greater than the Nyquist rate. For low-pass signals, the highest frequency component is the signal bandwidth f_B. If a signal with a very narrow bandwidth f_B is located at a center frequency f_c, its highest frequency component is then $f_c+f_B/2$. If f_c is large, choosing a f_s much greater than the highest frequency would lead to an unreasonably large f_s. Band-pass ΣΔ modulation [4] allows high-resolution conversion of band-pass signals if f_s is much greater than the signal bandwidth f_B, rather than the highest signal frequency.

Unlike low-pass ΣΔ modulators that realize NTF zeros at DC or low frequencies on the unit circuit of the Z plane, band-pass modulators have NTFs that realize zeros or notches at the center frequency, f_c, in the signal band of interest, [f_c-$f_B/2$, $f_c+f_B/2$]. Consequently, quantization noise that occurs over the signal band is attenuated, and noise power is pushed outside this band. No matter where the signal band is centered, the smaller the signal bandwidth relative to the sampling frequency, there is less in-band noise power for a given NTF. Noise outside the signal band can then be attenuated with a digital decimation filter and, so, high-resolution conversion is possible for large oversampling ratio $f_s/2f_B$.

Band-pass ΣΔ modulators operate in much the same manner as low-pass ΣΔ modulators. A band-pass ΣΔ modulator can be constructed by connecting a filter and quantizer in a loop, as shown in Figure 2.10.

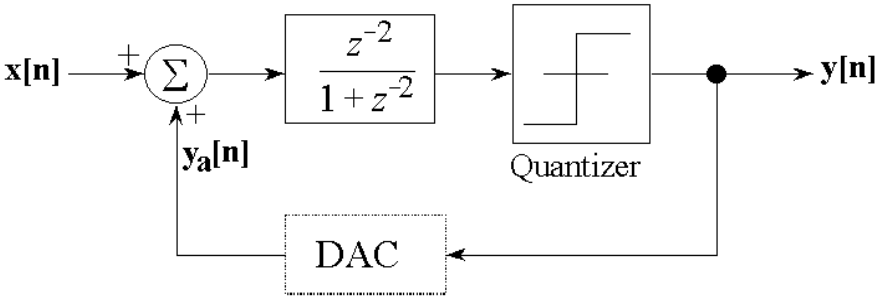


Figure 2.10–Block Diagram of a second-order band-pass ΣΔ modulator.

The filter is a discrete-time resonator whose transfer function is $H(z) = z^{-2}/(1+z^{-2})$. If the DAC is ideal, it is replaced by a unity gain transfer function. The modulator output $Y(z)$ in the frequency domain is then given by:

$$Y(z) = X(z) \cdot z^{-2} + E(z) \cdot (1 + z^{-2}) \qquad (2.7)$$

so that the STF $H_x(z)$ is z^{-2}, which again is simply a delayed versoin of input, and the NTF $H_e(z)$ is $1+z^{-2}$, which is the quantization noise shaped by a band-notched filter.

Most of the designs for band-pass modulators can be derived in a similar way as the designs for low-pass modulators. For instance, applying the transformation $z \rightarrow -z^2$ to a low-pass modulator, the zeros of $H_e(z)$ would be mapped from DC to $\pm\pi/2$. This transformation places the center frequency at $\omega_o=\pi/2$, and thus for a fixed center frequency, the sampling frequency is dictated by the relation $f_s=4f_c$. Also, since this transformation preserves the oversampling ratio, the oversampling ratio of the modulator is again determined by the signal parameters: $OSR=f_s/2f_B$. Figure 2.11 shows a contrast between the pole-zero placements of $H_e(z)$ for a first-order low-pass modulator and a second-order band-pass modulator. The NTF, $H_e(z)$, for the first-order low-pass modulator is $1-z^{-1}$, and $H_e(z)$ for the second-order band-pass modulator using the $z \rightarrow -z^2$ transformation is $1+z^{-2}$.

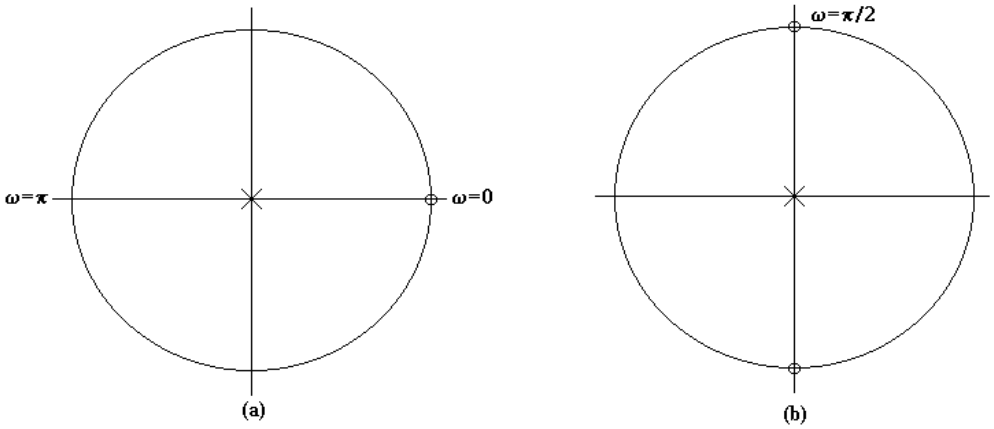


Figure 2.11–The pole/zero locations for (a) low-pass and (b) band-pass ΣΔ modulator.

The band-pass modulator derived from the transformation is stable if and only if the low-pass modulator is stable and the SNDR of the modulators are identical. The magnitude spectrum of a second-order band-pass ΣΔ NTF is plotted in Figure 2.12. The frequency axis has been normalized with respect to the sampling frequency, f_s.

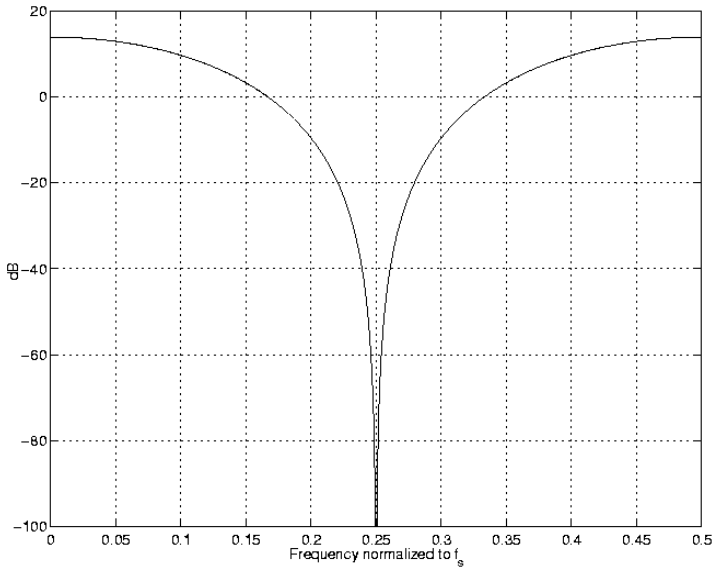


Figure 2.12–Second-order band-pass NTF magnitude spectrum in dB.

The in-band quantization noise after the noise-shaping will be given by:

$$
\begin{aligned}
n_o^2 &= \int_{f_c-f_B/2}^{f_c+f_B/2} E^2(f)\cdot\left|1+z^{-2}\right|^2 df \\
&= \int_{f_c-f_B/2}^{f_c+f_B/2} \frac{\sigma_e^2}{f_s/2}\cdot\left|1+z^{-2}\right|^2 df \\
&= \frac{2\sigma_e^2}{f_s}\cdot\int_{f_c-f_B/2}^{f_c+f_B/2}(2+2\cos\frac{4\pi f}{f_s})df \\
&= \frac{4\sigma_e^2}{f_s}\cdot(f+\frac{f_s}{4\pi}\sin\frac{4\pi f}{f_s})\Big|_{f_c-f_B/2}^{f_c+f_B/2} \\
&= \frac{4\sigma_e^2}{f_s}\cdot\{f_B+\frac{f_s}{4\pi}[2\cos\frac{4\pi f_c}{f_s}\sin\frac{4\pi f_B}{2f_s}]\} \\
&= \frac{4\sigma_e^2}{f_s}\cdot\frac{f_s}{4\pi}\cdot[\frac{4\pi f_B}{f_s}-2\sin\frac{2\pi f_B}{f_s}] \qquad (f_c=\frac{f_s}{4}) \\
&= \frac{8\sigma_e^2}{4\pi}\cdot[\frac{2\pi f_B}{f_s}-\frac{2\pi f_B}{f_s}+\frac{1}{3!}\cdot(\frac{2\pi f_B}{f_s})^3-...] \\
&\approx \frac{\sigma_e^2\cdot\pi^2}{3}\cdot(\frac{1}{OSR})^3
\end{aligned}
\qquad (2.8)
$$

Therefore, each doubling of the sampling frequency decreases the in-band noise by 9 dB and, thus, increases the resolution by one and a half bits. Figure 2.13 shows the quantization noise spectrum before and after the second-order band-pass ΣΔ noise shaping.

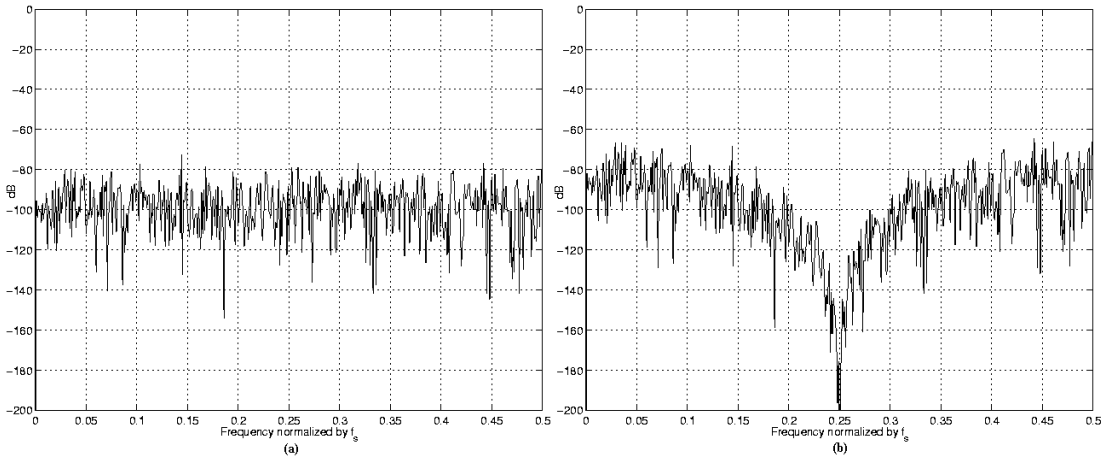


Figure 2.13–Quantization Noise Spectrum. (a) Before second-order band-pass ΣΔ noise-shaping, (b) After second-order band-pass ΣΔ noise-shaping.

2.6 Continuous-Time design and implementation of Band-pass ΣΔ modulator [5],[6],[7]

The discrete-time band-pass ΣΔ modulator eases the conversion of a band-pass signal with a narrow bandwidth around the center frequency of the signal. However, the switched-capacitor [8],[9],[10] or switched-current [11] implementation are limited in that the sampling frequency of the modulators cannot be too high (usually at under 100 MHz). Even using the double-sampling technique [12] or 2-path technique [13],[14], the center frequency of the band-pass signal is still limited to below 50 MHz. The modulator cannot operate at 70 MHz for high-IF conversion. Therefore, a continuous-time design and implementation method for high-IF conversion is worth investigating.

In a discrete-time system or switched-capacitor design, due to the discrete-time nature of the modulator design, the DAC output waveform in the feedback loop of the ΣΔ modulator does not have much effect on the modulator performance. The variations of the digital-to-analog signal during the clock period ϕ and ϕ' are not seen by a switched-capacitor filter. However, a continuous-time filter responds to an input signal continuously, unlike the switched-capacitor filter that is discrete in nature. Therefore, a continuous-time ΣΔ loop-filter has to be designed according to the DAC output waveform. Figure 2.14 shows the block diagram of a continuous-time ΣΔ modulator.

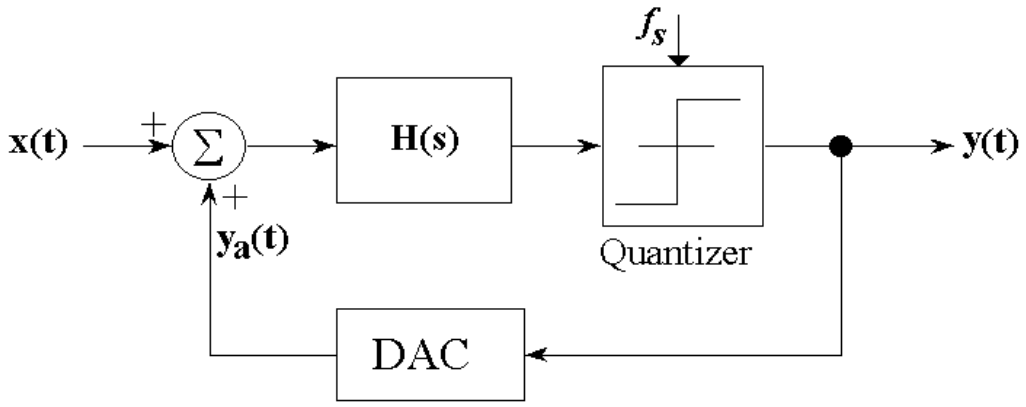


Figure 2.14–Block Diagram of a continuous-time ΣΔ modulator.

There are differences between a continuous-time modulator and a discrete-time modulator. Firstly, the loop-filter of the continuous-time modulator is a transconductor-capacitor filter or a LC filter, not a switched-capacitor filter or a switched-current filter in discrete-time modulator. Secondly, a sample-and-hold circuitry should be added in a continuous-time modulator, which in practice can simply be combined with the quantizer in the loop.

To design a continuous-time modulator, the DAC transfer function should be defined and its waveform should be considered. A good performance 1-bit DAC can be implemented using a zero-order-hold circuitry with a transfer function of $ZOH(s)=1-e^{-sT}/s$ where T is the sampling period. Afterwards, a discrete-time Z-domain to continuous-time S-domain transformation should be done in order to implement a continuous-time band-pass ΣΔ modulator. Two common transformations can be considered: bilinear transformation and impulse-invariant-transformation.

Bilinear transformation maps all frequencies in the S-domain to the Z-domain and vice versa, but the frequencies are non-linearly mapped. Impulse-invariant-transformation maps the frequencies linearly from $-\pi f_s/2$ to $\pi f_s/2$ while other frequencies will be aliased into the transformed band; therefore, anti-aliasing the

signal is important when using this transformation. There is a 70 MHz band-pass IF filter before the modulator that served the anti-aliasing filter purpose in our proposed receiver. Therefore, for design simplicity, the impulse-invariant-transformation was chosen:

$$Z^{-1}[H(z)] = L^{-1}[\frac{1-e^{-sT}}{s} H(s)]\Big|_{t=nT} \quad (2.9)$$

where *H(z)* is the discrete-time transfer function of the loop-filter in the modulator, *H(s)* is the continuous-time transfer function for the loop-filter, and $1\text{-}e^{-sT}/s$ is the transfer function of the DAC in the loop where $T=1/f_s$.

For a continuous-time loop-filter, *H(s)* has the form of

$$H(s) = \sum_{k=1}^{N} \frac{a_k}{s - s_k} \quad (2.10)$$

Its impulse response is

$$h(t) = \sum_{k=1}^{N} a_k e^{s_k T} u(t) \quad (2.11)$$

After the convolution with the DAC,

$$\begin{aligned} h_{eq}(t) &= ZOH * h(t) \\ &= \int_{-\infty}^{+\infty} ZOH \cdot h(t-\tau) d\tau \\ &= \begin{cases} \int_0^t h(t-\tau) d\tau & when\ 0 \le t < T \\ \int_0^T h(t-\tau) d\tau & when\ t \ge T \\ 0 & when\ t < 0 \end{cases} \\ &= \begin{cases} \int_0^t \sum_{k=1}^{N} a_k e^{s_k (t-\tau)} d\tau & when\ 0 \le t < T \\ \int_0^T \sum_{k=1}^{N} a_k e^{s_k (t-\tau)} d\tau & when\ t \ge T \end{cases} \end{aligned}$$

Hence,

$$h_{eq}(t)=\begin{cases}\sum_{k=1}^{N}\frac{a_k}{-s_k}e^{s_k t}(e^{-s_k t}-1) & when\ 0\le t<T\\ \sum_{k=1}^{N}\frac{a_k}{-s_k}e^{s_k t}(e^{-s_k T}-1) & when\ t\ge T\end{cases} \quad (2.12)$$

Looking at samples of loop impulse response at sampling times $t=nT$,

$$h_{eq}(nT)=\begin{cases}0 & when\ 0\le t<T\\ \sum_{k=1}^{N}\frac{a_k}{-s_k}e^{s_k nT}(e^{-s_k T}-1) & when\ t\ge T\end{cases} \quad (2.13)$$

The z-domain loop transfer function of the loop then can be derived from the above equivalent impulse response:

$$\begin{aligned}H(z)&=\sum_{n=-\infty}^{+\infty}h(n)z^{-n}=\sum_{n=1}^{+\infty}[\sum_{k=1}^{N}\frac{a_k}{-s_k}e^{s_k nT}(e^{-s_k T}-1)]z^{-n}\\ &=\sum_{k=1}^{N}[\frac{a_k}{-s_k}(e^{-s_k T}-1)\sum_{n=1}^{+\infty}(e^{s_k T}z^{-1})^n]\\ &=\sum_{k=1}^{N}\frac{a_k}{-s_k}(1-e^{s_k T})\frac{z^{-1}}{1-z_k z^{-1}}\ where\ z_k=e^{s_k T}\\ &\therefore H(z)=\sum_{k=1}^{N}\frac{a_{k,eq}z^{-1}}{1-z_k z^{-1}},\ a_{k,eq}=\frac{a_k}{-s_k}(1-e^{s_k T})\end{aligned} \quad (2.14)$$

From the above, a continuous-time loop-filter can be designed from a discrete-time loop-filter:

$$H(z)=\frac{z^{-2}}{1+z^{-2}}\longrightarrow H(s)=-\frac{\pi}{4T}[\frac{s-\frac{\pi}{2T}}{s^2+(\frac{\pi}{2T})^2}] \quad (2.15)$$

where T is the sampling period of the modulator, i.e. $T=1/f_s$.

Equation (2.15) assumes the loop delay for the ΣΔ modulator is zero. However, in practical implementation, the quantizer is not delay-free. Therefore, if we add more delay such that the total loop delay becomes exactly one sampling period T, a digital delay z^{-1} is implemented in the loop. If we reserve this z^{-1} in the discrete-time transfer function and implement the z^{-1} by digital delay cell,

$$H(z) = \frac{z^{-1}}{1+z^{-2}} \longrightarrow H(s) = \frac{\pi}{4T}\left[\frac{s+\frac{\pi}{2T}}{s^2+\left(\frac{\pi}{2T}\right)^2}\right] \qquad (2.16)$$

A continuous-time second-order band-pass ΣΔ modulator at 70 MHz can be designed and implemented accordingly. The loop-filter can be implemented by a transconductor-capacitor filter or a LC filter as mentioned above; the quantizer can be implemented by a latched-type comparator; the ZOH circuit can be implemented by a D flip-flop; the DAC can be implemented by a steering current source; and the addition can be done using current addition.

In this project, both zero-delay and one-delay band-pass ΣΔ modulator are implemented. As we will describe in the following chapters, a zero-delay modulator is implemented using 0.8μm technology and source-degeneration Gm-cells while a one-delay modulator is implemented using 0.5μm technology and triode-region Gm-cells.

Chapter 3 System Design of the ΣΔ modulator

3.1 Introduction

In Chapter 2, a continuous-time band-pass ΣΔ modulator design is discussed. This chapter will focus on the system simulation using different programs for the ΣΔ modulator. C and HSPICE have been used for doing the system simulation using ideal model for each building block. System level design for the loop-filter will be discussed in Section 3.2. Then, two modulators will be described in the following sections: the design and system simulation of the zero-delay ΣΔ modulator will be described in Section 3.3, and the design and system simulation of the one-delay ΣΔ modulator will be described in Section 3.4.

3.2 System level loop-filter design

In Chapter 2, the continuous-time band-pass ΣΔ modulator design requires a continuous-time loop-filter with the transfer function either as equation (2.15) for zero-delay modulator or as equation (2.16) for one-delay modulator. For continuous-time analog operation, there exists three types of filter implementation methods: LC filter, switched-capacitor filter and transconductor-capacitor (Gm-C) filter. The LC filter implementation requires large values of inductance and capacitance, which are not realistic for monolithic integration. As mentioned in Chapter 2, switched-capacitor filters are too slow for 280 MHz sampling operation, therefore, only the Gm-C filter can be considered for the loop-filter implementation.

The main building block of continuous-time filters is an integrator. A Gm-cell and a capacitor can be used to realize an integrator in Gm-C technology as shown in Figure 3.1.

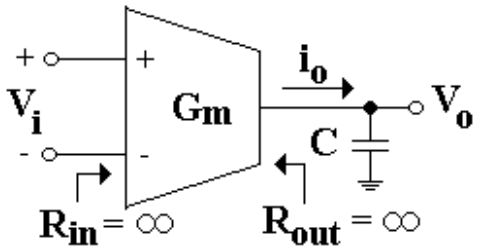


Figure 3.1—A single-ended Gm-C integrator.

A Gm-cell is a device with an output current linearly related to the input voltage. Here, the output of the transconductor is the current i_o and both the input and output impedance of the Gm-cell are infinite. The output current and the differential input voltage signal have the following relation, where Gm is the transconductance of the Gm-cell:

$$i_o = Gm \cdot V_i \qquad (3.1)$$

This output current is then applied to the integrating capacitor, C, resulting in a voltage across C:

$$V_o = \frac{i_o}{sC} = \frac{GmV_i}{sC} \qquad \Rightarrow \qquad \frac{V_o}{V_i} = \frac{Gm}{C} \cdot \frac{1}{s} \qquad (3.2)$$

Hence, the output voltage is an integration of the differential input voltage multiplied by a time-constant, *Gm*/*C*. A fully differential integrator is shown in Figure 3.2.

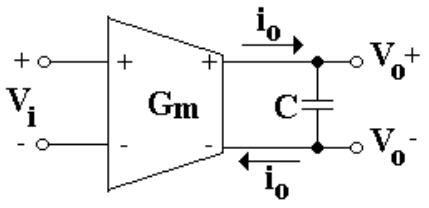


Figure 3.2—Fully-differential Gm-C integrators.

A second-order filter, or biquad, with transfer function:

$$H(s)=\frac{Y(s)}{X(s)}=\frac{b_1 s+b_0}{s^2+a_1 s+a_0} \qquad (3.3)$$

in Gm-C technology can be realized using the block diagram as shown in Figure 3.3.

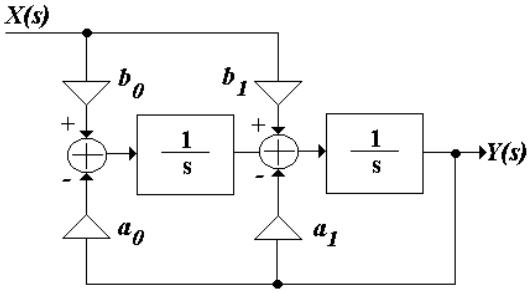


Figure 3.3—Block diagram of the biquad filter described in equation (3.3).

The block diagram in Figure 3.3 can be simply realized using Gm-cells as shown in Figure 3.4.

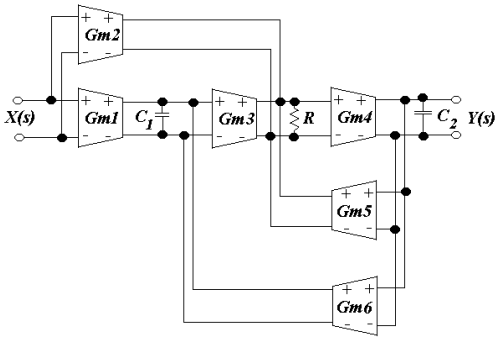


Figure 3.4—Gm-C implementation of the filter described in equation (3.3).

The corresponding transfer function is given by:

$$H(s)=\frac{Y(s)}{X(s)}=\frac{\frac{Gm2\cdot Gm4\cdot R}{C_2}s+\frac{Gm1\cdot Gm3\cdot Gm4\cdot R}{C_1\cdot C_2}}{s^2-\frac{Gm5\cdot Gm4\cdot R}{C_2}s-\frac{Gm3\cdot Gm6\cdot Gm4\cdot R}{C_1\cdot C_2}} \quad (3.4)$$

To implement the transfer function as equations (2.15) or (2.16), the building block diagram in Figure 3.4 can be simplified as shown in Figure 3.5.

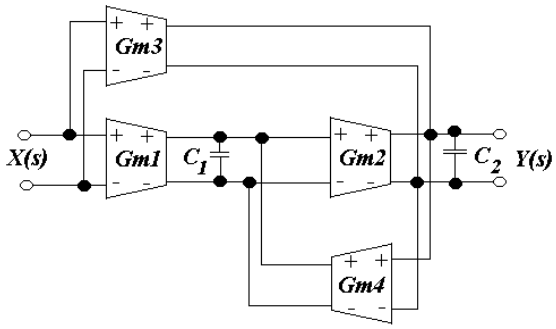


Figure 3.5—Block diagram for loop-filter.

The transfer function of the loop-filter is:

$$H(s)=\frac{Y(s)}{X(s)}=\frac{\frac{Gm3}{C_2}s+\frac{Gm1\cdot Gm2}{C_1\cdot C_2}}{s^2-\frac{Gm2\cdot Gm4}{C_1\cdot C_2}} \quad (3.5)$$

By equating coefficients in equations (2.15) or (2.16) and (3.5), the values of the transconductances and capacitors can be chosen for the loop-filter implementation.

The ideal loop-filter response with transfer function as equation (2.15) for zero-delay band-pass ΣΔ modulator is simulated using MATLAB and is being shown in Figure 3.6. The loop-filter is a very high-Q band-pass filter with center frequency at

70 MHz. The phase of the filter at frequencies before 70 MHz is -135^o. It is then changed from -135^o to 45^o at 70 MHz abruptly, indicating a 180^o phase shift.

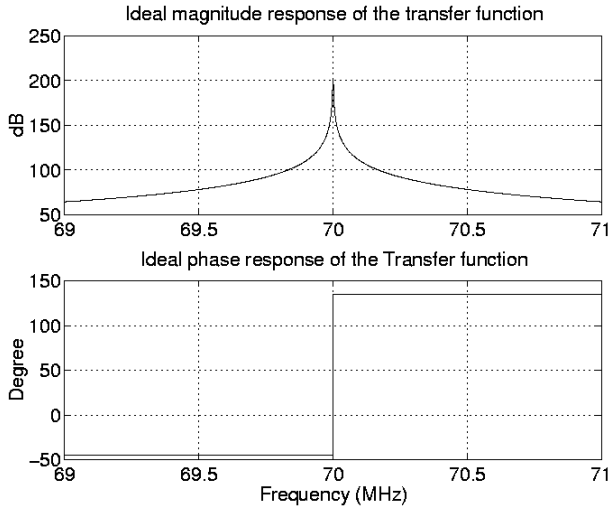


Figure 3.6—Ideal magnitude and phase response of the loop-filter described in equation (2.15).

The ideal response of the loop-filter can never be achieved, however, as the Gm-cells are not ideal. We assumed the Gm-cell has infinite output impedance. In fact, every Gm-cell has finite output impedance. The transfer function implemented as equation (3.5) will be changed as follows:

$$H(s)=\frac{Y(s)}{X(s)}=\frac{\frac{Gm3}{C_2}s+[\frac{Gm1\cdot Gm2}{C_1\cdot C_2}+\frac{Gm3}{(R_1//R_4)C_1C_2}]}{s^2+[\frac{1}{(R_2//R_3)C_2}+\frac{1}{(R_1//R_4)C_1}]s+[-\frac{Gm2\cdot Gm4}{C_1C_2}+\frac{1}{(R_2//R_3)(R_1//R_4)C_1C_2}}$$

(3.6)

where R_x is the output impedance of the x-th Gm-cell.

As shown in equation (3.6), if the output impedance of the Gm-cells is infinite, equation (3.6) will then be simplified to equation (3.5). Using ideal voltage-controlled-current-source (VCCS) in HSPICE with different output impedances, the simulated magnitude and phase response is shown in Figure 3.7.

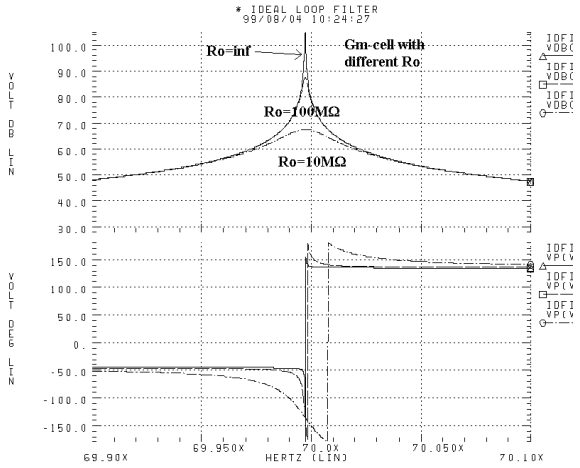


Figure 3.7—HSPICE simulation of the loop-filter described in equation (2.15).

The ideal loop-filter response with transfer function as equation (2.16) for one-delay band-pass ΣΔ modulator is simulated using MATLAB and is being shown in Figure 3.8. The loop-filter is a very high-Q band-pass filter with center frequency at 70 MHz. The phase of the filter at frequencies before 70 MHz is 45^o. It is then changed from 45^o to -135^o at 70 MHz abruptly, indicating a 180^o phase shift. The HSPICE simulated response with different output impedances is shown in Figure 3.9.

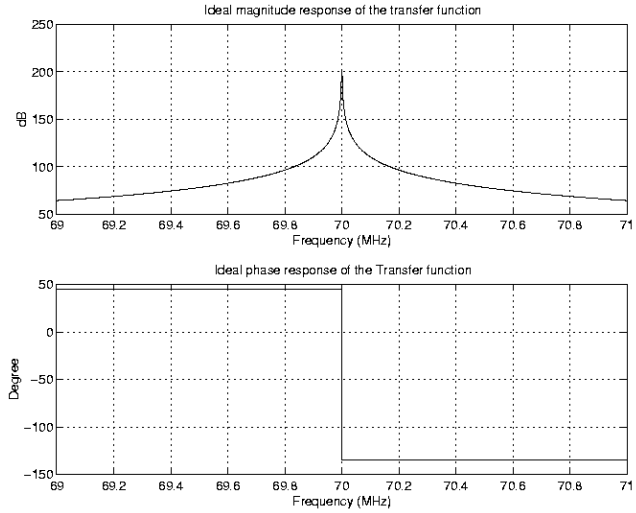


Figure 3.8—Ideal magnitude and phase response of the loop-filter described in equation (2.16).

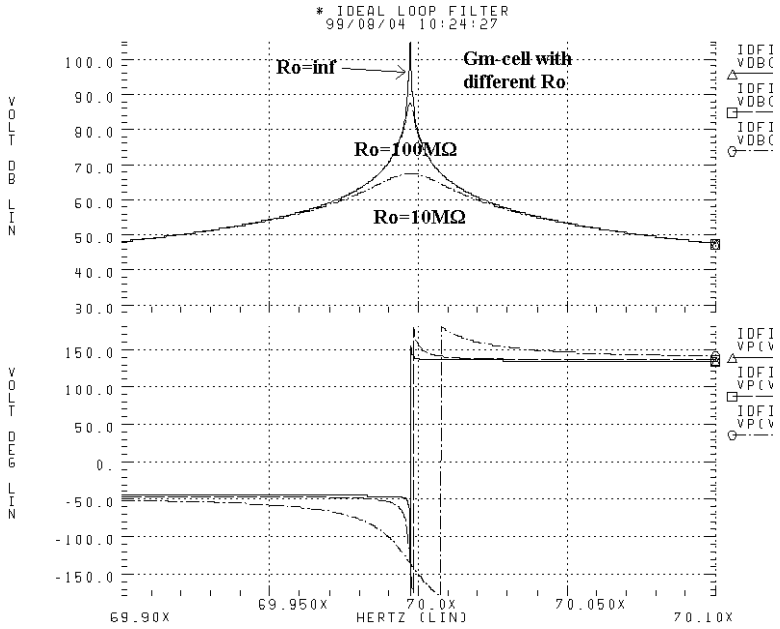


Figure 3.9— HSPICE simulation of the loop-filter described in equation (2.16).

3.3 Zero-delay ΣΔ modulator

System simulation of the zero-delay ΣΔ modulator has been conducted using C programming and HSPICE. In C programming, everything should be in time-domain rather than s-domain or z-domain. Therefore, according to the block diagram of the loop-filter as shown in Figure 3.3, a system-level block diagram of the modulator is derived and shown in Figure 3.10. The simulation is then programmed according to equations (3.7) to (3.9).

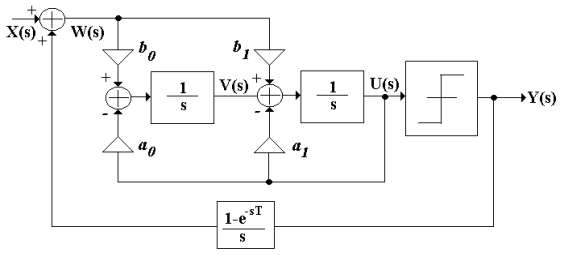


Figure 3.10—Full block diagram of continuous-time band-pass ΣΔ modulator.

$$y(k) = sign[u(k)] = sign[\hat{u}(kT)] \tag{3.7}$$

$$u(k+1) = \hat{u}(kT) + \hat{y}(kT)\cdot T + b_1 \int_{kT}^{(k+1)T} \hat{x}(t)dt + \int_{kT}^{(k+1)T} \hat{v}(t)dt - a_1 \int_{kT}^{(k+1)T} \hat{u}(t)dt \tag{3.8}$$

$$v(M+1) = \hat{v}(MT_o) - a_o \hat{u}(MT_o)\cdot \Delta t + b_o \int_{MT_o}^{(M+1)T_o} \hat{x}(t)dt + \hat{y}(t)\cdot T_o \tag{3.9}$$

Figure 3.11 shows the C simulation result of the zero-delay ΣΔ modulator. The simulation assumes the loop-filter has an infinite Q and zero loop-delay. Another C simulation assuming the loop-filter has a finite Q of 50 and zero loop-delay has performed and the simulation result is shown in Figure 3.12.

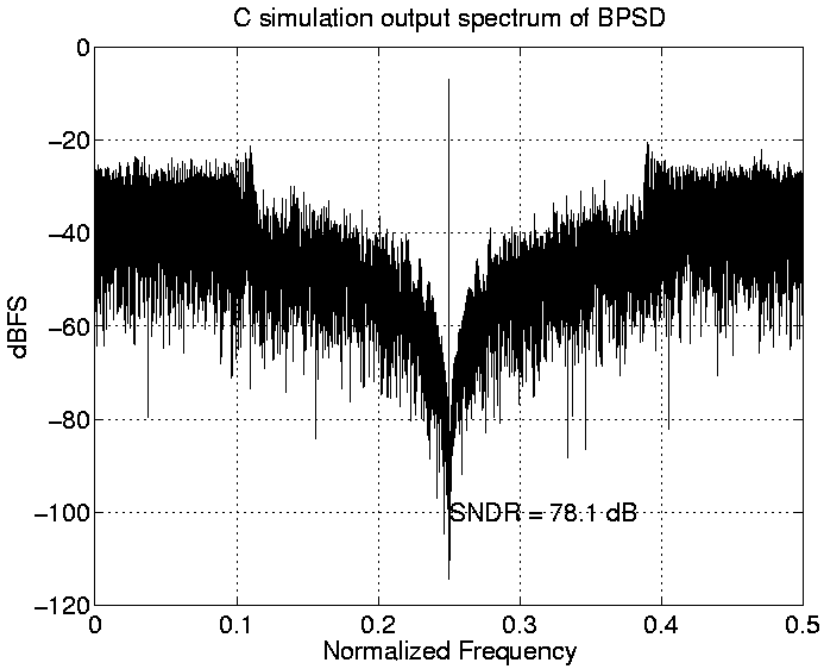


Figure 3.11—C simulation of zero-delay ΣΔ modulator with infinite-Q loop-filter.

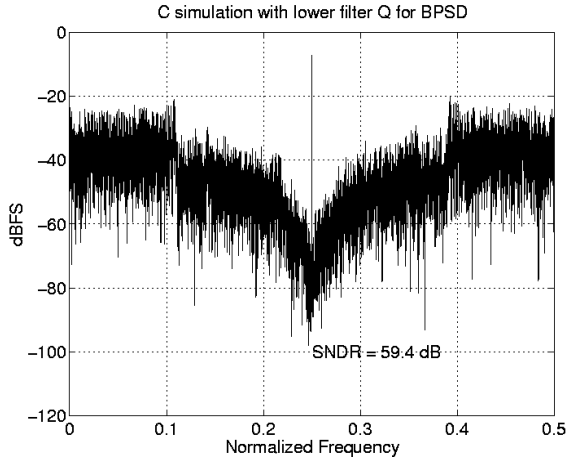


Figure 3.12—C simulation of the zero-delay ΣΔ modulator with loop-filter Q=50.

As shown in the simulation results, the modulator with an infinite-Q loop-filter can achieve SNDR of 78.1 dB while for the Q=50 loop-filter can achieve SNDR of 59.4 dB. A high-Q loop-filter have a better performance in terms of the SNDR. Therefore, Gm-cells with high output impedance are necessary.

As the system loop-filter will be implemented using Gm-C, ideal voltage-controlled-current-source (VCCS) as ideal Gm-cell has been used in HSPICE system simulation. Figure 3.13 shows the HSPICE ideal building block simulation result of the zero-delay ΣΔ modulator. The simulation assumes zero loop-delay and 10 MΩ output impedance for the Gm-cells.

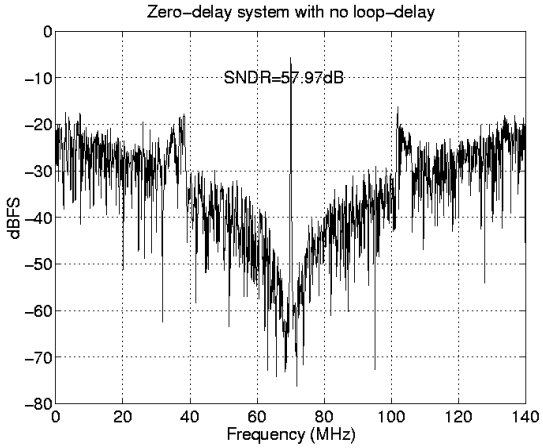


Figure 3.13—HSPICE ideal building block simulation of zero-delay ΣΔ modulator.

The Q value of the loop-filter for 10 MΩ output impedance Gm-cells is around 500. The simulated SNDR of the system can achieve 57.97 dB.

The above simulations assume the linear range of the Gm-cell is not limited. However, it is unrealistic to have unlimited linear range Gm-cells. Unfortunately, not only the Q of the loop-filter affects the performance of the modulator, but the linear range of the Gm-cell also affects the performance of the modulator. Two non-linear Gm-cell models are used for HSPICE simulation, one with ±500 mV linear range and the other one with ±100 mV linear range. Figure 3.14 and Figure 3.15 shows the HSPICE simulation using Gm-cell models with ±500 mV linear range and ±100 mV linear range respectively.

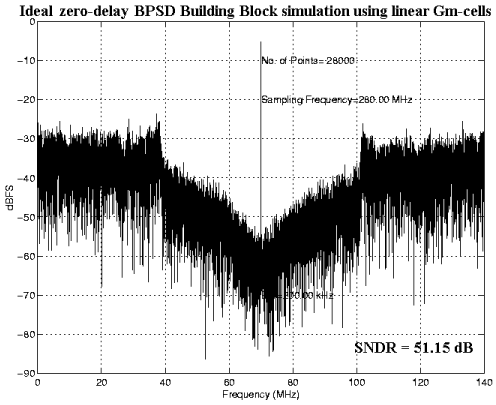


Figure 3.14—HSPICE building block simulation using ±500 mV linear range Gm-cells.

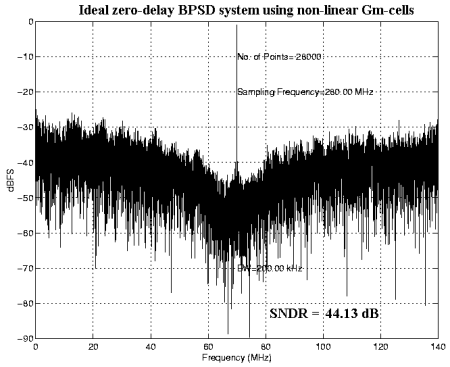


Figure 3.15—HSPICE building block simulation using ±100 mV linear range Gm-cells.

The modulator with ±500 mV linear range Gm-cells can achieve 51.2 dB of SNDR while the one with ±100mV linear range Gm-cells can achieve 44.1 dB only. Therefore, Gm-cells with large linear range are needed for a high-performance modulator.

In all the simulations shown above, loop-delay of the system is assumed to be zero. In practice, the loop-delay of the system cannot be zero. Figure 3.16 shows the simulation result when the loop-delay of the modulator is 2.6 ns. The loop-delay degrades the SNDR performance of the modulator [7]. The simulated SNDR is 44.84 dB. Since loop-delay is unavoidable in the modulator, it is better to make the loop-delay to be exactly equal to one sampling period in order to change the design to one-delay modulator.

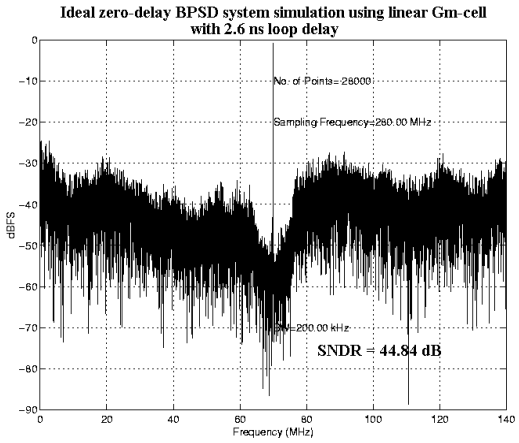


Figure 3.16—HSPICE ideal building block simulation for zero-delay ΣΔ modulator with 2.6 ns loop-delay.

3.4 One-delay ΣΔ modulator

Figure 3.17 shows the C simulation result of the zero-delay ΣΔ modulator. The simulation assumes the loop-filter has an infinite Q and zero loop-delay. Another C simulation assuming the loop-filter has a finite Q of 50 and zero loop-delay has performed and the simulation result is shown in Figure 3.18.

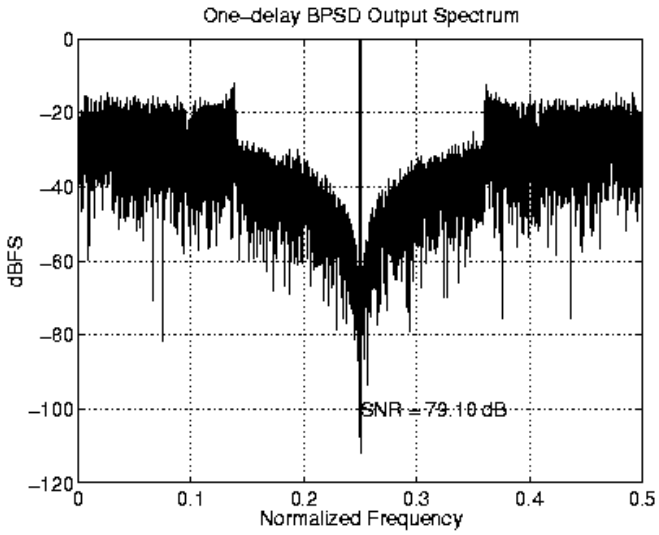


Figure 3.17—C simulation of one-delay ΣΔ modulator with infinite-Q loop-filter.

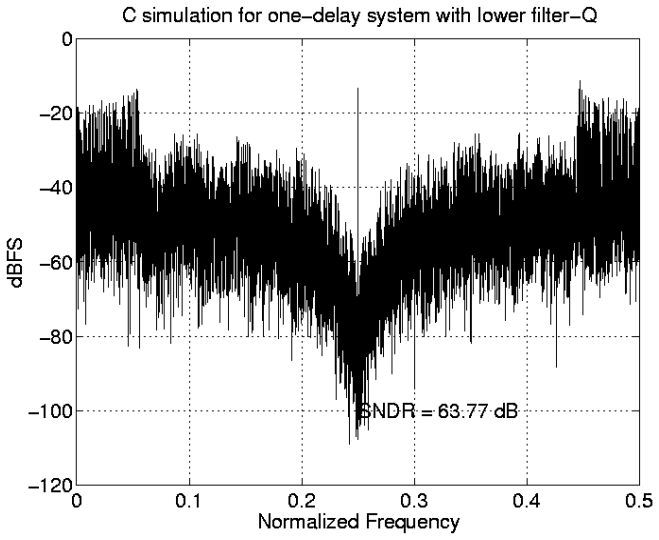


Figure 3.18—C simulation of one-delay modulator with loop-filter Q=50.

As shown in the simulation results, the modulator with an infinite-Q loop-filter can achieve SNDR of 79.1 dB while for the Q=50 loop-filter can achieve SNDR of 63.8 dB. Figure 3.19 shows the HSPICE ideal building block simulation result of the one-delay ΣΔ modulator. The simulation assumes 10 MΩ output impedance for the Gm-cells.

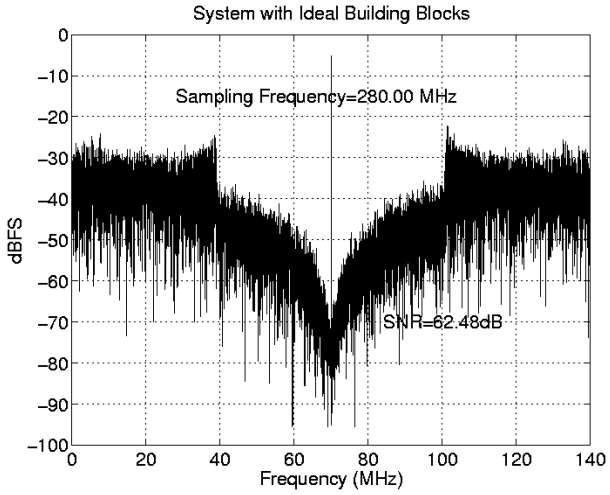


Figure 3.19—HSPICE ideal building block simulation of one-delay ΣΔ modulator with loop-filter Q=50.

The Q value of the loop-filter for 10 MΩ output impedance Gm-cells is around 500. The simulated SNDR of the system can achieve 62.5 dB.

Chapter 4 Gm-cell designs for loop-filter

4.1 Introduction

This chapter will focus on Gm-cell designs for the Gm-C loop filter. Three types of Gm-cells will be discussed: general differential-pair Gm-cell in Section 4.2, source-degeneration Gm-cell in Section 4.3, and triode-region Gm-cell in Section 4.4. After the Gm-cell discussions, two Gm-C loop-filters implemented using source-degeneration Gm-cells and triode-region Gm-cells will be described and compared in Section 4.5.

4.2 General differential pair Gm-cell

A typical CMOS Gm-cell design is a differential-pair as shown in Figure 4.1.

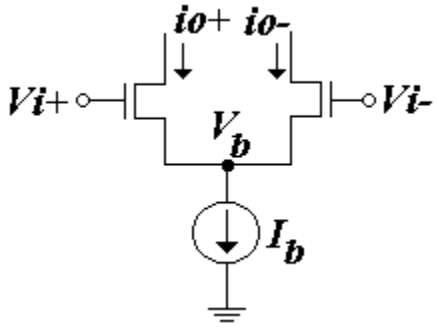


Figure 4.1—CMOS differential-pair.

Assuming the two transistors are working in the saturation region, the output current i_o of the differential-pair is

$$i_o = i_{o+} - i_{o-} = \sqrt{2\mu C_{ox}\frac{W}{L} I_b V_{id}^{\ 2} - \frac{1}{4}(\mu C_{ox}\frac{W}{L})^2 V_{id}^{\ 4}} \qquad (4.1)$$

The Gm of the differential-pair is then

$$Gm = \frac{\partial i_o}{\partial V_{id}} \qquad (4.2)$$

$$= \sqrt{2\mu C_{ox}\frac{W}{L}I_b} - \frac{3(\mu C_{ox}\frac{W}{L})^{\frac{3}{2}}}{4\sqrt{2I_b}}V_{id}^{\ 2} + \ldots$$

From equation (4.2), for small input signals, the Gm is constant. However, for large input signals, Gm drops and becomes non-linear. As a result, techniques for linearizing Gm-cells are needed to be used.

4.3 Source-degeneration Gm-cell

The first way to design a linear Gm-cell is source degeneration [17] as shown in Figure 4.2.

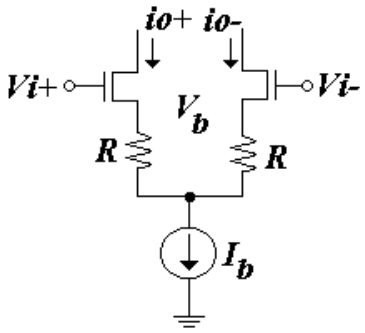


Figure 4.2—Source-degeneration CMOS differential-pair.

Gm of the degenerated differential-pair is

$$Gm = \frac{gm}{1 + gm \cdot R} \qquad (4.3)$$

where *gm* is the transconductance of a single transistor. When *gmR* is much larger than 1, the Gm of the degenerated-differential-pair can be approximated as *1*/*R*.

However, it is unrealistic for a very large value of *R* to be implemented monolithically. Therefore, triode region transistor is used to implement the degeneration resistor R. The resistance of a triode region transistor is:

$$R = \frac{1}{\mu C_{ox} \frac{W}{L}(V_{gs} - V_t - V_{ds})} \qquad (4.4)$$

A source-degeneration Gm-cell using 0.8μm technology has been designed. The circuit schematic is shown in Figure 4.3.

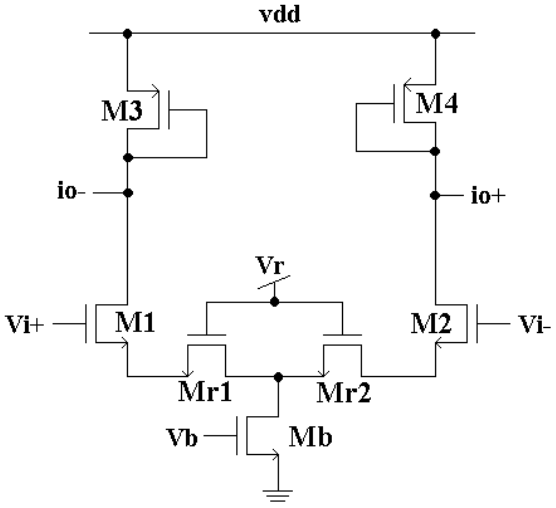


Figure 4.3—Designed source-degeneration Gm-cell.

It is desired to have very high output impedance, in the order of tens of MΩ, for Gm-cells for high-Q filters. However, it is difficult to obtain. For the design as shown in Figure 4.3, the output impedance is in the order of tens of kΩ, therefore, a Q-tuning circuitry is needed to enhance the Q-value of the filter by increasing the output impedance of the Gm-cell. A usual technique called negative-impedance-compensation (NIC) [15] technique is used in Gm-C filter to increase the output impedance of the Gm-cell. The source-degeneration Gm-cell with the NIC circuit is shown in Figure 4.4. The transistors Mqb, Mq1 and Mq2 formed a negative-Gm-cell.

Assuming the absolute Gm value of the negative-Gm-cell is Gmn, the output impedance of the source-degneration Gm-cell with NIC will be:

$$R_{o,eq} = \frac{1}{1/R_{o,gmcell} - Gmn} \qquad (4.5)$$

The voltage Vq controls the current supply to the transistors Mq1 and Mq2 in order to vary the negative Gm value. The negative Gm can be tuned to equal to the positive output impedance of the source-degeneration Gm-cell, and the output impedance of the whole Gm-cell will then be infinity.

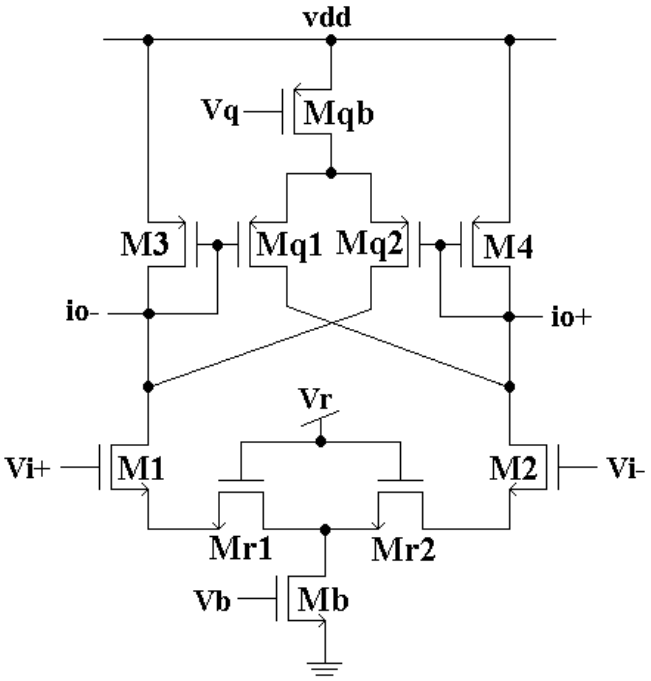


Figure 4.4—Source-degeneration Gm-cell with NIC circuit.

Figure 4.5 shows the HSPICE simulation results of the source-degeneration Gm-cell with NIC circuit. The linear range of the Gm-cell is being defined as the input voltage range that has Gm value deviates below 1% from the nominal Gm

value. The linear range of this Gm-cell is around ±90mV with 3 V power supply. The current supply to the Gm-cell is 0.75 mA.

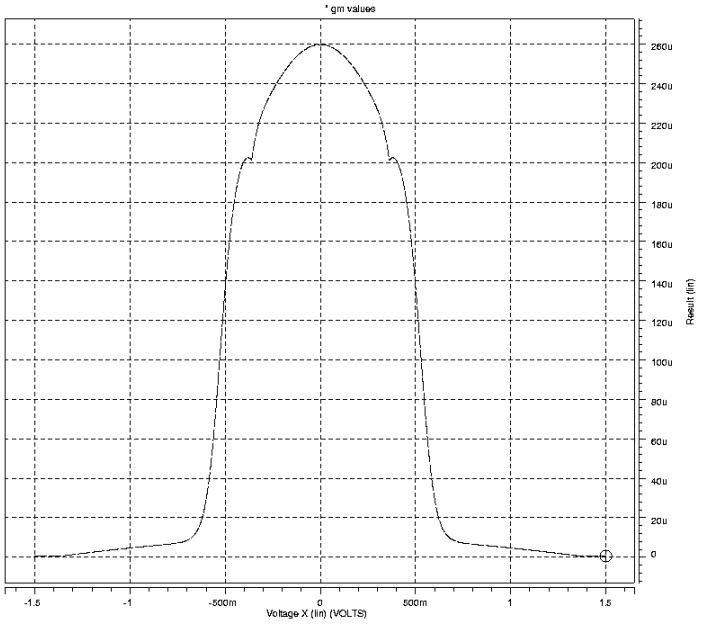


Figure 4.5—HSPICE simulation result of the source-degeneration Gm-cell.

4.4 Triode-region Gm-cell

Another method of designing a linear Gm-cell is to use a triode-region transistor [7],[16] as shown in Figure 4.6. The current of a triode-region transistor is shown in equation (4.6) and the transconductance *gm* is shown in equation (4.7).

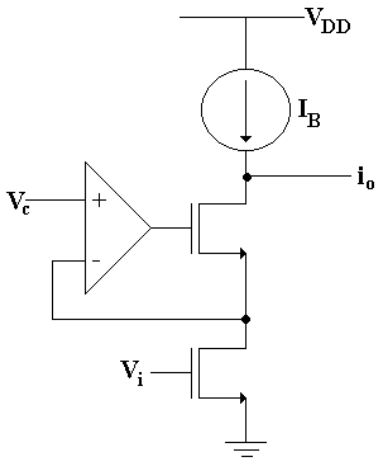


Figure 4.6—Triode-region Gm-cell.

$$I_D = \mu C_{ox} \frac{W}{L}(V_{gs} - V_t - \frac{V_{ds}}{2})V_{ds} \quad (4.6)$$

$$gm = \frac{\partial I_D}{\partial V_{gs}} = \mu C_{ox} \frac{W}{L} V_{ds} \quad (4.7)$$

The op-amp in Figure 4.6 serves two functions. Firstly, it is used to control the V_{ds} of the transistor to be equal to V_c, so that the *gm* value can be proportional to a constant voltage V_c. The reference voltage V_c should satisfy the following condition in order to enforce the transistor to operate in the triode region:

$$V_c < V_{gs} - V_t \quad (4.8)$$

Secondly, it is used to enhance the output impedance of the Gm-cell. As the op-amp is being used to fix the V_{ds} of the triode-region transistor, the bandwidth requirement of the op-amp is not stringent. However, the gain of the op-amp should be reasonably large, so that the V_{ds} of the triode-region transistor can follow the control voltage V_c as close as possible.

A differential architecture of using the triode-region Gm-cell is shown in Figure 4.7. The cascode structure provides large output impedance to the Gm-cell. However, a major problem in the circuit is that its common-mode gain is equal to its differential-mode gain.

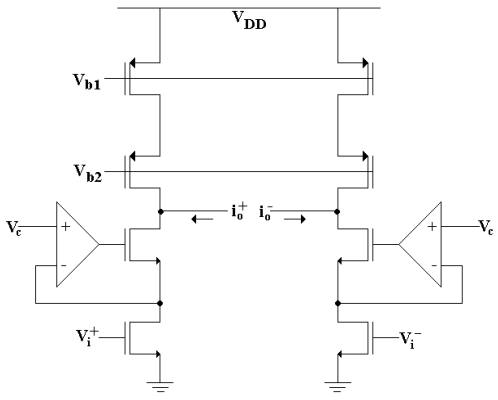


Figure 4.7—Differential triode-region Gm-cell.

The high common-mode gain problem can be solved by modifying the circuit to a fully differential cross-coupled architecture, as shown in Figure 4.8. The output cross-coupling connection reduces the common-mode gain of the Gm-cell. Figure 4.9 shows the schematic of the designed op-amp used in the Gm-cell.

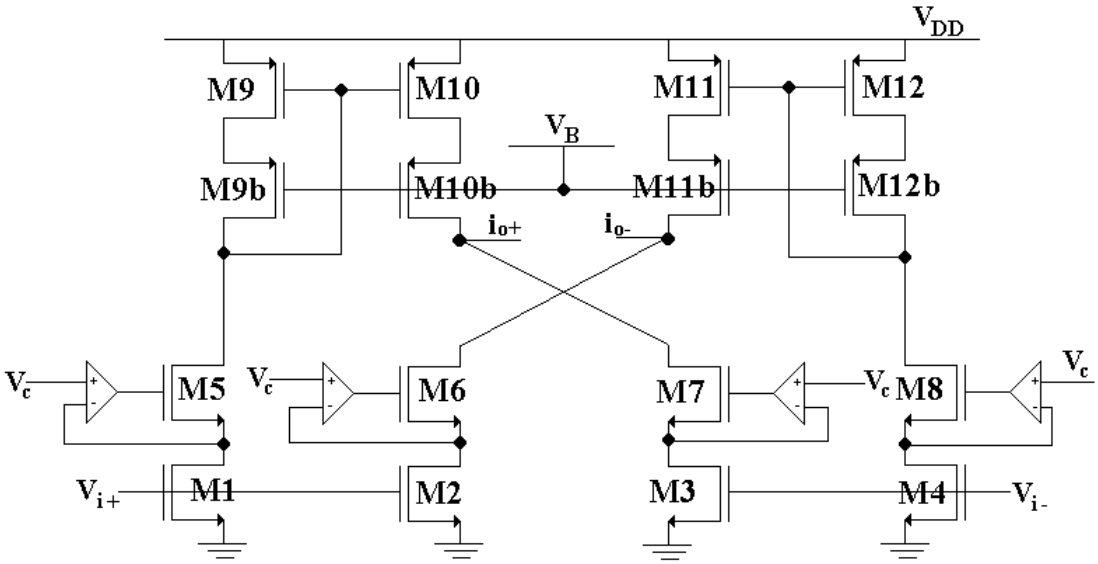


Figure 4.8—Fully differential triode-region Gm-cell.

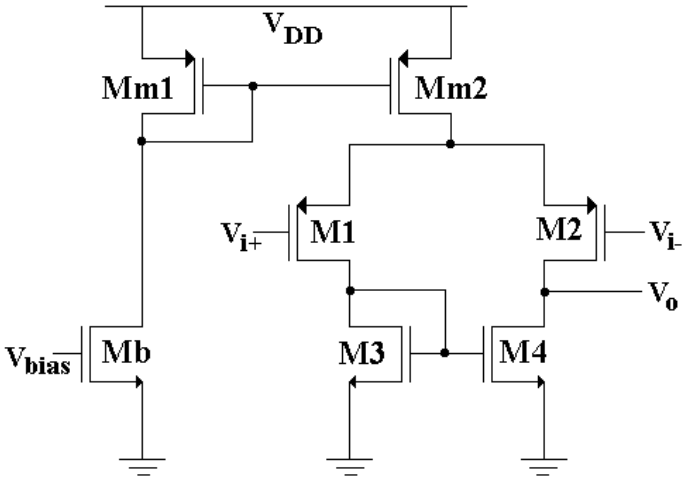


Figure 4.9—Schematic of the designed Op-amp.

It is difficult to obtain very high output impedance for the triode-region Gm-cell, too. For the design as shown in Figure 4.8, the output impedance is approximately 1MΩ. Though the output impedance is already larger than the design using the source-degeneration Gm-cell, it is still not high enough for the loop-filter with a very high Q value. Therefore, a Q-tuning circuitry is still needed to enhance the Q-value of the filter by increasing the output impedance of the Gm-cell. In the design as shown in Figure 4.8, the output impedance of the Gm-cell is already negative due to the output cross coupling connection. Therefore, a positive resistor can be used in place of another linear negative Gm-cell. The positive resistor can be implemented using a PMOS transistor operating in the triode-region. The resistance can be controlled through the gate voltage of the PMOS transistor and hence the filter Q can be tunable. A fully differential triode-region Gm-cell using 0.5μm technology has been designed. Figure 4.10 shows the HSPICE simulation results of the designed op-amp and Figure 4.11 shows the HSPICE simulation results of the fully differential triode-region Gm-cell using 3 V power supply.

The gain of the op-amp is 34 dB, and the bandwidth of the op-amp is 4 MHz with 0.2pF capacitive loading at the output.

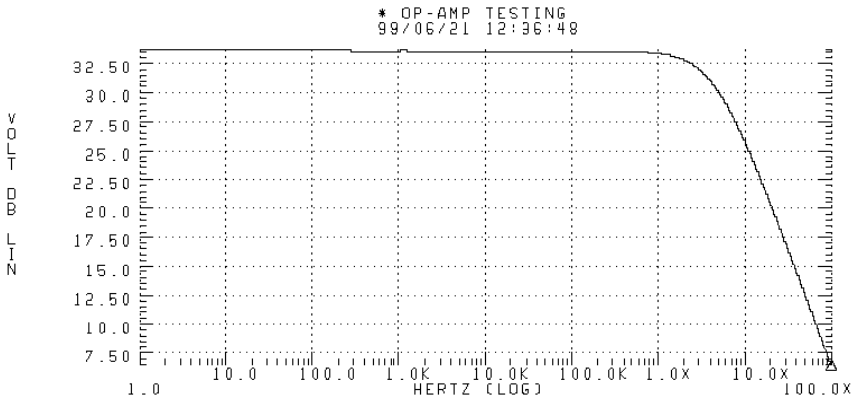


Figure 4.10—HSPICE simulated AC response of the designed op-amp.

Figure 4.11—HSPICE simulation result of the fully differential triode-region Gm-cell.

The linear range of the fully differential triode-region Gm-cell is ±600mV with 3 V power supply. The current supply to the Gm-cell is 2.5 mA. Table 4.1 shows the performance comparison between source-degeneration Gm-cell and triode-region Gm-cell.

Parameters	Source-degeneration	Triode-region
Linear range	±90 mV	± 600 mV
Current supply at 3 V	0.75 mA	2.5 mA

Table 4.1—Performance comparison between source-degeneration and triode-region Gm-cells.

4.5 Gm-C loop-filter implementation

A Gm-C loop-filter having transfer function as equation (2.15) is being designed and simulated. The loop-filter is implemented using source-degeneration Gm-cells with Q-tuning circuitry and simulated using HSPICE. The simulation result is shown in Figure 4.12. The total current supply of the filter is 3 mA at 3 V power

supply. The simulated equivalent input noise of the filter is 9.23 μV for a band-width of 200 kHz, or equivalently 20.64 nV/√Hz.

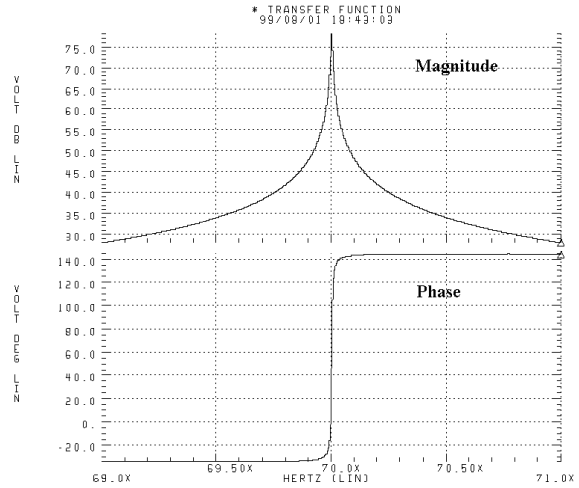


Figure 4.12—Circuit Level HSPICE simulation of the loop-filter as equation (2.15) with Q-tuning.

The IIP_3 of this filter is –23.2 dBm and the 1-dB compression point is –43.6 dBm as shown in Figure 4.13.

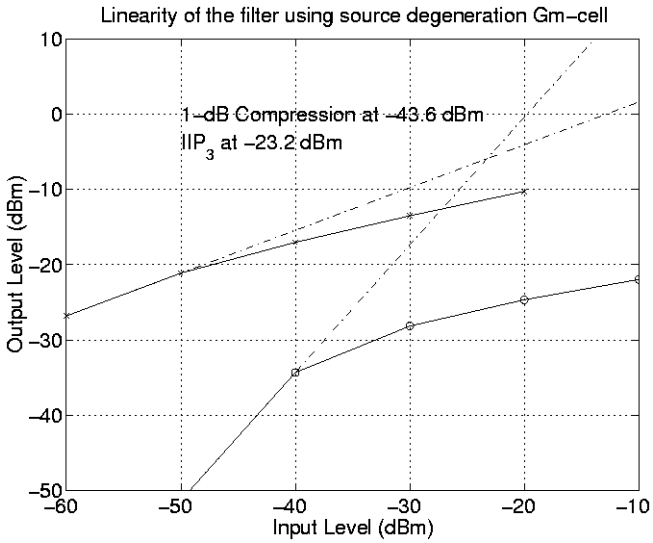


Figure 4.13—1-dB Compression point and IIP_3 of the filter using source-degeneration Gm-cells.

Another Gm-C loop-filter having transfer function as equation (2.16) has been designed and simulated. The loop-filter is implemented using triode-region Gm-

cells with Q-tuning circuitry and simulated using HSPICE. The simulation result is shown in Figure 4.14. The total current supply of the filter is 10 mA at 3 V power supply. The simulated equivalent input noise of the filter is 25.58 μV for a band-width of 200 kHz, or equivalently 57.20 nV/√Hz.

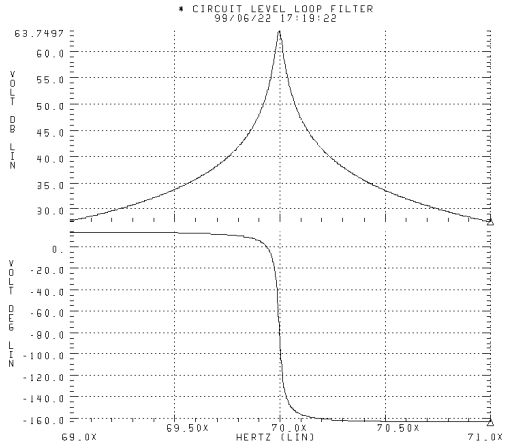


Figure 4.14—Circuit Level HSPICE simulation of the loop-filter as equation (2.16) with Q-tuning.

The IIP_3 of this filter is –16 dBm and the 1-dB compression point is –20 dBm as shown in Figure 4.15. Table 4.2 shows the differences in performances between the two loop-filters.

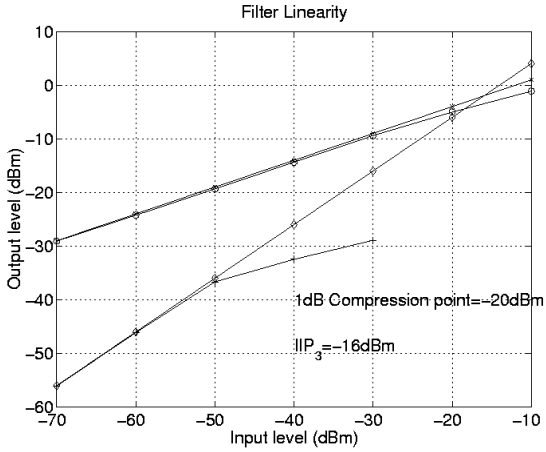


Figure 4.15—1-dB Compression point and IIP_3 of the filter using triode-region Gm-cells.

Parameters \ Design	Source-degeneration	Triode-region
Center frequency	70 MHz	70 MHz
Gain at center frequency	77 dB	63.75 dB
Q	> 100	> 100
1-dB compression point	-43.6 dBm	-20 dBm
IIP_3	-23.2 dBm	-16 dBm
Equivalent input noise	9.23 μV or 20.64 nV/√Hz	25.58 μV or 57.20 nV/√Hz
Total current supply	3 mA	10 mA

Table 4.2—Summary of the simulation results of the two loop-filters.

The current supply to the loop-filter implemented using source-degeneration Gm-cells is less than that implemented using triode-region Gm-cells. The reason is that the triode-region Gm-cells need extra current for op-amp biases. The noise of the loop-filter using source-degeneration is better than that using triode-region. The reason is that the triode-region MOS transistors are noisier than saturation-region MOS transistors. However, as the linear range of the Gm-cells using the triode-region is much larger than that using source-degeneration. Therefore, the linearity of the loop-filter implemented using triode-region transistor is better than that implemented using source-degeneration.

Chapter 5 Quantizer Design

5.1 Introduction

A core component of any analog-to-digital converter (ADC) is a quantizer. As mentioned in Chapter 2, Nyquist converters need precise analog components in their conversion circuits. Typically, a quantizer design includes a very precise sample-and-hold circuit and a high-accuracy comparator working at Nyquist sampling frequency. The accuracy requirement of the comparator depends on the accuracy requirement of the converter, e.g. an 8-bit ADC requires a comparator with at least 8-bit accuracy. In contrast, in ΣΔ modulators, the comparator is required to work at a high oversampling frequency but its resolution can be as small as 1 bit. Therefore, the comparator design in ΣΔ modulators focuses more on a high-speed operation instead of accuracy.

In Section 5.2, a latched-type comparator for the quantizer design will be described. As mentioned in Chapter 2, the quantized signal should be a non-return-to-zero (NRZ) waveform, therefore a zero-order-hold (ZOH) circuit is needed. In Section 5.3, a true-single-phase-clock (TSPC) D flip-flop for the ZOH circuit will be described. Finally, a simple feedback DAC design and the HSPICE simulation of the whole quantizer will be shown in Sections 5.4 and 5.6 respectively.

5.2 Comparator Design

To combine the sample-and-hold function and the comparator function in a quantizer, the latched-type comparator [18],[19] is the best choice. Figure 5.1 depicts

the schematic of the latched-type comparator in the quantizer design. The operation of the comparator is described as follows:

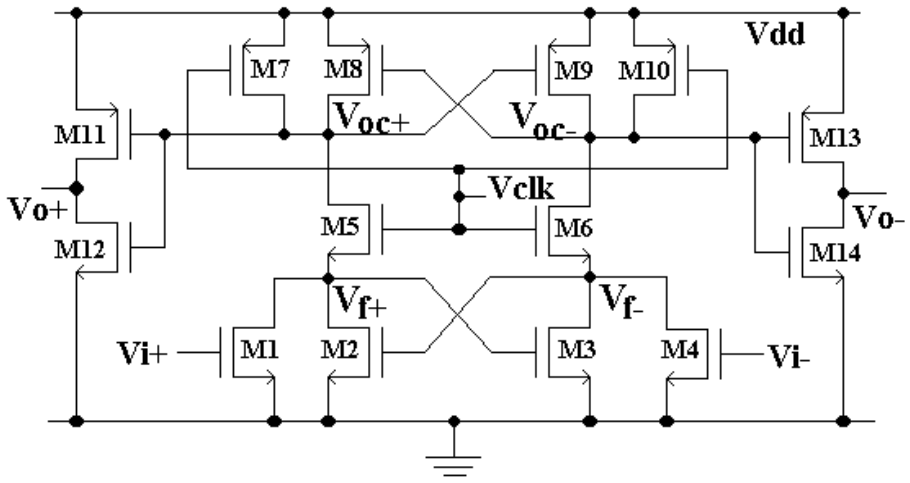


Figure 5.1—Schematic of the latched-type comparator.

M1 and M4 are the discharge-current-controlling transistors which are connected to a feedback network formed by M2 and M3; M5 and M6 are transfer gates for strobing; M8 and M9 form another regenerative feedback; M7 and M10 are precharge transistors; M11-M14 formed two inverters which act as buffers to isolate the latch from the output load and to amplify the comparator output.

During the pre-charge phase, i.e. when V_{clk} goes low, transistors M5 and M6 are cut off and the comparator does not respond to any input signal. The voltages V_{oc+} and V_{oc-} will be pulled to positive rail, V_{dd}, and the output of the inverters will be pulled to ground. At the same time, M1 and M4 discharge the voltages V_{f+} and V_{f-} to ground.

During the evaluation phase, i.e. when V_{clk} goes high, both the voltages V_{oc+} and V_{oc-} drop from the positive rail and both the voltages V_{f+} and V_{f-} rise from ground

initially. If the voltage at V_{i+} is higher than that at V_{i-}, M1 draws more current than M4. Thus, V_{oc+} drops faster than V_{oc-} and V_{f-} rises faster than V_{f+}. As V_{oc+} drops a threshold voltage below V_{dd}, M9 turns on and charge V_{oc-} to high level while V_{oc+} keeps going to ground as shown in Figure 5.2. Also, as V_{f-} rises a threshold voltage above ground, M2 turns on and discharge V_{f+} to ground while V_{f-} keeps rising to V_{dd}.

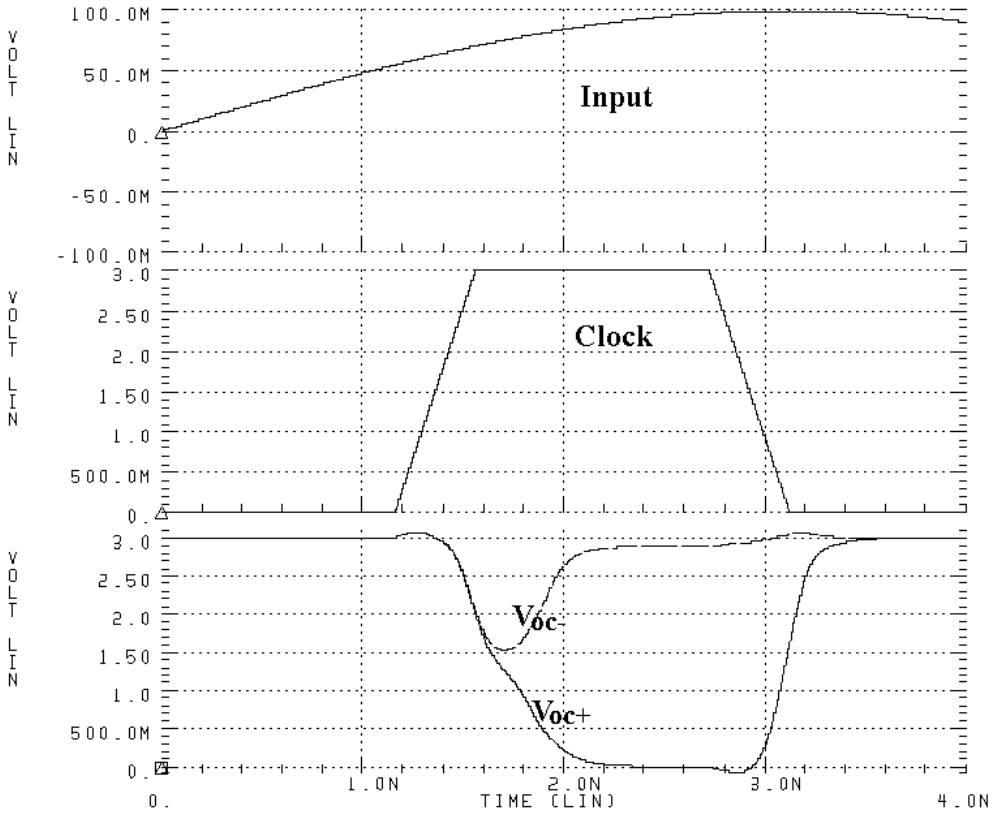


Figure 5.2—Regenerative action of the latched-type comparator.

The regenerative action of M8 and M9 together with that of M2 and M3 pulls V_{oc+} to ground and pulls V_{oc-} to positive rail. Hence, following the inverters M11-M14, V_{o+} is pulled to positive rail and V_{o-} is pulled to ground. The operation for the case when the voltage at V_{i-} is higher than that at V_{i+} is similar.

In designing the W/L ratios of the transistors for the comparator, considerations have to be made for high-speed operation. The delay of the whole comparator determines the fastest operation frequency of the comparator. The delay

of the comparator, t_{delay}, can be divided into two parts: the comparator core delay, t_{dc}, and the inverter delay, t_{di}:

$$t_{delay} = t_{dc} + t_{di} \qquad (5.1)$$

For high-speed operation, the sizes of transistors M5 and M6 should be large enough so that their resistance values are minimal but should be small enough at the same time to reduce the capacitance in order to have minimal t_{dc}. The sizes of transistors M1 and M4 should be large enough to ensure quick response to the input signal, but small enough for minimal gate capacitances for high-speed operation. The sizes of transistors M2, M3, M8 and M9 should be small enough for high-speed operation, but large enough for quick regenerative action. Finally, the inverter transistors M11-M14 should be large enough for driving the output load to reduce the t_{di}, but small enough for minimal gate-capacitances to reduce the t_{dc}.

Table 5.1 shows the W/L ratios of the transistors of the two designs of the comparator.

Transistor	0.8µm	0.5µm	Transistor	0.8µm	0.5µm
M1	9.6µ/0.8µ	7.2µ/0.6µ	M8	64µ/0.8µ	33.6µ/0.6µ
M2	20µ/0.8µ	30µ/0.6µ	M9	64µ/0.8µ	33.6µ/0.6µ
M3	20µ/0.8µ	30µ/0.6µ	M10	59.2µ/0.8µ	44.4µ/0.6µ
M4	9.6µ/0.8µ	7.2µ/0.6µ	M11	59.2µ/0.8µ	44.4µ/0.6µ
M5	59.2µ/0.8µ	24µ/0.6µ	M12	19.2µ/0.8µ	14.4µ/0.6µ
M6	59.2µ/0.8µ	24µ/0.6µ	M13	59.2µ/0.8µ	44.4µ/0.6µ
M7	59.2µ/0.8µ	44.4µ/0.6µ	M14	19.2µ/0.8µ	14.4µ/0.6µ

Table 5.1—W/L ratios of the transistors of the two comparators.

Figure 5.3 and Figure 5.4 shows the HSPICE simulation results of the comparator under different testing conditions. 3 V power supply and 0.5pF output

capacitive loading are used in the simulations. The input testing vector in Figure 5.4 is chosen in such a way that all the worst-case input situations are covered.

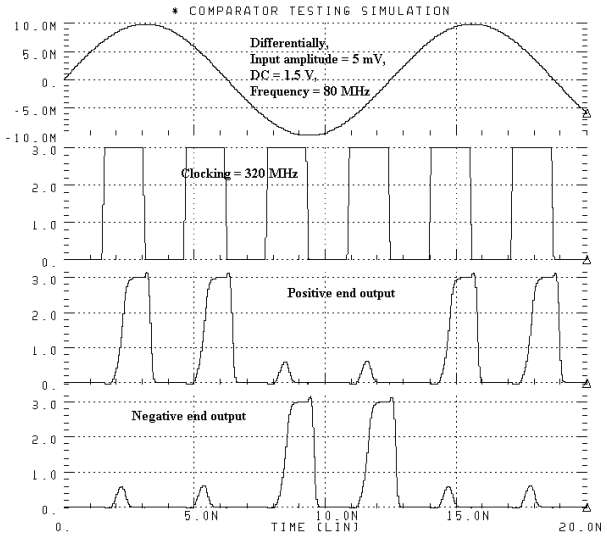


Figure 5.3—HSPICE Simulation of the comparator (320 MHz Clock, 80 MHz sinusoidal input).

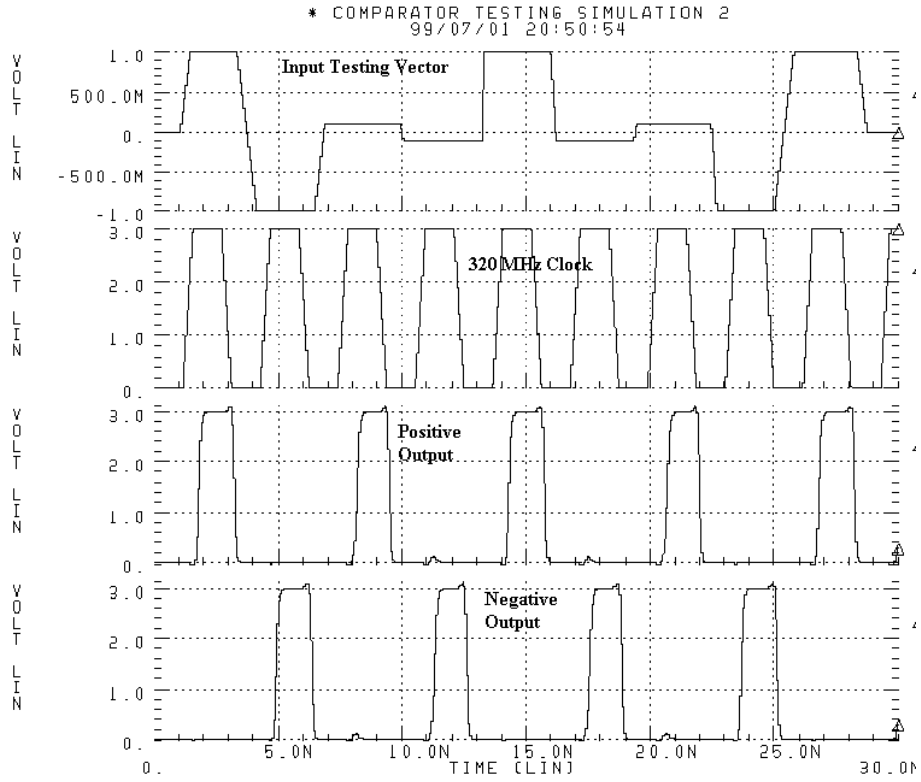


Figure 5.4—HSPICE Simulation of the comparator (320 MHz Clock, input testing vector).

For the design using 0.8μm technology, the rising time delay, t_{dr}, from the clock to the output is 0.95ns. The falling time delay, t_{df}, from the clock to the output is 0.53ns. The rising time, t_r, of the output is 0.73ns and the falling time, t_f, of the output is 0.28ns. The total current supply of the comparator is 3 mA at operation frequency of 280 MHz and 3 V power supply.

For the design using 0.5μm technology, the rising time delay, t_{dr}, from the clock to the output is 0.83ns. The falling time delay, t_{df}, from the clock to the output is 0.27ns. The rising time, t_r, of the output is 0.62ns and the falling time, t_f, of the output is 0.15ns. The total current supply of the comparator is 2.6 mA at operation frequency of 280 MHz and 3 V power supply. Table 5.2 shows the summary of the simulated results of two designed latched-type comparators.

	0.8μm	0.5μm
Operation frequency	320 MHz	320 MHz
Rising time delay	0.95 ns	0.83 ns
Falling time delay	0.53 ns	0.27 ns
Rising time	0.73 ns	0.62 ns
Falling time	0.28 ns	0.15 ns
Current supply at 3 V at 280 MHz	3 mA	2.6 mA

Table 5.2—Summary of simulated results of the latched-type comparators.

5.3 D flip-flop Design

In order to convert the return-to-zero (RZ) output of the comparator to a NRZ output, a D flip-flop is added after the latched-type comparator. It is too slow for usual static D flip-flop to be used in a 280 MHz sampling system, therefore, a TSPC D flip-flop [20],[21] is chosen. Figure 5.5 shows the schematic of the design of the

TSPC D flip-flop, and Figure 5.6 shows the operation of this negative-edge triggered TSPC D flip-flop.

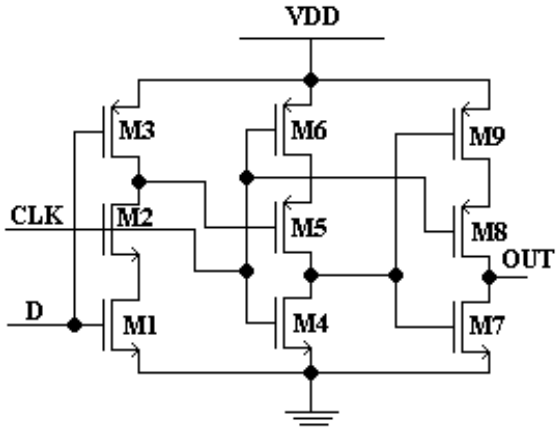


Figure 5.5—Schematic of the TSPC D flip-flop.

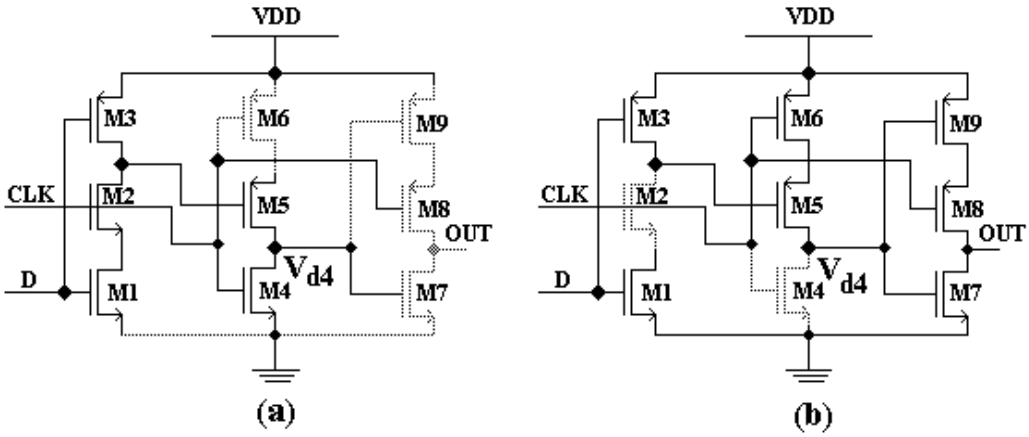


Figure 5.6—Operations of the TSPC D flip-flop. (a) Clock is high, (b) Clock is low.

When the clock signal is high, as shown in Figure 5.6(a), the transistors M6 and M8 are cut off and the transistors M2 and M4 are turned on. The voltage V_{d4} is being pulled to ground and hence forces the transistor M7 cut off. The output node is therefore disconnected to either positive rail or the ground and the output therefore is being latched to the previous value. On the other hand, the transistors M1-M3 formed

a clock-buffered inverter. When the clock signal is high, the drain voltage of the transistor M2 is the output of this inverter. The output of this inverter connects to the gate of the transistor M5 and the output value of this inverter is being stored in the gate capacitor of the transistor M5.

When the clock signal is low, as shown in Figure 5.6(b), the transistors M2 and M4 are cut off and the transistors M6 and M8 are turned on. The inverter formed by the transistors M1-M3 is being disconnected due to the cut off of the transistor M2. However, the charges stored in the gate capacitor of the transistor M5 will not be reduced. If the gate voltage of the transistor M5 is zero originally, the voltage V_{d4} will be pulled to positive rail through the transistors M5 and M6. If the gate voltage of the transistor M5 is at positive rail originally, the voltage V_{d4} will remain at ground as the it was being pulled to ground when the Clock signal is high. The drain voltage of the transistor M5 drives the clock-buffered inverter formed by the transistors M7-M9 and the output of the D flip-flop is the output of this inverter.

The operation speed of the TSPC D Flip-flop is affected by the large RC delay due to the stacked structures. However, the effect of transistor sizing is not evident, because most transistors are drivers and loads concurrently. The propagation delay can be reduced by increasing the sizes of clocked transistors M2, M4, M6 and M8. However, increasing the sizes of those transistors will increase the load capacitance to the clock driver and thus increase the power consumption. Table 5.3 shows the W/L ratios of transistors of two D flip-flops.

Transistor	0.8μm	0.5μm	Transistor	0.8μm	0.5μm
M1	4.8μ/0.8μ	3.6μ/0.6μ	M6	60μ/0.8μ	60μ/0.6μ
M2	20μ/0.8μ	15μ/0.6μ	M7	72μ/0.8μ	54μ/0.6μ
M3	14.4μ/0.8μ	30μ/0.6μ	M8	52μ/0.8μ	39.6μ/0.6μ
M4	20μ/0.8μ	15μ/0.6μ	M9	52μ/0.8μ	39.6μ/0.6μ

M5	20μ/0.8μ	15μ/0.6μ			

Table 5.3—W/L ratios of transistors of two D flip-flops.

Figure 5.7 and Figure 5.8 show the HSPICE simulation results of the TSPC D flip-flop. For the design using 0.8μm technology at 3 V power supply and 300 MHz clock signal, the setup time of the D flip-flop is 0.81ns and the hold time of the D flip-flop is 0.24ns. The minimum input voltage that this D flip-flop treats the input as high is 2.0V and the maximum input voltage that the D flip-flop treats the input as low is 1.2V. The current supply for this D flip-flop is 2.1 mA at 280 MHz operation.

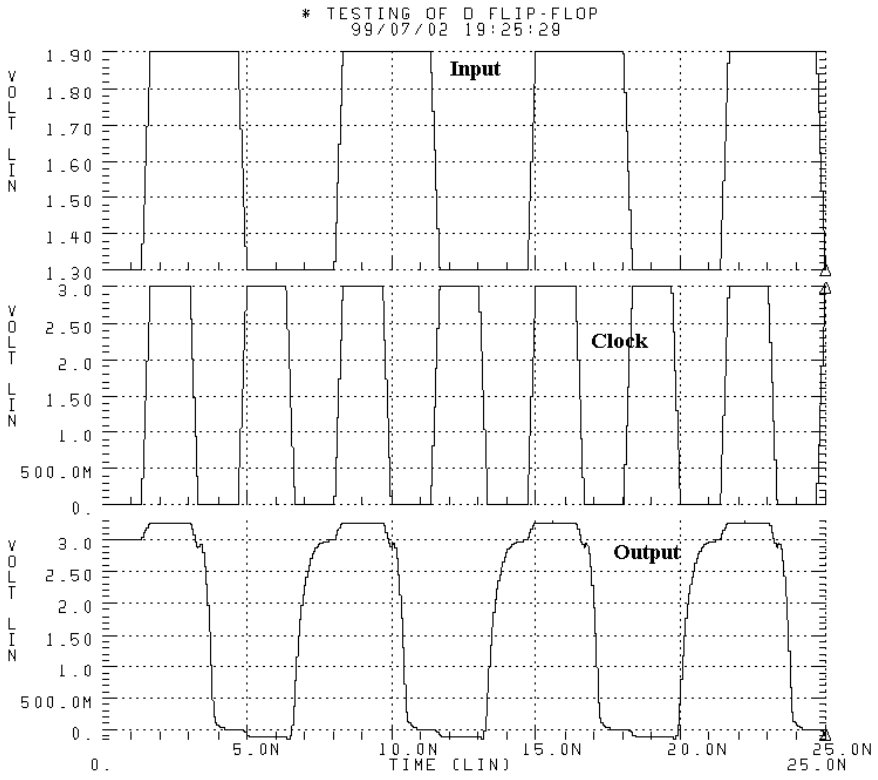


Figure 5.7—HSPICE simulation result (input voltage) of the TSPC D flip-flop.

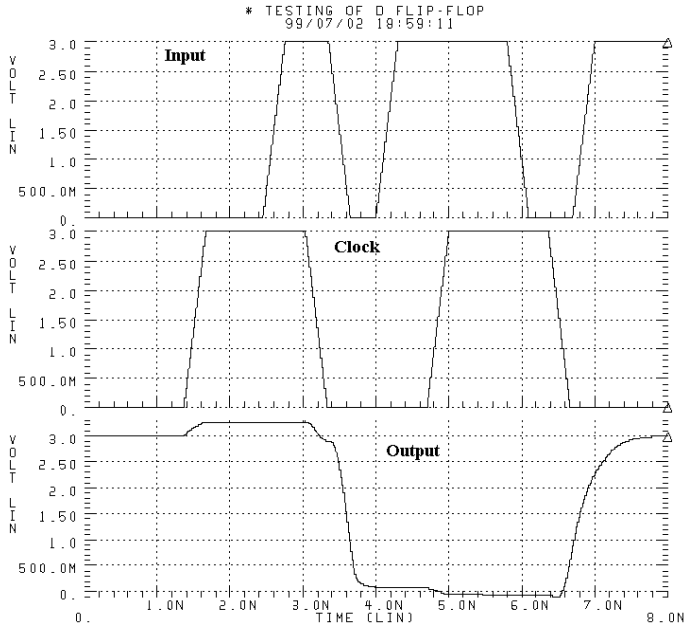


Figure 5.8—HSPICE simulation result (Setup/Hold time) of the TSPC D flip-flop.

For the design using 0.5μm technology at 3 V power supply and 300 MHz clock signal, the setup time of the D flip-flop is 0.6ns and the hold time of the D flip-flop is 0.32ns. The minimum input voltage that this D flip-flop treats the input as high is 1.9V and the maximum input voltage that the D flip-flop treats the input as low is 1.3V. The current supply for this D flip-flop is 1.8 mA at 280 MHz operation. Table 5.4 shows the summarized simulation results of the two designed D flip-flops.

	0.8μm	0.5μm
Operation frequency	300 MHz	300 MHz
Setup time	0.81 ns	0.6 ns
Hold time	0.24 ns	0.32 ns
Minimum high input voltage	2 V	1.9 V
Maximum low input voltage	1.2 V	1.3 V
Current supply at 3 V & 280 MHz	2.1 mA	1.8 mA

Table 5.4—Summary of the simulation results of the D flip-flops.

5.4 Feedback DAC Design

A feedback DAC is required for continuous-time Gm-C implementation of the ΣΔ modulator. The DAC should be linear and fast, therefore, a 1-bit quantizer architecture is chosen and hence a 1-bit DAC are designed. The feedback DAC for the ΣΔ modulator using 0.8μm is implemented by a simple differential-pair to convert the output voltage to a current level. The adder is done by current addition of the Gm-cell current output and the current output of the DAC. Figure 5.9 shows the schematic of the Gm-cell with the feedback DAC. The effective feedback voltage is determined by the feedback current level of the DAC. In this 0.8μm design, an effective feedback voltage of 1 V has been chosen and hence the DAC feedback current level was chosen to be 260 μA at 3 V differential-pair input.

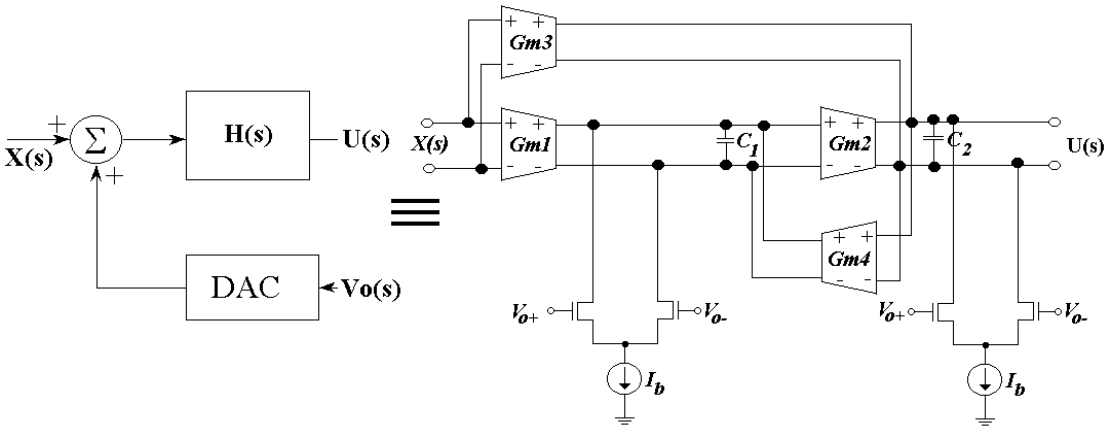


Figure 5.9—Differential-pair as feedback DAC in the ΣΔ modulator.

The feedback DAC for the ΣΔ modulator using 0.5μm is implemented by parallel one more DAC transistor to the input transistor of the triode-region Gm-cell. The adder is done by current addition of the triode-region Gm-cell current output and the current output of the DAC transistor. shows the schematic of the simplified triode-region Gm-cell with the feedback DAC. In this 0.5μm design, an effective feedback

voltage of 0.1 V has been chosen and hence the DAC feedback current level was chosen to be 66.9 μA at 3 V differential-pair input.

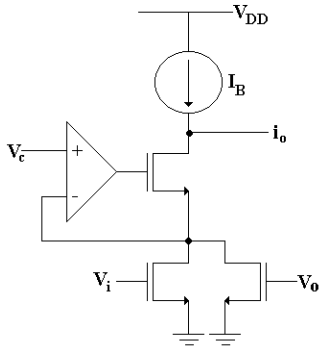


Figure 5.10—Simplified triode-region Gm-cell with feedback DAC transistor.

5.5 Delay cells in one-delay ΣΔ modulator

A main difference between the zero-delay ΣΔ modulator and the one-delay ΣΔ modulator is that the one-delay design requires its loop-delay exactly equals to a sampling period T. In our second design, a one-delay ΣΔ modulator is implemented. The delay cell for the modulator is an inverter chain. The inverter chain is actually served two functions: as a delay cell and as an output buffer. The inverter chain consists of six inverters. The first two inverters are smaller in size in order to reduce the loading to the D flip-flop. The other four inverters are larger in size in order to have enough driving power to drive the output.

Parameters	PMOS W/L	NMOS W/L
Large Inverter	216μ/0.6μ	108μ/0.6μ
Small Inverter	72μ/0.6μ	36μ/0.6μ

Table 5.5—Summary of the inverter sizes in the inverter chain.

5.6 Quantizer simulation

The quantizer consists of a latched-type comparator and two TSPC D Flip-flops. Figure 5.11 and Figure 5.12 show the HSPICE simulation results of the quantizer responding to a sinusoidal input and an input-testing vector respectively. The quantizers for both the 0.8μm technology design and the 0.5μm technology design are operating at 320 MHz Clock signal with similar performance. The current supply to the 0.8μm quantizer is around 7 mA and the current supply to the 0.5μm quantizer is around 6.2 mA.

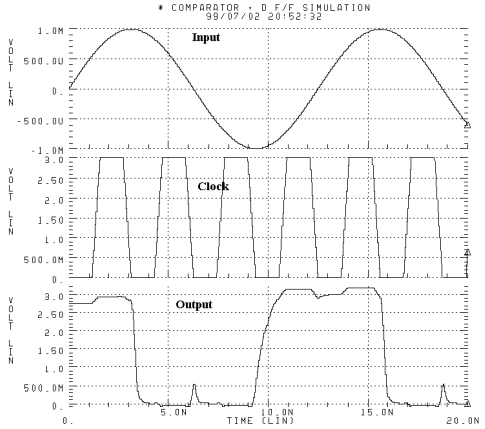


Figure 5.11—HSPICE simulation result (sinusoidal 80 MHz input + 320 MHz Clock input) of the quantizer.

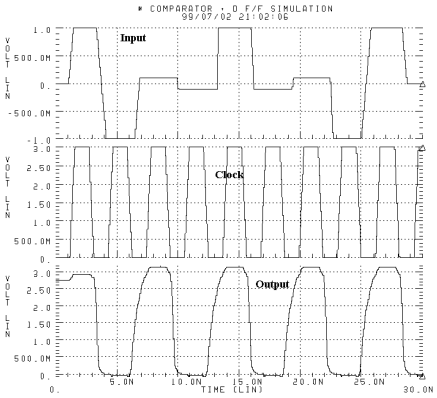


Figure 5.12—HSPICE simulation result (input testing vector + 320 MHz Clock input) of the quantizer.

Chapter 6 The ΣΔ modulator prototype

6.1 Circuit simulation of zero-delay ΣΔ modulator

HSPICE circuit simulations of the zero-delay band-pass ΣΔ modulator will be shown. The circuit building block diagram of the ΣΔ modulator is shown in Figure 6.1. The circuits are being designed using HP 0.8μm technology. A full circuit system simulation has been performed and the result is shown in Figure 6.2.

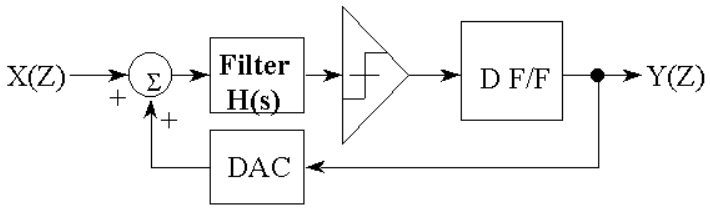


Figure 6.1—Circuit blocks in zero-delay ΣΔ modulator.

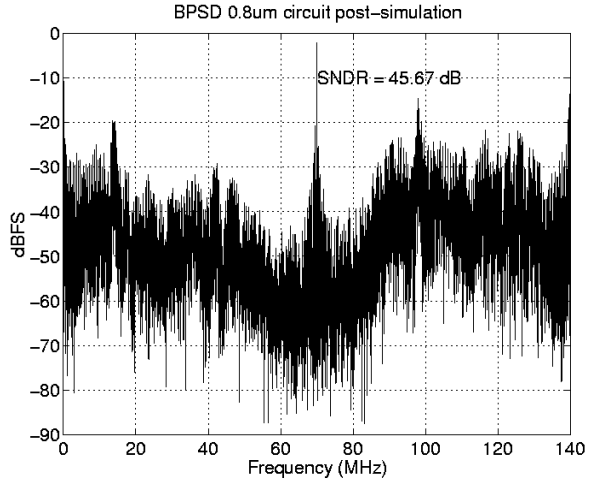


Figure 6.2—HSPICE circuit simulation of the zero-delay ΣΔ modulator.

The input signal is 200 mV amplitude sinusoidal 70.06 MHz signal. The feedback DAC voltage is 1 V. The SNDR of the prototype is 45.67 dB. The circuit simulation is close to the HSPICE ideal building block simulation with 2.6 ns loop-

delay. The non-zero delay in the circuit is due to the delay of the comparator and the D flip-flop are non-zero.

6.2 Layout of the zero-delay ΣΔ modulator

Figure 6.3 shows the layout of the Gm-C loop-filter using source-degeneration Gm-cells. G_{m1} and G_{m3} need good matching as they are the input Gm-cells. G_{m2} and G_{m4} need good matching as they are used to build the gyrator. C1 and C2 are divided into two smaller capacitors for matching purpose. The area of the filter is 145μm×X373μm.

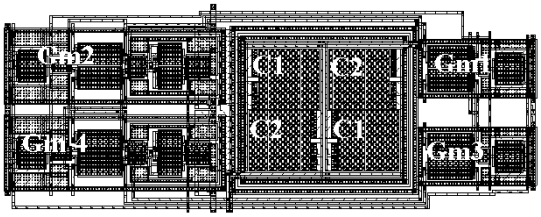


Figure 6.3—Layout of the Gm-C loop-filter using source-degeneration Gm-cells.

Figure 6.4 shows the layout of the zero-delay ΣΔ modulator and Figure 6.5 shows the chip photo of the fabricated circuit. The filter and the DAC are put closed together. The comparator, D flip-flops and inverters are digital circuitry, therefore, they are put a little bit apart from the analog filter. A guard ring is drawn outside the filter to prevent the digital noise affect the analog filter.

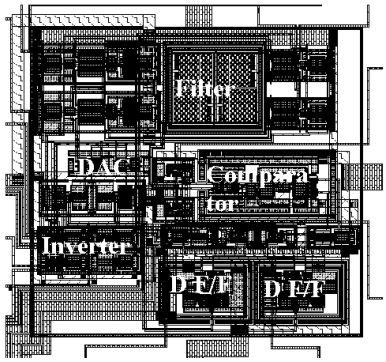


Figure 6.4—Zero-delay ΣΔ modulator layout.

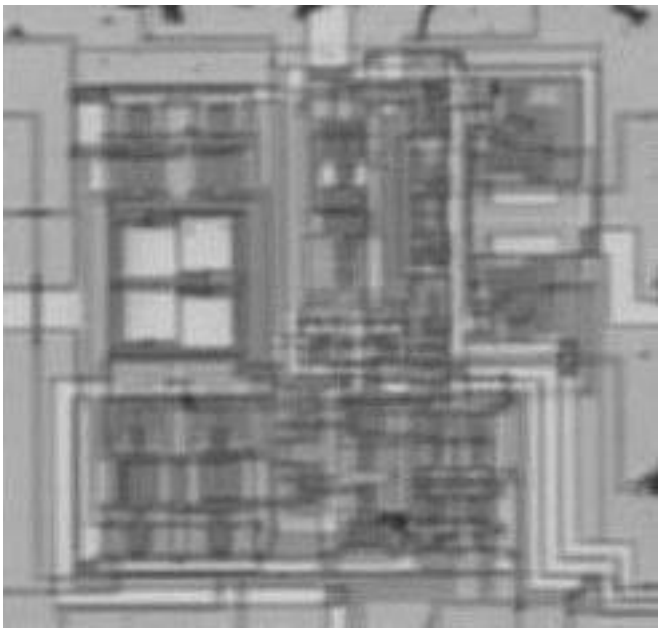


Figure 6.5—Chip photo of the zero-delay ΣΔ modulator.

Components	Area
Filter	145μm×X373μm
Comparator	194μm×92.4μm
D flip-flop	82.4μm×105.8μm
Inverter as output buffer	19.6μm×64.4μm
DAC	39.8μm×51.2μm
Total area	339.2μm×383.4μm

Table 6.1—Summary of the area of the layout for the zero-delay ΣΔ modulator.

6.3 Measurement results of the zero-delay ΣΔ modulator

Individual components such as the filter, the comparator and the D flip-flop measurement results will be presented first, then the whole zero-delay ΣΔ modulator measurement results will be presented. Firstly, the filter measurement results will be presented. Figure 6.6 and Figure 6.7 show the frequency tuning ability and Q tuning ability of the 0.8μm loop-filter.

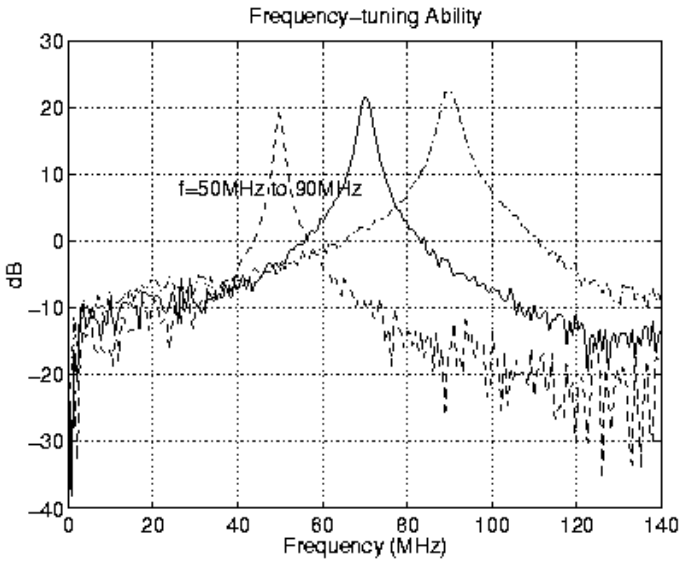


Figure 6.6—Frequency tuning ability of the 0.8μm loop-filter.

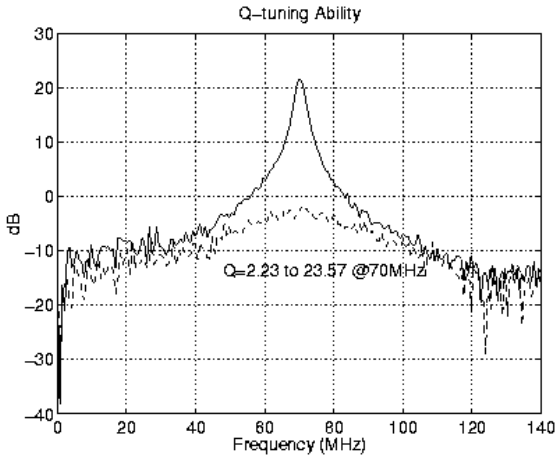


Figure 6.7—Q tuning ability of the 0.8μm loop-filter.

The filter can be tuned by varying the resistances of the degeneration resistors of the Gm-cells. From the measurement result, the filter can be tuned from 50 MHz to 90 MHz. The Q of the loop-filter can be tuned from as low as 2 to at least 23.57. Actually, the Q of the loop-filter can be tuned further. However, the filter is too sensitive that some perturbation will shift the Q to infinity at a value higher than 23.57 and then oscillation occurs. Therefore, the measurable Q is from 2 to 23.57. The measured gain of the filter at 70 MHz with Q equals to 23.57 is 21 dB. Figure 6.8 shows the measured loop-filter linearity. The 1-dB compression point of the filter is

measured to be –55 dBm and the IIP_3 is measured to be around 14 dBm. The current supply to the filter is 2.83 mA at 3 V power supply.

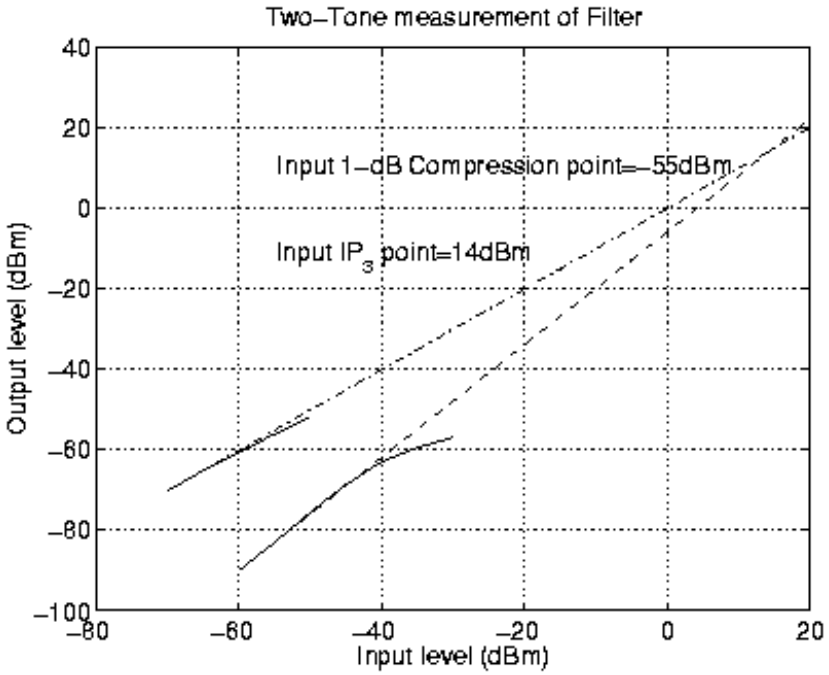


Figure 6.8—Measured 0.8µm loop-filter linearity.

Parameters	Performance
Center frequency	Tunable from 50 MHz to 90 MHz
Q	> 23.57
Gain at center frequency	> 21 dB
1-dB compression point	-55 dBm
IIP_3	~14 dBm
Current supply at 3 V	2.83 mA

Table 6.2—Summary of the measurement results of the 0.8µm loop-filter.

Secondly, the comparator performance will be presented. Figure 6.9 and Figure 6.10 show the measurement results of the 0.8µm comparator.

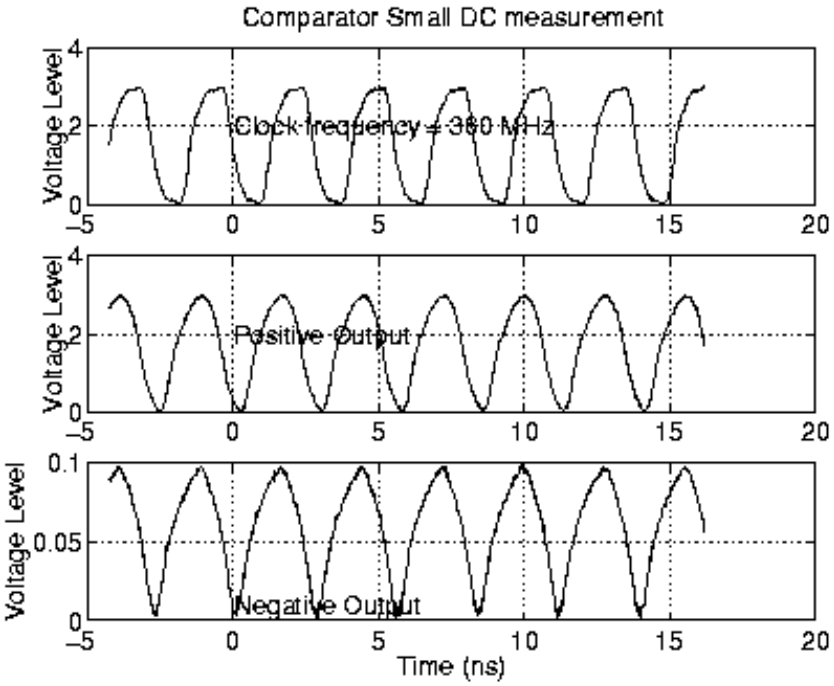


Figure 6.9—Constant DC difference input measurement for 0.8µm comparator.

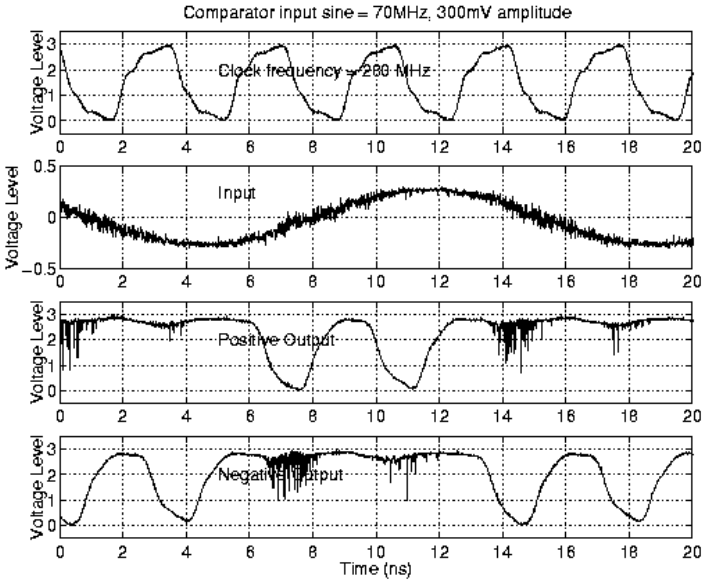


Figure 6.10—280 MHz sinusoidal input measurement for 0.8µm comparator.

The minimum DC difference input that the comparator could detect is 80 mV. And the highest operation frequency for the comparator is 360 MHz. Since an inverter has been added after the comparator, the measured output is inverted compared to the

output from the circuit simulations as shown in Figure 5.3. The current supply to the comparator is 2.88 mA.

Thirdly, the D flip-flop performance will be presented. Figure 6.11, Figure 6.12 and Figure 6.13 show the measurement results of 0.8µm D flip-flop.

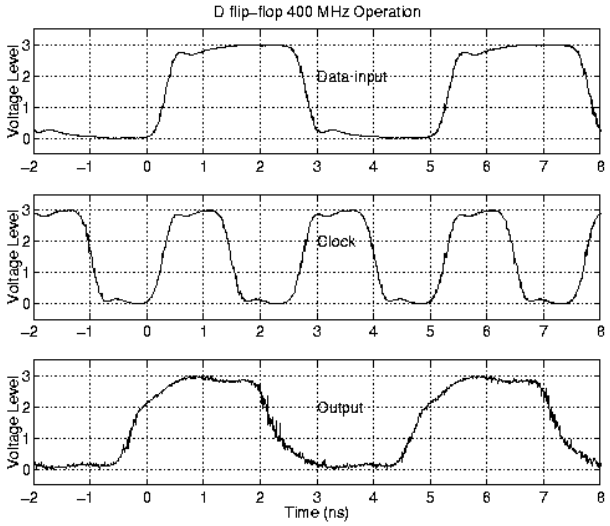


Figure 6.11—400 MHz operation measurements for 0.8µm D flip-flop.

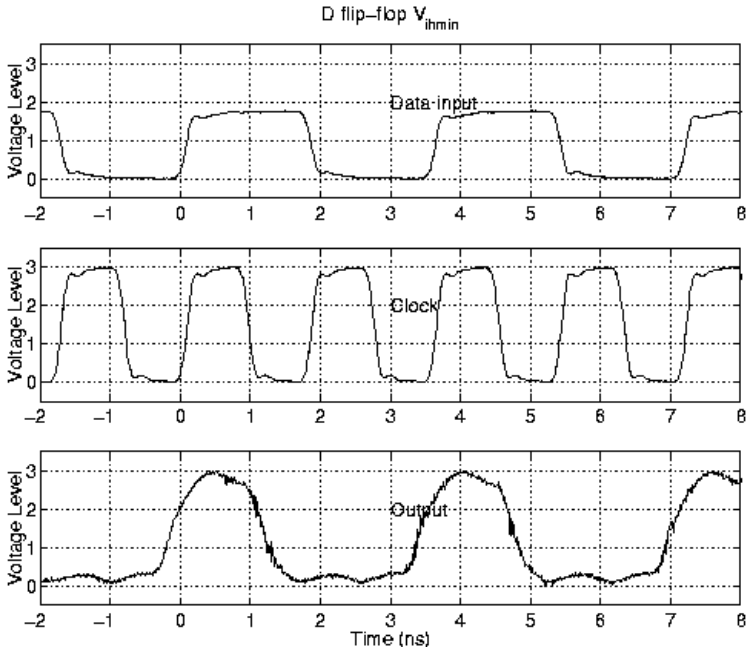


Figure 6.12—Minimum input high voltage level measurement for 0.8µm D flip-flop.

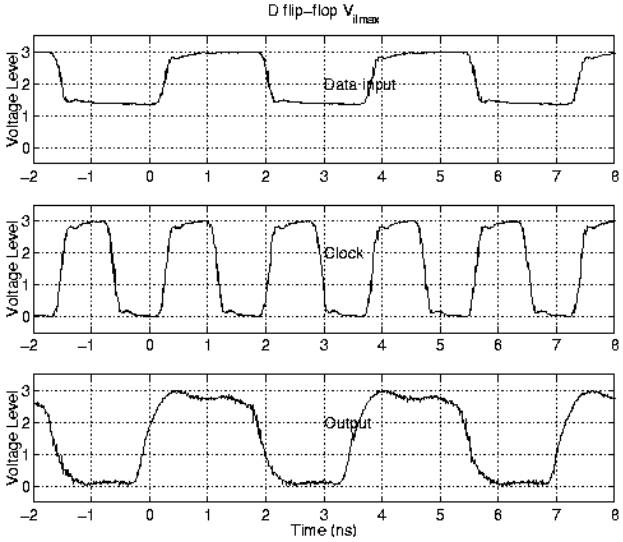


Figure 6.13—Minimum input low voltage level measurement for 0.8μm D flip-flop.

The highest operation frequency that this 0.8μm D flip-flop can operate is 400 MHz. The minimum high input voltage is 1.78 V and the maximum input low voltage is 1.35 V. The setup time of the D flip-flop is measured as 0.5 ns and the hold time of the D flip-flop is measured as 0.19 ns. The current supply of the D flip-flop is 2.1 mA.

Finally, the zero-delay ΣΔ modulator measurements will be presented. Figure 6.14 and Figure 6.15 show the measurement results of the zero-delay ΣΔ modulator.

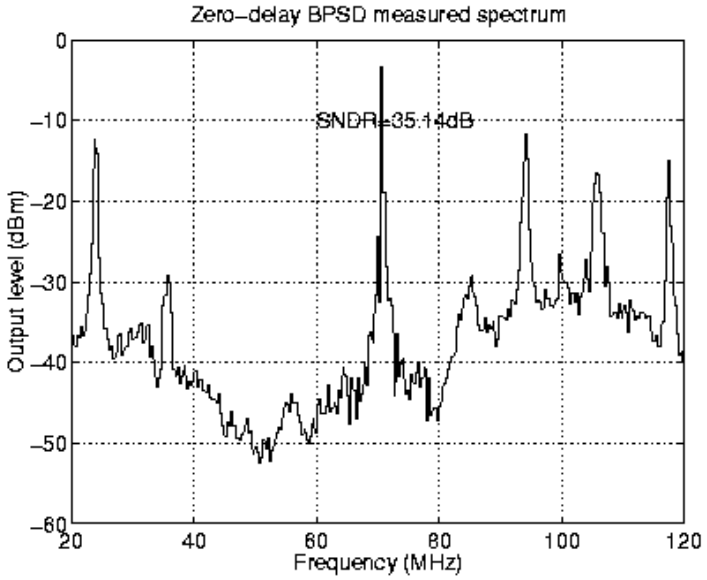


Figure 6.14—Measurement result of the zero-delay ΣΔ modulator.

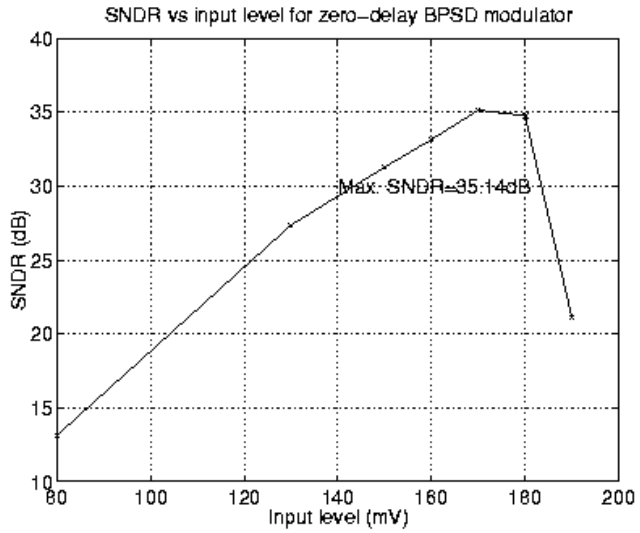


Figure 6.15—SNDR vs input level for the zero-delay ΣΔ modulator.

The best SNDR that the fabricated zero-delay ΣΔ modulator can achieve is 35.14 dB, which is equivalently 5.9 bits of resolution. Also, the SNDR is linearly decreasing with decreasing input level. The maximum SNDR occurs at the 170 mV input signal level. The current supply to the modulator is around 10 mA.

6.4 Circuit simulation of one-delay ΣΔ modulator

In this section, several HSPICE simulations of the band-pass ΣΔ ADC prototype will be shown. The circuit building block diagram of the ΣΔ ADC is shown in Figure 6.16. The following prototypes are being simulated:

- the comparator and the D flip-flop are real circuits; the Gm-cells, the DAC and the adder are ideal elements.
- the Gm-cells are real circuits; the comparator, the D flip-flop, the DAC and the adder are ideal elements.
- all building blocks are real circuits.

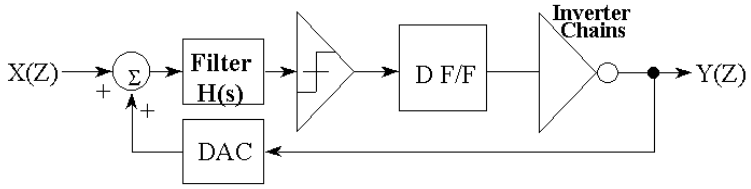


Figure 6.16—Circuit building block diagram of the ΣΔ ADC.

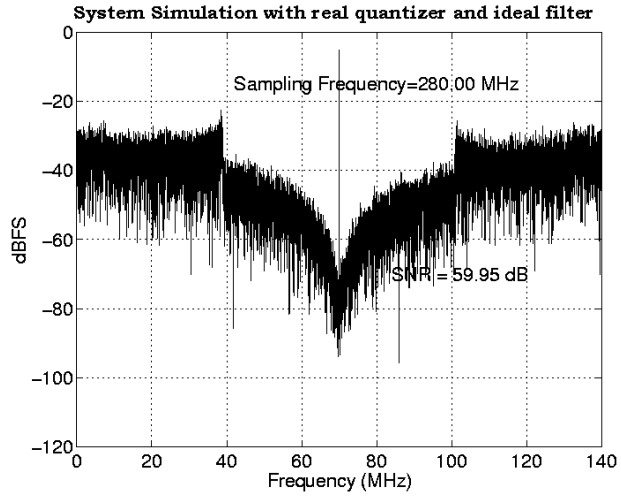


Figure 6.17—HSPICE simulation of the ΣΔ ADC with ideal loop-filter, DAC, adder and real quantizer circuit.

Figure 6.17 shows the HSPICE simulation result of the ΣΔ modulator with a real circuit quantizer (the comparator, the D Flip-flop, and the inverter chains) and other ideal building blocks (the loop-filter, the DAC and the adder). The SNDR of the prototype is 59.95 dB with 50mV amplitude sinusoidal 70.05 MHz signal input and 100mV feedback DAC voltage.

Figure 6.18 shows the HSPICE simulation result of the ΣΔ ADC with real circuit loop-filter and other ideal building blocks (the comparator, the D Flip-flop, the inverter chains, the DAC and the adder). The SNDR of the prototype is 56.40 dB with 50mV amplitude sinusoidal 70.05 MHz signal input and 100mV feedback DAC voltage.

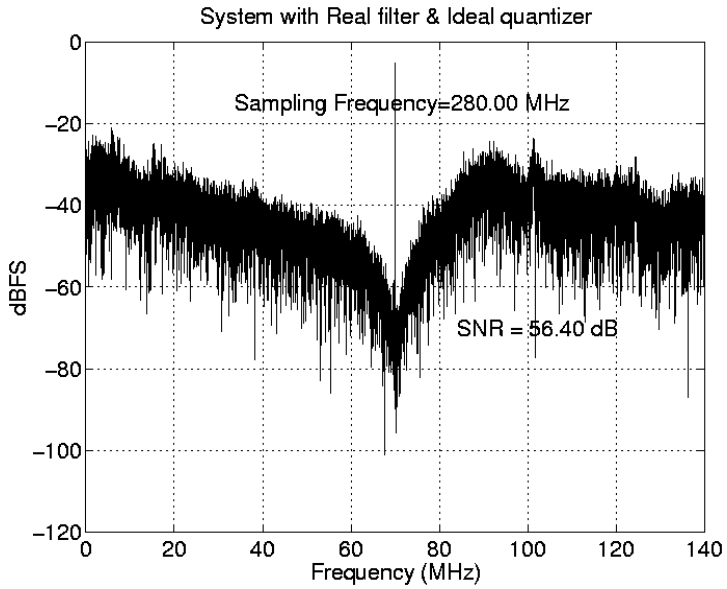


Figure 6.18—HSPICE simulation result of the ΣΔ ADC with real filter and other ideal building blocks.

Figure 6.19 shows a HSPICE simulation of the full circuit implementation of the ΣΔ modulator prototype. The input signal is a 70.05 MHz 50 mV amplitude sinusoidal. The feedback DAC voltage is 100 mV. The SNDR of the prototype is 50.15 dB.

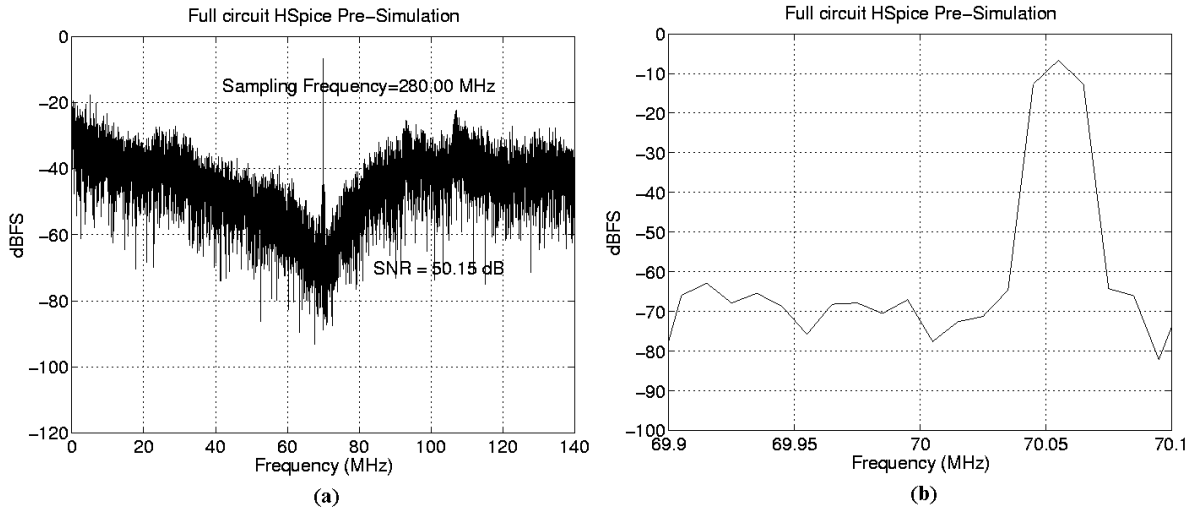


Figure 6.19—HSPICE simulation result of full circuit ΣΔ modulator (70.05 MHz input). (a) Full spectrum, (b) In-band (200kHz) spectrum.

The HSPICE circuit simulation result using ideal filter with real quantizer is 2.5 dB less than that of the HSPICE ideal building block simulation. The 3 dB difference may come from the non-idealities in the quantizer itself. The HSPICE circuit simulation result using real filter and ideal quantizer is 6 dB less than that of the HSPICE ideal building block simulation. The 6 dB difference may come from insufficient Q of the loop-filter. Finally, for all real circuit, there are 12 dB difference between the circuit and the ideal building block simulation. The difference may come from the combined effect of the two problems described above.

6.5 Layout of the one-delay ΣΔ modulator

Figure 6.20 and Figure 6.21 show the layout of the loop-filter and the whole one-delay band-pass ΣΔ modulator respectively. G_{m1} and G_{m3} need good matching as they are the input Gm-cells. G_{m2} and G_{m4} need good matching as they are used to build the gyrator. The design uses linear capacitors to implement capacitors C1 and C2. The analog and digital parts are separated and a guard ring is drawn to surround the filter to prevent the analog filter affected by the digital noise. The area of the filter is 434.6μm×229.4μm and the area of the whole one-delay ΣΔ modulator is 856.7μm×420.9μm.

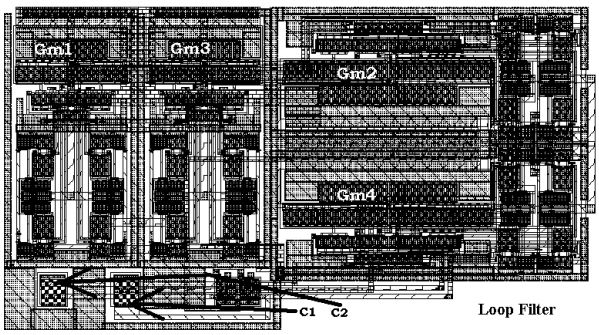


Figure 6.20—Layout of the loop-filter.

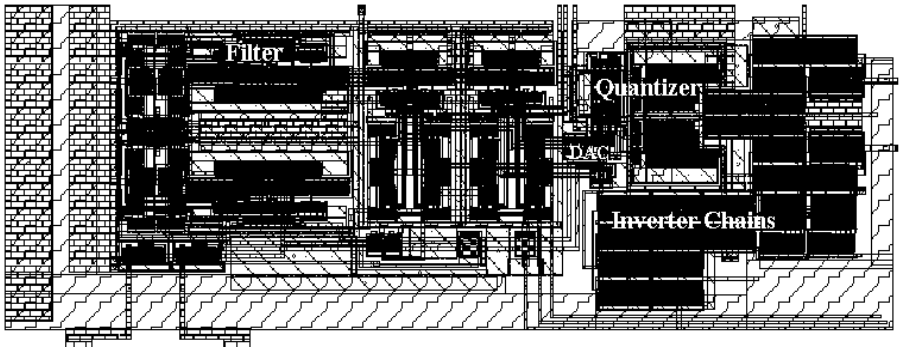


Figure 6.21—Layout of the ΣΔ ADC.

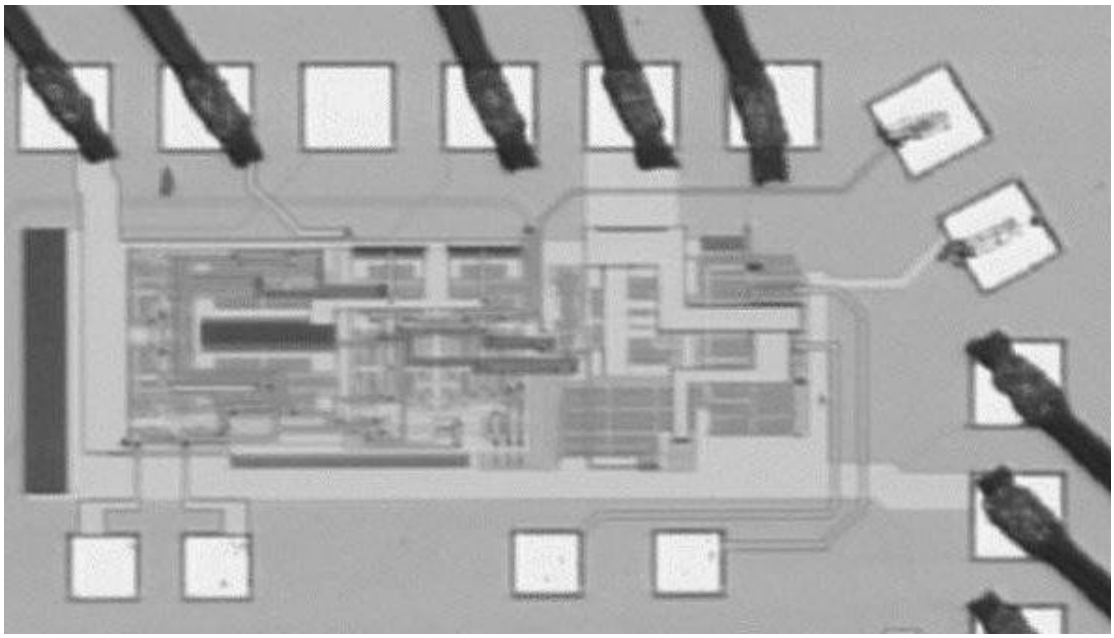


Figure 6.22—Chip photo of the one-delay ΣΔ modulator.

Components	Area
Filter	434.6μm×229.4μm
Comparator	46.8μm×101μm
D flip-flop	94.4μm×60.6μm
Inverter in inverter chains	53.1μm×31.8μm
DAC	11.7μm×11.9μm
Total area	856.7μm×420.9μm

Table 6.3—Summary of the area of the layout for the one-delay ΣΔ modulator.

6.6 Measurement results of the one-delay ΣΔ modulator

Individual components such as the filter, the comparator and the D flip-flop measurement results will be presented first, then the whole one-delay ΣΔ modulator measurement results will be presented. Firstly, the filter measurement results will be presented. Figure 6.23 and Figure 6.24 show the frequency tuning ability and Q tuning ability of the 0.5μm loop-filter.

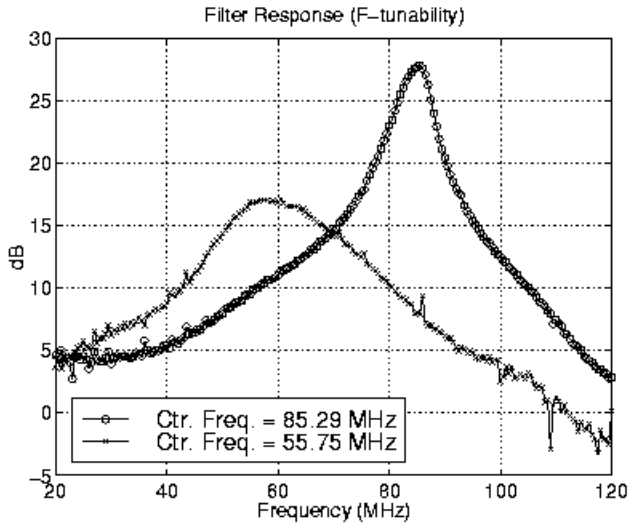


Figure 6.23—Frequency tuning ability of the 0.5μm loop-filter.

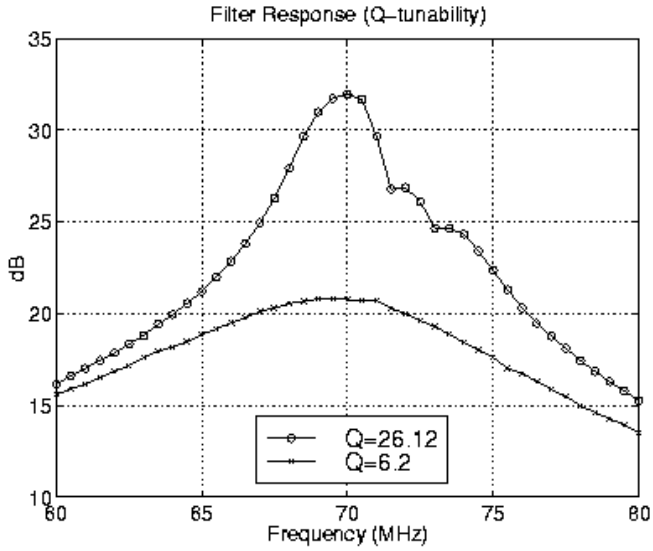


Figure 6.24—Q tuning ability of the 0.5μm loop-filter.

The filter can be tuned by varying the reference voltage V_c of the of the Gm-cells. From the measurement result, the filter can be tuned from 55.75 MHz to 85.29 MHz. The Q of the loop-filter can be tuned from as low as 6 to at least 26.12. Actually, the Q of the loop-filter can be tuned further. However, the filter is too sensitive that some perturbation will shift the Q to infinity at a value higher than 26.12 and then oscillation occurs. Therefore, the measurable Q is from 6 to 26.12. The measured gain of the filter at 70 MHz with Q equals to 26.12 is 32 dB. Figure 6.25 shows the measured loop-filter linearity. The 1-dB compression point of the filter is measured to be –43 dBm and the IIP_3 is measured to be –26.3 dBm. The current supply to the filter is 9.5 mA at 3 V power supply.

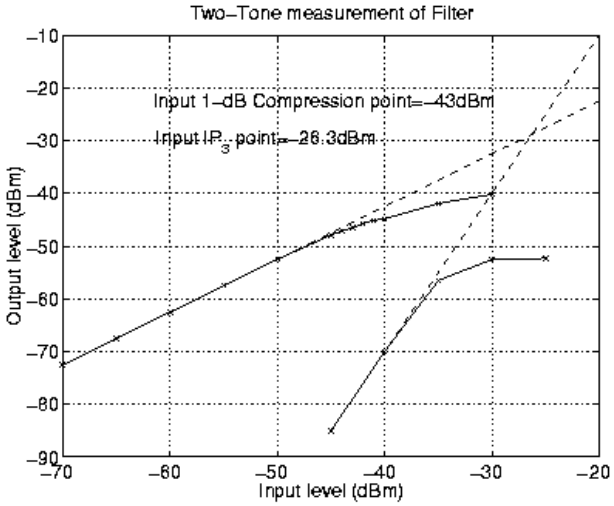


Figure 6.25—Measured 0.5µm loop-filter linearity.

Parameters	Performance
Center frequency	Tunable from 55.75 MHz to 85.29 MHz
Q	> 26.12
Gain at center frequency	> 32 dB
1-dB compression point	-43 dBm
IIP_3	-26.3 dBm
Current supply at 3 V	9.5 mA

Table 6.4—Summary of the measurement results of the 0.5µm loop-filter.

Secondly, the comparator performance will be presented. Figure 6.26 and Figure 6.27 show the measurement results of the 0.5µm comparator.

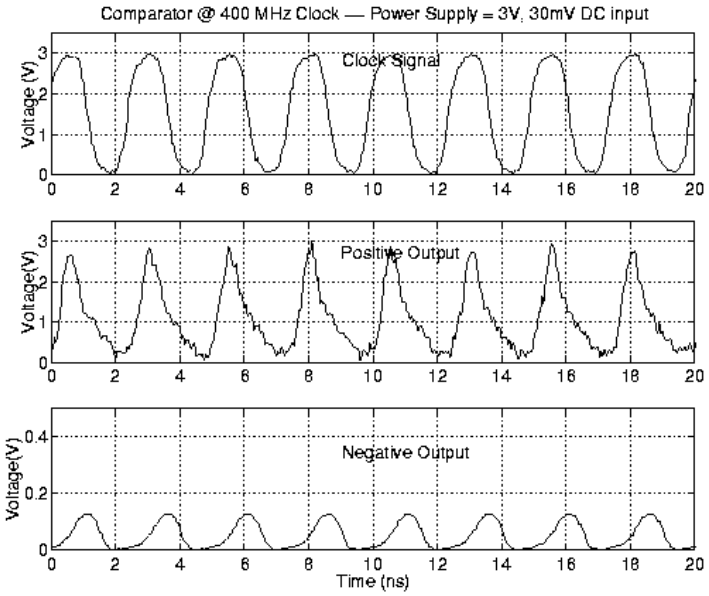


Figure 6.26—Constant DC difference input measurement for 0.5µm comparator.

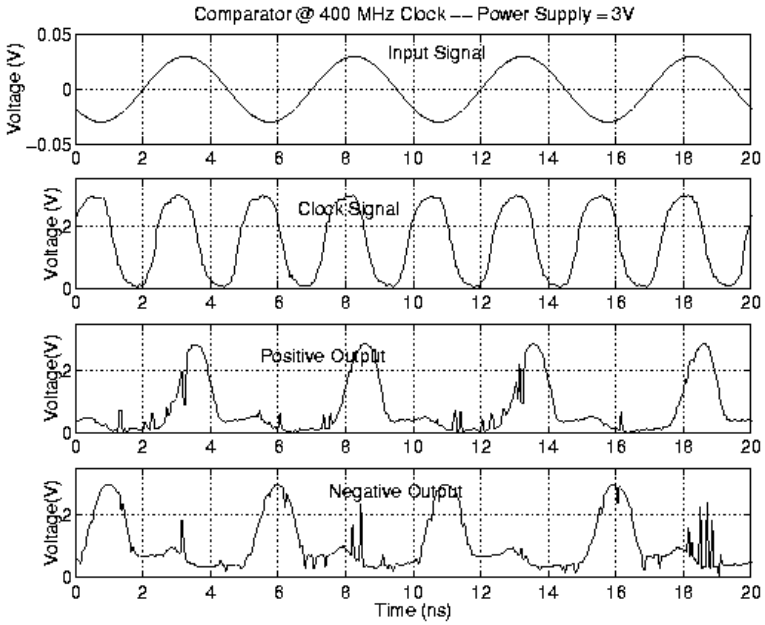


Figure 6.27—400 MHz sinusoidal input measurement for 0.5µm comparator.

The minimum DC difference input that the comparator could detect is 30 mV. And the highest operation frequency for the comparator is 400 MHz. The rising time delay t_{dr} and the falling time delay t_{df}, of the comparator is measured as 0.4 ns and 0.2

ns respectively. The rising time and the falling time is measured as 0.5 ns and 0.2 ns respectively. The current supply at 3 V at 280 MHz operation is 2.36 mA.

Parameters	Performance
Operation frequency	400 MHz
Rising time delay	0.4 ns
Falling time delay	0.2 ns
Rising time	0.5 ns
Falling time	0.2 ns
Current supply at 3 V at 280 MHz	2.36 mA

Table 6.5—Summary of the measurement result of 0.5µm comparator.

The comparator can also operate under 2.5 V power supply, Figure 6.28 shows the measurement result of the comparator operating at 2.5 V power supply. Table 6.6 shows the summary of the measurement result of 0.5µm comparator operating at 2.5 V power supply.

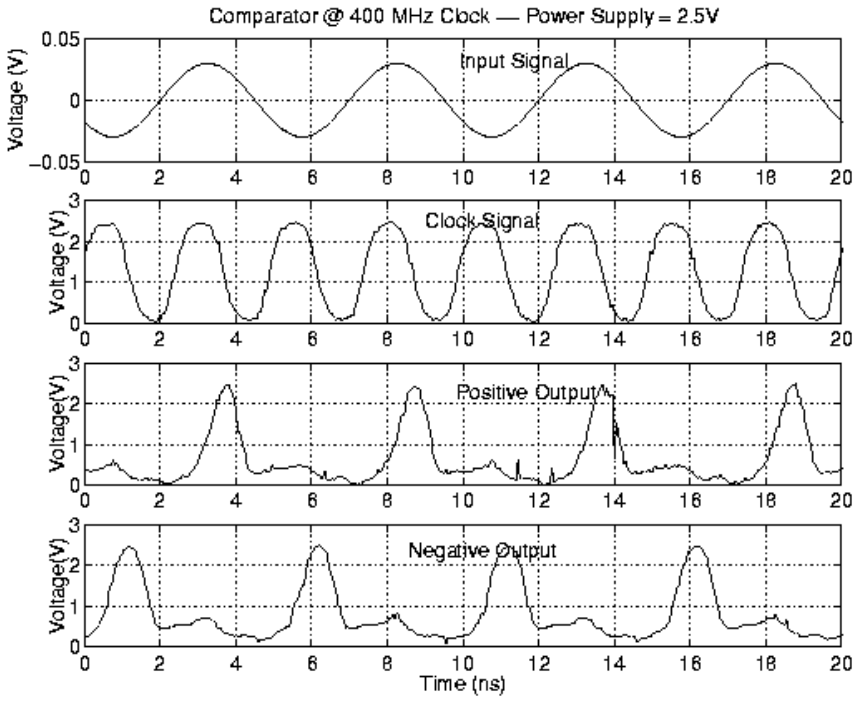


Figure 6.28—0.5µm comparator operating at 2.5 V power supply.

Parameters	Performance
Operation frequency	400 MHz
Rising time delay	0.54 ns
Falling time delay	0.3 ns
Rising time	0.7 ns
Falling time	0.3 ns
Current supply at 2.5 V at 280 MHz	2.2 mA

Table 6.6—Summary of the measurement result of 0.5µm comparator operating at 2.5 V power supply.

Thirdly, the D flip-flop performance will be presented. Figure 6.29, Figure 6.30 and Figure 6.31 show the measurement results of 0.5µm D flip-flop.

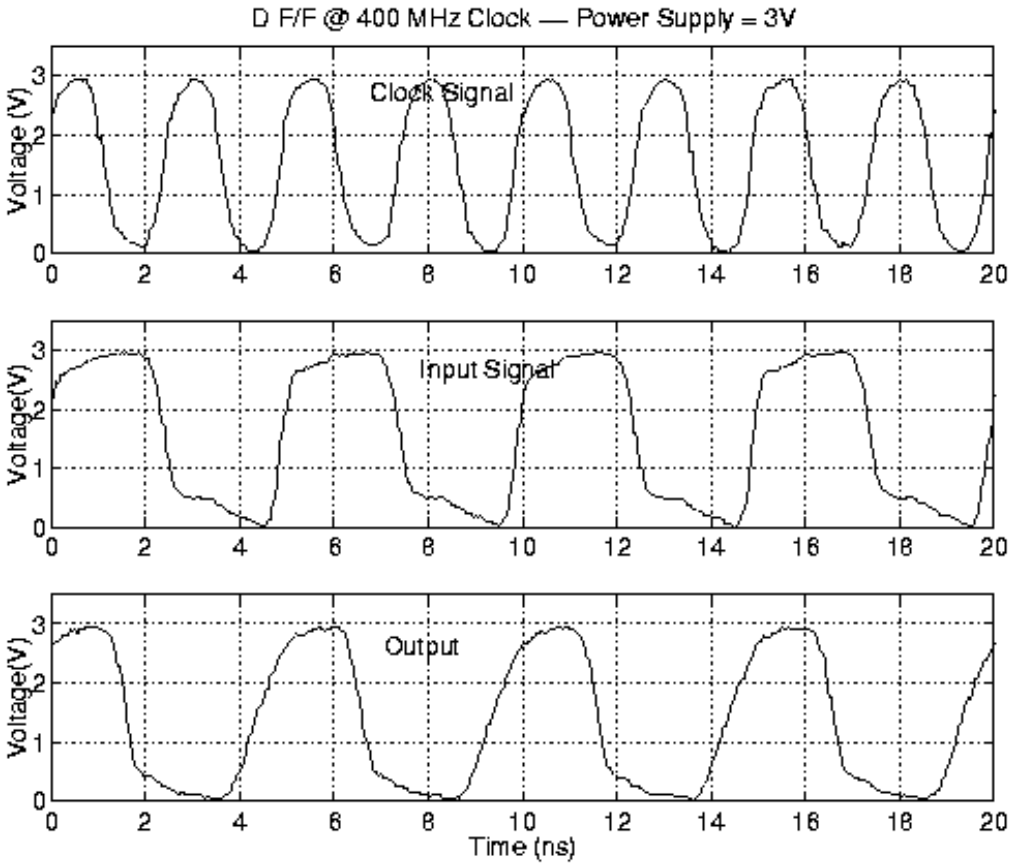


Figure 6.29—400 MHz operation measurements for 0.5µm D flip-flop.

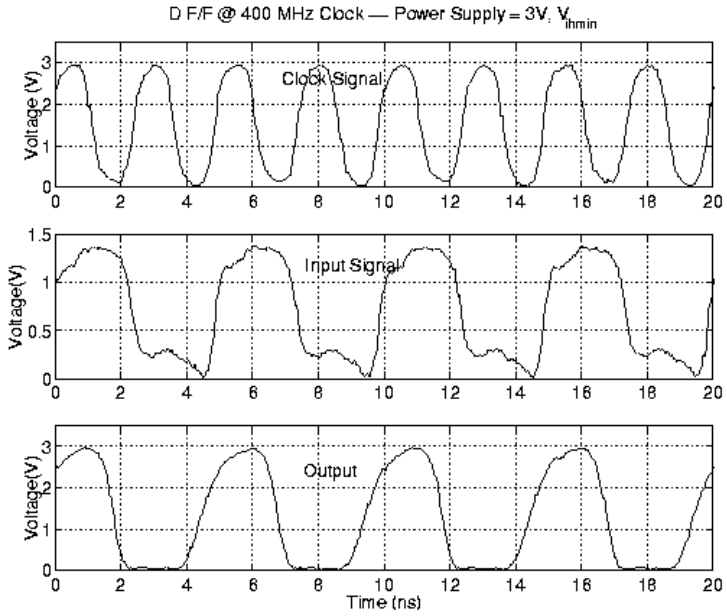


Figure 6.30—Minimum input high voltage level measurement for 0.5µm D flip-flop.

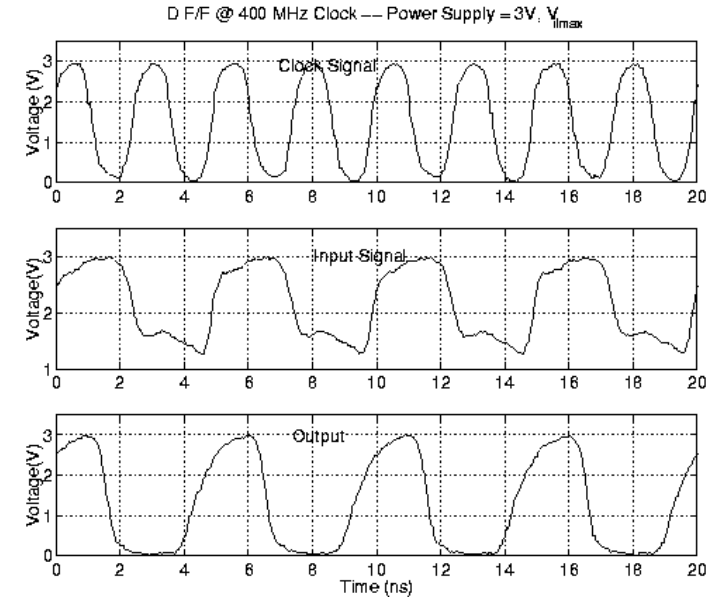


Figure 6.31—Minimum input low voltage level measurement for 0.5µm D flip-flop.

The highest operation frequency that this 0.5µm D flip-flop can operate is 400 MHz. The minimum high input voltage is 1.4 V and the maximum input low voltage is 1.25 V. The setup time of the D flip-flop is measured as 0.17 ns and the hold time of the D flip-flop is measured as 0.21 ns. The current supply to the D flip-flop is 1.57 mA at both 3 V power supply and 2.5 V power supply.

Finally, the zero-delay ΣΔ modulator measurements will be presented. Figure 6.32, Figure 6.33 and Figure 6.34 show the measurement results of the one-delay ΣΔ modulator.

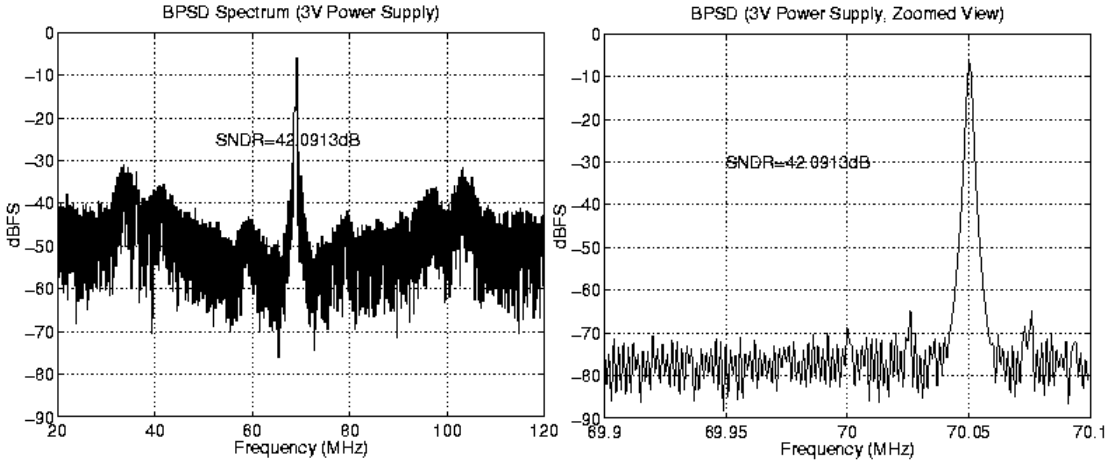


Figure 6.32—Measurement result of the one-delay ΣΔ modulator at 3 V power supply.

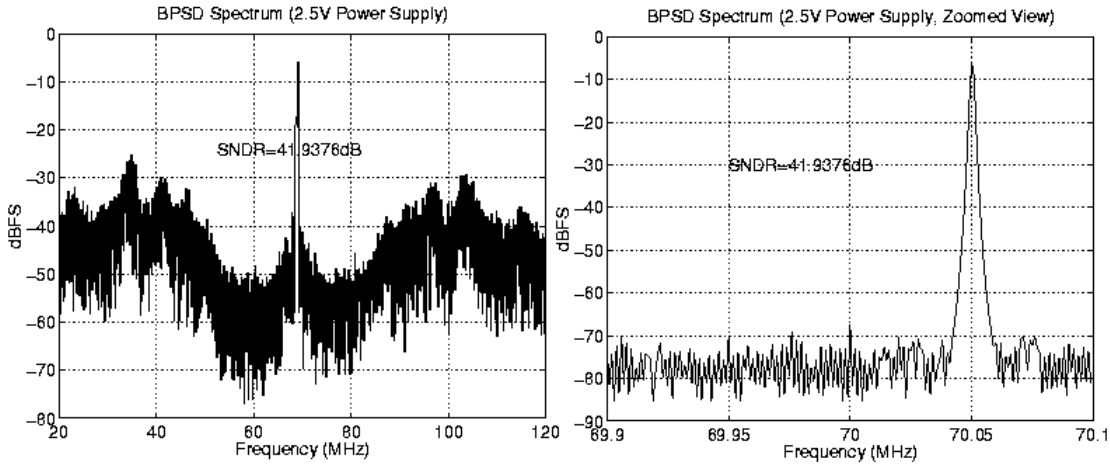


Figure 6.33—Measurement result of the one-delay ΣΔ modulator at 2.5 V power supply.

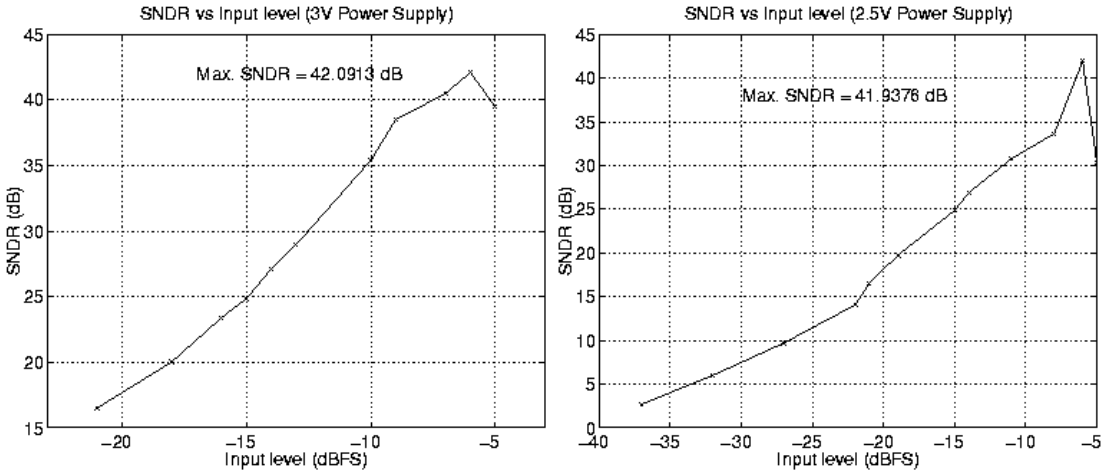


Figure 6.34—SNDR vs input level for the one-delay ΣΔ modulator.

The best SNDR that the fabricated one-delay ΣΔ modulator can achieve is 42.09 dB, which is equivalently 7.0 bits of resolution. Also, the SNDR is linearly decreasing with decreasing input level as shown in Figure 6.34. The maximum SNDR occurs at the 1dBm (or –6 dBFS) input signal level at 3 V power supply. The current supply to the modulator is 15.5 mA at both 3 V and 2.5 V power supply.

6.7 Summary of performances

Table 6.7 shows a summary of performances of two modulators.

Components	0.8μm	0.5μm
Filter		
Operation frequencies	50 – 90 MHz	55.75 – 85.29 MHz
Gain at 70 MHz	> 21 dB	> 32 dB
Q	> 23.57	> 26.12
1-dB compression point	-55 dBm	-43 dBm
IIP_3	14 dBm	-26.3 dBm
Current supply	2.83 mA	9.5 mA
Comparator		
Maximum operation frequency	360 MHz	400 MHz

Current supply	2.88 mA @ 3 V	2.36 mA @ 3 V, 2.2 mA @ 2.5 V
D flip-flop		
Maximum operation frequency	400 MHz	400 MHz
Setup time	0.5 ns	0.17 ns
Hold time	0.19 ns	0.21 ns
Current supply	2.1 mA	1.57 mA @ both 3 V and 2.5 V
ΣΔ modulator	Zero-delay	One-delay
Maximum achievable SNDR	35.14 dB	42.09 dB

Table 6.7—Summary of measurement results of two modulators.

Chapter 7 Conclusion

7.1 Conclusion

Two 70 MHz second-order continuous-time band-pass ΣΔ modulators have been fabricated and tested using 0.8μm and 0.5μm CMOS technology. They show out a high-speed data conversion at IF equals to 70 MHz. The current supply to the circuit is small implies the power consumption of the circuit is small also. Measured SNDR for 0.8μm design is 35.14 dB (5.9 bits of resolution) and for 0.5μm design is 42.09 dB (7 bits of resolution). However, there are some problems in the circuit.

The problem of the 0.8μm design are the non-symmetrical noise-shape and the low measured SNDR. The problems are due to the following reasons:

- insufficient linear range of the Gm-cell, and
- excess loop-delay in zero-delay modulator design.

Design	f_B	IF	SNDR	Power	Vdd	# of orders	Process
1 [24]	200 kHz	100 MHz	45 dB	330 mW	2.7/3.3 V	4^{th}-order	0.5μm CMOS
2 [25]	200 kHz	950 MHz	49 dB	135 mW	5 V	2^{nd}-order	0.5μm Bipolar
3 [12]	2 MHz	40 MHz	45 dB	65 mW	3.3 V	4^{th}-order	0.5μm CMOS
My design	200 kHz	70 MHz	42 dB 41.9 dB	47 mW 35 mW	3 V 2.5 V	2^{nd}-order	0.5μm CMOS

Table 7.1—ΣΔ modulators performance comparison.

Table 7.1 shows a performance comparison between different designs and my design. As not much work on 70 MHz modulator has been reported, a direct comparison cannot be made. However, we can still compare the performances of different modulators correspondingly.

My design can operate at 2.5 V power supply with only 35 mW power dissipation, which is small compared to other designs. Also, my design can achieve 42 dB SNDR by using only 2^{nd}-order architecture, which is already comparable to other 4^{th}-order designs.

7.2 Future Work

There are two possible future work that can be done to improve the ΣΔ modulator. Firstly, a fourth-order band-pass ΣΔ modulator may be worth for consideration as fourth-order band-pass ΣΔ modulator has better performance in terms of SNDR than second-order one. Secondly, a variable delay-cell can be introduced in the loop in order to adjust the loop-delay and study the loop-delay effect on the modulator. Thirdly, DAC feedback level (DAC gain) of the modulator system should be studied in detail.

Another future work is to integrate the modulator with the other building blocks of a wireless receiver to demonstrate the advantages of band-pass data conversion. This work is being done currently and another fabrication will be submitted in a soon time.

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