Design of CMOS Wide-band Switched-Capacitor Bandpass Filters

By

Ng Wai Hon

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Ng Wai Hon

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This is to certify that I have examined the above Mphil thesis
and have found that it is complete and satisfactory in all respects,
and that any and all revisions required by
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Abstract

For switched-capacitor (SC) circuits, power consumption is proportional to the number of the opamps used. In a classical filter design, two opamps are needed to realize a second-order biquadratic filter. Double-sampling pseudo-2-path technique can be used to implement a simple second-order biquadratic filter (resonator) with only one opamp. However, since no damping capacitor exits, such a double-sampling pseudo-2-path technique cannot be used to implement a wide-band SC filter.

On the other hand, demand for high data-rate integrated circuits has rapidly grown due to the technological development in many applications, such as WCDMA and WLAN. Signal bandwidths of these applications are from several MHz to several ten MHz. For low IF systems, the quality factor of the channel-selection bandpass filter becomes very low. At the same time, the filter needs to have sharp transition from passband to stopband in order to provide enough attenuation for adjacent channel signals, which cannot still be achievable with conventional low-Q SC bandpass filters.

In this project, two wide-band SC filters are designed. The first design aims at low-power and high-frequency filters for video applications. The second design focuses on achieving high roll-off for low-Q filter applications. Both designs are realized in a 0.35-μm CMOS process with V_{tp}=0.80V and V_{tn}=0.65V.

In the first project, a modified double-sampling pesudo-2-path technique has been proposed to implement a fully differential 3-V 44-MHz wideband bandpass filter. Using

only three opamps, the filter implements a 6^{th}-order bandpass response with a center frequency of 44MHz and a bandwidth of 6.28MHz (Q=7) with an effective sampling frequency of 176MHz. A 3-step variable gain is designed with each step being 6dB. The dynamic range is measured to be 57.3dB (@ 3% IM3), and the IIP3 is measured to be 27dBm at a voltage gain of –3dB. The proposed filter consumes a power of 92.5mW and an active chip area of 950um X 510um.

In the second project, a high roll-off wide-band SC bandpass filter employing a double-sampling technique is proposed. The post-simulation results show the proposed design achieves a 10-MHz center frequency with a bandwidth of 2.5MHz. The attenuation at 2.5-MHz away from the center frequency is larger than 35dB while consuming a total power of 99mW and a chip area of 2000um X 1000um. The fabrication of the filter is in progress.

Acknowledgment

It is my pleasure to take this opportunity to express my heartfelt gratitude to the people who have helped and supported me during this two years of Mphil studies. Without their support, my research would not been successfully completed on time.

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Chapter 1

Introduction

Electronic filters are used in all communication and signal processing circuitry. In many wireless receivers, intermediate frequency (IF) filters are needed as a channel selective function to filter out adjacent signals. Two filter specifications will be discussed, including 44-MHz SC bandpass filter and 10-MHz SC bandpass filter.

1.1 Background of Bandpass Filters

Due to technological development, the signals bandwidths become several MHz to several ten MHz. The baseband circuits have to handle the signal bandwidth that is more than 1MHz. Figure 1.1 illustrates a typical double-IF receiver architecture [1].

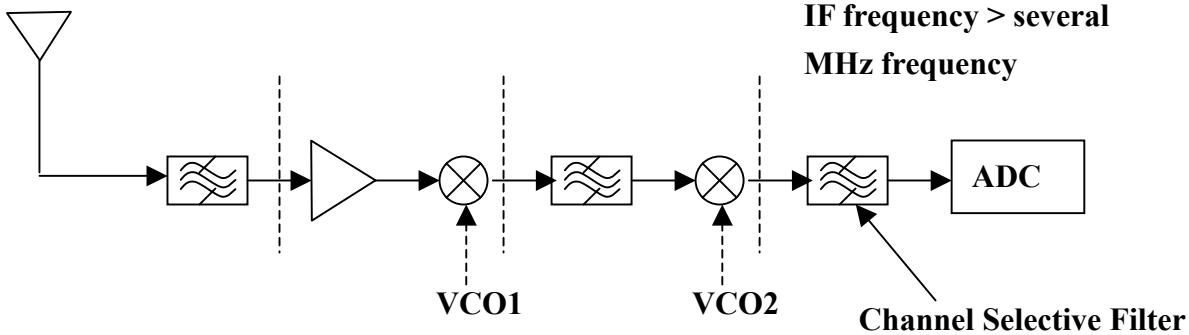


Figure 1.1 A simple double-IF receiver architecture

In this architecture, signals are downconverted into the low-IF range. Channel

selective filters are employed to select the wanted signals. The general requirements of channel selective filter are (1) it can be operated at high frequency range (MHz range to ten MHz range), (2) it should has a sharp transition from passband to stopband in order to get the wanted signals and filter out adjacent channels. (3) To accept different input signal levels, the dynamic range and linearity of filters should good enough for their application. Figure 1.2 shows the role of the channel selective filter in frequency domain. Nowadays, surface acoustic wave (SAW) filters [2] are employed to do the channel selection. The advantages of using SAW filters, are their stable center frequencies, a sharp transition from the passband to the stopband and no extra power is needed for operation. However, much power has to be supplied to drive the 50-Ω input impedance of these off-chip filters. The noise is coupled into the external connections. And the off-chip filters will increase the cost of the receivers. These motivate the design of on-chip filters.

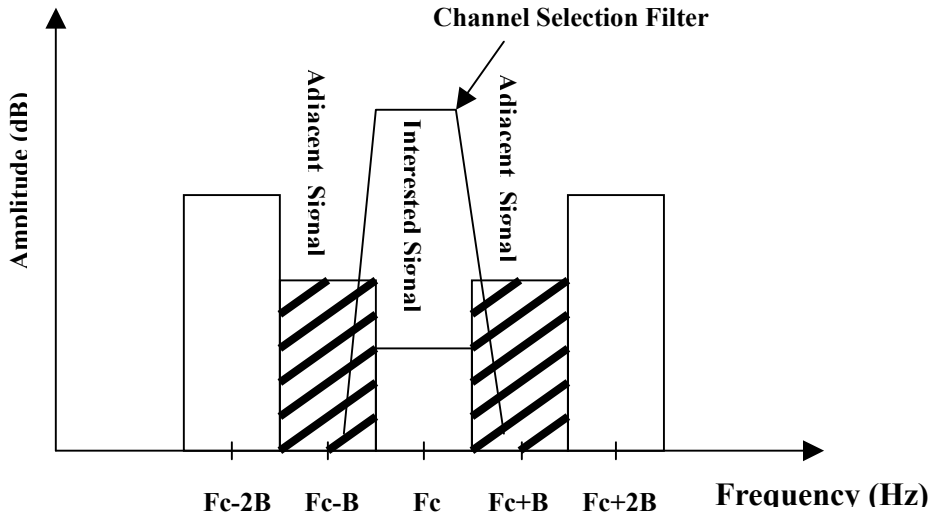


Figure 1.2 Function of channel selective filters

1.2 Choice of IF Filters

There are different kinds of on-bandpass filters, including simple RC filters, Gm-C filters and switched-capacitor filters. The simple RC filters suffer the variation of capacitors and resistors. And much bigger area is needed to lay the resistor. On the other hand, Gm-C also suffer the process variation of transistors and capacitors. Therefore, both of the filters need to employ automatic frequency-tuning and Q-tuning circuits to solve the mismatch problem. For switched-capacitor circuits, if the low-frequency gain and unity-gain frequency of the opamp is larger enough, transfer function only depends on the capacitor ratio and the linearity of the filter is also determined by the linearity of the capacitors. Two capacitors can be achieved an error of less than 0.1% matching in a standard CMOS technology. Therefore, SC filters achieve high performance.

In this project, two filters are designed for two different applications. One filter is for high frequency range. The other one is to achieve a sharp transition from passband to stopband.

1.3 Challenges of the 44-MHz SC Filter

The switched-capacitor filter is chosen to realize the 44-MHz bandpass filter due to

its characteristics. For portable applications, power consumption of the filters should be as low as possible to save power. However, for high frequency SC circuits, the power consumption is dominated by the opamp. The challenge of the first project is to design a bandpass SC circuit that consumes less power and maintain a good performance at the same time.

1.4 Challenges of the 10-MHz SC Filter

The maximum sampling frequency of conventional bandpass filters with a high roll-off characteristic are limited by the delay and subtract switched capacitors. The challenges of the second project are to design a SC filter that has a high roll-off characteristic and can be operated at high frequency range.

1.5 Thesis Overview

The conventional switched-capacitor bandpass design will be presented in chapter two, where the topology, capacitors values calculation and double-sampling technique of SC circuits will be given.

In chapter three, the drawback of the conventional single-sampling pseudo-2-path technique and double-sampling pseudo-2-path technique will be investigated. The proposed doubled-sampling pseudo-2-path technique is employed to realize a wide-band SC bandpass filter. The system level simulation of the bandpass filter is verified by SWITCAP2 simulator.

The transistor level implementation of the 44-MHz SC bandpass filter in standard CMOS process is presented in Chapter four. A single-stage opamp is chosen to achieve a low-frequency gain of 67dB with a unity-gain bandwidth of 900MHz. The pre-simulations of the 44-MHz SC bandpass filter are simulated by Hspice and are presented.

The layout consideration and post-simulation results of the 44-MHz SC bandpass filter are presented in Chapter five. Some layout technique and considerations are given to minimize non-ideal effects.

Chapter six discusses the testing results and methodologies of the 44-MHz SC bandpass filter. The measurement results show the designed filter achieves the center frequency of 44MHz and is operated up to 176-MHz sampling frequency.

In chapter seven, the limitation of the conventional SC bandpass filter will be discussed. In the system level, the wide-band SC bandpass filter with a high roll-off characteristic is proposed. In the circuit level, the novel highpass filter will be proposed to achieve higher sampling rate. The system level simulation of the filter is simulated by SWITCAP2.

The layout consideration and post-simulation results of the SC bandpass filter are presented in Chapter eight.

Reference

[1] Behzad Razavi, RF microelectronics, *Upper Saddle River, NJ : Prentice Hall PTR,* c1998

[2] Data Sheet X 6965D, www.epcos.com

Chapter 2

Synthesis of Classical Double-Sampling SC Bandpass Filter

Switched-capacitor (SC) bandpass filters can be implemented by using simple biquadratic filters or ladder highpass filters with an N-path technique [1][2]. Although the ladder filter is insensitive with the element variation, biquadratic filters [3] [4] are more attractive than ladder filters at the frequencies in a mega-hertz range. The primary reason is that ladder filters include many loops that will degrade the speed of the filters. Because biquadratic filters can employ double-sampling technique [5], the required unity-gain frequency of the opamp can be reduced by 2.

To design a high-speed SC filter, the biquadratic filters will be investigated in the first section of this chapter. The double-sampling technique will be discussed in the next section. In the last section, the case of sampling frequency equal to four times the center frequency will be discussed.

2.1 Specification of SC Bandpass Filter

The biquadratic banpass filter structure is chosen due to its characteristics. In order to reduce the capacitor spread of the whole filter, a cascading of three second-order bandpass filter is used to form a six-order bandpass filter. The detail consideration of number of orders is investigated in appendix A. The quality factor (Q) of the second-order bandpass filter is approximately half of the quality factor of the six-order bandpass filter. Table 2.1 summarizes the specification of the sixth-order bandpass filter.

Table 2.1 Specifications of the sixth-order banpass filter

Parameters	**Specifications**
Voltage Supply	3V
Power Consumption	90mW
Passband Gain	0dB
Center Frequency (Fc)	44MHz
Bandwidth	6MHz
Sampling Frequency	176MHz
Quality Factor	7.333
Filter Orders	6
Attenuation @ Fc +/- 6MHz	-9dBc

2.2 Classical Biquadratic Bandpass Filter

To investigate SC filters, the second-order transfer function in the s-domain should be considered. The following explanation adopts Ki's method [6]. Equation 2.1 shows one of the bandpass transfer functions in the s-domain.

$$H(s) = \frac{\frac{S}{Q\,\Omega_O}\left(1 - \frac{S}{2f_s}\right)}{1 + \frac{1}{Q}\frac{S}{\Omega_O} + \frac{S^2}{\Omega_O}} \qquad \textbf{(2.1)}$$

The quality factor of the bandpass filter is controlled by the value of Q. The Ω_O is the pre-warped pole frequency. By employing the bilinear transformation (Equation 2.2), the bandpass filter in z-domain (Equation 2.3) is obtained.

$$S = \frac{2}{T}\frac{1-Z^{-1}}{1+Z^{-1}} \qquad \textbf{(2.2)}$$

where the $T = 1/f_s$, f_s is the sampling frequency.

$$H(z) = \frac{\frac{X_O}{2Q}\frac{4}{X_O^2 + X_O/Q + 1}Z^{-1}(1-Z^{-1})}{1 + (2 - \frac{4}{X_O^2 + X_O/Q + 1} - \frac{X_O}{2Q}\frac{4}{X_O^2 + X_O/Q + 1})Z^{-1} + (1 - \frac{X_O}{2Q}\frac{4}{X_O^2 + X_O/Q + 1})Z^{-2}} \qquad \textbf{(2.3)}$$

where X_O is equal to $2/\Omega_O T$.

The corresponding SC bandpass filter to Equation 2.3 is illustrated at Fig. 2.1.

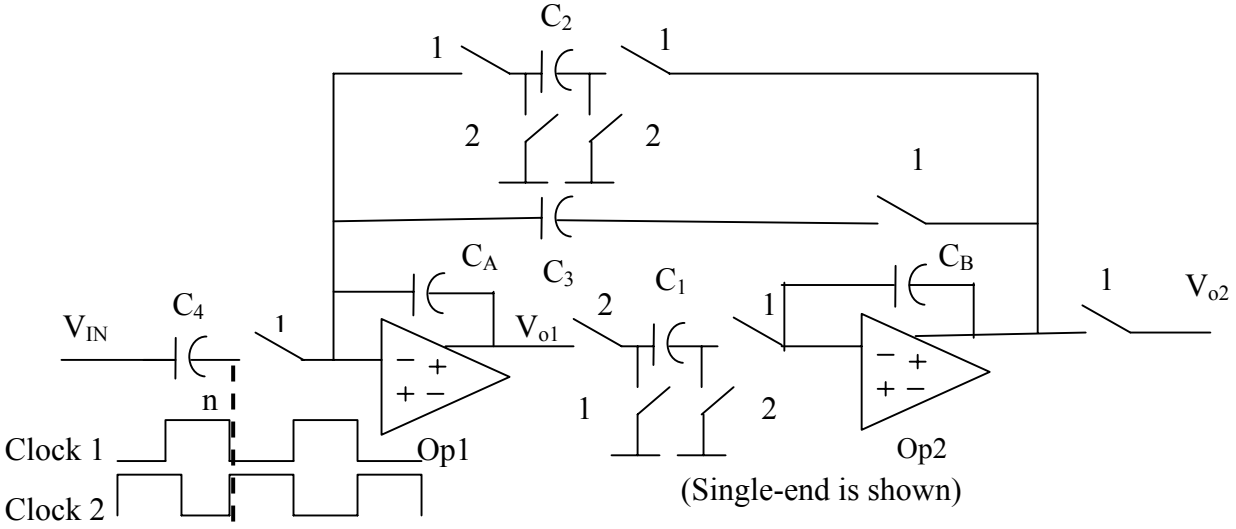


Figure 2.1 Classical SC Bandpass Filter

The time-domain charge transfer method [6] is employed to analyze the SC bandpass

filter. At n, clock 1 is high, capacitor C_A receives charges from C_8, C_3 and C_2 and capacitor C_B receives charges from C_1. Two equations 2.4 and 2.5 can be derived for capacitors C_A and C_B.

$$C_A[V_{01}(n)-V_{01}(n-1)] = -C_8[V_{in}(n)-V_{in}(n-1)] - C_3[V_{02}(n)-V_{02}(n-1)] - C_2V_{02}(n-1) \quad \textbf{(2.4)}$$

$$C_B[V_{02}(n)-V_{02}(n-1)] = C_1V_{01}(n-1) \quad \textbf{(2.5)}$$

By using z-domain transformation, two z-domain equations 2.6 and 2.7 are derived.

$$C_A(1-Z^{-1})V_{01}(Z) = -C_8(1-Z^{-1})V_{in}(Z) - C_3(1-Z^{-1})V_{02}(Z) - C_2V_{02}(Z) \quad \textbf{(2.6)}$$

$$C_B(1-Z^{-1})V_{02}(Z) = C_1Z^{-1}V_{01}(Z) \quad \textbf{(2.7)}$$

From equations 2.6 and 2.7 with substitution, the z-domain of SC bandpass transfer function is shown in equation 2.8.

$$H(Z) = \frac{V_{O2}(Z)}{V_{in}(Z)} = -\frac{\frac{C_1C_4}{C_AC_B}Z^{-1}(1-Z^{-1})}{1-(2-\frac{C_1C_3}{C_AC_B}-\frac{C_1C_2}{C_AC_B})Z^{-1}+(1-\frac{C_1C_3}{C_AC_B})Z^{-2}} \quad \textbf{(2.8)}$$

By comparing equations 2.3 and 2.8, all the capacitors values can be determined. The relationships between the capacitors and the parameters in equation 2.3 are listed in following equations.

$$\frac{C_1C_4}{C_AC_B} = \frac{X_O}{2Q}\frac{4}{X_O^2+X_O/Q+1} \quad \textbf{(2.9)}$$

$$\frac{C_1C_3}{C_AC_B} = \frac{X_O}{2Q}\frac{4}{X_O^2+X_O/Q+1} \quad \textbf{(2.10)}$$

$$\frac{C_1C_2}{C_AC_B} = \frac{4}{X_O^2+X_O/Q+1} \quad \textbf{(2.11)}$$

Equation 2.8 shows that there is a zero value at dc. Therefore, the roll-off of the SC

bandpass filter at the left-hand side is higher than the right-hand side. In order to have the same roll-off at the both sides, the delay and subtract switched capacitor C_8 is replaced by the inverting switched capacitor. This modification does not change the pole of the SC filter. As explained in following section, if this second-order filter is employed to form a high-order filter, this modification can improve the speed of the whole filter.

2.3 Double-Sampling Technique

In fig. 2.1, capacitors C_A and C_B only receive charge at clock 1. Actually, another set of capacitors can be employed in parallel with the original one and worked at another clock phase. This is called double-sampling technique. This means the output voltage can be taken at both clock phases. Figure 2.2 and equation 2.12 shows the double-sampling SC bandpass filter and corresponding z-domain transfer function respectively.

$$H(Z) = \frac{V_{O2}(Z)}{V_{in}(Z)} = -\frac{\frac{C_1C_4}{C_AC_B}Z^{-2}}{1-(2-\frac{C_1C_3}{C_AC_B}-\frac{C_1C_2}{C_AC_B})Z^{-1}+(1-\frac{C_1C_3}{C_AC_B})Z^{-2}} \qquad \textbf{(2.12)}$$

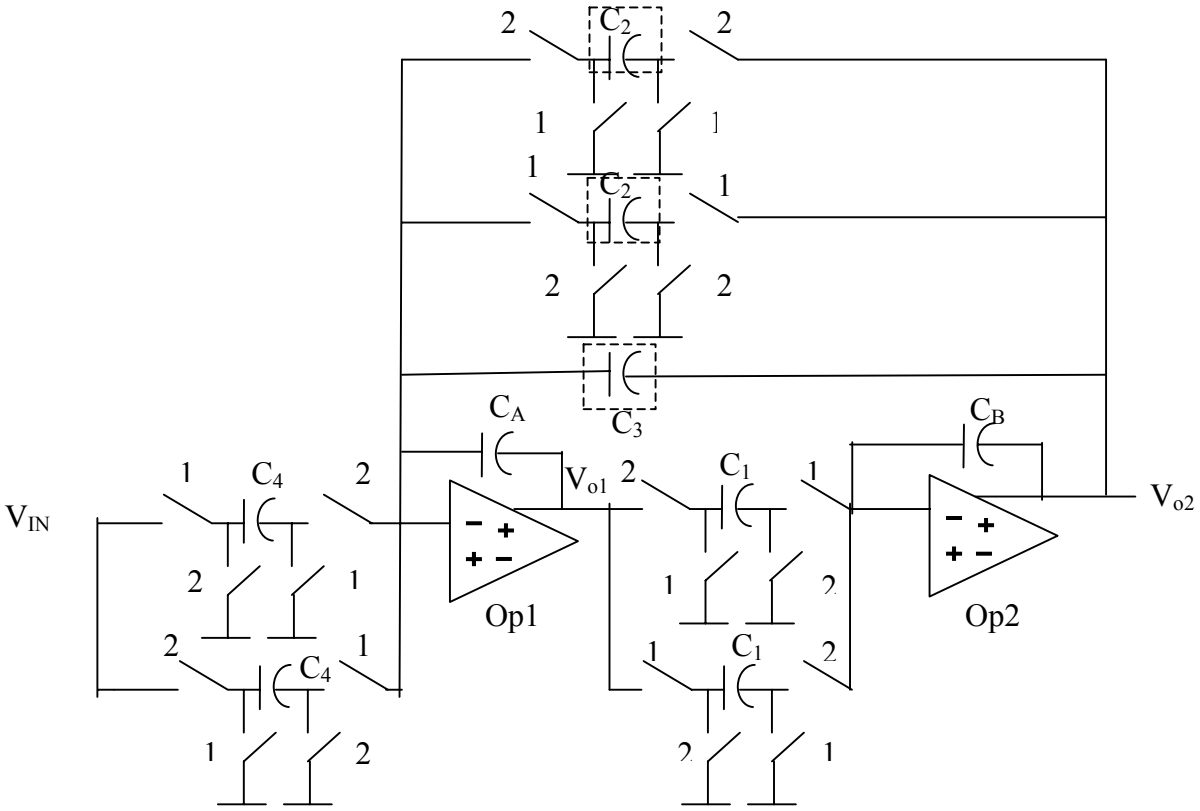


Figure 2.2 Double-sampling SC banpass filter

Since the output data rate is doubled by employing the double-sampling method, the clock frequency of the filter can be reduced by 2 to get the same output data rate in the single-sampling method. This means that the unity-gain frequency of the opamp can also be relaxed by 2. However, the double-sampling method generates an image signal due to the mismatch between two paths. The mismatch problem can be minimized by some layout techniques.

The dot boxes in fig. 2.2 show the delay and subtract switched capacitors. These capacitors are directly connected two opmaps. This decreases the operational speed of the filter. The reason is that the output voltage of the opamp one (Op 1) cannot reach its

final value before the output voltage of the opamp two (Op 2) reaches its settled value. Therefore, it is important to avoid these delays and subtract switched capacitors between any two opamps, especially for high-speed applications.

2.4 Choice of Sampling Frequency

In switched-capacitor bandpass filter, the designed locations of poles depend on the input frequency and sampling frequency. In this project, the input frequency that equals to (2n+1)/4 times the sampling frequency will be considered. n can be any numbers as long as larger than -1/2. It is because there are no negative input frequencies. Different locations of poles will effect the requirement of a pre-filter and an ADC (that follows the IF filter). The function of the pre-filter is to filter out the image signal. Without the pre-filter, the image signals will be mixed down to the interested band by the sampling frequency. This will affect the wanted signal. If the ADC is also switched-capacitor circuit, it will employ the same sampling frequency in the IF filter. The over-sampling ratio (OSR) will affect the performance of the ADC. In general, high over-sampling ratio is good for ADC. The details about the characteristics of ADC will not be discussed here. In the following paragraphs, n is larger than -1/2 and smaller than 1/2 will be discussed first. And then n is larger than 1/2. After that, the cases for n equal to any integer numbers will be investigated.

Case 1: 1/2 > n > -1/2

In this case, the input frequency is within the Nyquist range. The poles of the filter will be set as same as the frequency location of input signal. Figure 2.3 and 2.4 shows the input held and hold circuit and the input frequency spectrum of the filter.

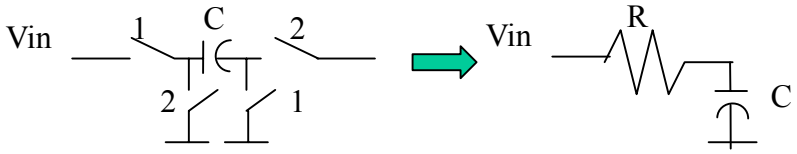


Figure 2.3 Input sample and hold circuit

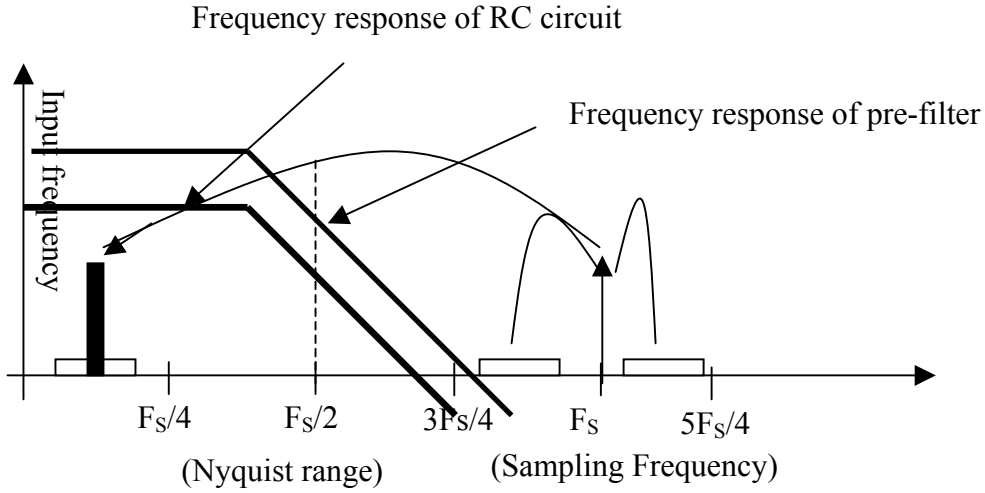


Figure 2.4 Input frequency spectrum with 1/2> n>-1/2

Input sample and hold circuits can be considered RC circuits. Since the input frequency is within Nyquist range, the bandwidth of the RC circuit should be designed to cover the input frequency and minimize the high frequency noise that will be mixed down by the sampling frequency. Moreover, a simple lowpass filter can be employed as a pre-filter. In general, the OSR is high in this case.

Case 2: n > 1/2

With n larger than 1/2, the input frequency is higher than Nyquist range. The input frequency should be mixed down by the sampling frequency to the location that is within the Nyquist range to do further processing. The poles of the bandpass filter are set to be Fs - Fin (where Fin is the input frequency). This operation is also called sub-sampling operation. Figure 2.5 illustrates the input frequency spectrum of the filter.

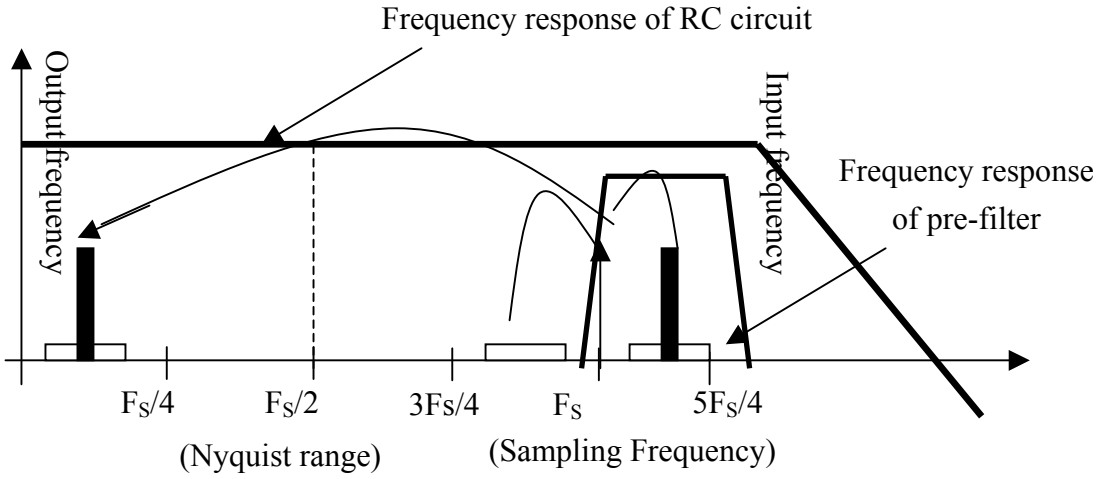


Figure 2.5 Input frequency spectrum with n> 1/2

The bandwidth of the RC circuit should be designed to cover the input frequency. However, this also covers some noise regions that will be translated to the output frequency location. Sub-sampling operation will degrade the dynamic range of the filter due to these extra noise sources. The advantage of this operation is it employs lower sampling frequency. However, a bandpass filter is required to be a pre-filter. This is because at least one of the image signals is located at lower side band. The OSR is also lower than the OSR in case 1.

Case 3: n is any integer numbers

Actually case 3 is the subset for case 1 or case 2. If n equals to zero, it is the subset for case 1. If n is larger than 1/2, it is the subset for case 2. If n is zero, the input frequency is 1/4 of the sampling frequency. The pole should be placed at 1/4 of the sampling frequency. If n is any other integer numbers, the input frequency will also be mixed to 1/4 sampling frequency. For example, sampling frequency equals to 4/5 of the input frequency, the output frequency is 1/5 of the input frequency. Therefore, for any integers n, the poles of the bandpass filter are also placed at 1/4 of the sampling frequency.

In the following sections, the SC bandpass filter is designed with zero value of n due to its advantages about the pre-filter requirement. The other point is to compare the proposed design and conventional biquadratic bandpass Filter. This is because pseudo-2-path technique fixes the location pole at 1/4 of the sampling frequency.

2.5 Realization of SC Bandpass Filter

Since the SC circuit is a discrete-time system, frequency wrapping from discrete-time domain (ω_d) to continuous-time domain ($\omega_a = \Omega_O$) should be done before calculating capacitors values. In bilinear transform, frequency wrapping is done by equation 2.13.

$$\omega_a = \frac{2}{T_S}\tan(\frac{\omega_d T_S}{2}) \qquad \textbf{(2.13)}$$

Where Ts is the sampling period.

With zero value of n (the pole equals to 1/4 sampling frequency), ω_a equals to $2/T_S$ and Xo =.$\omega_a T_S/2 = 1$.

In this case, the coefficient of Z^{-1} in denominator is:

$$\begin{aligned}
&2 - \frac{C_1C_3}{C_AC_B} - \frac{C_1C_2}{C_AC_B} \\
&= 2 - \frac{X_o}{2Q}\frac{4}{X^2{}_o + X_o/Q + 1} - \frac{4}{X^2{}_o + X_o/Q + 1} \\
&= 2 - \frac{1}{2Q}\frac{4}{2 + 1/Q} - \frac{4}{2 + 1/Q} \\
&= \frac{4 + 8Q - 4 - 8Q}{2Q(2 + 1/Q)} \\
&= 0
\end{aligned}$$

This means the coefficient of Z^{-1} in denominator equals to zero value independent the value of Q. The value of Q only determines the value of C_1, C_3, C_A, C_B . The following equation shows the relationship among Q, C_1, C_3, C_A, C_B .

$$\begin{aligned}
&\frac{C_1C_3}{C_AC_B} \\
&= \frac{X_o}{2Q}\frac{4}{X^2{}_o + X_o/Q + 1} \\
&= \frac{1}{2Q}\frac{4}{2 + 1/Q} \\
&= \frac{2}{2Q + 1}
\end{aligned}$$

The resulted equation is:

$$H(Z) = \frac{V_{O2}(Z)}{V_{in}(Z)} = -\frac{\frac{C_1C_4}{C_AC_B}Z^{-2}}{1 + (1 - \frac{C_1C_3}{C_AC_B})Z^{-2}} \qquad \textbf{(2.14)}$$

By taking C_8=1, C_A=1 and C_B=1, all the capacitors can be determined by equation 2.9 - 2.11. The values of the capacitors are changed a little bit due to mathematics error and listed in table 2.2.

Table 2.2 summarizes the calculated capacitors values

Parameters	**Ω_O**	**C_1**	**C_2**	**C_3**	**C_8**	**C_A**	**C_B**
Value	352M	0.343	4.83	1	1	1	1

To minimize the common-mode noise, clock-feedthrough noise and increasing the dynamic range, the fully-differential structure is adopted. The frequency response of the two output nodes (V_{01}, V_{02}) of the filter are simulated with SWITCAP2 [7] as shown in fig. 2.6 and fig. 2.7 respectively. The opamps are ideal opamps in the simulation.

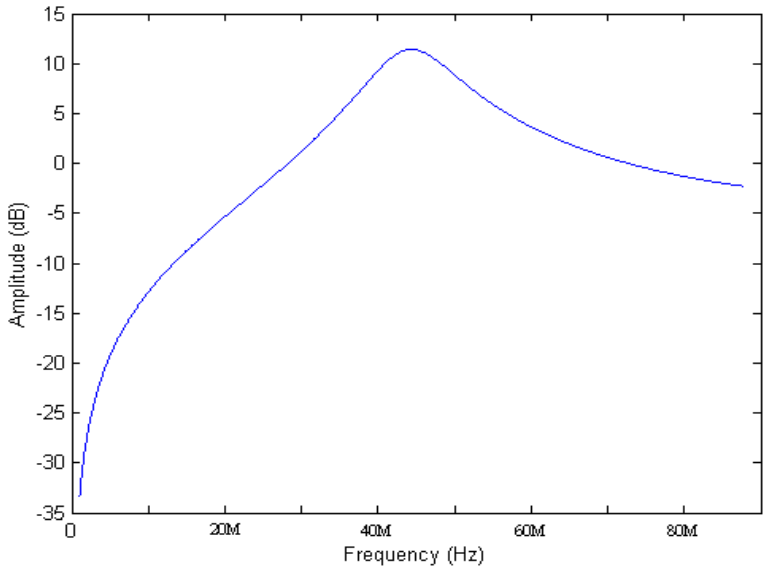


Figure 2.6 Frequency response at the voltage node V_{01}

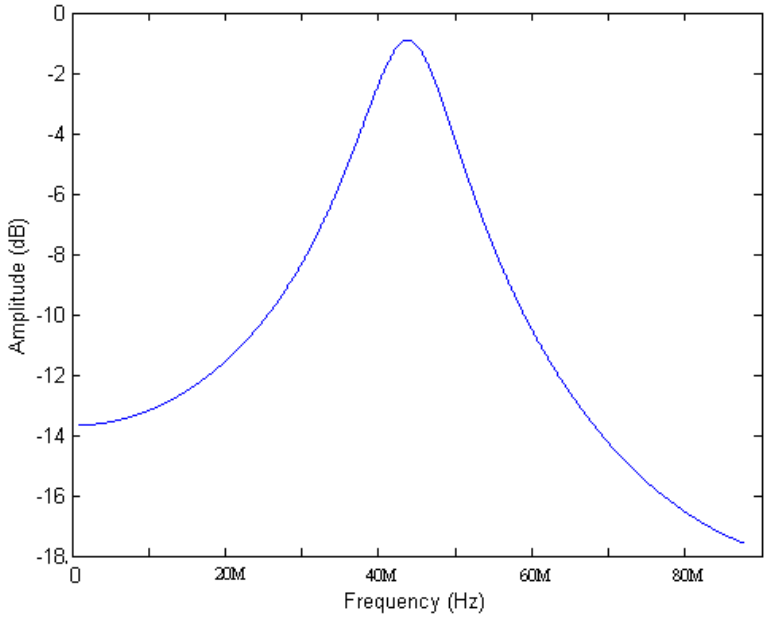


Figure 2.7 Frequency response at the voltage node V_{02}

The center frequency is located at 44MHz and bandwidth is around 11.77MHz. However, the gains at (V_{01} and V_{02}) nodes are different due to non-optimized capacitors values. This will degrade the performance of the SC filter. By employing dynamic range optimization and capacitance spread optimization [1], the performance of the SC filter can be improved. The frequency response of the optimized SC and optimized capacitors values are shown in fig. 2.8 and table 2.3. Table 2.4 summarizes the characteristics of the second-order bandpass filter.

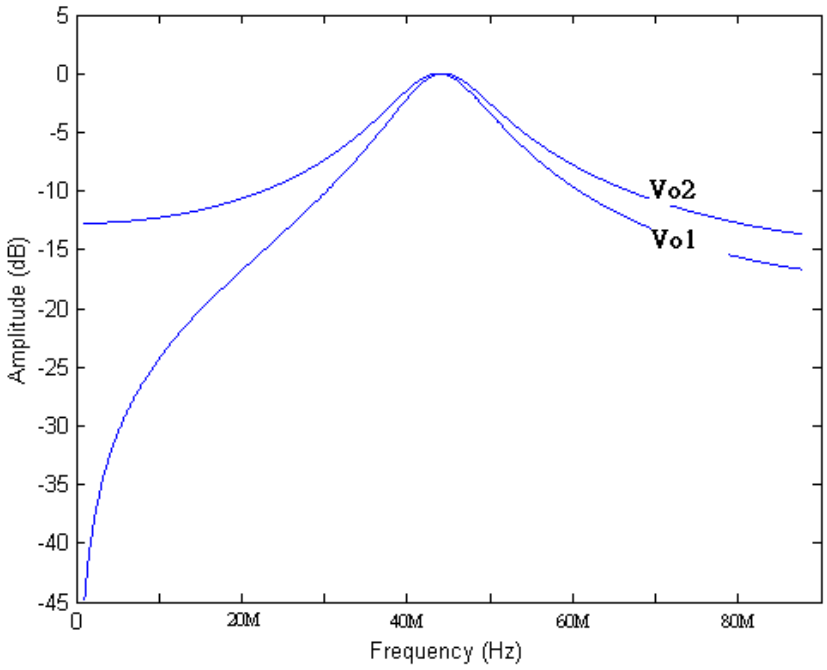


Fig. 2.8 Optimized frequency response at the both voltage nodes

Table 2.3 summarizes the optimized capacitors values

Parameters	Ω_O	C_1	C_2	C_3	C_8	C_A	C_B
Value	352M	1.419	1.168	0.242	0.269	1	1

Table 2.4 Summary of the second-order banpass filter characteristics

Parameters	**Simulated Results**
Passband Gain	0dB
Center Frequency	44MHz
Bandwidth	11.77MHz
Effective Sampling Frequency	176MHz
Quality Factor	3.74
Filter Orders	2

Cascading three second-order bandpass filters forms the six-order bandpass filter. The

frequency response and characteristics of the sixth-order SC bandpass filter are illustrated in fig. 2.9 and table 2.5.

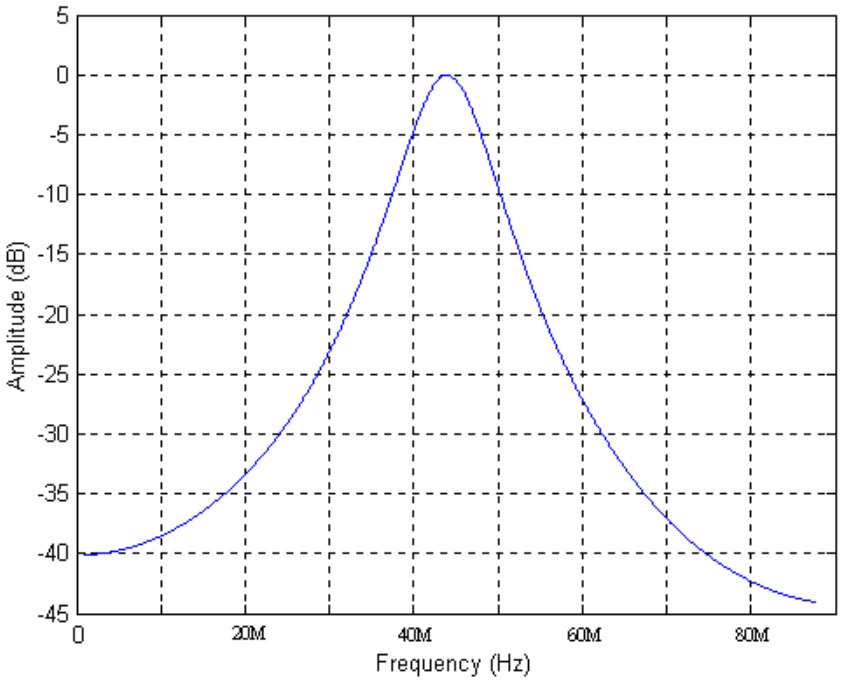


Figure 2.9 Frequency response of the sixth-order SC bandpass filter

Table 2.5 Summary of the six-order banpass filter characteristics

Parameters	**Simulated Results**
Passband Gain	0dB
Center Frequency (Fc)	44MHz
Bandwidth	6MHz
Effective Sampling Frequency	176MHz
Quality Factor	7.33
Filter Orders	6
Capacitor Spread	5.863
Attenuation @ Fc +/- 6MHz	-9.1dB

The system-level simulation results show the SC bandpass filter achieves the center

frequency of 44MHz with a bandwidth of 6MHz. The degraded attenuation at 10MHz is due to "sin(x)/x" response [1].

Reference

[1] R. Gergorian and G. Temes, Analog MOS Integrated Circuits For Signal Processing, *John Wiley & Sons, New York*, 1986

[2] P. V. Ananda Mohan, V. Ramachandran and M. N. S. Swamy, Switched Capacitor Filters - Theory, Analysis and Design, *Prentice Hall International (UK) Ltd*., 1995

[3] A. Nagari and G. Nicollini, "A 3-V 10-MHz pseudodifferential SC band-pass filter using gain enhancement replica amplifier." *IEEE J. Solid-State Circuits*, vol. 33, pp. 626-630, Apr. 1998.

[4] A. Nagari, A. Baschirotto, F. Montecchi and R. Castello, "A 10.7-MHz BiCMOS High-Q Double-Sampled SC Bandpass Filter", *IEEE J. Solid-State Circuits*, vol. 32, pp. 1491-1498, Oct. 1997.

[5] J. J. F. Rijns and H. Wallinga, “Spectral Analysis of Double-Sampling Switched-Capacitor Filters”, *IEEE Transactions on circuit and systems*, vol. 38, pp1269-1279, November 1991.

[6] Wing-Hung Ki, Gain- and Offeset-Compensated Switched-Capacitor Circuits, Ph. D. dissertation, University of California Los Angeles, 1995

[7] Shen-Iuan Liu, Chien-Hung Kuo, Ruey-Yuan Tsai, and Jingshown Wu, “A Double-Sampling Pseudo-Two-Path Bandpass ΔΣ Modulator,” *IEEE J. Solid-State Circuits*, vol. 35, pp. 276-280, February. 2000

Chapter 3

High-Speed Switched-Capacitor Filter with Low Power Consumption

In recent years, much research has been done on designing a simple biquadratic switched-capacitor (SC) resonator using the Pseudo-2-Path (P2P) technique [1][2]. The reason is that the P2P technique can realize " z to z^2 transformation ". This means that a second-order biquadratic filter can be implemented by a single opamp rather than two opamps. From the power-consumption point of view, P2P technique is good for implementing some simple biquadratic SC filters, especially for high-speed applications.

In this chapter, limitations of the reported SC resonator [3] will be discussed. A modified Double-Sampling Pseudo-2-Path technique is proposed to implement a 3-V 44-MHz bandpass filter.

3.1 Classical 2-Path Filters

In order to explain the principle of 2-path filters, the frequency response of a switched-capacitor highpass filter (SC-HPF), which is shown in Fig. 3.1, should be considered. The SC-HPF is sampled with a sampling frequency $F_S/2$ and thus is a sample-data system. By the Nyquist theorem, only the signal within $F_S/2$ can be correctly processed by the SC-HPF. This is called Nyquist range (NF). The frequency response of the highpass filter will be periodic repeated every $F_S/2$. In Fig. 3.1, the SC-HPF has a bandpass characteristic at the half of the sampling frequency Fs.

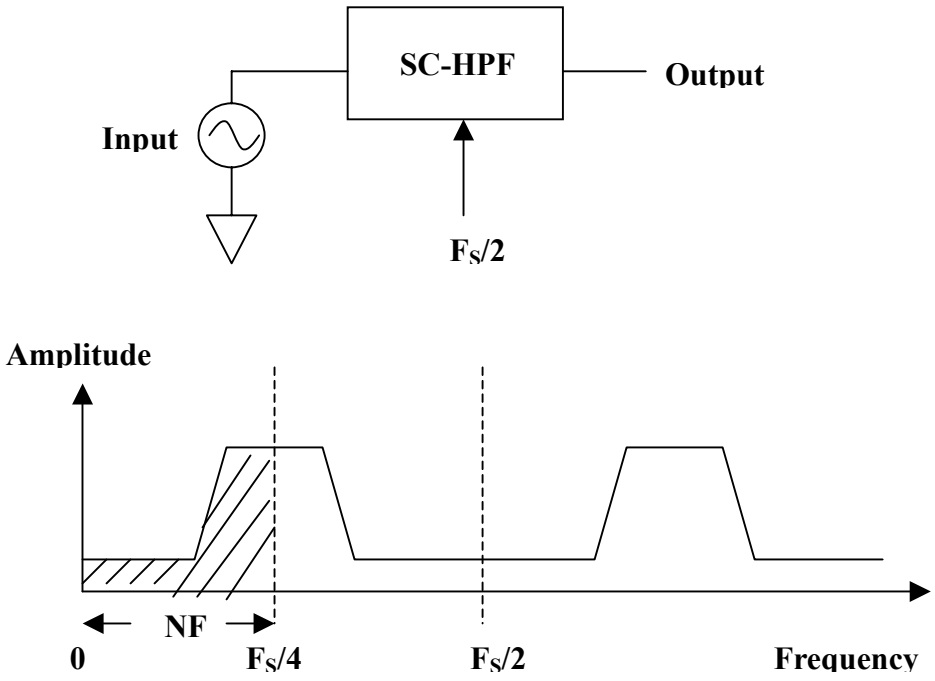


Figure 3.1 Frequency response of SC Highpass filter

In order to have a bandpass response, another SC-HPF is employed in parallel to increase the number of samples per period and extend the Nyquist range to $F_S/2$. The

2-path filter and its frequency response are shown in Fig. 3.2.

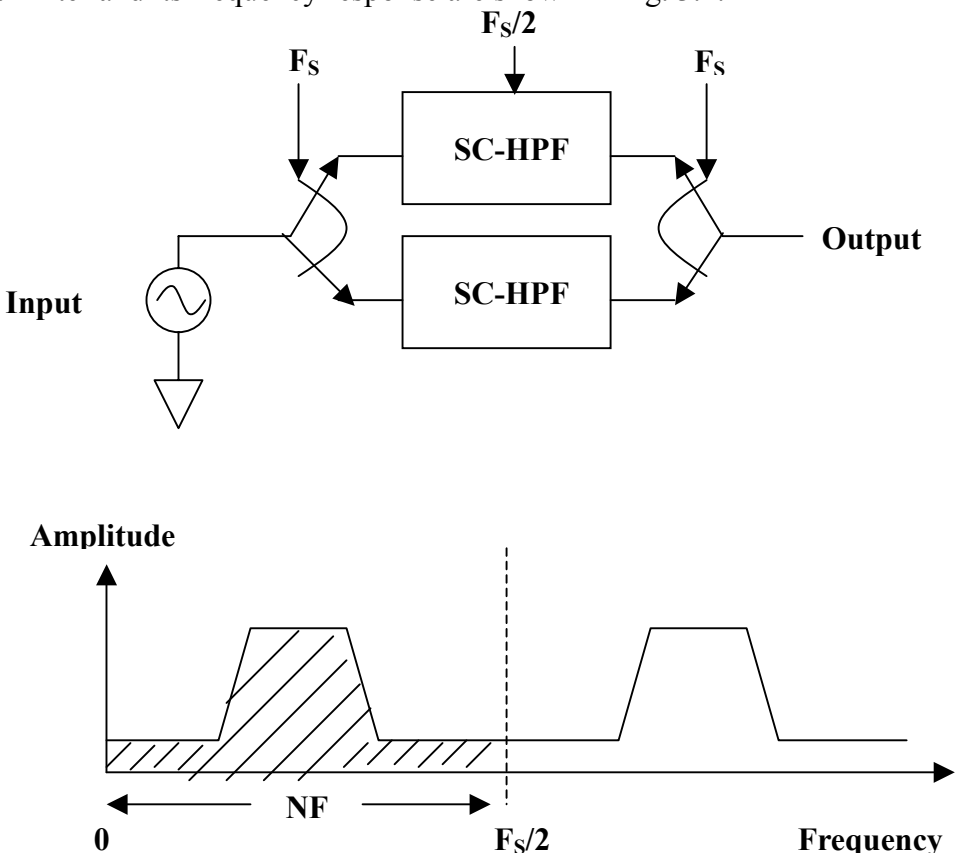


Figure 3.2 Frequency response of 2-path SC Highpass filter

The 2-path technique only extends the Nyquist range. The frequency response of the 2-path highpass filter is the same as the frequency response of a highpass filter without changing capacitor values. The highpass filter is converted from lowpass filter with " z to -z transform ". The lowpass filter is less sensitive to the element variations. Therefore, the SC 2-path highpass filter is preferable to the conventional bandpass filter. However, the 2-path SC filter needs 2 times more components and approximately 2 times more power consumption. Another disadvantage of the 2-path technique is the mismatch between the 2 paths will generate spurious output signals and

mirror-frequency noise.

3.2 Classical Pseudo-2-Path Filter

In the 2-path filter, only one path is active at each time. Therefore, the opamps in the 2 paths can be shared. This method not only saves the power consumption by 2 but also minimizes spurious output signal and mirror-frequency noise. One of the pseudo-2-path integrator [1] that employs a RAM-type cell is redrawn and shown in Fig. 3.3.

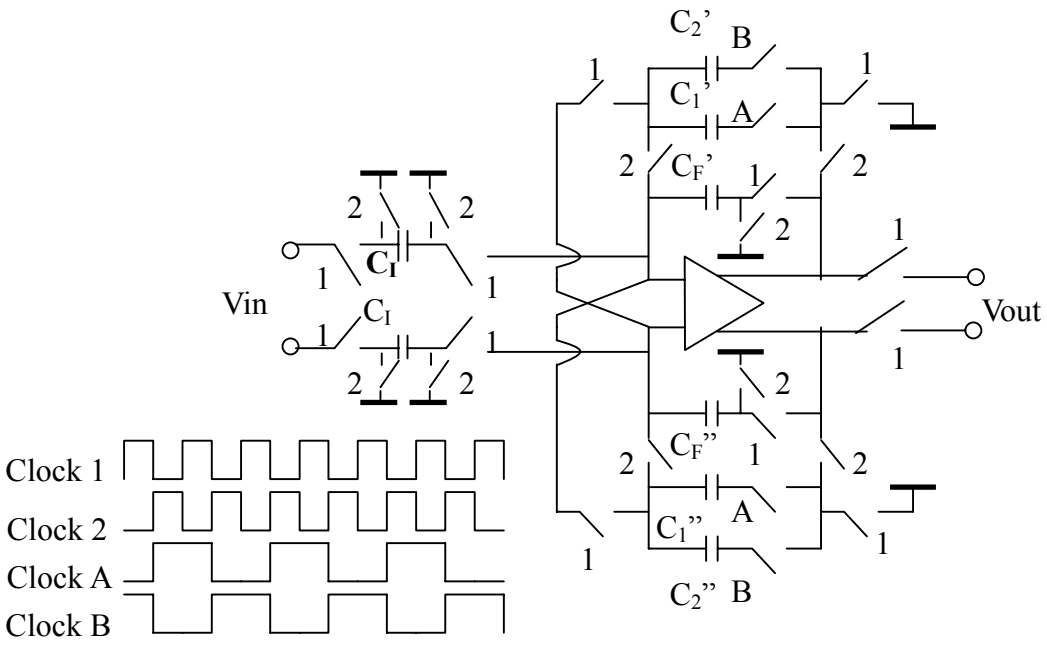


Figure 3.3 Differential pseudo-2-path transformed SC integrator

The C_1' (C_1") and C_2' (C_2") are the capacitors of the storage array. The capacitors values of C_F' (C_F"), C_1' (C_1") and C_2 '(C_2") are designed to the same. The reason is that, if the capacitors of the storage array are smaller than the integrating capacitors C_F'(C_F"),

there is a gain and it may excess the dynamic range of the opamp. On the other hand, the capacitors of the storage array are larger than the integrating capacitors C_F'(C_F"), then the higher performance of the opamp is needed. The two paths are controlled by both clocks A and B. The operation for clock A and clock B are the same. For ease of explanation, only the operation with clock A is high will be investigated. When clock A and clock 1 are high, the charge in C_I and C_2" (C_2') are transferred to C_F' (C_F"). The sign inversion occurs at clock 1. When clock 2 is high, the charges in C_F' (C_F") are moved to one pair of the storage arrays. The charges in the storage arrays will be delayed by 2 sampling periods. Then the z-transfer function of the integrator is

$$H(z) = \frac{C_I}{C_F} \frac{1}{(1+z^{-2})} \qquad \textbf{(3.1)}$$

However, the pseudo-2-path filter needs one idle phase to upload the charge in the integration capacitor to the memory capacitor. As a result, the double-sampling technique [3] that is described in chapter 2 cannot be used. Table3.1 summarizes the characteristics among the biquadratic bandpass filter, the 2-Path bandpass filter and the Pseudo-2-Path bandpass filter.

Table 3.1 Summary of characteristics of different kinds of bandpass filters

Parameters	Biquadratic Filter	2-Path Filter	Pseudo-2-Path Filter
Operation mode	Single or double sampling	Single or double sampling	Single sampling
No. of orders/ No. of Opamp	1	1	2
Sampling Frequency	F_S	F_S	F_S
Sampling Frequency	Any locations within $F_S/2$	$F_S/4$	$F_S/4$

3.3 Double-Sampling Pseudo-2-Path Technique

Though the classical pseuod-2-path filter can achieve a bandpass response with very high accuracy, double-sampling technique cannot be employed. The main idea of latest reported double-sampling pseudo-2-path (DSP2P) technique [4] is to arrange the clock phases to avoid the charge upload phase in the classical technique. The DSP2P filter is illustrated in Fig. 3.4.

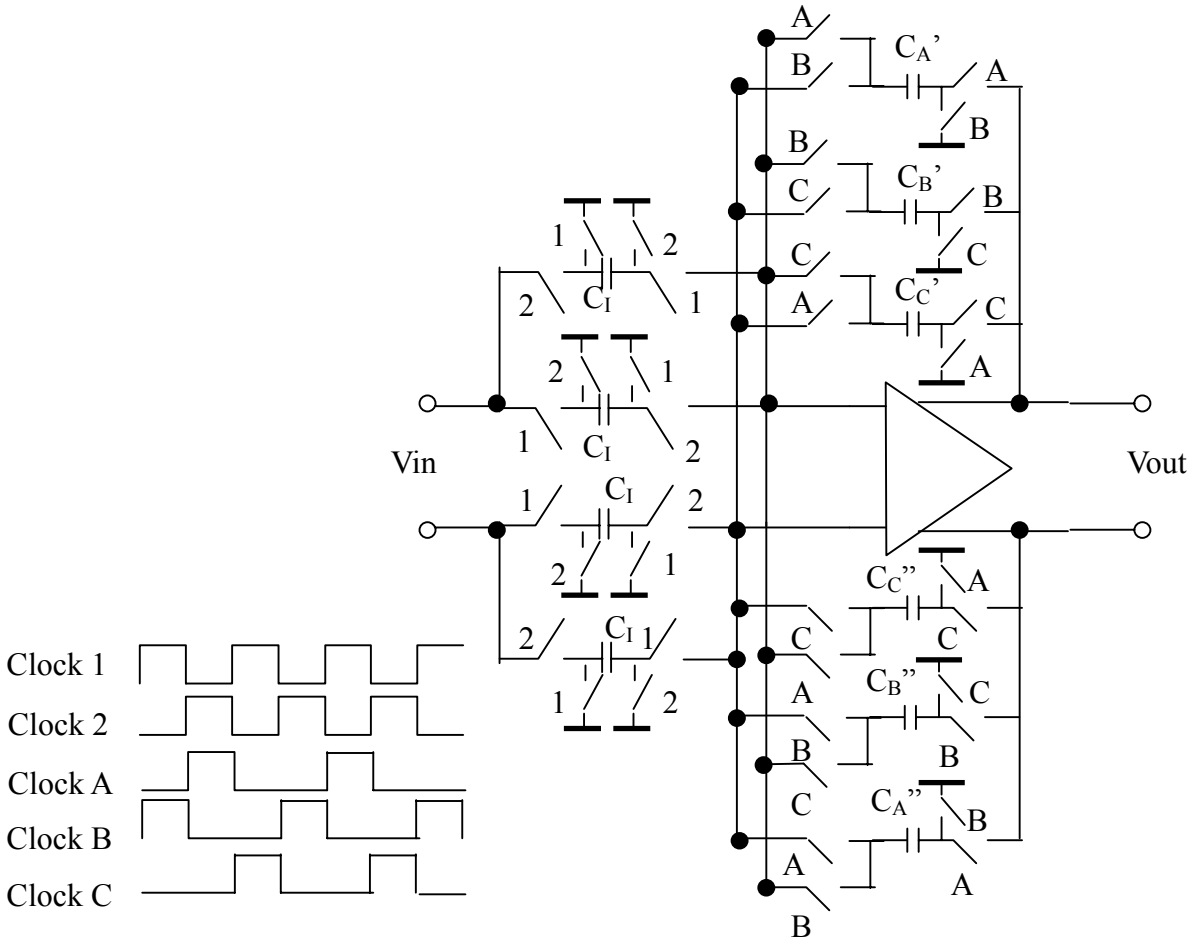


Figure 3.4 Double-sampling pseudo-two-path bandpass filter

The CI is the sampling capacitor. The storage capacitors include C_A' (C_A"), C_B' (C_B") and C_C' (C_C") and they are the same size. The operation at clocks A, B and C are the same. For ease of explanation, only the operation when clock A is high will be discussed. When clock A is high, the charges in C_C' (C_C") and CI will be transferred to C_A" (C_A'). This operation implements the sign inversion " z to -z transform " and each capacitor array will hold the capacitor by 2 sampling periods. This realizes the " z to z^2 transform ". Therefore, the z-domain transfer function is

$$H(z) = \frac{C_I}{C_A} \frac{z^{-1}}{(1+z^{-2})} \qquad \textbf{(3.2)}$$

The difference between Equation 3.1 and 3.2 is the z^{-1} term. However, z^{-1} term does not change the frequency response of the circuit. We can see that no charge upload phase is needed in this circuit. Therefore, this circuit can employ the double-sampling technique.

This circuit has advantages to implement some cascading biquadratic SC filters.

(1) The primary reason is this circuit does not have any direct capacitor to other stages. This means each second-orders SC filter is settled independently.

(2) This circuit needs one opamp to realize an simple second-order banpass filter. This will reduce the power consumption by 2.

However, there are some drawbacks of this circuit.

(1) The quality factor of this bandpass filter is equal to one. Therefor this only suitable for implementing a resonator bandpass filter.

(2) Five clock phases are required in this circuit. The complicated clock phases are not preferable.

(3) Any mismatch among the paths will introduce the spurious output signals and complex mirror-frequency noise due to complex clock phases.

3.4 Modified Double-Sampling Pseudo-2-Path Technique

The modified double-sampling pseudo-two technique is proposed to implement a relative low Q banpass filter and minimize the drawbacks above. The modified technique employs additional capacitors to reduce the quality factor of the filter. A special clock phase arrangement is employed to reduce number of required clock phases. Figure 3.5 shows the proposed circuit.

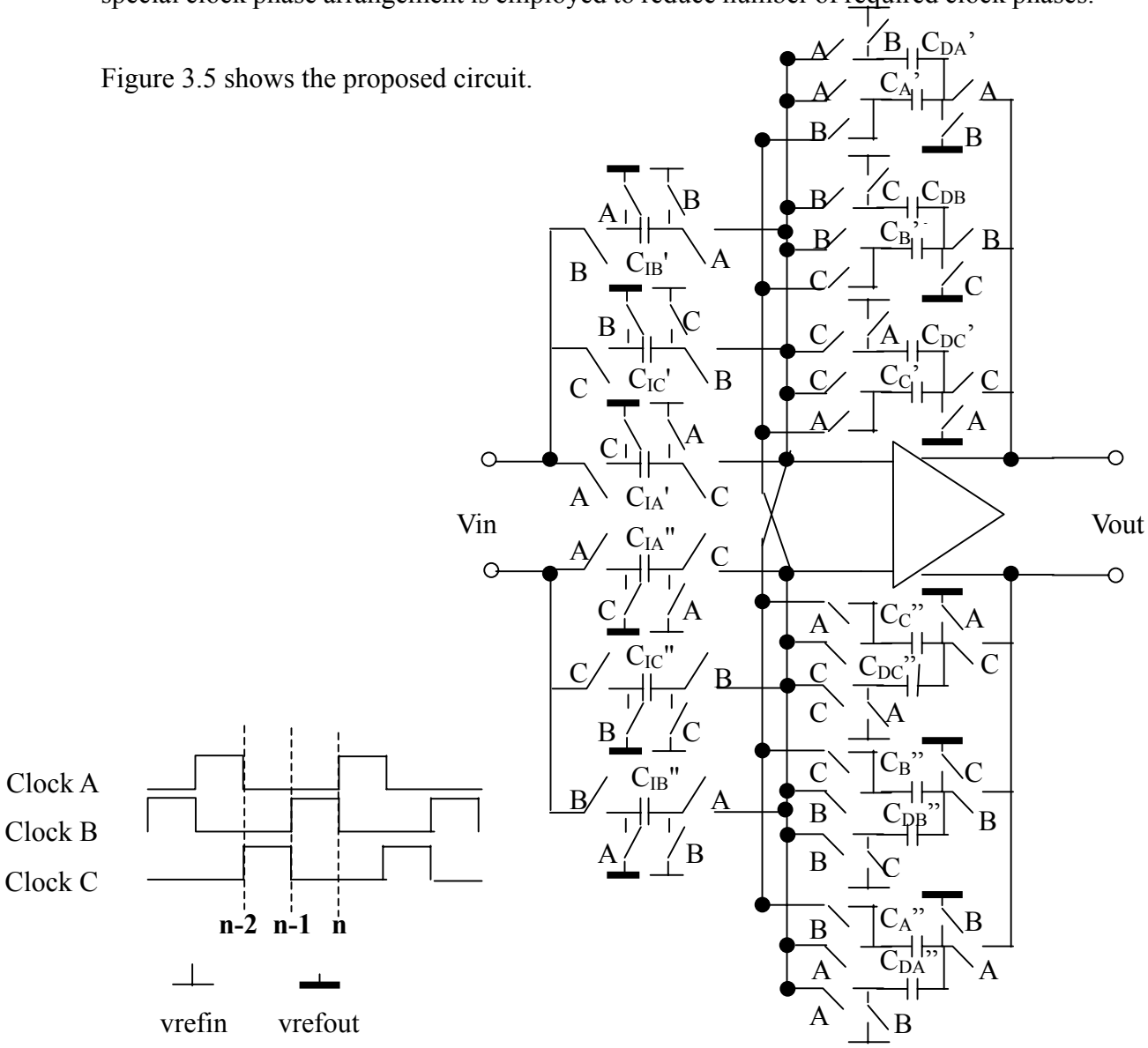


Figure 3.5 The modified double-sampling pseudo-2-path filter

The damping capacitor pairs (C_{DA}', C_{DA}''), (C_{DB}', C_{DB}'') and (C_{DC}', C_{DC}'') are

employed in the filter and form the capacitor arrays with storage capacitor pairs (C_A', C_A"), (C_B', C_B") and (C_C', C_C"). Capacitor pairs (C_{IA}', C_{IA}"), (C_{IB}', C_{IB}") and (C_{IC}', C_{IC}") are the sampling capacitors. Two reference voltages (vrefin and vrefout) are employed to operate the filter. Vrefin is the reference voltage (1.34V) for input node of the opamp. Vrefout is the reference voltage (1.5V) for output node of the opamp. If the input and output nodes of the opamp are settled at 1.34V and 1.5V respectively, no charge will be transferred with no input signal. In order to explain the operation principle of the proposed circuit in clear way, the time period from "n-2" to "n" will be investigated and is shown in Fig.3.6.

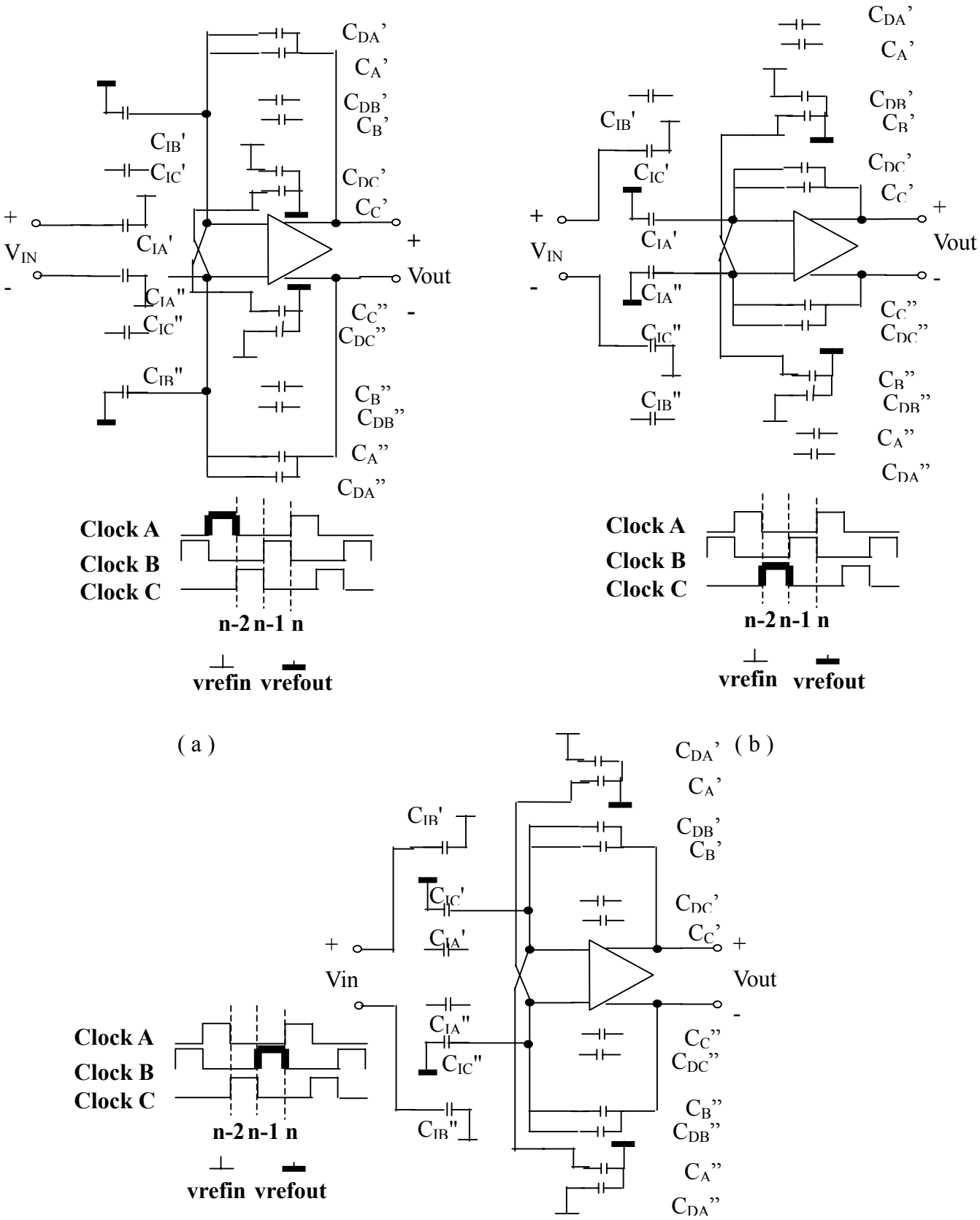


Figure 3.6 (a) Clock A (b) Clock C (c) Clock B

All the capacitor arrays have the same capacitor size. At time n-2, the output voltage Vout[n-2] is stored in capacitors (C_{DA}', C_A') and (C_{DA}", C_A"). At time n-1, the input voltage Vin[n-1] is sampled in capacitor pair (C_{IC}', C_{IC}"). Note that (C_{DA}', C_{DA}") are fully discharged. At time n, the capacitors (C_B', C_{DB}') and (C_B", C_{DB}") receive sampled charge from capacitors (C_{IC}', C_A") and (C_{IC}", C_A'). By doing so, the z-domain transfer function is obtained. The mathematical description of the circuit in time-domain are derived by Equation 3.3 and 3.4.

$$\left.\begin{aligned}(C_B'+C_{DB}')Vout^+(n) &= C_A''Vout^-(n-2)+C_{IC}'Vin^+(n-1)\\ (C_B''+C_{DB}'')Vout^-(n) &= C_A'Vout^+(n-2)+C_{IC}''Vin^-(n-1)\end{aligned}\right\} \quad \textbf{(3.3)}$$

$$(C_B+C_{DB})Vout(n) = -C_AVout(n-2)+C_{IC}Vin(n-1) \quad \textbf{(3.4)}$$

From Equation 3.4, the z-domain transfer function (Equation 3.5) is derived with time domain to z domain transformation. For clear explanation, C_I, C and C_D represent all the sampling capacitors, storage capacitors and damping capacitors respectively.

$$\frac{Vout\ (z)}{Vin\ (z)} = \frac{C_I}{C+C_D}\frac{z^{-1}}{1+(C/(C+C_D))z^{-2}} \quad \textbf{(3.5)}$$

The modified double-sampling pseudo-2-path technicque can realize a more generic bandpass filter. In addition, the quality factor of the filter is only controlled by two capacitors (C storage capacitor and C_D damping capacitor). In the classical

biquadratic filter, the quality factor is determined by four capacitors. It is attractive to implement some high-speed filters due the difficult realization of high gain and high speed opamp. More important, the modified technique can save approximately half of power consumption than classical double-sampling biquadratic SC filters. Table 3.2 summarizes the characteristics of the biquadratic filter, the previous DSP2P filter and the proposed DSP2P filter.

Table 3.2 Summary of characteristics of biquadratic filter, previous DSP2P filter and propsed DSP2P filter

Parameter	Biquadratic bandpass Filter	Previous DSP2P bandpass Filter [4]	Proposed DSP2P bandpass Filter
No. of needed clock phases	2	5	3
Operation mode	Single or Double sampling	Single or Double sampling	Single or Double sampling
No. of orders/ No. of Opamp	1	2	2
Type of Filters	Resonator or wideband bandpass Filter	Resonator (only)	Resonator or wideband bandpass Filter

3.5 Implementation of Selective Gain

In wireless receivers, the power of input signal is not a constant value. If the input signal is large, the filter may amplify the signal and thus it will saturate the following stages. On the other hand, the signal level is not large enough to be detected by the following stages. Therefore, variable gain is very important for wireless receivers. Equation 3 indicates that the gain of designed filter is controlled by the sampling capacitor. This means the selective gain can be implemented by adding another sampling capacitor to sample the input signal and transfer the charge to the integrator. Figure 3.7 shows the implementation of selective gain in one sampling capacitor.

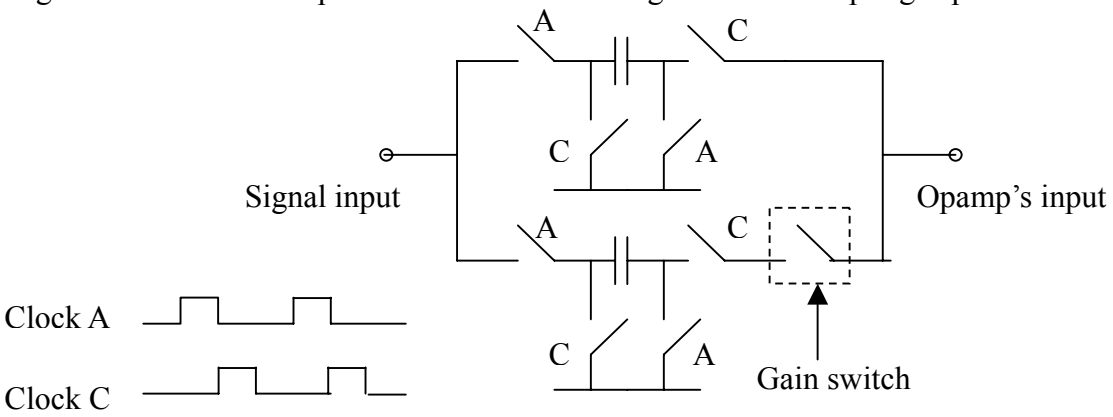


Figure 3.7 Implementation of selective gain

The gain can be selected by turning on the gain switch. This will allow a more sampled charge to the integrator. Otherwise, the integrator will receive less charge.

3.6 System Simulation

The modified technique was employed to build a six-order banpass filter by cascading three identical second-order bandpass filters. The system block diagram is redrawn and shown in Fig. 3.8 for easy discussion.

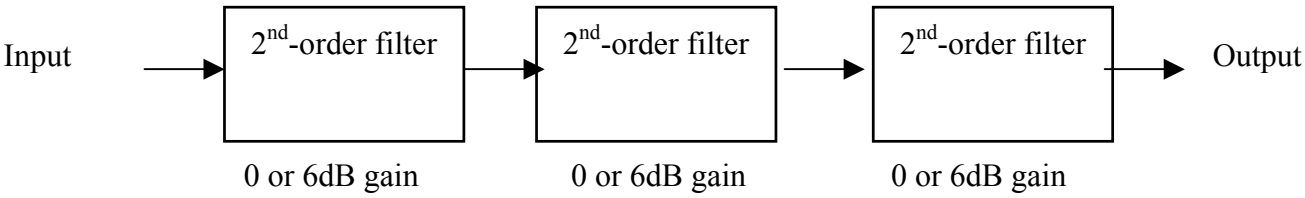


Figure 3.8 Block diagram of the sixth-order filter

The capacitors values are summarized in table 3.1. Figure 3.9 illustrates the frequency response of the filter with 0dB to 18dB gain respectively. And the group delay of the filter is shown in fig. 3.10.

Table 3.1 Summary of capacitor values of modified DSP2P filter

Capacitors	**Values/ pF**
C (Storage Capacitor)	0.385
Cd (Damping Capacitor)	0.2
CI (sampling Capacitor)	0.21

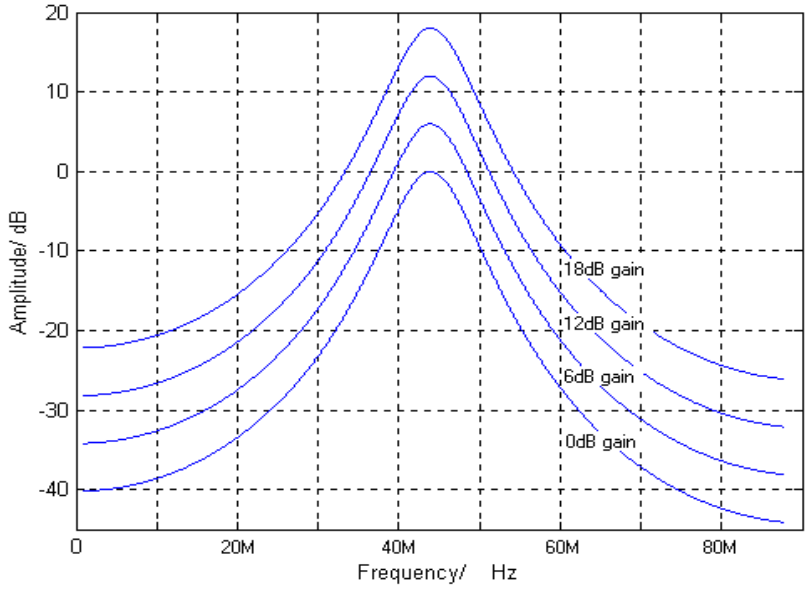


Figure 3.9 Frequency response of the modified DSP2P filter with gain setting

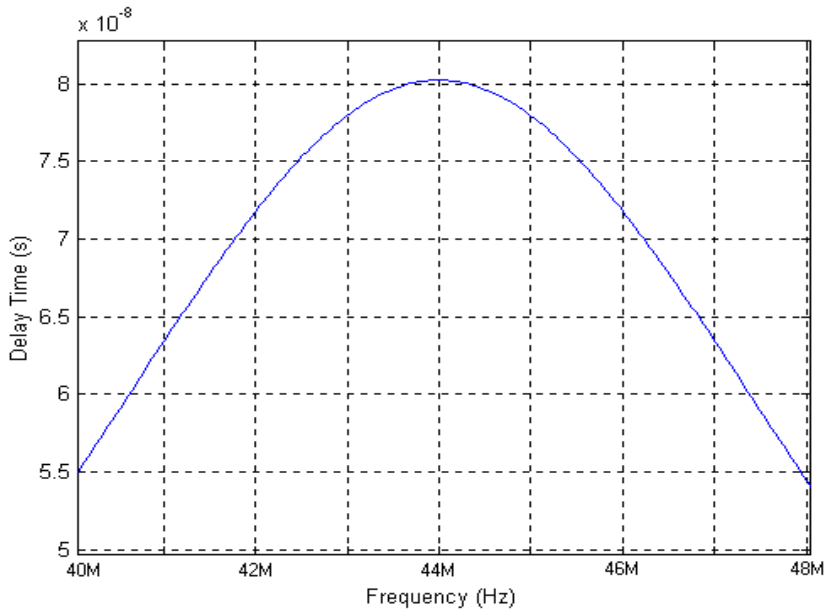


Figure 3.10 Delay time vs frequency of the filter

The frequency response of the modified double-sampling pseudo-2-path filter is the same as that obtained in the classical double-sampling biquadratic SC filter. The center frequency is located at 44MHz with 6MHz bandwidth. Table 3.2 summarizes the

designed filter characteristics.

Table 3.2 Summary of modified double-sampling pseudo-2-path filter characteristics

Parameters	**Simulation Results**
Center Frequency	44MHz
Bandwidth	6MHz
Passband Gain	0dB to 18dB (6dB each step)
Attenuation @ Fc +/- 6MHz	-9.1dBc
Group Delay	18ns
Filter orders	6
No. of Opamps	3
Capacitor Spread	1.93
Effectively Sampling Frequency	176MHz

Reference

[1] G. Palmisano and F. Montecchi, "Simplified Pseudo-N-Path Cells for z to –zN Transformed SC Active Filters", IEEE Transactions on Circuits and Systems, vol. 36, No. 3, pp.461-3, March 1989.

[2] J. C. Lin and Joseph H. Nevin, "Differential Charge-Domain Bilinear-Z Switched-Capacitor Pseudo-N-Path Filters", IEEE Transactions on Circuits and Systems, vol. 35, No. 4, pp.409-415, April 1988.

[3] J. J. F. Rijns and H. Wallinga, "Spectral Analysis of Double-Sampling Switched-Capacitor Filters", *IEEE Transactions on circuit and systems*, vol. 38, pp1269-1279, November 1991.

[4] Shen-Iuan Liu, Chien-Hung Kuo, Ruey-Yuan Tsai, and Jingshown Wu, "A Double-Sampling Pseudo-Two-Path Bandpass ΔΣ Modulator," IEEE J. Solid-State Circuits, vol. 35, pp. 276-280, February. 2000.

Chapter 4

Transistor Level Implementation of a 44-MHz SC Filter

The proposed double-sampling pseudo-2-path technique only needs one opamp to implement a second-order bandpass filter. For high-speed applications, a high dc-gain and fast transient response opamp is needed to maintain the transfer function. At 3-V voltage supply, the single-stage cascode opamp [1] [2] is preferred to the multi-stage cascade opamp [3] [4]. In this chapter, the required opamp's performance will be discussed. To maintain the operation of the filter, the three complementary clock phases generator is designed. The full-differential telescopic opamp with dynamic common-mode feedback that is employed in the filter will be investigated. Finally, the transistor-level simulation of the filter by Hspice will be given.

4.1 Opamp Consideration and Specification

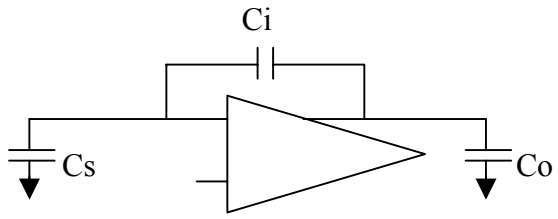
Voltage supply and power consumption: The opamp is designed at 3-V supply. For high-speed application, the minimum current consumption of the opamp is limited by the slew-rate requirement. The power consumption of the opamp is designed to be around 30mW. Therefore the power consumption of the whole filter is around 90mW.

DC gain and phase margin: By SWITCAP2 [5], the minimum dc gain of the opamp is 60dB to maintain the transfer function. The phase margin of the opamp should be larger than 60^{O} to avoid stability problems.

Unity-gain frequency: The minimum of the unity-gain frequency of the opamp is related to the minimum of the settling time of the opamp. For classical SC circuit [6], the required unity-gain frequency of the opamp is about 5 to 10 times larger than the sampling frequency. Therefore the unity-gain frequency of the opamp is designed to have at least 880MHz. Since the sizes of the cascode transistors are big for high current draw circuit and chosen opamp is a single-pole topology, the parasitic capacitors at output nodes need to be taken into account of the load capacitor.

Settling time: The settling time of the opamp is designed to be less than 60% of the sampling time (5.68nsec). To achieve 0.1% settling accuracy, the time constant (Γ) of the opamp should be smaller than 5.68nsec X 0.6 / 7 = 0.4868nsec [6]. Since the chosen opamp is

a single-pole amplifier, the unity-gain frequency strongly depends on the load capacitor. Moreover, in the SC circuits, the opamp will be connected in the feedback loop by capacitors. Figure 4.1 illustrates the feedback loop in the integration phase. The feedback factor (F_B) and loading capacitor (C_L) in this filter are 0.4 and 1.1pF. The capacitor Cs includes the sampling capacitor and parasitic capacitor at input node of the opamp. Therefore, the minimum unity-gain frequency to meet the settling time is 1/(2 π x 0.4 x 0.4868nsec) = 820 MHz.



where

F_B= Ci/(Ci+Cs)

C_L=Co+Cs*Ci/(Cs+Ci)

Figure 4.1 Feedback loop in the integration phase

Slew rate: SC circuit is a sample and hold circuit. Therefore, the opamp should have a high enough slew rate to rise the output node's voltage at the beginning of the clock period. Then the opamp will be operated at settling mode. The relationship among the time of slew rate (T_{SR}), settling time ($T_{settling}$) and clock period (T_s) is shown in equation 4.1.

$$T_{SR}+T_{settling} < T_s \qquad \textbf{(4.1)}$$

In this case, the loading capacitor is equal to Co plus Ci. Note that the value of the loading capacitor in slew mode is different in settling mode. The reason is that the input node of the opamp seems to be a virtual ground in the slew mode. The slew rate's time is set to less than 20% of the sampling period. For the output swing is 1.1V, the slew rate equals to

1.1/(0.2*5.68nsec) = 0.88V/ns.

The specifications of the opamp are set by the equations or considerations above. Table 4.1 summaries the specifications of the required opamp.

Table 4.1 Specifications of the opamp

Parameters	**Specifications**
Supply Voltage	3V
Power Consumption	<90mW
Low-Frequency Gain	>60dB
Unity-Gain Frequency	>820MHz
Phase Margin	$>60^{o}$
Output Swing	>1.1V
Settling Time	<0.4868nsec
Slew Rate	0.88V/ns
Load Capacitor	1.5pF

4.2 Opamp Design

A Single-stage telescopic operational amplifier with gain boosting technique is employed to achieve high gain-bandwidth product with low power consumption. The opamp is implemented with TSMC 0.35um CMOS N-well process with NMOS and PMOS threshold voltages of 0.6V and –0.8V respectively. Figure 4.2 shows the opamp circuit.

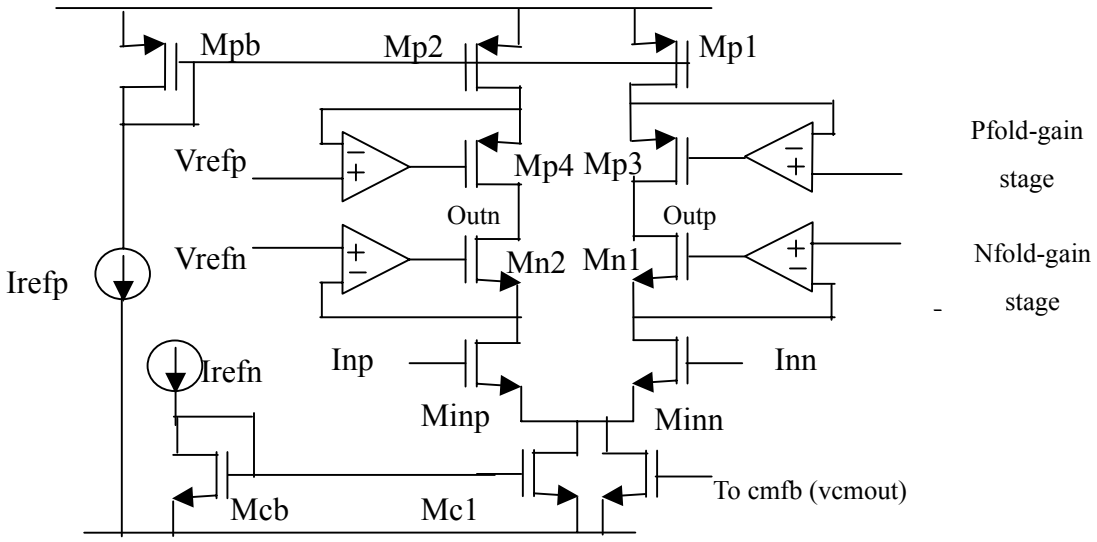


Figure 4.2 Schematic of the telescopic opamp with gain boosting technique

In order to have a high-speed opamp, all the transistors (except Mc1, Mc2 and Mcb) are set to the minimium channel length (0.4um). A NMOS differential input pair is employed to mininize the input capacitors that are considered as the parasitic capacitors of the input nodes. To have more than 60dB low-frequency gain and 820MHz unity-gain frequency, the size of the W/L of the input pair is set to large enough to have high transconductance (gm) and all the transitors should be operated in saturation region. Since the designed opamp is a differential output, the dynamic common-mode feedback (CMFB) circuit is needed to control the opamp in the high-gain region. Regarding stability, the current-source transistor is formed by two NMOS transistors (Mc1 & Mc2). The output voltage of the CMFB is only fed to Mc2. Additionally, the channel length of Mc1 and Mc2 are 0.6um. This can enhance the common-mode rejection rate of the opamp. Table 4.2 summarizes the transistor sizes of the telescopic opamp.

Table 4.2 Summary of the transistor sizes of the telescopic opamp

Transistors	Sizes	Quantity
Minp, Minn	6u/0.4u	24
Mn1, Mn2	5.8u/0.4u	36
Mp1, Mp2	5.2u/0.4u	80
Mp3, Mp4	5.2u/0.4u	48
Mc1, Mc2	5u/0.6u	80
Mcb	5u/0.6u	4
Mpb	5.2u/0.4u	8

The gain boosting technique (it amplifies the output resistance of the transistors Mn1, Mn2, Mp3 and Mp4) is used to have a high low-frequency gain opamp. Since the dc voltage levels for the opamps used to boost the output resistance of NMOS and PMOS are different, two different input-stage opamps are designed and are shown in fig. 4.3.

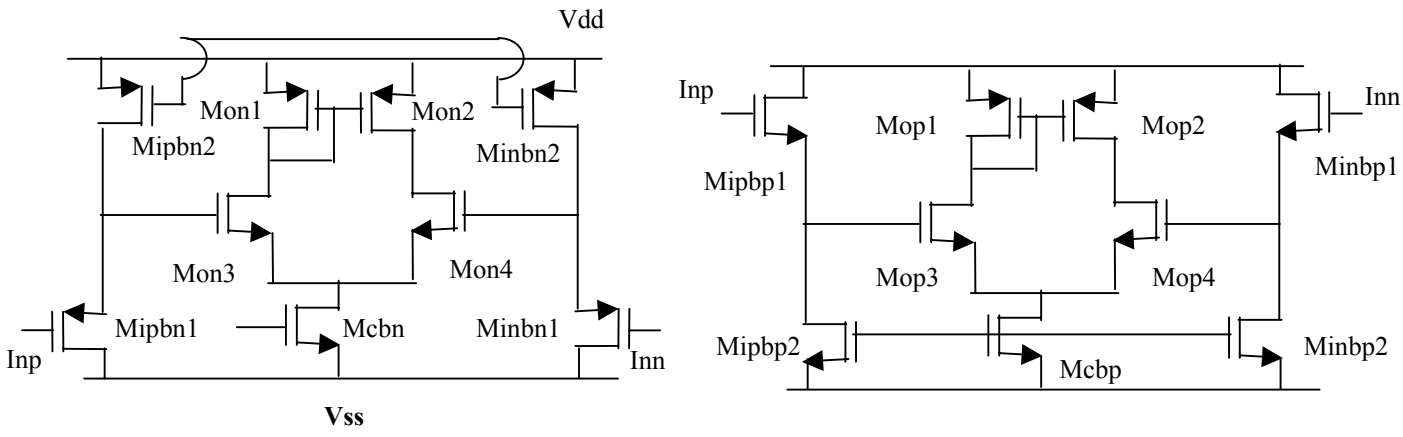


Figure 4.3 (a) Schematic Nfold-gain opamp *(b) Schematic Pfold-gain opamp*

In order to operate all the transistors in saturation mode, the input signal should be shifted to the suitable voltage level by level shifters (transistors Mipbp, Minbp and Mipbn, Minbn in

Pfold-gain opamp and Nfold-gain opamp). The opamps for gain boosting are also the single-stage topology. Table 4.3 and 4.4 summary the transistor sizes of the Nfold-gain opamp and Pfold-gain opamp respectively.

Table 4.3 Summary of the transistor sizes of the Nfold-gain opamp

Transistors	**Sizes**	**Quality**
Mipbn1, Minbn1	5.2u/0.4u	8
Mipbn2, Minbn2	5.2u/0.4u	4
Mon1, Mon2	4.2u/0.6u	4
Mon3, Mon4	6.6u/0.6u	4
Mcbn	5u/0.8u	12

Table 4.4 Summary of the transistor sizes of the Pfold-gain opamp

Transistors	**Sizes**	**Quality**
Mipbp1, Minbp1	5.2u/0.4u	4
Mipbp2, Minbp2	5.2u/0.4u	4
Mop1, Mop2	4.2u/0.6u	4
Mop3, Mop4	8.2u/0.6u	4
Mcbp	5u/0.8u	12

4.3 Simulation Results of the Opamp

The designed opamp is simulated with Hspice in the transistor level. Figure 4.4 illustrates the frequency response of the designed opamp. The simulation shows the low-frequency gain is 67dB and the unity-gain frequency is 900MHz with the phase margin of 63^{o}.

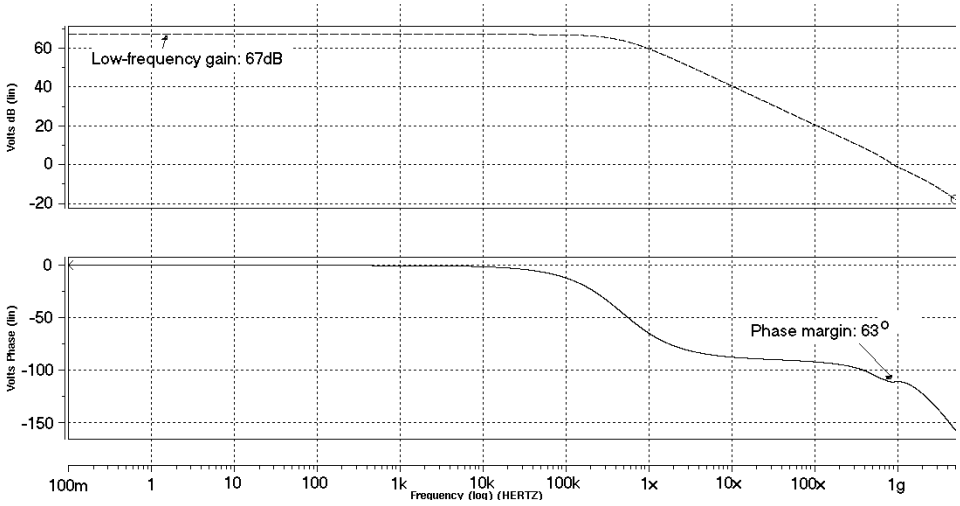


Figure 4.4 Amplitude response and phase of the opamp

The slew rate simulation of the opamp is done by input a differential voltage (2.2V) to the input nodes of the opamp. The transient response of the positive output node of the opamp is shown in fig. 4.5.

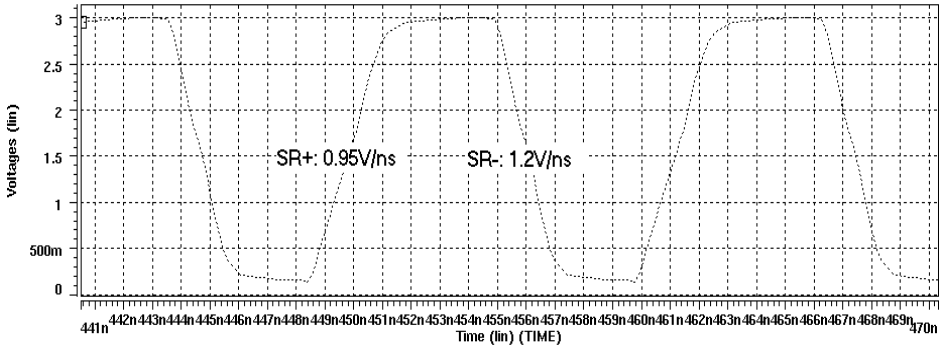


Figure 4.5 Slew-rate simulation results of the opamp

The simulation result indicates the slew rate for the positive trigger and for the negative trigger are 1.2V/ns and 0.95V/ns respectively. The simulation results of the designed opamp are summarized in table 4.5.

Table 4.5 Summary of the simulation results of the opamp

Parameters	**Pre-Sim Results (whole opamp)**	**Pre-Sim Results (Main opamp)**	**Pre-Sim Results (Gain-boosting stages)**
Supply Voltage	3V	3V	3V
Power Consumption	28.5mW	21.5mW	7mW (total power consumption)
Low-Frequency Gain	67dB	40dB	27dB
Unity-gain frequency	900MHz	910MHz	450MHz
Phase margin	63^o	67^o	60^o
SR(up)	0.95V/ns	0.97V/ns	N/A
SR(down)	1.2V/ns	1.25V/ns	N/A
Output Swing	+/- 1.1V	+/- 1.1V	N/A
Load Capacitor	1.5pF	1.5pF	N/A

4.4 Dynamic Common-Mode Feedback (CMFB)

Since the opamp is a differential output topology, the common-mode feedback circuit is needed to set the opamp in the high gain region. For a switched-capacitor circuit, there are two ways to do the CMFB circuit including continuous-time and discrete-time methods. In the discrete-time method, the dynamic CMFB circuit [7] [8] only works in the integration phase. Therefore, in general, the dynamic CMFB consumes less power than continuous-time CMFB. From the above consideration, the dynamic CMFB is adopted and shown in fig 4.6. In the real circuit implement, three CMFB circuits that work in the alternative clock phases are used.

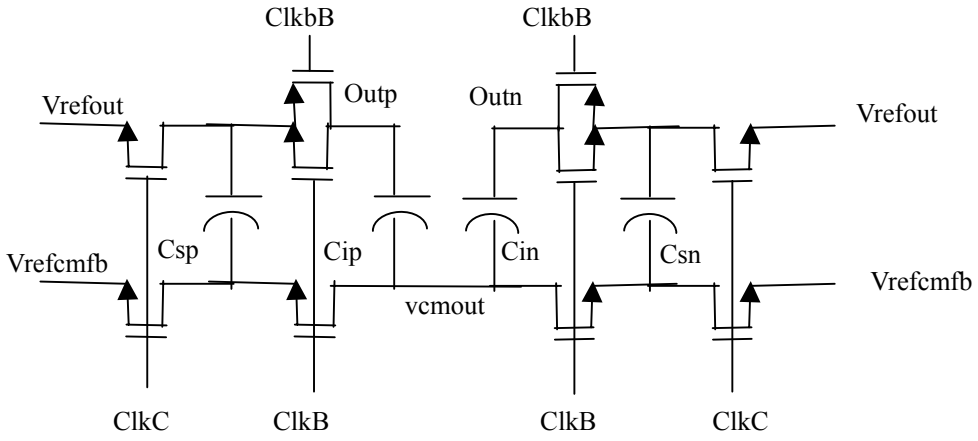


Figure 4.6 Dynamic Common-mode Feedback Circuit

Since the voltage at the output nodes of the filter can be as high as Vdd – 2Vdsat – Vdsmargin and as low as 3Vdsat+2Vdsmargin, a single MOS switch is not enough to achieve the whole dynamic range of the opamp. Complementary switches are employed to replace those switches. The differences between the dc output reference voltage and the voltage for the current transistor are stored in the charge form in the capacitors Csn and Csp at the clock C phase. When the complementary clock B phases are on, the reference charges will control the output dc voltage of the opamp. Figure 4.7 illustrates the transient response of the positive output node and vcmout node of the opamp with CMFB circuit. The output voltage of the opamp and the output voltage of the CMFB circuit is settled at 1.5V and 0.88V respectively, when clock phase is high.

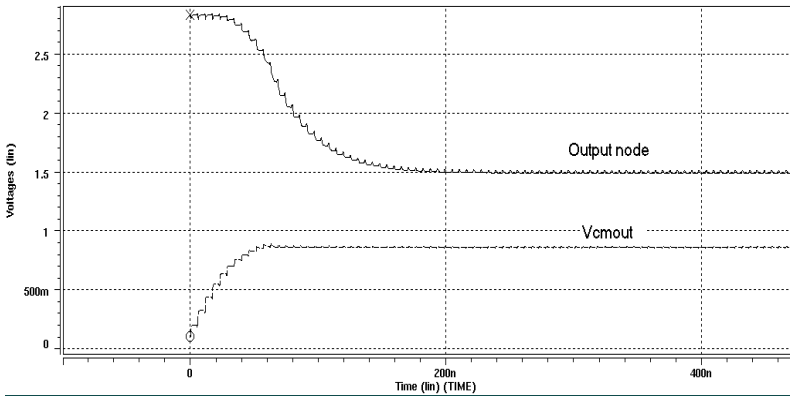


Figure 4.7 Transient response of the output node and the vcmout node of the opamp

4.5 Three Complementary Clock phases generator

In the modified double-sampling pseudo-2-path bandpass filter, the three complementary clock phases generator is required and is designed on chip. The on-chip clock generator not only achieves the whole system on a chip goal but also minimizes the mismatch among the paths. Figure 4.8 illustrates the block diagram of the clock generator [9].

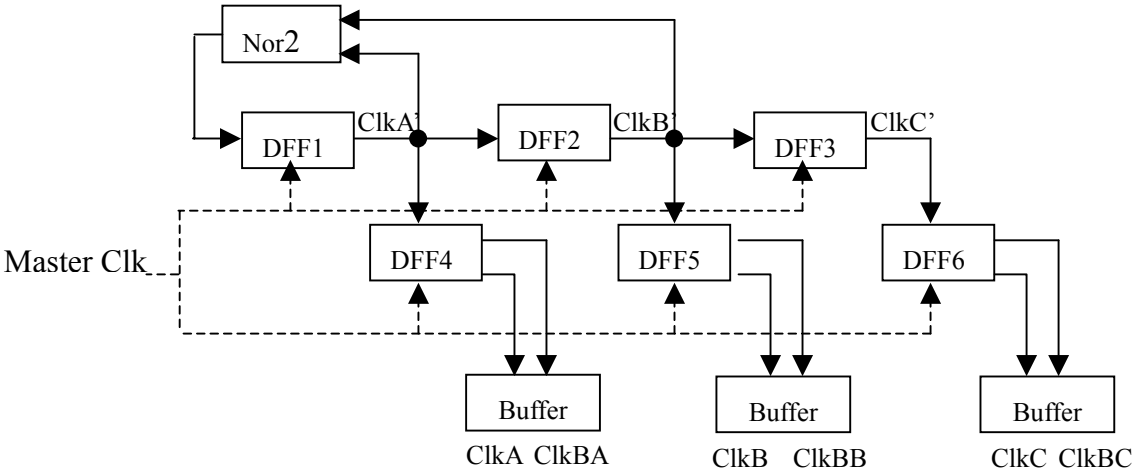


Figure 4.8 Block diagram of the clock generator

The D-type fip-flop circuit includes two C2MOS Latch and is illustrated in fig. 4.9. The D-type flip-flop circuit (DFF) 1, 2 and 3 are employed to divide the master clock frequency by 3. The Nor2 is a logic circuit to provide a high voltage output when two low voltages inputs.

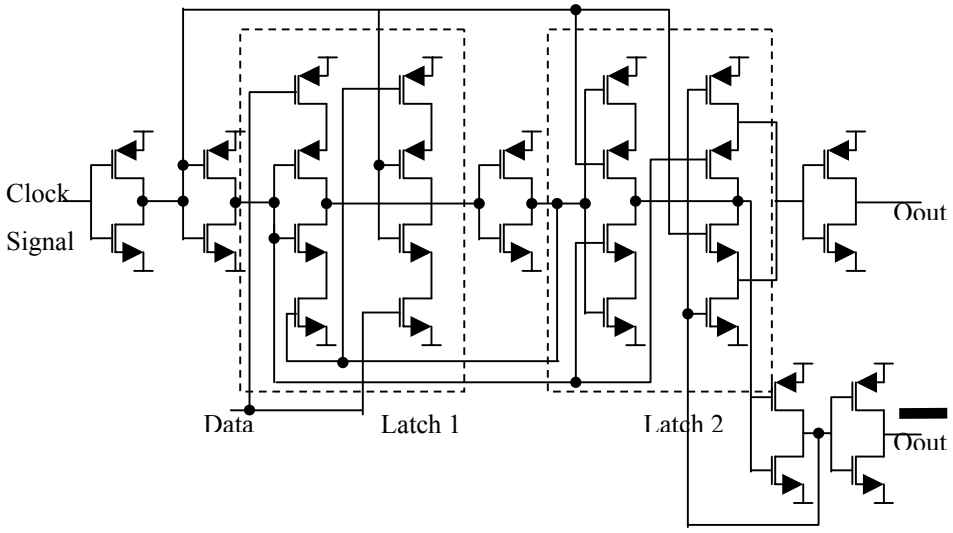


Figure 4.9 Schematic of the D-type flip flop

The ClkA',ClkB' and ClkC' are the non-overlap three clock phases and have the same frequency. In order to have a better synchronization among the three complementary clock phases, ClkA', ClkB' and ClkC' are applied to DFF4, DFF5 and DFF6 respectively and delay elements are inserted in the output buffer (shown in fig. 4.10). Clock phases (ClkA, ClkBA), (ClkB, ClkBB) and (ClkC, ClkBC) are generated out and are employed to drive the switches in the whole filter. The transient responses of the three complementary clock phases are plotted in fig. 4.11.

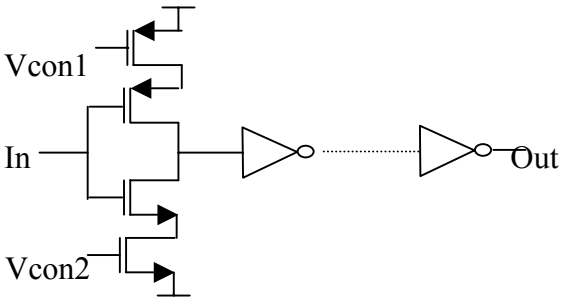


Figure 4.10 Output buffer with delay elements

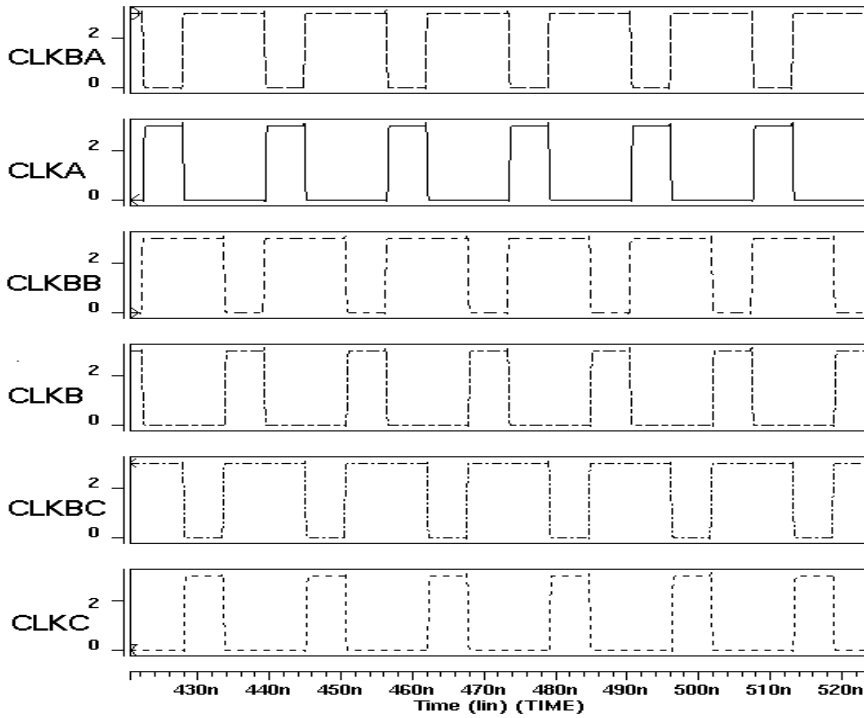


Figure 4.11 Simulated transient response of the outputs of the clock generator

4.6 Transistor-Level Simulation of the 44-MHz Bandpass Filter

The designed opamp with dynamic CMFB circuit is employed to build the fully differential 44-MHz bandpass filter. The transient response at the output node of the filter without applied input signal is shown in fig. 4.12.

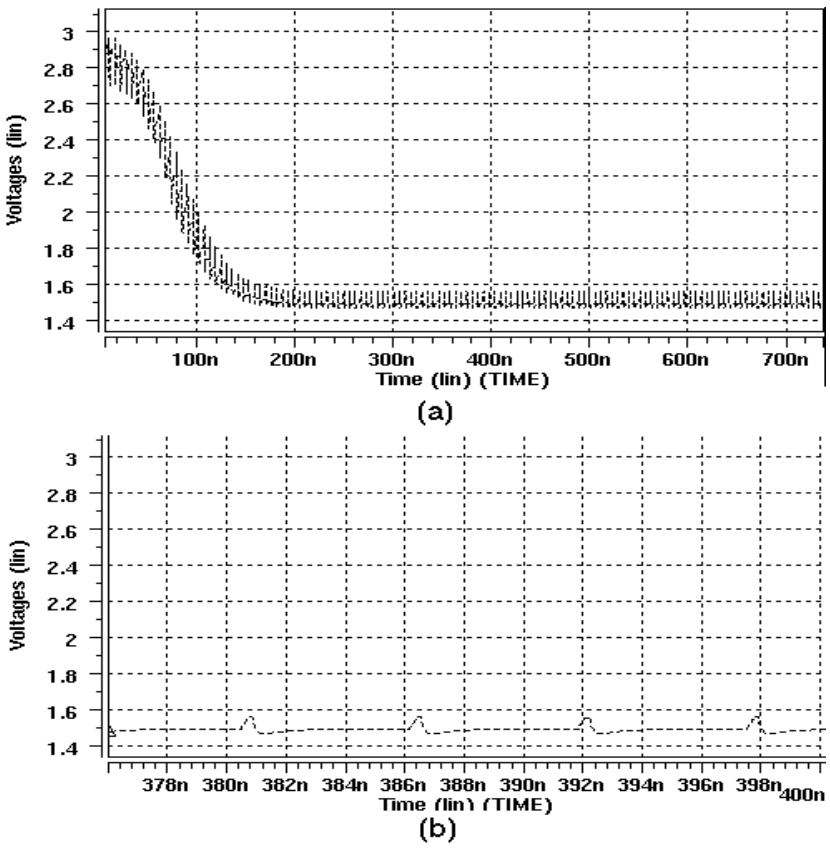


Figure 4.12 (a) Simulated transient response of the output of the bandpass filter (b) Close view version

The glitches in the transient response of the filter's output are due to the non-overlap clock phases. However, these glitches do not cause any settling error in the filter. The output voltage of the filter can be settled at 1.5V in every clock periods.

To operate the 44-MHz bandpass filter, the 176-MHz mater clock frequency is applied to the clock generator. In order to simulate the characteristics of the 44-MHz SC filter, 5 input signal frequencies (including 44-MHz center frequency, 47-MHz and 41-MHz two 3-dB corners, 10-MHz and 70-MHz two stop-band) with 0.1 Vp-p are employed in the filter. Figure 4.13 shows the transient response of the differential output signals of the filter.

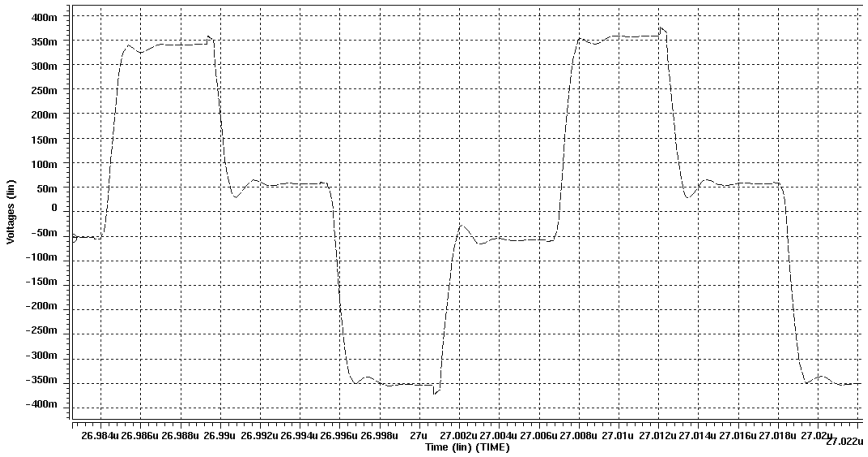


Figure 4.13 Simulated transient response of the differential output signals of the filter

By performing Fast-Fourier-Transformation (FFT) on the transient response, the frequency spectrum of the differential outputs of the filter is obtained and is illustrated in fig. 4.14.

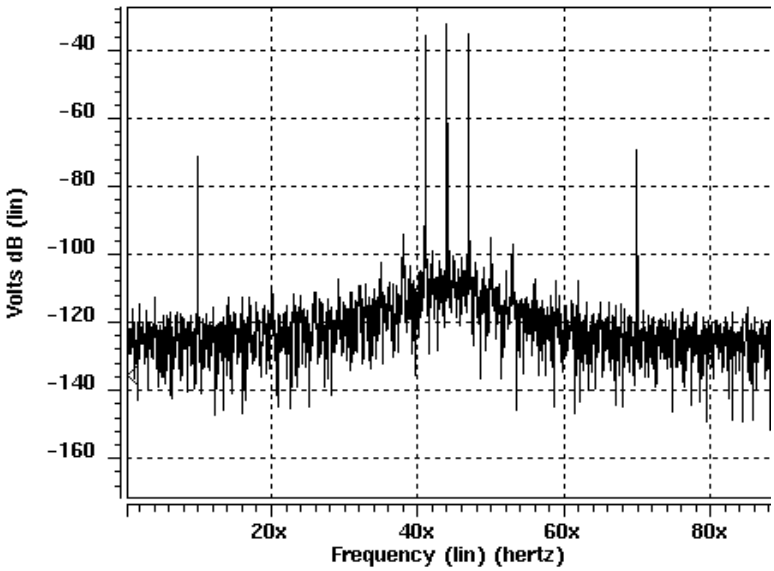


Figure 4.14 Simulated frequency spectrum of filter

The simulation results show that the signal outputs at 41-MHz and 47-MHz are lower than 44-MHz by 3 dB. The corresponding quality factor is 7.33 and the amplitude difference between the center frequency and the stop-band frequency is 38 dB. These simulation results

are same as the system simulation results. Table 4.6 summarizes the simulation results of the 44-MHz bandpass filter.

Table 4.6 Summary of the simulation results of the DSP2P 44-MHz bandpass filter

Parameters	Simulation Results
Supply Voltage	3V
Power Consumption	85.5mW
Center Frequency	44MHz
Effectively Sampling Frequency	176MHz
Bandwidth	47MHz-41MHz=6MHz
Passband Gain	0dB (with 18dB selectable gain)
Quality Factor (Q)	7.33
Capacitor Spread	1.925

Reference

[1] S. M. Mallya. and J.H. Nevin, "Design procedures for a fully differential folded-cascode CMOS operational amplifer", *IEEE Journal of Solid-State Circuits*, Vol. 24, No. 6, Dec.1989, p.1737-1740

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[6] R. Gregorian and G. C. Temes, *Analog MOS integrated circuits for signal processing*, John Wily & Sons, New York, 1986

[7] K. Suyama and Y. Tsividis, “Simulation of mixed switched-capacitor/digital networks with signal-driven switcheds.” *IEEE Journal Solid-State Circuits*, vol. 25, no. 6, pp.1403-1413,

Dec. 1990

[8] R. Castello and P. R. Gray, "A High-Performance Micropower Switched-Capacitor Filter", *IEEE Journal of Solid-State circuits*, pp. 1122 – 1132, Dec. 1985

[9] Dr. H.C. Huang, *Elec 303 Labwork Manual*, HKUST, 2000

Chapter 5

Layout Considerations and Post-Simulation

5.1 Layout and Post-Simulation of the Opamp

The schematic of the opamp is shown again in fig. 5.1 for easy discussion.

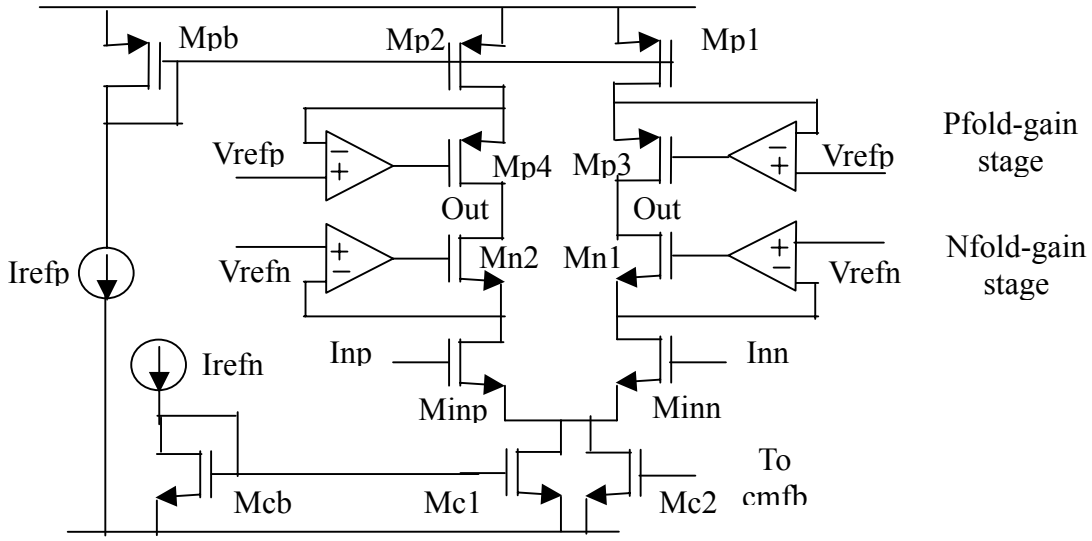

Figure 5.1 Schematic of the opamp

To minimize the offset of the opamp, the differential input pair (Minp and Minn), NMOS current source (Mc1 and Mc2) and PMOS current source (Mp1 and Mp2) transistors are laid in the pairs with common-centroid symmetry [1]. The four opamps (for boosting the impedance of the output transistors) are laid in symmetry with the telescope opamp. The layout floorplan and layout of the opamp are illustrated in fig. 5.2 and fig. 5.3 respectively.

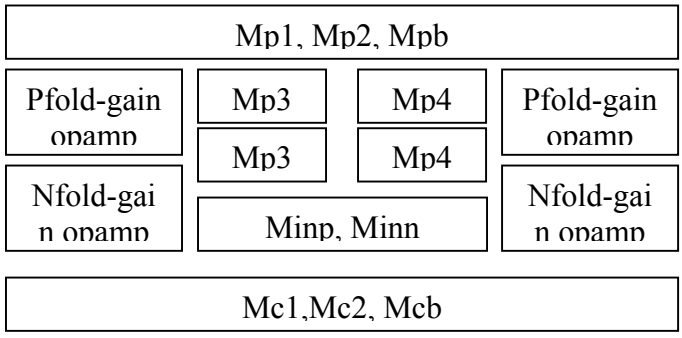

Figure 5.2 Layout floorplan of designed opamp

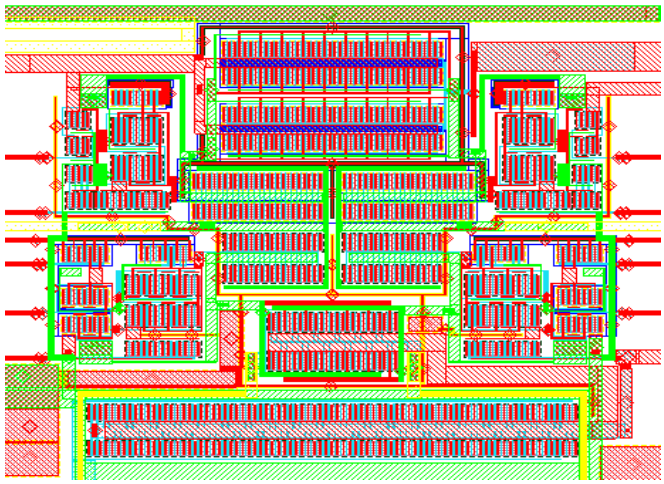

Figure 5.3 Layout of designed opamp

The post-simulation of the opamp is done by Hpsice with the TSMC 0.35um process. Figure 5.4 shows the opamp achieves a low-frequency gain with 67dB and unity-gain frequency of 900MHz with a phase margin of 63^{o}. The post-simulation results of the opame are summarized in table 5.1.

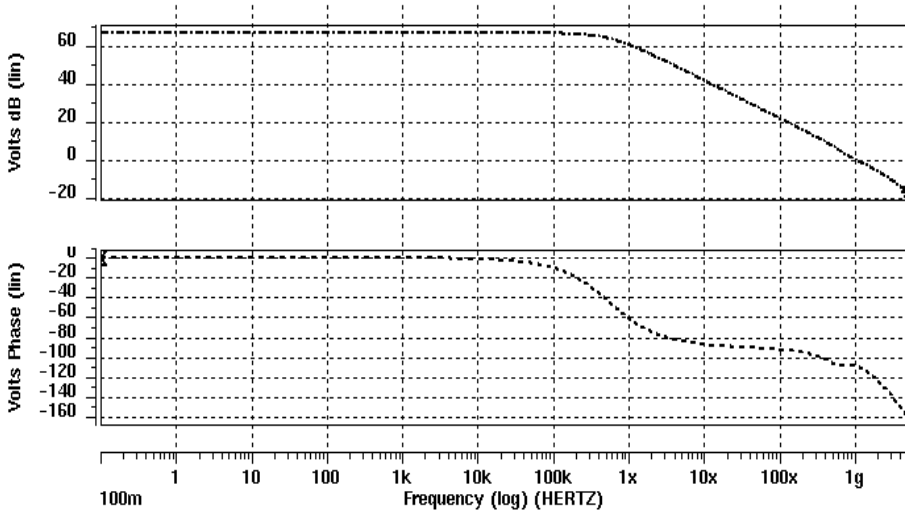

Figure 5.4 Frequency response of the opamp

Table 5.1 Summary of the post-simulation results of the opamp

Parameters	**Pro-Simulation Results**
Supply Voltage	3V
Power Consumption	28.5mW
Low-Frequency Gain	67dB
Unity-gain frequency	900MHz
Phase margin	63^{o}
SR(up)	0.93V/ns
SR(down)	1.18V/ns
Output Swing	+/- 1.1V
Load Capacitor	1.5pF

5.2 Layout of the SC Dynamic Common-Mode Feedback Circuit

Figure 5.5 shows one set of the dynamic common-mode feedback (CMFB) circuits. In practice, three sets of the dynamic CMFB circuits are employed. In order to have accurate operation and set both output terminals at the middle of the rails, capacitors Cip and Cin are laid with common-centroid symmetry. Figure 5.6 and 5.7 illustrates the layout floorplan and layout of the SC dynamic CMFB circuit.

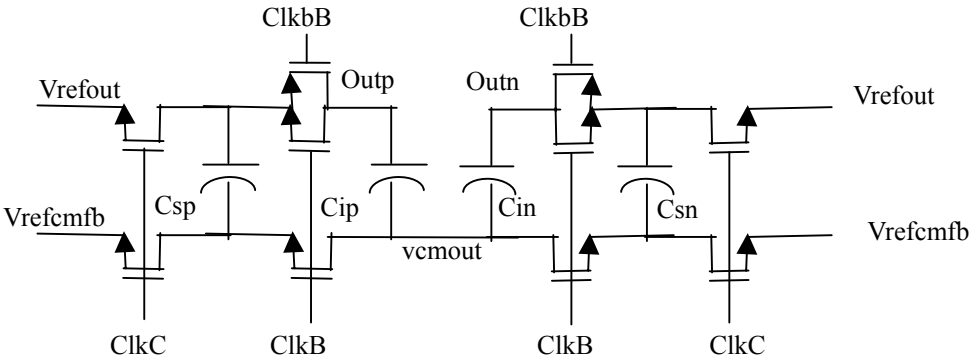

Figure 5.5 Schematic of the SC Dynamic CMFB circuit

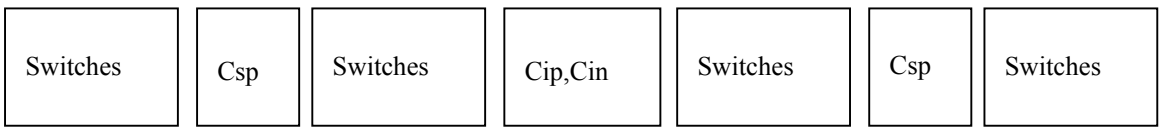

Figure 5.6 Layout floorplan of the SC Dynamic CMFB circuit

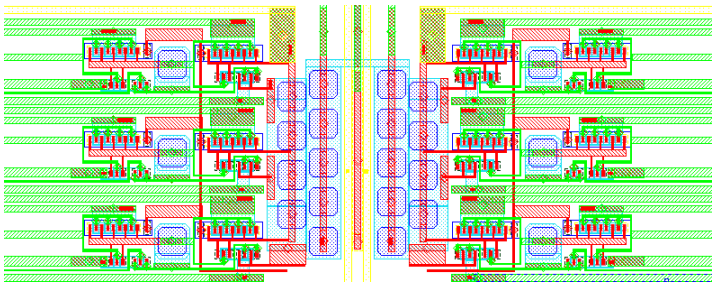

Figure 5.7 Layout of the SC Dynamic CMFB circuit

5.3 Layout of Linear Capacitors

Double polysilicons are used to implement all the linear capacitors in the filter in double-ploy four-metal 0.35um CMOS process. The horizontal view of the structure model of the linear capacitor (C_{linear}) is shown in fig. 5.8.

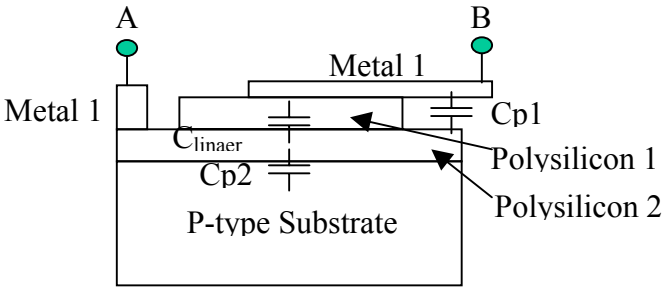

Figure 5.8 Horizontal view of linear capacitor

The two terminals of the linear capacitor are node A and node B. The parasitic capacitor Cp1 is formed by the metal 1 and ploysilicon 2. Since this parasitic capacitor Cp1 is parallel with the linear capacitor C_{linear}, the Cp1 will introduce an error to the total capacitor values. However, the value Cp1 is much smaller than C_{linear} due to thick distance, the Cp1 can be neglected with smaller overlap area between the metal 1 and polysilicon 2. The polysilicon 2 and P-type substrate will form the parasitic capacitor Cp2. The value of it is about 11% of the linear capacitor C_{linear}. If Cp2 is connected to the output node of the opamp, Cp2 will increase the loading capacitor of the opamp. On the other hand, if Cp2 is connected to the input node of the opamp, Cp2 will decrease the feedback factor in the integration phase and increase the parasitic capacitor in the

input node of the opamp. Since the increased loading capacitor will affect the performance of the filter more seriously than decreased feedback factor, the Cp2 is preferable to connect to the input node of the opamp. The layout of the linear capacitor is illustrated in fig. 5.9.

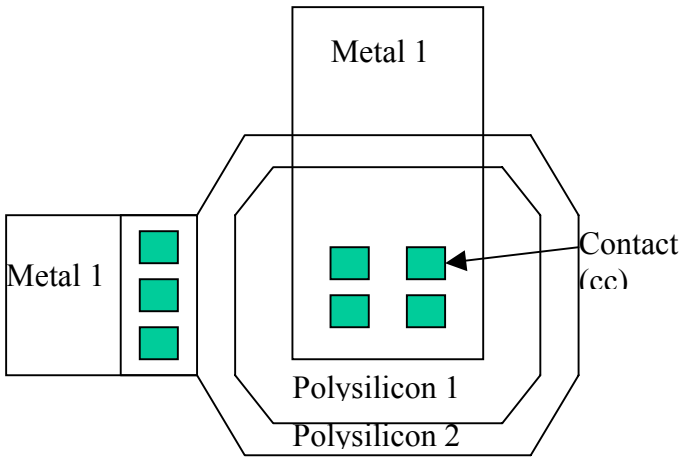

Figure 5.9 Layout of the linear capacitor

The linear capacitor is laid with squared structure [1] to minimize the capacitor error due to over-etching. All the corers of the polysilicon 1 are 45^{o} to have a better shape.

5.4 Layout of the Double-Sampling Pseudo-2-Path (DSP2P) Filter

The layout floorplan of the double-sampling pseudo-2-path filter is illustrated in fig. 5.8. Since the biasing buses are connected to some sensitive nodes (for example, the gate of the current source transistor), the biasing buses are laid at the top to minimize the clock feedthrough from the clock buses. In order to minimize the injected switching noise to the opamp, the ground-shielded guard ring is used to surround the opamp. The positive and negative sides of the capacitor arrays and switches are laid in symmetry. The layout of the DSP2P filter is shown in fig. 5.10.

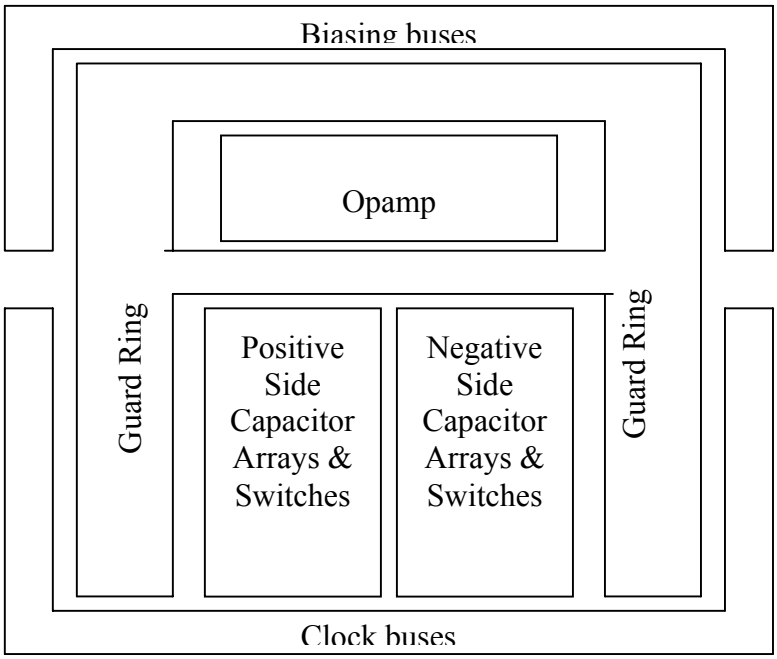

Figure 5.10 Layout floorplan of the DSP2P filter

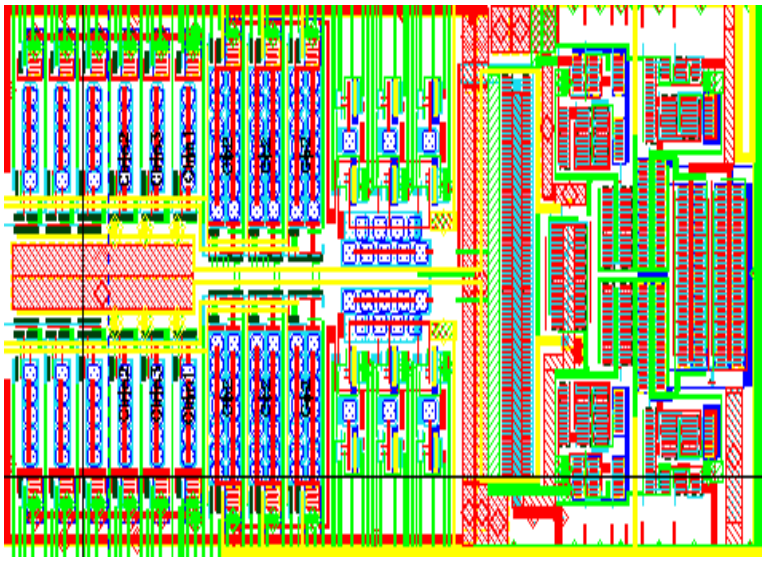

Figure 5.11 Layout of the DSP2P filter

5.5 Layout and Post-Simulation of the six-order SC Bandpass Filter

To minimize the clock slew, three of the second-order bandpass filters are laid in parallel. The three phases clock generator is placed at the bottom to minimize the noise

to the opamp from the generator. The layout flooplan and layout of the sixth-order SC bandpass filter are shown in fig. 5.12 and 5.13.

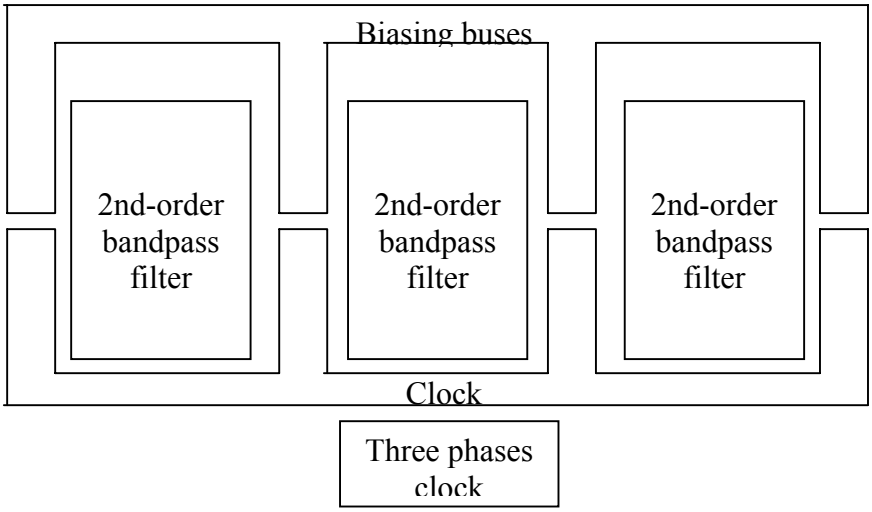

Figure 5.12 Layout floorplan of the sixth-order filter

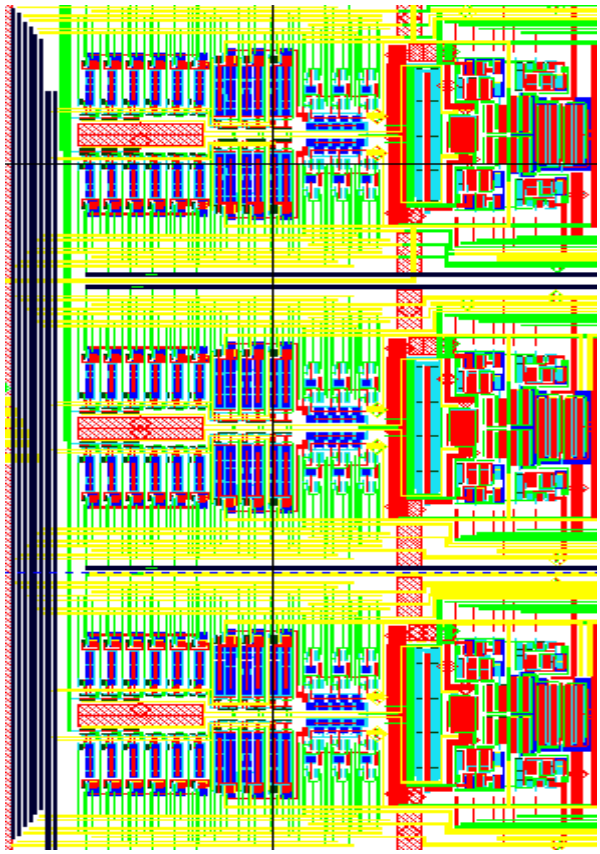

Figure 5.13 Layout of the sixth-order filter

Figure 5.14 shows frequency spectrum of the sixth-order filter with 0.1Vpp input signals at 44MHz (center frequency), 41MHz and 47MHz (two 3dB concers), 10MHz and 70MHz (two stopband frequencies). The signals at 11.7MHz, 14.7MHz and 17.7MHz are generated by the mismatch between the paths. The signals at 70.3MHz, 73.3MHz and 76.3MHz are the third harmonic of 41MHz, 44MHz and 47MHz and folded by the one clock phase frequency (for example, 41MHz X 3 - 58.7MHz = 73.3MHz). However, these signals will not locate at the interested band. The post-simulation of the six-order filter shows the proper operation at 44-MHz center frequency. Table 5.2 summarizes the post-simulation results of the filter.

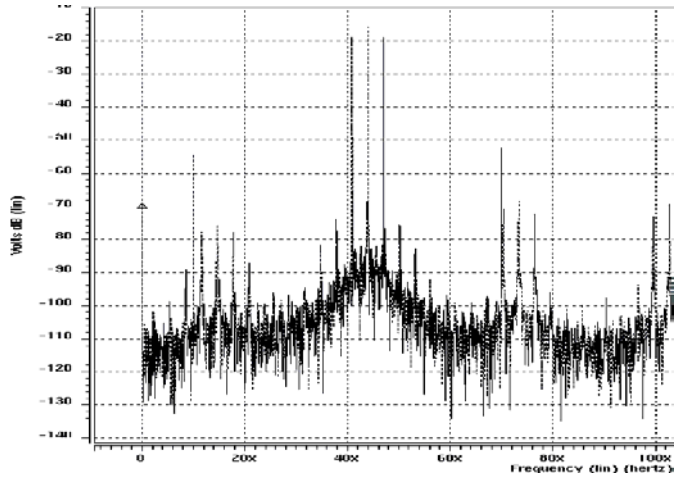

Figure 5.14 Frequency spectrum of the sixth-order filter

Table 5.2 Summary of the post-simulation results of the DSP2P 44-MHz bandpass filter

Parameters	Simulation Results
Supply Voltage	3V
Power Consumption	85.5mW
Center Frequency	44MHz
Effectively Sampling Frequency	176MHz
Bandwidth	47MHz-41MHz=6MHz
Passband Gain	0dB (with 18dB selectable gain)
Quality Factor (Q)	7.33
Capacitor Spread	1.925

Reference

[1] H. C. Luong, *Elec 504 Course Notes*, HKUST, 2000

Chapter 6

Measurement Considerations and Methodologies

In this chapter, the measurement considerations and methodologies will be discussed. The testing results of the opamp and the 44-MHz SC bandpass filter will be presented. From the measurement results, the possibility of operating SC bandpass fiters at 44-MHz is verified. Figure 6.1 illustrates the die photo of the testing chip, which consists of the 3-V 44-MHz SC bandpass filter and the testing circuit of the opamp.

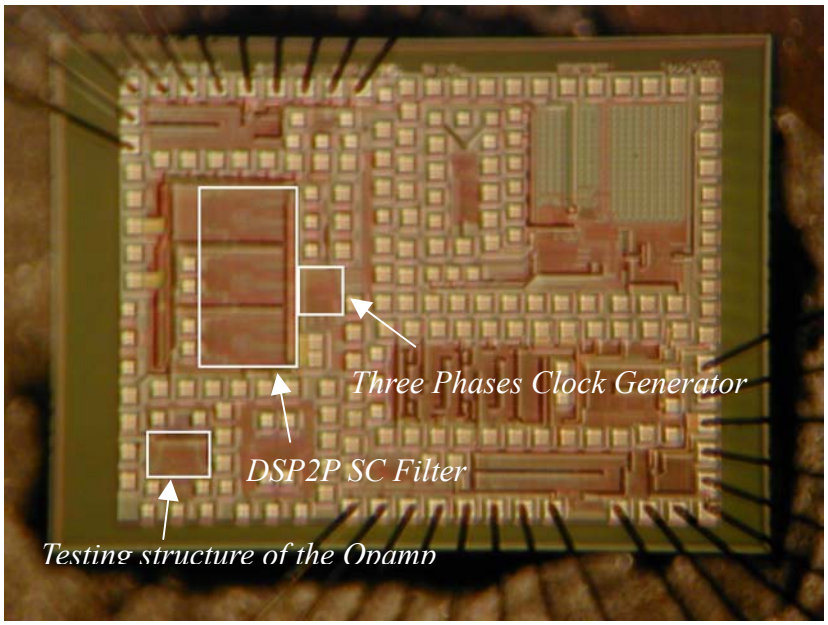

Figure 6.1 Die photo of the testing chip

6.1 Testing Considerations and Methodologies of the Designed Opamp

Since the low-frequency gain of the opamp is around 60dB, a feedback network is needed to stabilize the output nodes of the opamp. Figure 6.2 shows the testing setup for measuring the Bode plots of the opamp.

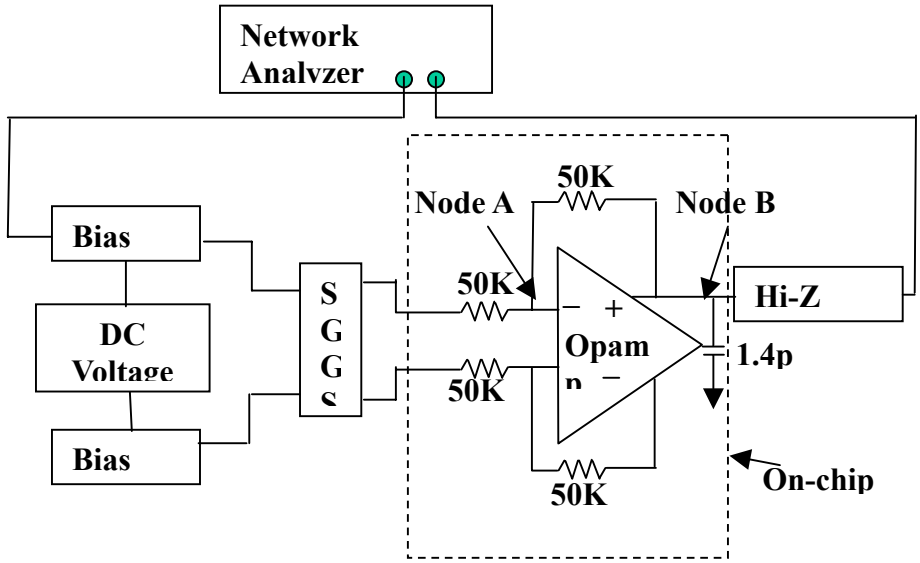

Figure 6.2 Testing setup for measuring frequency response of the opamp

The network analyzer is used to obtain the frequency response of the opamp. Since there is no on-chip buffer, the frequency response of the opamp is measured at the single-end by employing a high-impedance (Hi-Z) probe instead of a high-speed probe. The dc voltage supply is at 1.18V to set the output and the input dc operating point of the opamp at 1.5V and 1.34 respectively. The high-impedance probe is connected at node A and node B to obtain nodeA(s) and nodeB(s) frequency responses. From these frequency responses, the frequency response of the opamp (Op(s)) can be found. Equations 6.1 and 6.2 show the amplitude plot and phase plot of the opamp respectively.

$$|Op(s)| = \left|\frac{nodeB(s)}{nodeA(s)}\right| \qquad \textbf{(6.1)}$$

$$\angle Op(s) = \angle\frac{nodeB(s)}{nodeA(s)} \qquad \textbf{(6.2)}$$

The measured results show the single-ended low-frequency gain of the opamp is 48dB with a unity-gain frequency of 300MHz. The phase margin of the opamp is 50^o with power consumption of 30.2mW from a 3V supply.

For measuring the settling time of the opamp, the signal generator and digital oscilloscope are used. The on-chip capacitors feedback network models the situation of the integration phase of the filter. The on-chip resistor feedback network is used to set the dc operating point of the opamp [1]. The testing setup is shown in fig. 6.3.

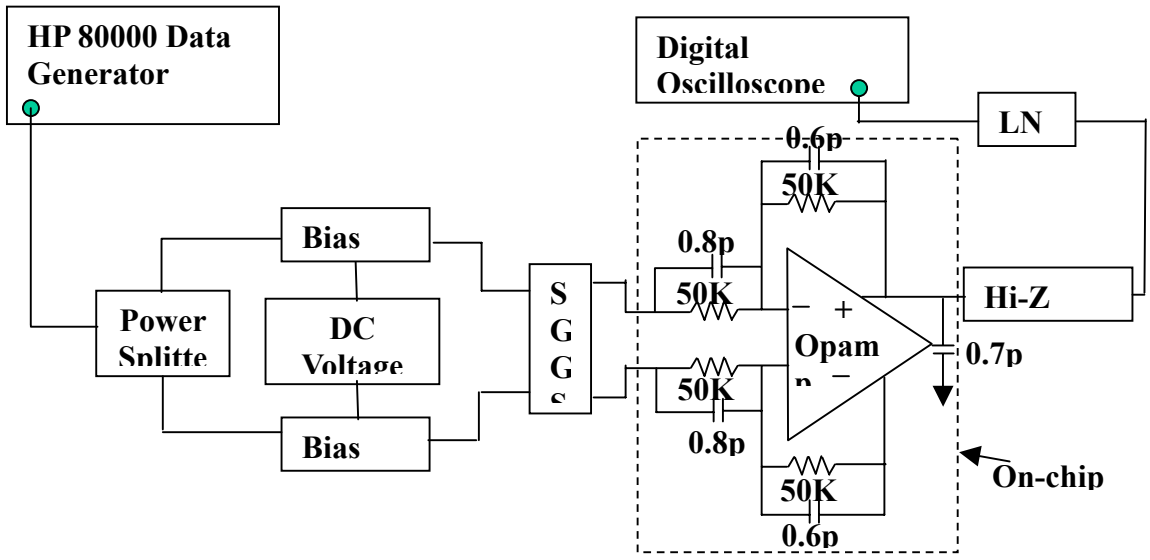

Figure 6.3 Testing setup for measuring the settling time of the opamp

The differential step-input voltage of 0.5Vp-p is applied to the inputs of the feedback network. The high-impedance (Hi-Z) probe is used to measure the transient

response of the opamp's outputs. Since the high-impedance probe has 20dB loss, the low noise amplifier (LNA) is employed to amplify the output signal so it can be sensed by the digital oscilloscope. Figure 6.4 illustrates the measurement result.

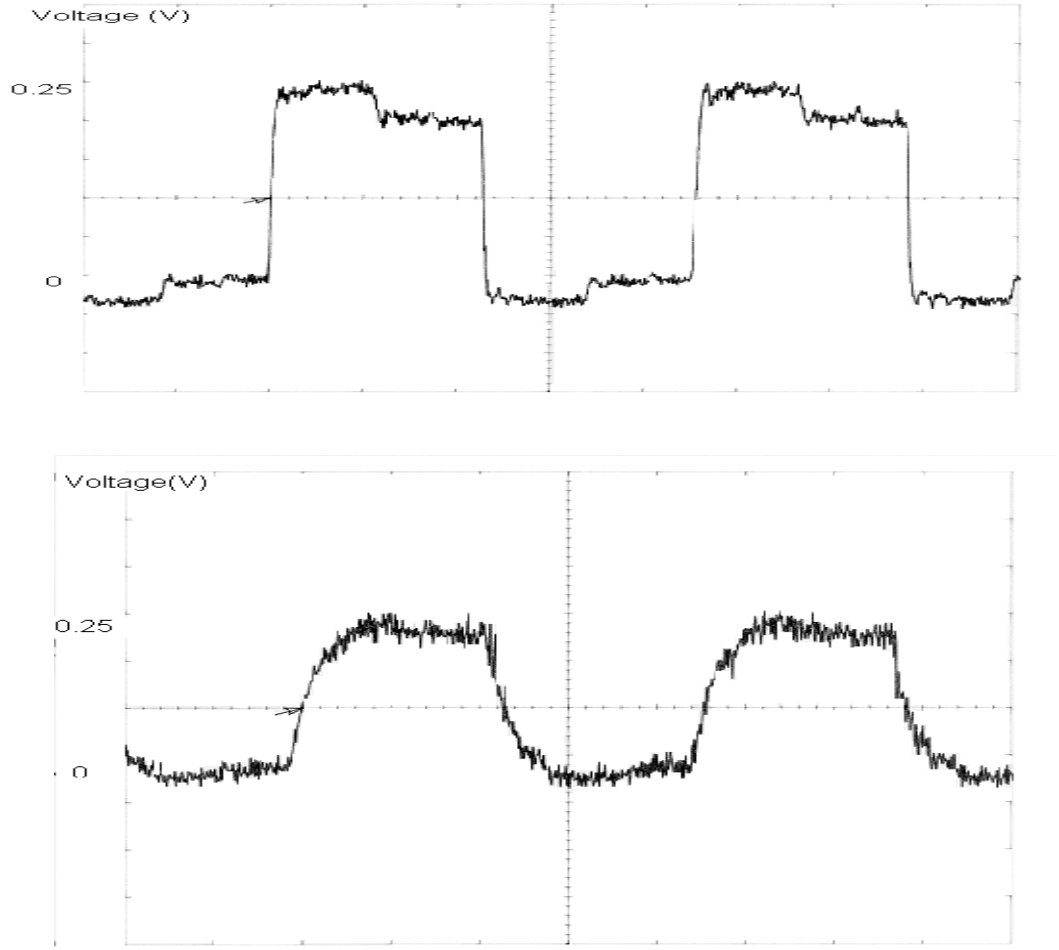

Figure 6.4 Measurement results of the settling time of the opamp

The measurement results show the settling of the opamp is less than 5n seconds. Other performances of the opamp are also measured. Table 6.1 summaries the opamp characteristics.

Table 6.1 Summary of the measurement results of the opamp

Parameters	**Results**
Technology	0.35um CMOS
Supply Voltage	3V
Low-Frequency Gain	54dB
Unity-Gain Frequency	600MHz
Phase Margin	50^{o}
Power Consumption	30.8mW
Output Swing	0.9V
Settling Time	<5ns

6.2 Measurement Results of the 44-MHz SC Bandpass Filter

The testing setup for measuring the 44-MHz SC bandpass filter is illustrated in fig. 6.5.

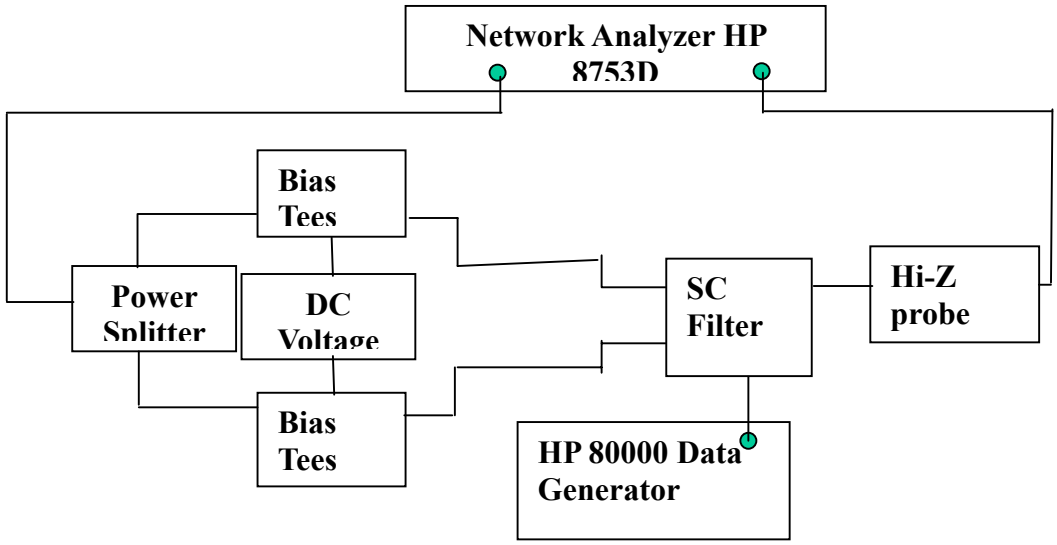

Figure 6.5 Testing setup of the 44-MHz SC bandpass filter

The data generator generates the 176Mhz square signal to the filter. The on-chip three phases clock generator is used to generate the three complementary clock phases (58.6MHz). The network analyzer is used to obtain the frequency response of the filter. The differential input signals are applied to the filter and a single-ended output signal is

measured by a high-impedance (Hi-Z) probe. The whole view and the close view of the measured frequency response of the filter are shown in fig. 6.6 and fig. 6.7 respectively. The frequency responses of the filter with different gain settings are illustrated in fig. 6.8.

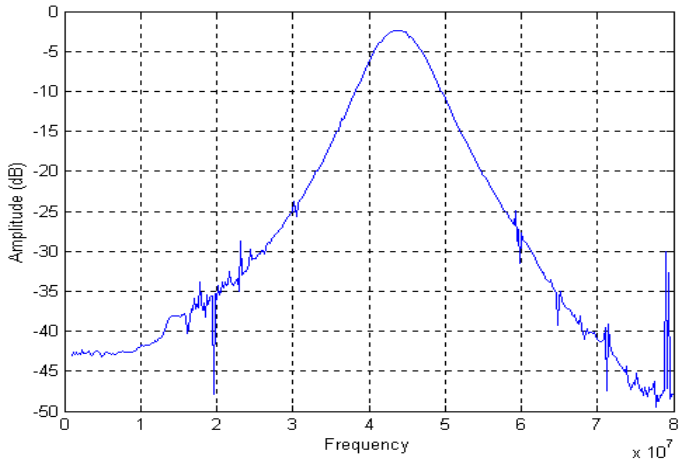

Figure 6.6 Frequency response of the 44-MHz SC bandpass filter

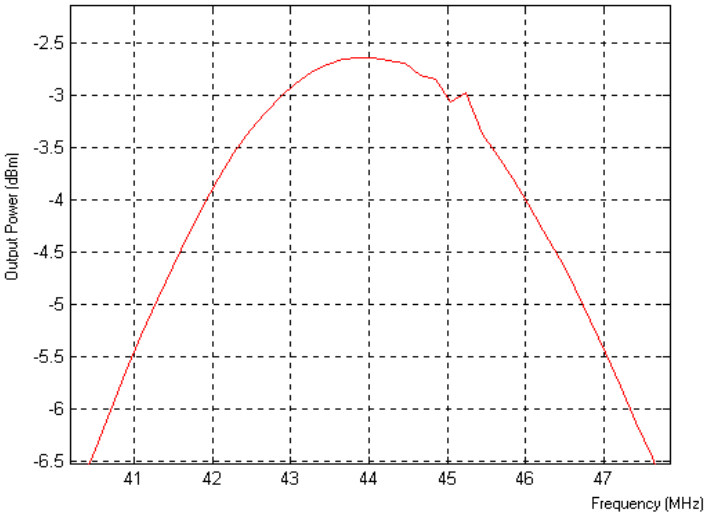

Figure 6.7 Close view of the frequency response of the 44-MHz SC bandpass filter

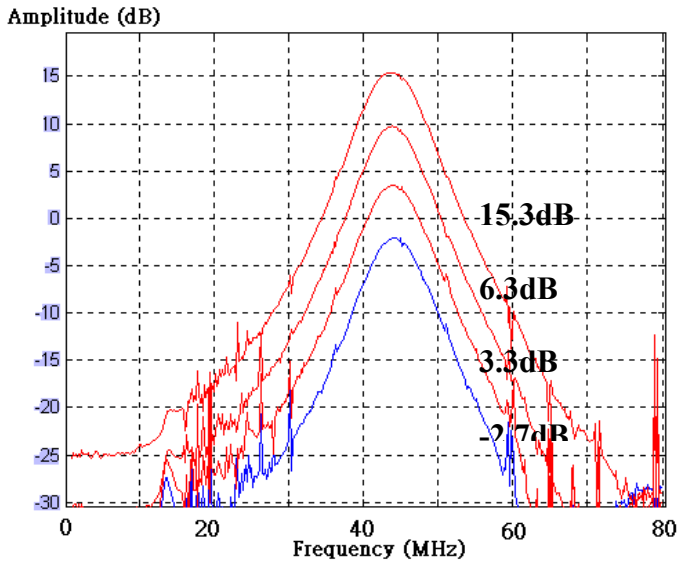

Figure 6.8 Frequency response of the SC bandpass filter with different gain setting

The measured results show the proposed SC bandpass filter can be operated at 44-MHz center frequency with quality factor of 7. The passband gain of the filter is -2.7dB. The degraded quality factor and passband gain is due to the lower dc gain of the opamp. The variation of the quality factor at different gain setting is within 1%.

The group delay of the SC filter is obtained by differentiation between the phase response of the filter with respect to the frequency [2]. The measured group delay is 23ns and is shown in fig. 6.9.

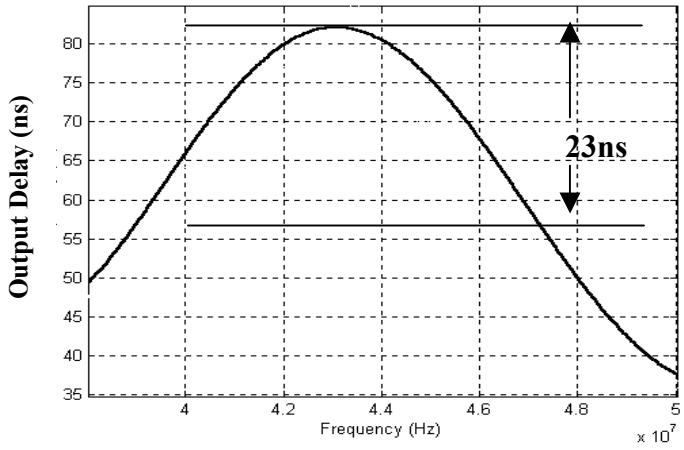

Figure 6.9 Measured group delay of the filter

To investigate the linearity of the filter, inter-modulation (IM3) and IP3 are measured with -2.7dB gain. The testing setup for measuring the linearity of the filter is illustrated in fig. 6.10.

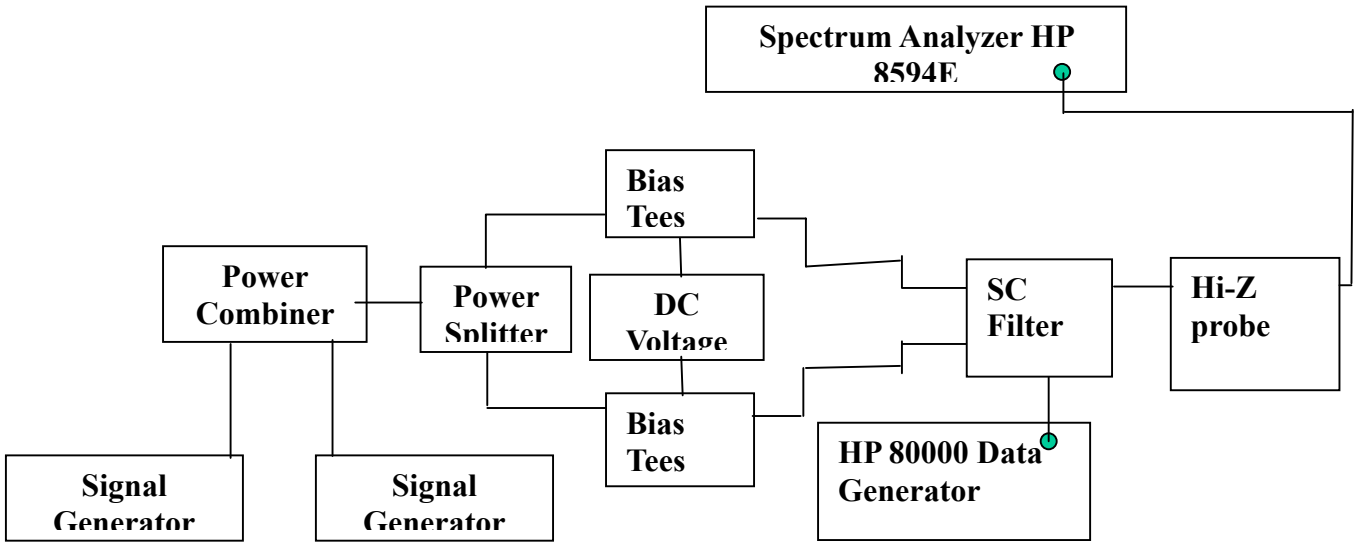

Figure 6.10 Testing setup for measuring the linearity of the filter

For measuring IM3, two sinusoidal signals at 43.5MHz and 44.5MHz are applied to the SC filter. The non-ideal linearity of the SC filter generates the signals at 42.5MHz and 45.5MHz. Figure 6.11 and 6.12 plot the 1% and 3% inter-modulation measurement results. The IM3 1% and 3% are measured with 0.36Vp-p and 0.89Vp-p input signals.

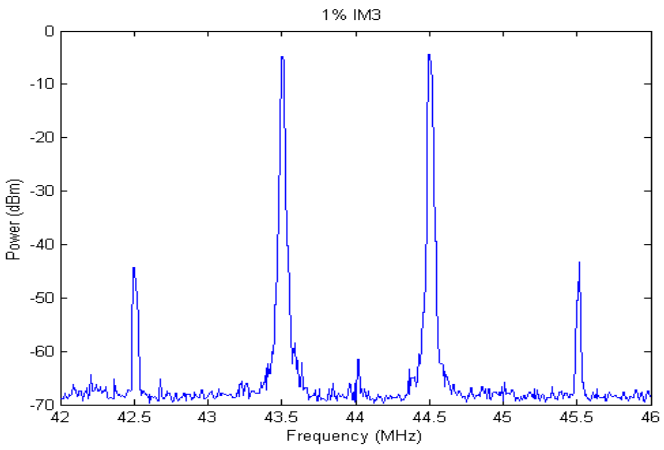

Figure 6.11 Measured IM3 1%

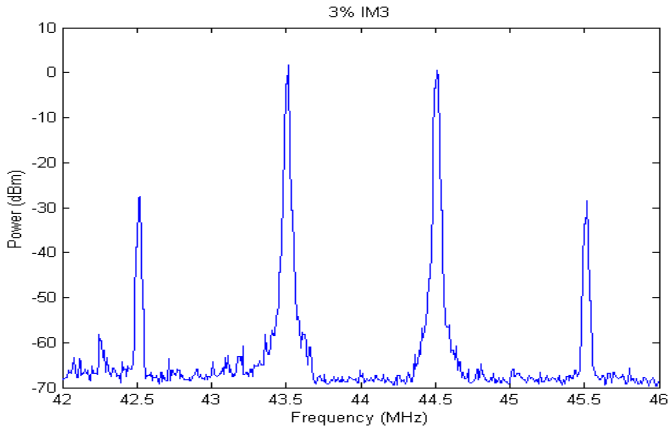

Figure 6.12 Measured IM3 3%

For the IP3 measurement, two sinusoidal signals at 50MHz and 56MHz are applied to the SC filter. The third harmonic distorted signal is located at 44MHz. The measured IP3 is illustrated in fig. 6.13. The measured IIP3 is 27dBm.

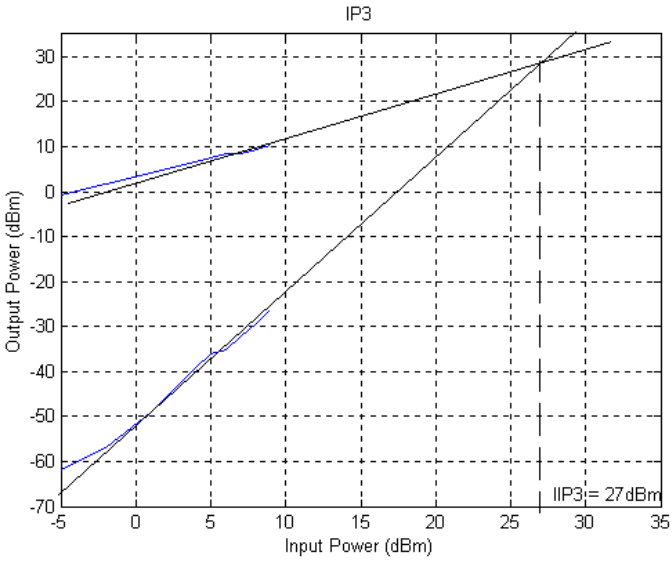

Figure 6.13 Measured IP3 of the SC filter

The measured peak output noise density is 162.52nV/√Hz. Therefore the total output noise power is 383.265u V_{rms}. The dynamic range (defined as $signal^{rms}/noise^{rms}$) at IM3 3% is 58dB. Table 6.2 summaries the measurement results of the 44-MHz SC filter and compares it with two low-Q SC bandpass filters.

Table 6.2 Summary the measurement results of the 44-MHz SC bandpass filter

Parameters	**This design**	**Nicollini [3]**	**R. F. Neves [4]**
Technology	0.35-um CMOS	0.8-um CMOS	0.8-um
Supply voltage	3V	3V	5V
Power consumption (Analog)	92.7 mW	23mW	125mW
Power consumption (Ditigal)	24.9 mW	N/A	N/A
Circuit Techniques	Double-Sampling Pseudo-2-Path	Decimation N-Path	Gain Enhancement Replica Amplifier
Sampling frequency	176MHz	107MHz	100MHz
Orders of filter	6	2	N/A
Q	7	10	7.5
Center frequency	44MHz	10.7MHz	37.5MHz
Attenuation @ Fc +/- 6MHz	-7.8dBc	N/A	N/A
IM3 3%	0.893Vp-p	N/A	N/A
Output noise density (at center frequency)	162.52nV/√Hz	1uV/√Hz	N/A
Total output noise	383.265u Vrms	707u Vrms	N/A
Dynamic range (1% IM3)	50.3 dB	58.4 dB	N/A
Dynamic range (3% IM3)	58.3 dB	N/A	N/A
Group delay	23ns	N/A	N/A
IIP3	27 dBm	N/A	N/A
Active area (Analog)	$0.4845mm^2$	$0.3mm^2$	$6.27mm^2$
Active area (Ditigal)	$0.036mm^2$	N/A	$1mm^2$

To conclude, the proposed double-sampling pseudo-2-path (DSP2P) filter is

realized in a 0.35μm standard CMOS process in a 3-V supply. With 176MHZ effective sampling frequency, the filter is operated at 44-MHz center frequency with 6.29MHz bandwidth with a total power consumption of 92.7mW. The filter demonstrates the possibility of operating the wide-band SC filter with the DSP2P technique at a high center frequency with low power consumption.

Reference

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Chapter 7

A Wide-band SC Bandpass filter with a High Roll-Off Characteristic

Demand for high data-rate integrated circuits has rapidly grown due to the technological development in all the applications, such as WCDMA and WLAN. The signal bandwidths of these applications are from several Mega-Hz to several ten Mega-Hz. If the signal is downconverted to a low IF, the quality factor of the required bandpass filter is very low. At the same time, the required bandpass filter is also needed to have a sharp transition from passband to stopband to eliminate the adjacent channel signals. It cannot be eliminated by the pre-filter. The roll-off of the conventional low-Q SC bandpass filter is not sharp enough. In this report, a high roll-off wide-band SC bandpass filter that can employ double-sampling technique is proposed

7.1 Specification of SC Bandpass Filter for Wireless Application

The biquadratic filter based structure is employed to realize the wide-band bandpass filter with high-roll-off characteristic. Table 7.1 summarizes the specification of the SC bandpass filter.

Table 7.1 Specification of the SC bandpass filter

Parameters	**Specification**
Passband Gain	10dB
Center Frequency (fc)	10MHz
Bandwidth	2.5MHz
Quality Factor	4
Sampling Frequency	40MHz
Attenuation @ fc +/- 2.5MHz	>35dB
Filter Order	12

7.2 Classical Filters with a high roll-off characteristic

Ladder filter (Based on Elliptic LCR Filter)

In Elliptic filter prototype, the transfer function has transmission zeros. Therefore, it is attractive to realize a high roll-off SC filter. Figure 7.1 illustrates a SC lowpass filter [1] (based on elliptic LCR filter with pseudo-2-path technique). The dot boxes indicate the delay and subtract switched capacitors. When clock 1 is high, all the opamps will be connected to form loops by the capacitors. As explain in section 2.3, these capacitors will degrade the speed of the filter. Therefore, elliptic SC ladder filter is not attractive to be implemented a wide-band SC filter at high center frequencies.

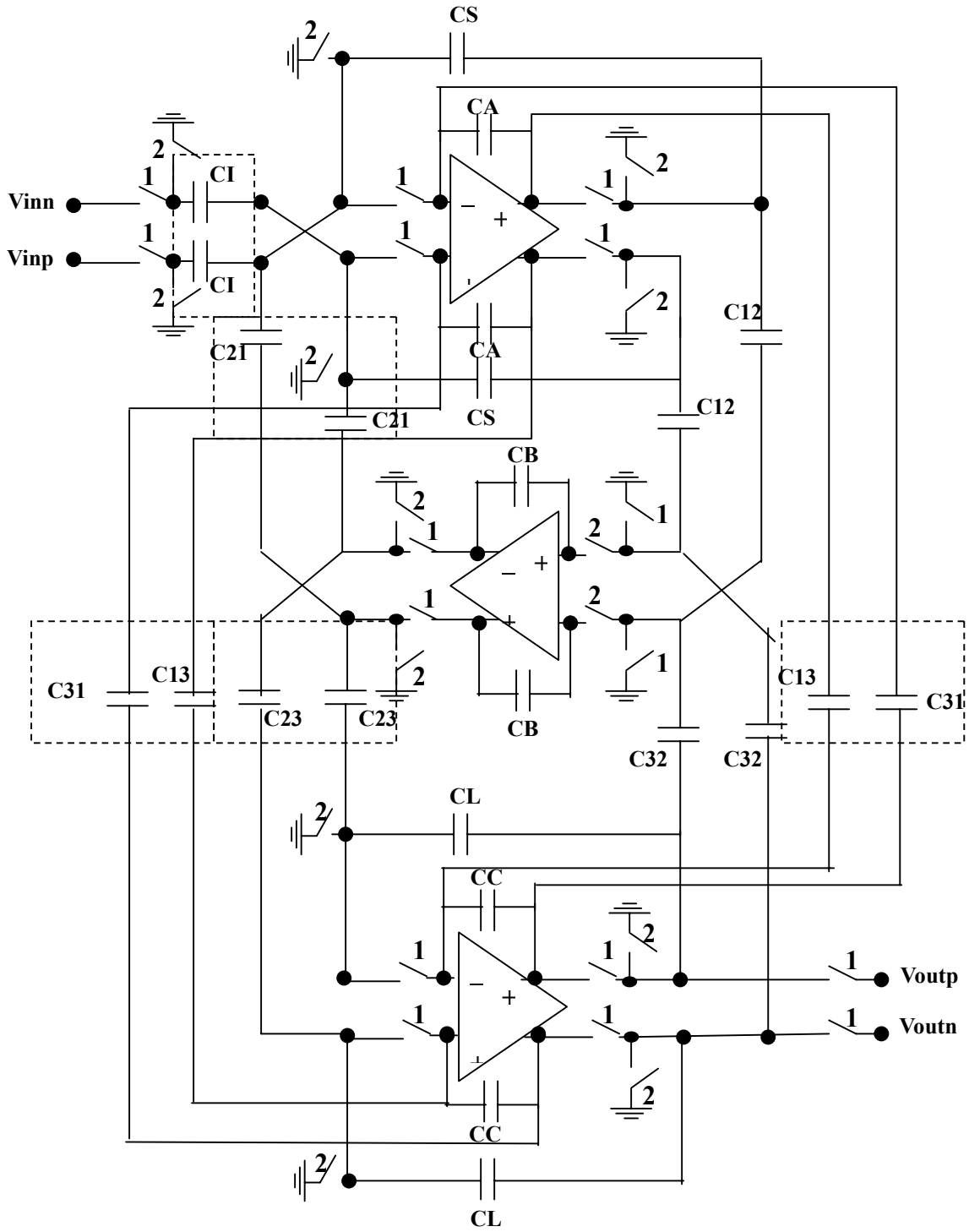

Figure 7.1 Schematic of a fully differential elliptic lowpass ladder filter

Biquadratic Filter

Figure 7.2 shows the conventional bandpass filter with a transmission zero [2].

Simple frequency reposes of that filter is plotted in fig. 7.3.

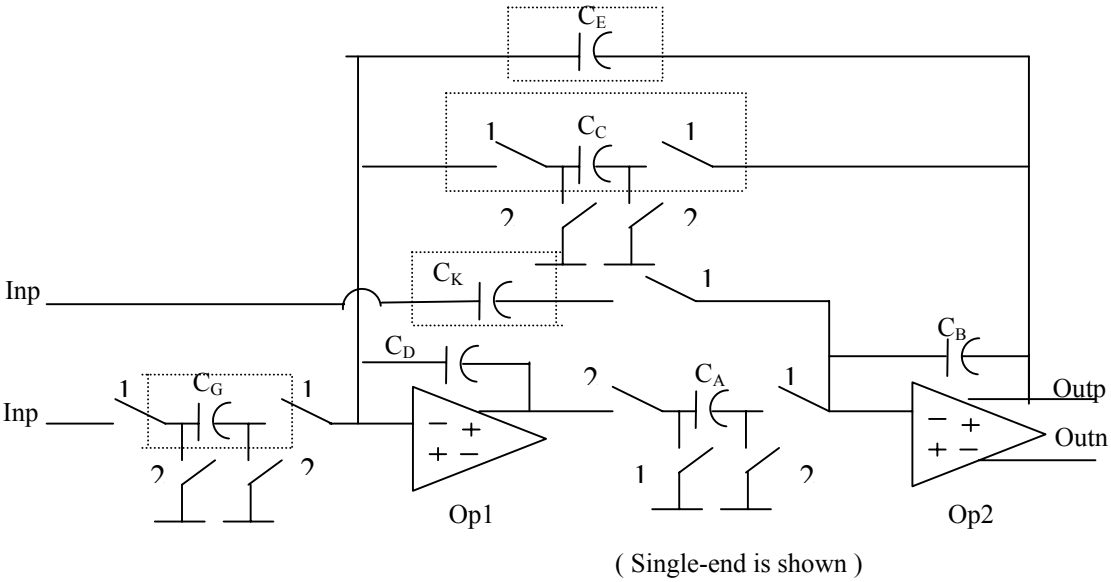

Figure 7.2 Schematic of the conventional high-pass filter with a transmission zero

The capacitor C_K, C_G are employed to form the transmission zero. The drawback of this schematic is the opamps will be connected by the capacitors (that are inside the dot boxes). As explain in section 2.3, these capacitors will limit the speed of the filter. Note that, opampe2 (Op2) works in integration phase and is directly connected with Op1 by capacitor C_C in phase one and holds the output voltage in phase two. Therefore, if other SC circuits follow this second-order filter, the output voltage of the filter will be taken in phase 2 [3]. This arrangement can relax the capacitor loading effect of Op2 at phase 1.

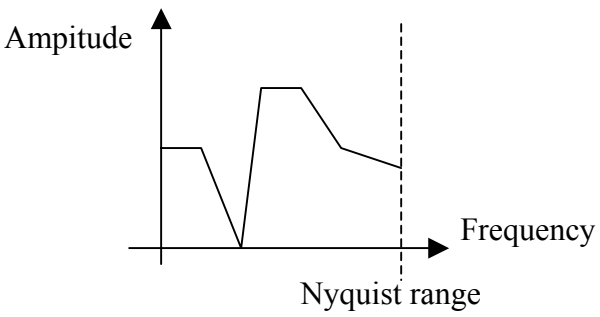

Figure 7.3 Simple frequency response of bandpass filter with a transmission zero

If filters need more transmission zeros to have enough attenuation and are

operated with double-sampling technique, more stages are cascaded to get the number of transmission zeros. However, this will limit the maximum sampling frequency dramatically due to the delay and subtract capacitor.

7.3 Proposed High Roll-Off Wide-Band SC Bandpass Filter

In the conventional biquadratic filter, there is a highpass filter with a zero term. If two high roll-off highpass filter with 2-path technique [4] are employed, the bandpass characteristic is obtained at $F_S/2$ and shown in fig.7.4. F_S and F_N are the sampling frequency and Nyquist range.

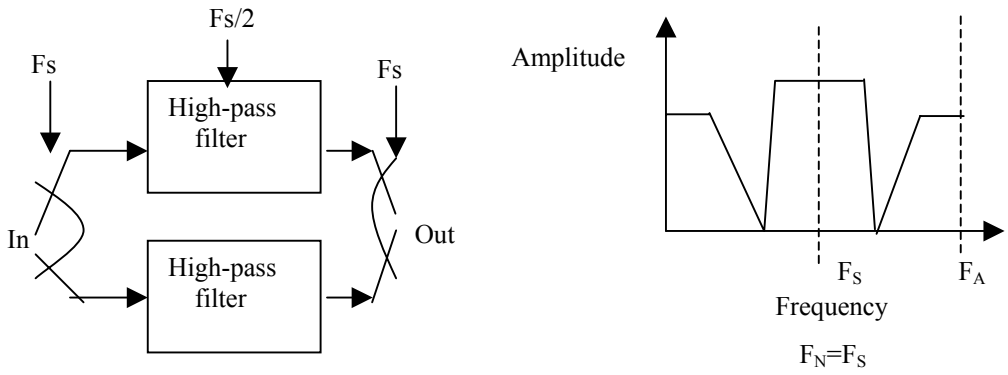

Figure 7.4 second-order highpass filters with 2-path structure

The main idea of the proposed architecture is that cascading two 2-path highpass filters to obtain enough roll-off at the adjacent channel. The block diagram of the proposed architecture is shown in fig. 7.5.

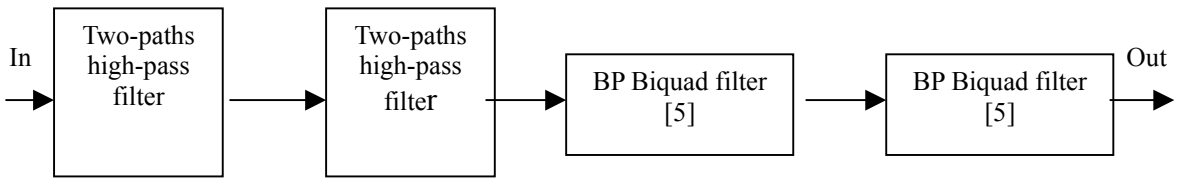

Figure 7.5 Block diagram of the proposed architecture

By employing 2-path technique, four transmission zeros can be designed

symmetric about the center frequency. To have enough attenuation at next two or three adjacent channels, two second-order bandpass filters [5] are used in the last two stages. The whole filter can employ double-sampling technique [6] to relax the requirement of the opamp.

7.4 Conventional High-Pass Filter with a Transmission Zero

The schematic of the high-pass filter with a transmission zero is same as fig. 7.2. The different capacitors values determine the filter is highpass filter or bandpass filter.

7.5 Proposed High-Pass Filter with a Transmission Zero

The proposed high-pass filter with a transmission zero term takes the advantage of the fully differential architecture and re-arrangement of the clock phase to avoid the directly connection among opamps.

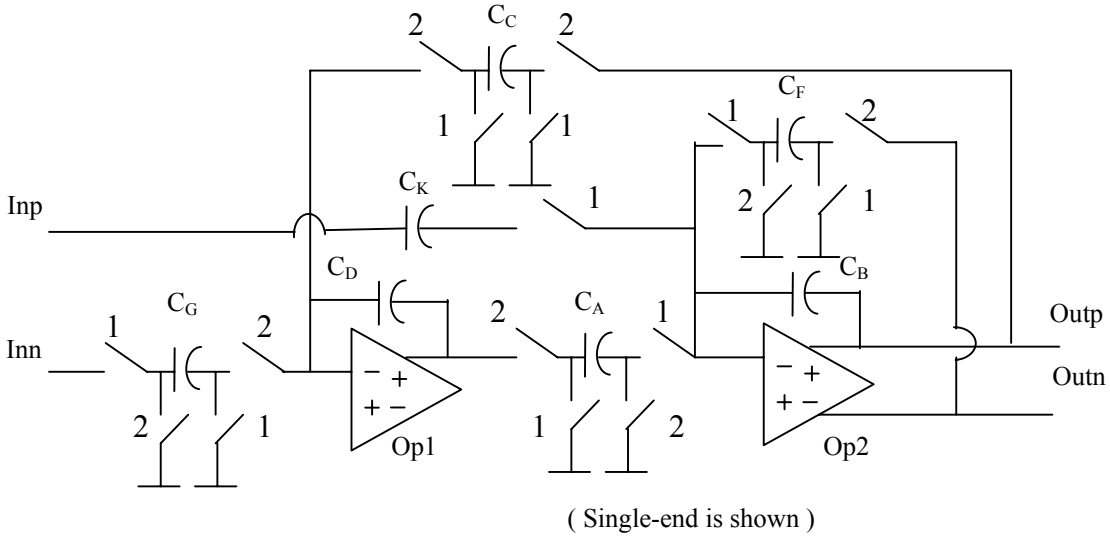

Figure 7.6 Schematic of proposed high-pass filter with a zero

In fig. 7.6, the capacitor C_G is an inverting switched capacitor. This modification avoids the any direct connection between the Op1 and the previous stage. In the proposed design, the Op2 only works in integration phase in clock one and holds the

output voltage to buffer Op1 and following stage. This arrangement reduces the loading capacitor of the Op2 at clock 1. At phase 2, since Op2 only hold the output voltage, the settling-time of the output nodes of the Op1 does not depend on the Op2. The above modification can allow the filter to work at higher sampling frequency. Equation 7.1 shows the transfer function of the filter in z-domain.

$$H(z)=\frac{C_DC_K-(2C_DC_K-C_AC_L-C_AC_G)z^{-1}+(C_DC_K-C_AC_L)z^{-2}}{C_DC_B-(2C_DC_B-C_AC_C-C_DC_F)z^{-1}+(C_DC_B-C_DC_F)z^{-2}} \quad \textbf{(7.1)}$$

7.6 Bandpass Filter with Fast-Settling Double-Sampling Structure [5]

Figure 7.7 illustrates the bandpass filter with fast-settling double-sampling structure. No delay and substrate capacitors are in this filter. Therefore, the opamps can be settled independently.

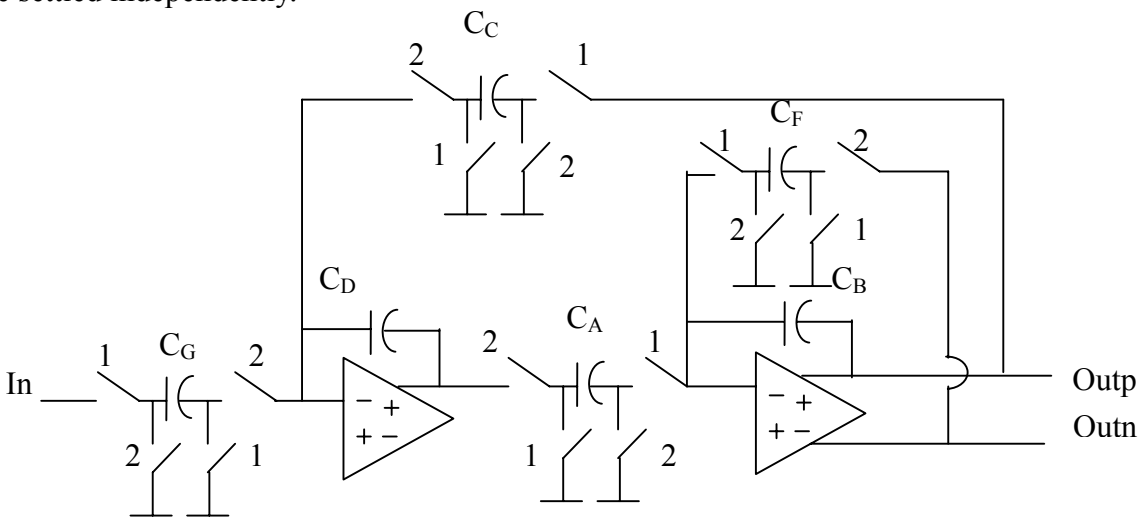

Figure 7.7 Bandpass filter with fast-settling double-sampling structure

7.7 System Simulation Results

The system simulation of the proposed filter is done by SWITCAP2 [8] and is illustrated in fig. 7.8.

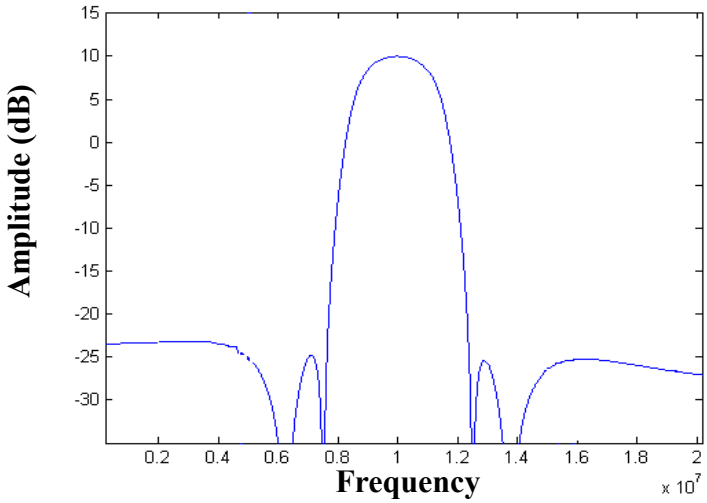

Figure 7.8 Frequency response of the proposed SC filter

As expected, four transmission zeros locate at 6.2MHz, 7.5MHz, 12.5MHz and 13.8MHz. The center frequency is at 10MHz with bandwidth of 2.5MHz. The attenuation at 7.5MHz and 12.5MHz are larger than 35dB. It is good enough for most of the receivers' requirement.

Figure 7.7 shows the comparison between the proposed filter and the conventional bandpass filter. The pole orders for both filters are 12. Table 7.2 summaries the comparison results.

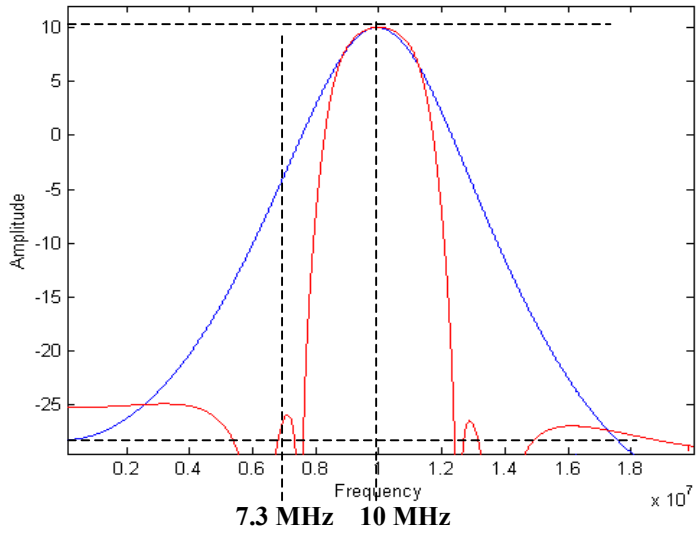

Figure 7.9 Comparison between proposed filter and conventional filter

Table 7.2 Summary of comparison results

Parameters	**Proposed Filter**	**Conventional Filter**
No. of Orders	12	12
Center Frequency	10MHz	10MHz
Bandwidth	2.5MHz	2.5MHz
Attenuation @ fc +/- 1.75MHz	10.6dB	4.32dB
Attenuation @ fc +/- 2.25MHz	27.5dB	7.25dB
Attenuation @ fc +/- 2.7MHz	36.35dB	11.7dB

Three different opamp gains (60dB, 70dB and 100dB) are employed to simulate the frequency response of the proposed filter and is illustrated in fig. 7.10. The simulation results shows opamp with 70dB gain is good enough to maintain the bandpass characteristic and attenuation. Table 7.3 summaries the proposed SC filter characteristics.

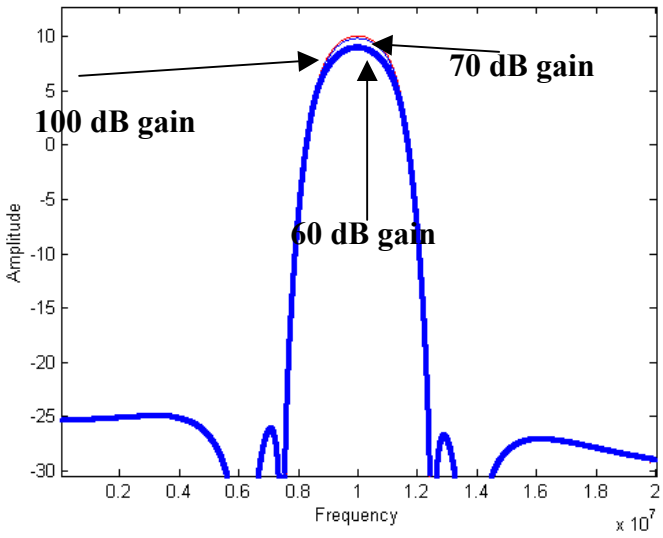

Figure 7.10 Frequency response of the proposed filter with different opamp's gain

Table 7.3 Summary of the proposed SC filter characteristics

Parameters	Simulation Results
Center Frequency	10MHz
Bandwidth	2.5MHz
Quality Factor	4
Sampling Frequency	40MHz
Passband Gain	10dB
Attenuation @ fc +/- 2.5MHz	>35dB
Filter Order	12
Maximum Capacitance Spread	5.76

The required dc gain of the opamp to maintain the transfer function of second design is much higher than the first design (44-MHz SC bandpass filter). There are two main reasons: (1) Each of the sample and hold circuit will store the gain error signal due to the opamp with a finite dc gain. (2) The highpass filter (Fig. 7.6) includes a transmission zero and poles in the transfer function. For the worse case, variation of the location of the zero and the pole are added up together. Then the transfer function will be changed more than just variation of the location of the pole.

Reference

[1] G. M. Jacobs, D. J. Allstot, R. W. Brodersen and P. R. Gray, "Design Techniques for MOS Switched Capacitor Ladder Filters", *IEEE Transactions on Circuits and Systems*, vol. 25 no.12, pp. 1014-1020, Dec. 1978.

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Chapter 8

Layout Considerations of a Wideband SC Bandpass Filter with a High Roll-Off Characteristic

In this chapter, layout consideration of the filter will be discussed. Several layout techniques are employed to minimize the non-ideal effects, including ground shield guard ring.

8.1 Post-Simulation Results and Layout Considerations of the Opamp

The specifications of the opamp are justified from the considerations in section 4.1. Table 8.1 summaries the specifications of the required opamp.

Table 8.1 Specifications of the opamp

Parameters	**Values**
Supply Voltage	2.7V
Power Consumption	10mW
Low-Frequency Gain	>80dB
Unity-Gain Frquency @ C_L=2pF	>200MHz
Phase Margin	$>60^o$
Slew rate @ C_L=2pF	0.32V/ns
Swing	+/- 1.1V

The telescopic opamp [1] with gain boosting technique is employed to implement a high low-frequency gain. A Dynamic common-mode feedback (CMFB) [2] [3] circuit is chosen to minimize the power consumption and set the operating voltage of the opamp. Figure 8.1 shows the circuit schematic of the opamp and CMFB circuit. The layout floorplan and layout of the opamp are illustrated in fig. 8.2 and 8.3 respectively.

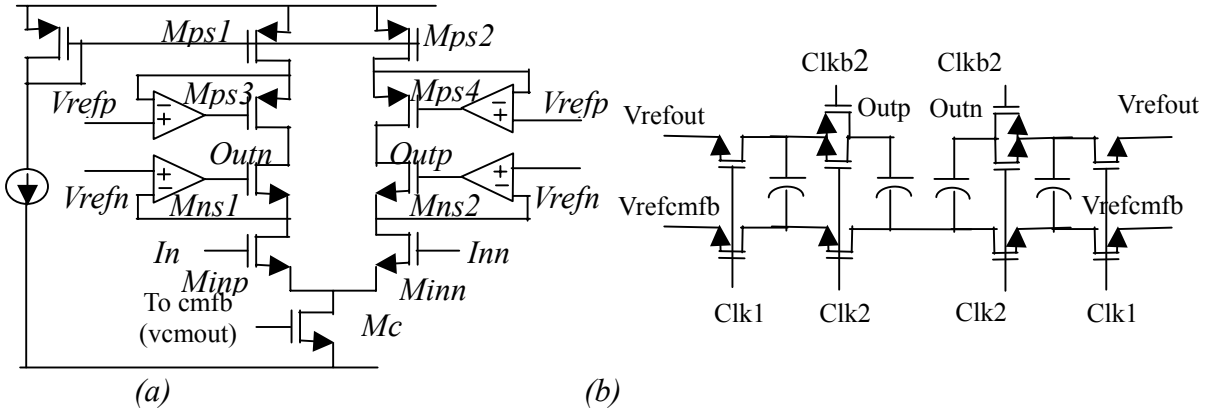

Figure 8.1 (a) Schematic of the opamp (b) Schematic of the dynamic CMFB circuit

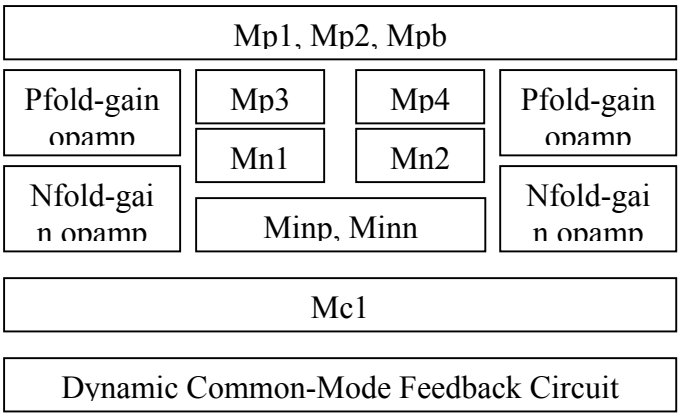

Figure 8.2 Layout floorplan of the opamp

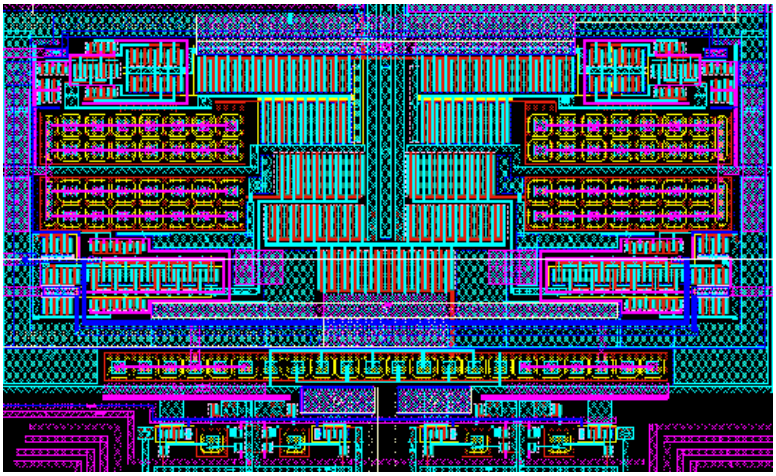

Figure 8.3 Layout of the opamp

The common-centroid symmetry [4] is employed to layout all the input pairs of the telescopic opamp and gain boosting stages. The post-simulation of the opamp is done by Hspice with a standard 0.35-um CMOS process. The simulated results show the opamp achieves 81.5dB with a unity-gain frequency of 430MHz. The frequency response of the opamp is illustrated in fig. 8.4. The other characteristics of the opamp are also simulated by Hspice and list in table 8.2.

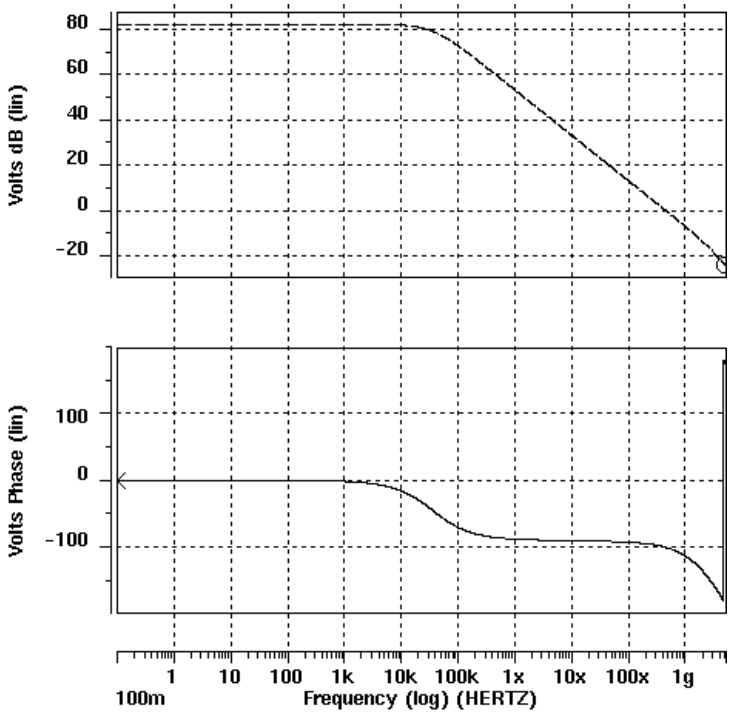

Figure 8.4 Bode plot of the opamp

Table 8.2 Summary of the characteristics of the opamp

Parameters	**Post-Simulated Results**
Supply Voltage	2.7V
Power Consumption	8.3mW
Low-Frequency Gain	81.5dB
Unity-Gain Frequency	430MHz
Phase Margin	79^{o}
Slew Rate (up)	0.412V/ns
Slew Rate (down)	0.32V/ns
Swing	+/- 1.1V

8.2 Post-Simulation Results and Layout Considerations of the Whole Filter

The layout floorplan of the whole filter is shown in fig. 8.5.

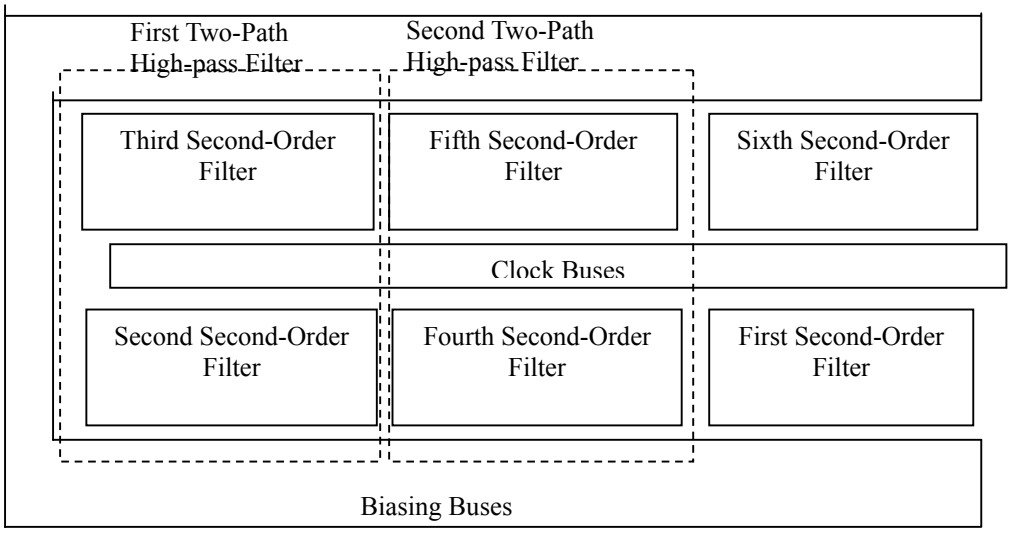

Figure 8.5 Layout floorplan of the whole filter

To minimize the cross-talk between the biasing buses and the clock buses, the clock buses are placed at the middle of the filter. The ground-shielded guard ring surrounds the opamp to minimize the injected noise to the opamp. The layout of the filter is shown in fig. 8.6.

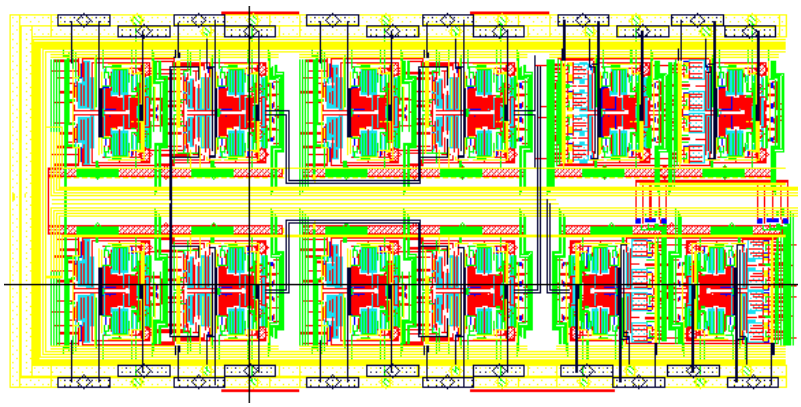

Figure 8.6 Layout of the whole filter

The system level simulation of the filter is shown in fig. 8.7 again for convenient discussion. Figure 8.8 shows the frequency spectrum of the filter with 0.1Vpp signals at 10MHz (center frequency), 8.7MHz and 11.25MHz (two 3dB corners) and eight other frequencies (that are employed to verify the attenuation).

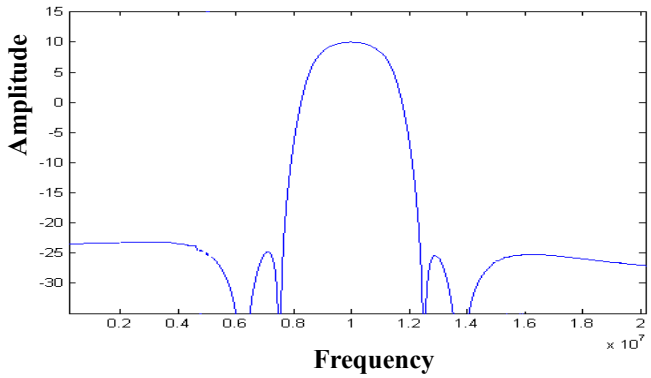

Figure 8.7 System-level simulation of the filter

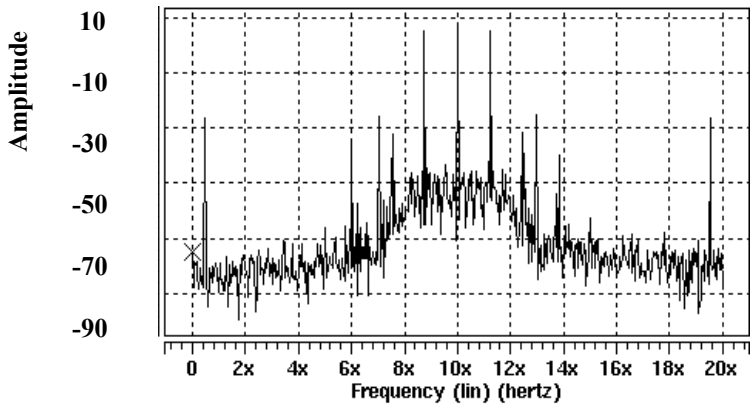

Figure 8.8 Post-simulation frequency spectrum of the filter

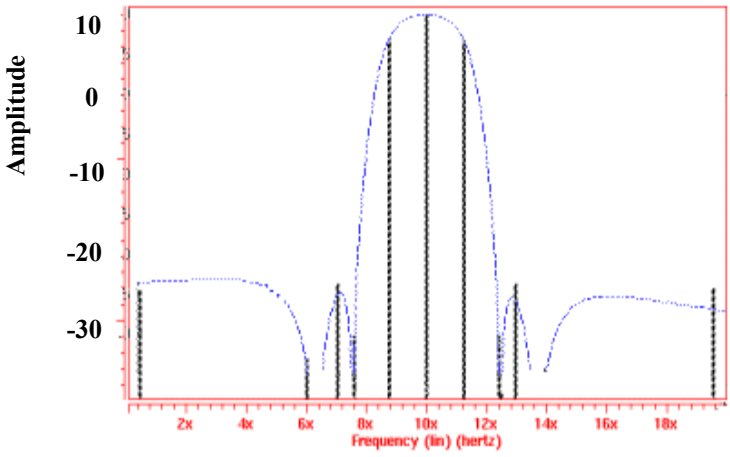

Figure 8.9 System-level simulated results vs Post-simulation results

From fig. 8.9, the post-simulation results is similar to system-level simulated results. The post-simulation shows the filter achieves the center frequency of 10MHz with a bandwidth of 2.5MHz. The attenuation at 2.5MHz away from center frequency is 34.5dB. Table 8.3 summaries the characteristic of the filter.

Table 8.3 Summary of the characteristic of the filter

Parameters	**Post-Simulation Results**
Supply Voltage	2.7V
Power Consumption	99mW
No. of Opamp	12
No. of Order	12
Center Frequency (fc)	10MHz
Bandwidth	2.5MHz
Quality Factor	4
Attenuation @ fc +/- 2.5MHz	34.5dB
Die Area	2000um X 1000um

To conclude, the proposed architecture achieves a wide-band SC bandpass filter with a high roll-off characteristic. It is still not done by pervious designs.

Reference

[10] Gulati, K. and Lee, H.-S, " A /spl plusmn/2.45 V-swing CMOS telescopic operational amplifier", *IEEE International Solid-State Circuits Conference*, Feb. 1998, p 324 -325, 456

[11] R. Castello and P. R. Gray, "A High-Performance Micropower Switched-Capacitor Filter", *IEEE Journal of Solid-State circuits*, pp. 1122 – 1132, Dec. 1985

[12] K. Suyama and Y. Tsividis, "Simulation of mixed switched-capacitor/digital networks with signal-driven switcheds." *IEEE Journal Solid-State Circuits*, vol. 25, no. 6, pp.1403-1413, Dec. 1990

[13] H. C. Luong, *Elec 504 Course Notes*, HKUST, 2000

Chapter 9

Conclusion

9.1 Conclusion

In this thesis, we demonstrate a modified doubled-sampling pseudoe-2-path second-order bandpass filter that consumes lower power and its location of poles is insensitive with the low-frequency gain of the opamp and a

novel wideband bandpass filter that has a high roll-off characteristic.

For the 44-MHz SC filter, the measurement results show the filter can operates at 44-MHz center frequency with a bandwidth of 6MHz by a sampling frequency up to176MHz. Total 18dB selectable gain is designed in the filter with each step gain of 6dB. The 6-order filter consists of 3 opamp that achieves a measured low-frequency gain of 54dB with a unity gain frequency of 600MHz and a phase margin of 50^{o}. The whole filter is realized with a standard 0.35um double polys and four metals CMOS process (TSMC). The 3% IM3 is measured with two 0.893Vpp input signals at frequencies of 43.5MHz and 44.5MHz (@ -3dB passband gain). The corresponding dynamic range is 58.3dB. The measured IIP3 is 27dBm with input two signals at 50MHz and 56MHz. The power consumption of the filter is 92.5mW and the power consumption of the three-phase generator is 24.9mW.

For the 10-MHz SC filter, the post-simulation results show the filter can operates at 10-MHz center frequency with a bandwidth of 2.5MHz and achieves a 34.5dB attenuation at +/- 2.5MHz away from 10MHz. The power consumption of the filter is 99mW to implement 12 complex poles filter. The power consumption per each

complex pole is 8.25mW.

9.2 Potential Improvement

In this project, two architectures are proposed. The first design can reduce the power consumption by 2 comparing with conventional bandpass filter. The second design can achieve high roll-off characteristic. Actually, two designs can be combined. However, five clock phases are required, two clock phases for highpass filter with a transmission zero, three clock phases for double-sampling pseudo-2-path bandpass filter. This requires a complex clock generator. The main limitation to construct a high-Q SC bandpass filter to operate at high frequency region is the requirement of the opamp. This is because, in general, a high-Q SC bandpass filter needs an opamp with a high dc-gain to maintain the transfer function.

The combined architecture is also designed for the 44-MHz bandpass filter and shown in fig. 9.1. The required orders of the combined architecture to achieve more than 40dB is 12. Comparing with the conventional architecture, it needs 28. The two two-paths highpass filters are employed to implement four transmission zeros. The two DSP2P bandpass filters are used to get enough attenuation at next two or three adjacent channels. Figure 9.2 and 9.3 show the whole view and close view of the system-level simulation results of the 44-MHz SC bandpass filter.

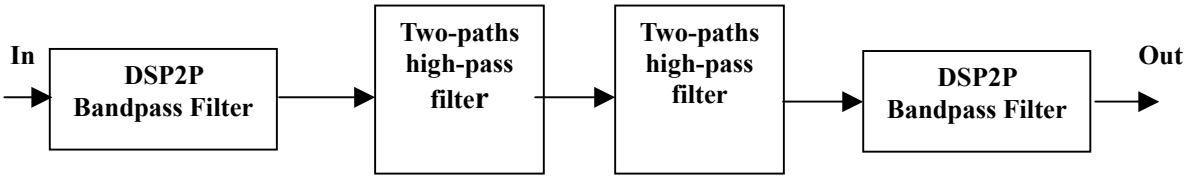

Figure 9.1 Combined architecture

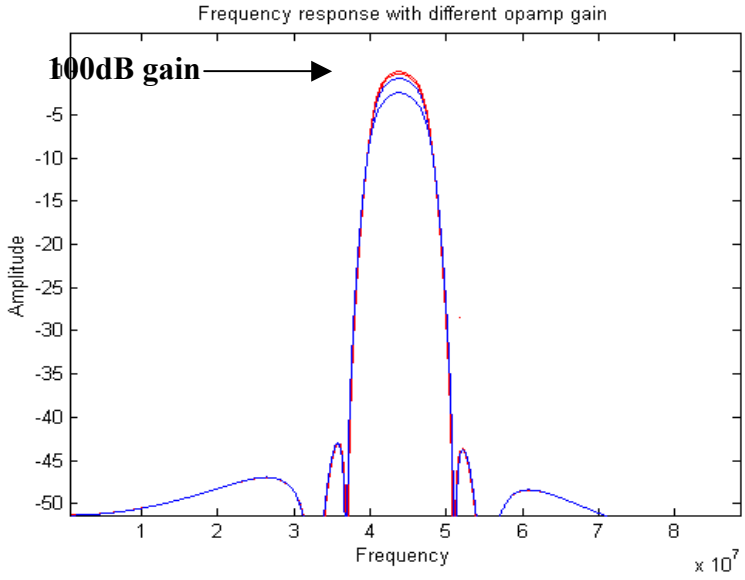

Figure 9.2 Whole view of frequency response of 44-MHz SC bandpass filter

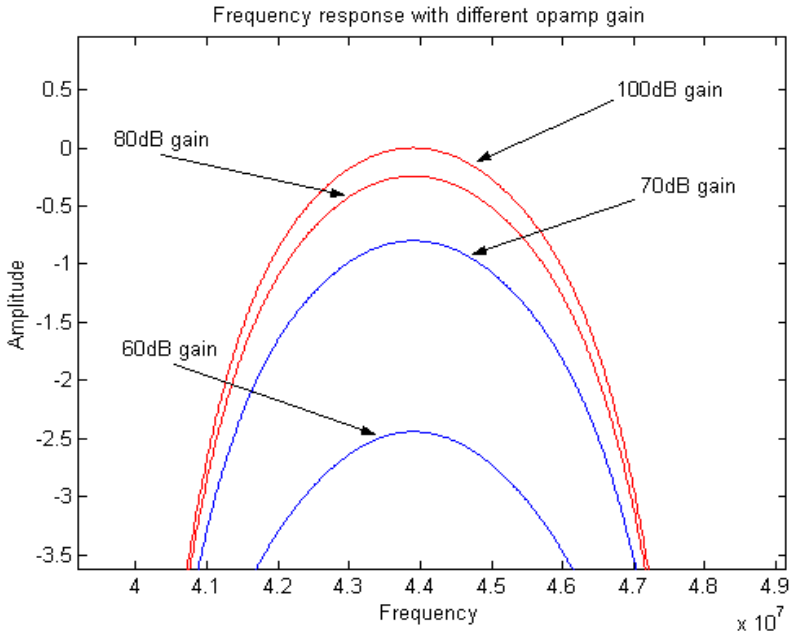

Figure 9.3 Whole view of frequency response of 44-MHz SC bandpass filter

The simulation results show an opamp with an 80dB dc gain is required. And the capacitor spread is 12. This means the slew rate of the opamp should be increased than the design opamp that is in the first filter (44-MHz SC bandpass filter).

There are several ways to improve the performance of the opamp. They are (1) Increasing the channel length of all transistors to have higher output impedance. (2) Increasing the transconductance in the input pair to increase the dc gain and unity-gain frequency. (3) Using higher supply voltage to have more voltage headroom to operate all transistors in more saturation region. (4) Using low threshold CMOS technologies.

The first two options will degrade the phase margin of the opamp. The third option will increase the power consumption in order to have same slew rate. With low threshold CMOS technologies, smaller W/L of the transistors can be used to reduce parasitic capacitors. From measurement results, the opamp achieves 56dB dc gain with a phase margin of 50^{o}. From the above consideration, the last two options are most workable solution.

Appendix A

Orders of Bandpass Filter Consideration

In this appendix, design approach for the bandpass filter is discussed. First of all, the required orders are determined by the analysis of butterworth filter. After that, hand calculation is employed to verify the exactly orders for the designed bandpass filter to get the enough roll-off.

A.1 Relationship between attenuation and number of orders

A bandpass filter can be formed by a lowpass filter [1]. Figure A.1 shows the relationship between the ratios of frequency in a lowpass and the ratios of bandwidth in a bandpass filter.

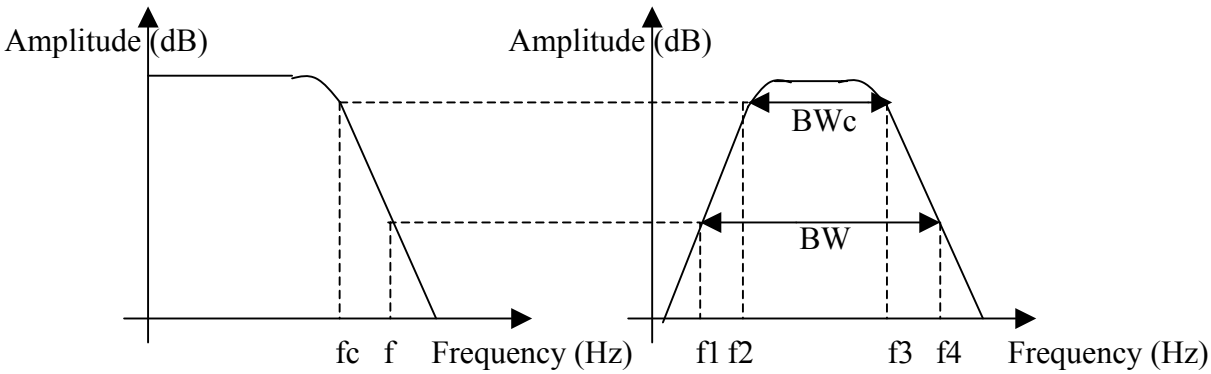

Figure A.1 Ratios of frequency in a lowpass filter and ratios of bandwidths in a bandpass

The orders of bandpass filter can be determined by the ratios of bandwidths between interested BW and cut-off bandwidth BWc (as opposed to the ratios f/fc). The

relationship between the attenuation and orders in a Butterworth lowpass filter is given by equation A.1:

$$\text{Attenuation at } \omega: \quad A_{dB}(\omega) = 10\log[1 + (\frac{\omega}{\omega_C})^n] \qquad (A.1)$$

where n is orders

For example, 50dB attenuation at f1 and f4 is required. The BW = f1 – f4 = 2BWc

Then attenuation at f respect fc in lowpass filter is 50dB. By equation A.1,

$50 = 10 \log[1 + (2)^n]$

$n \cong 16.6$

Therefore minimum orders for a bandpass filter to achieve 50dB attenuation at 2BWc is 34.

A.2 Orders for Designed 44-MHz SC Bandpass Filter

According to the considerations in section A.1, the orders for bandpass filter to achieve SAW's specification is 34. This means that at least cascading 17 stages of a second-order bandpass filter is needed to have this attenuation. This will consume much power. Moreover, the aim of this project is to demonstrate the possibility of operating a SC filter at this high frequency region. Therefore, the attenuation at 6MHz away form the center frequency is set to be –9dBc. The specification of the 44-MHz SC bandpass filter and the SAW filter are summarized in table A.1 again for easy discussion.

Table A.1 Summary of specification of the 44-MHz SC Bandpass Filter

Parameters	**Specifications of this project**	**Specification of the SAW**
Passband Gain	0dB	0dB
Center Frequency (Fc)	44MHz	44MHz
Bandwidth	6MHz	6MHz
Attenuation @ Fc +/- 6MHz	-9dBc	-50dBc

According to the considerations of section A.1, a sixth-order bandpass filter is needed to obtain more than -9dB attenuation at 38MHz or 50MHz. In general, cascading m stages of second-order bandpass filters, the relationship between the quality factor of each stage and the quality factor of the whole filter is shown in equation A.2.

$$Q_{stage} = Q_{whole\_filter} \times \sqrt{2^{1/m} - 1} \qquad \text{(A.2)}$$

As explain in section 2.5, the locations of the poles in the bandpass filter are set to 1/4 sampling frequency in this project. By employing equation 2.9, 2.10 and 2.11 (that are given again in equation A.3, A.4 and A.5), all the capacitors in the whole filter can be found. The schematic of the second-order bandpass filter and the resulted Z-domain equation are shown in fig. A1 and equation A.6 respectively.

$$\frac{C_1 C_4}{C_A C_B} = \frac{X_O}{2Q} \frac{4}{X_O^2 + X_O/Q + 1} \qquad \text{(A.3)}$$

$$\frac{C_1 C_3}{C_A C_B} = \frac{X_O}{2Q} \frac{4}{X_O^2 + X_O/Q + 1} \qquad \text{(A.4)}$$

$$\frac{C_1 C_2}{C_A C_B} = \frac{4}{X_O^2 + X_O/Q + 1} \qquad \text{(A.5)}$$

where X_O equals to $2/\Omega_a T_s$, Ω_a equals to $(2/T)\tan(\Omega_d T_s/2)$ and T_s is the sampling period

$$|H(e^{j\omega T_s})| = \frac{\frac{C_1C_4}{C_AC_B}}{\sqrt{[1+(1-\frac{C_1C_3}{C_AC_B})(2\cos^2(\omega T_s)-1)]^2 + 4\sin^2(\omega T_s)\cos^2(\omega T_s)(1-\frac{C_1C_3}{C_AC_B})^2}} \quad \text{(A.7)}$$

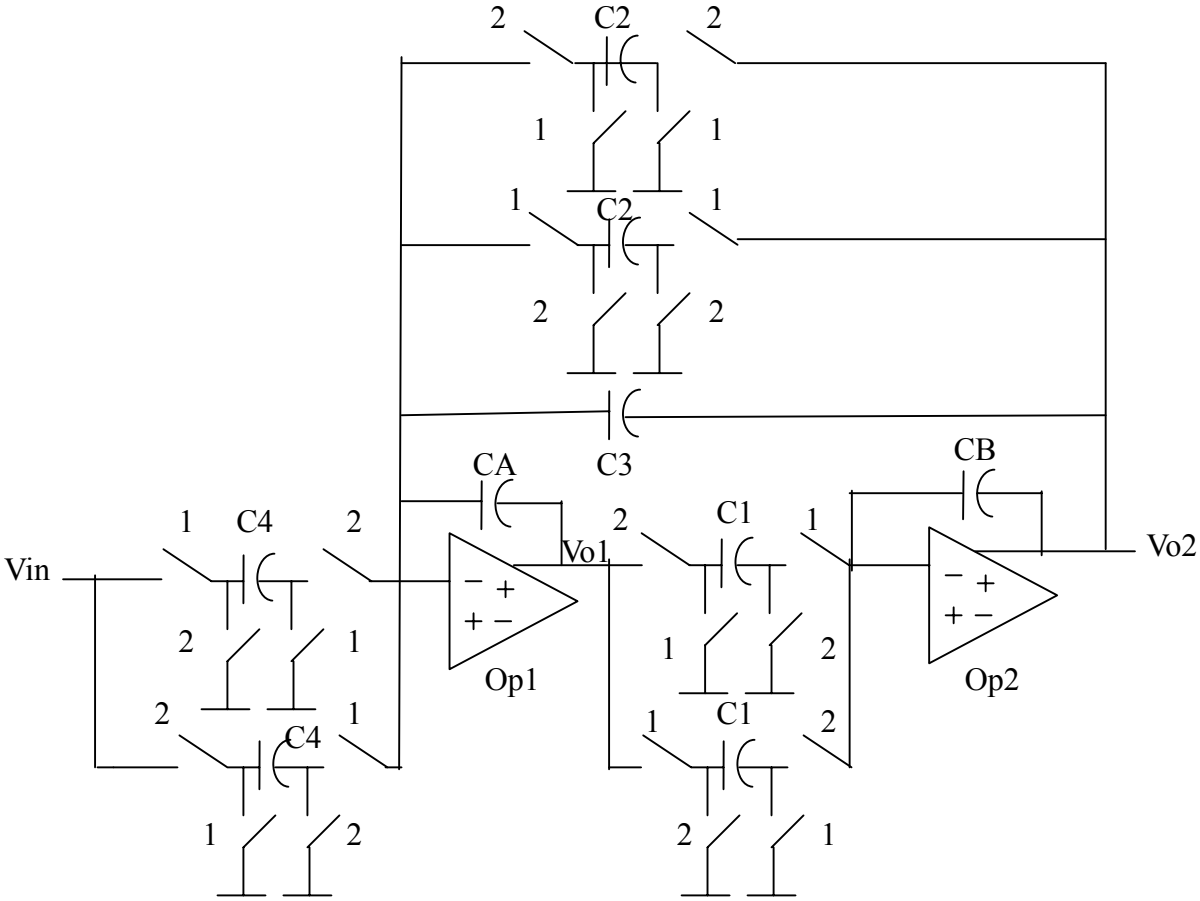

Figure A.2 Schematic of a second-order bandpass filter

$$H(Z) = \frac{V_{O2}(Z)}{V_{in}(Z)} = -\frac{\frac{C_1C_4}{C_AC_B}Z^{-1}}{1+(1-\frac{C_1C_3}{C_AC_B})Z^{-2}} \quad \text{(A.6)}$$

By putting $Z = e^{j\omega T}$ in equation A.6 and calculating the magnitude of the transfer function, equation A.7 is derived. By employing equation A.7, attenuation at any locations of different orders of bandpass filters can be found out. Table A.2 summarizes the performance of a sixth-order banpass filter.

TableA.2 Summary the performance of sixth-order bandpass filter

Parameters	Sixth-order bandpass filter
Q of each stage	3.74
Q of whole filter	7.33
Attenuation at 38MHz of each stage	-3.03dB
Attenuation at 38MHz of whole filter	-9.1dB
C1	0.343
C2	4.83
C3	1
C4	1
CA	1
CB	1

The calculation results point out that sixth-order bandpass filter is good enough to achieve the attenuation requirement.

Reference

[1] Sundaram Natarajan, “Theory and Design of Linear Active Networks”, *McGraw-Hill Book Company*, 1989.