1-V Switched-Capacitor Pseudo-2-Path Filter

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Abstract

Demand for low-power low-voltage integrated circuits (ICs) has rapidly grown due to the increasing importance of portable equipment in all market segments including telecommunications, computers, and consumer electronics. The need for low-voltage ICs is also motivated by the new submicron CMOS technology scaling that requires all transistor's gate-to-source (V_{GS}) voltage to operate in less than 1.5V in the year 2001 and 0.9V in 2009, as predicted by the Semiconductor Industry Association. In recent years, a lot of researches were done on designing switched-capacitor (SC) filters for low supply voltages. The primary reason is that SC filters achieve high filter accuracy with low distortion. SC filters that can operate with a single 1-V supply in standard CMOS process have been designed using the switched-opamp technique without any clock voltage multiplier or low-threshold devices. However, this switched-opamp (SO) technique requires the opamps to turn off after their integrating phases and thus cannot be applied to realize a SC pseudo-N-path filter.

In this project, a modified switched-opamp technique has been proposed to realize a fully-differential 1-V SC pseudo-2-path filter in HP 0.5um CMOS process with V_{Tp} = 0.86V and V_{Tn} = 0.7V. A fully-differential two-output-pair switchable opamp is designed to achieve a low-frequency gain of 69dB to preserve the filter transfer function accuracy. With the use of SC dynamic level shifters, an output signal swing of 1.4-V_{pp} can be achieved even with a single 1-V supply. The filter implements a bandpass response with center frequency of 75kHz and bandwidth of 1.7kHz (Q=45) with a sampling frequency of 300kHz. It consumes a power of about 310μW and occupies a chip area of 800μmx1000μm.

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I would like to take this opportunity to express my gratitude to many people who have been continuously supporting me throughout the two years master program in the HKUST. Their supports and advice helped me get through a lot of problems during the research.

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Preface

There have been increasing interests on the inventions and improvements of Micro-ElectroMechanical Systems (MEMS) since 1970s. MENS devices are small in size and low cost. It also allows high degree of design flexibility compared with conventional systems that consists of mechanical parts. The advantages of putting gyroscope in micro scale are obvious, since conventional gyroscopes are large in size, easily wear out after several thousand hours of operation and very expensive. In this project, we have explored the design and fabrication issues on making vibrating piezoelectric microgyroscope on silicon crystal, which is explored in Chapter 1 of this thesis. The preparation and poling method of the piezoelectric material - PZT (Lead Zicronate Titanate) is covered. The operation of the microgyroscope and its testing results are presented. Some critical fabrication steps of the piezoelectric microgyroscope will be discussed while the complete fabrication process is attached in the appendix for your reference.

Based on the performance of the microgyroscope, a 1-V switched-capacitor (SC) pseudo-2-path bandpass filter is designed and implemented. The filter will be applied in the lock-in amplifier, which is used as the signal conditioning circuitry for improving the signal-to-noise-ratio (SNR) of the microgyroscope. The principle of the lock-in amplifier is introduced in Chapter 2, where different ways of implementing narrowband bandpass filters are discussed.

The details in the synthesis of a classical SC pseudo-2-path filter are covered in Chapter 3. Techniques like Z to –Z transformation and RAM-type path cells are discussed in details.

In Chapter 4, the considerations and limitations of operating SC circuits at low supply voltage are explored. The shortcomings of the conventional switched-opamp techniques are

pointed out and a modified switched-opamp technique is proposed. The proposed switched-opamp technique is verified and illustrated through the design and implementation of a 1-V SC pseudo-2-path filter. A fully-differential two-output-pair switchable opamp is introduced the first time in literature. For improving the output dynamic range, SC dynamic level shifters are applied. The performances of the filter are verified by SWITCAP2 simulations.

The transistor level implementation of the 1-V SC pseudo-2-path filter in standard CMOS process is presented in Chapter 5. A 1-V fully-differential two-output-pair switchable opamp is designed in HP 0.5μm CMOS process to achieve a low-frequency gain of 80dB with a unity-gain frequency and phase margin of 7.5MHz and 54° respectively. A dynamic common-mode feedback (CMFB) circuit is designed to operate with 1-V switchable opamp. Unlike continuous time CMFB circuit, the dynamic CMFB circuit does not reduce the output dynamic range of the opamp. An on-chip voltage buffer is designed for driving capacitance from external pads and measuring equipment. The HSPICE simulations results of the building blocks and the 1-V SC pseudo-2-path filter are presented.

The layouts and post-simulations results of the building blocks and the filter are discussed and summarized in Chapter 6. The testing results and methodologies are covered in great details in Chapter 7. Testing results show proper operation of the 1-V SC pseudo-2-path filter, from which the proposed modified switched-opamp technique is verified. A conclusion is drawn at the end of this thesis to explore the potential applications of the proposed switched-opamp technique as well as its limitations and ways of improvements.

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Chapter 1

Design and Fabrication of Piezoelectric Microgyroscope

The lack of input and output transducers with a performance/price ratio comparable to that of standard integrated circuits has motivated a lot of researchers on the inventions and improvements of many creative Micro-electromechanical-systems (MEMS) over the past 20 years. MEMS devices are small in size and low cost. It also allows high degree of design flexibility compared with conventional systems that consist of mechanical parts. With the evolutions of fabrication materials and novel architectures, many useful MEMS devices, like microgyroscopes, accelerometers, gas sensors and so on, have been put in production lines in industries for different applications.

Being angular rate sensors, microgyroscopes have received a lot of attentions due to its wide range of applications in military (e.g. missile control and auto-pilot systems), automotive industry (e.g. crash sensors and vehicle navigation) and low-end consumer markets (e.g. video-camera image stabilization, virtual reality and intelligent toys). In order to boost the MEMS devices performance and further reduce the cost of most miniature information processing systems, a lot of efforts have been put on integrating MEMS devices with on-chip

signal-conditioning circuitry in recent years. In view of this, a novel piezoelectric microgyroscope is designed and fabricated on silicon [1]. Its operation principle is given, and the theory is confirmed by experimental results.

1.1 Poling Piezoelectric Materials

Piezoelectricity is a property of certain classes of crystalline materials. When mechanical pressure is applied to one of these materials, the crystalline structure produces a voltage proportional to the pressure, this is referred as the "direct piezoelectric effect" (Fig. 1.1(a)). In the reverse, when an electric field is applied to one of these materials, the crystalline structure changes shape, producing dimensional changes in the material, this is known as the "reciprocal piezoelectric effect" (Fig. 1.1(b)).

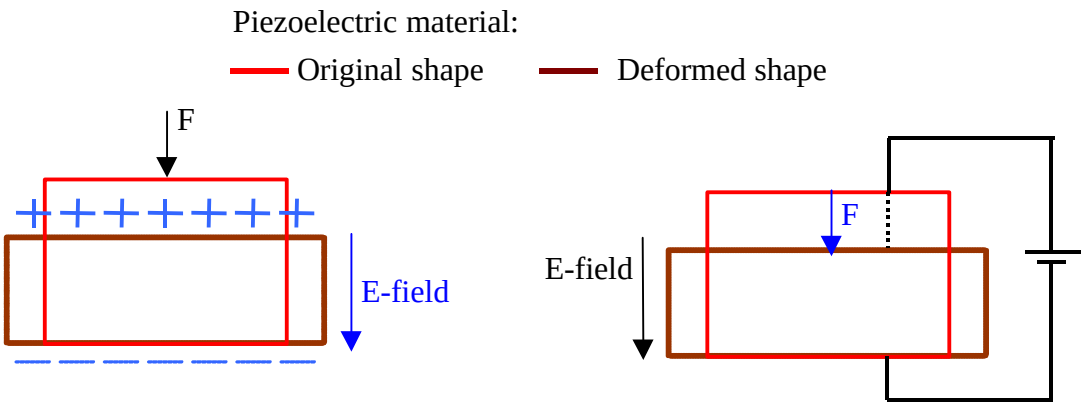


Fig. 1.1 (a) Direct piezoelectric effect (b) Reciprocal piezoelectric effect

However, newly prepared piezoelectric materials have random responses toward an applied pressure or electric field, and thus they are usually accomplished with a poling step to precisely orient the mechanical and electrical axes to response to the applied pressure and electric field respectively. This is similar as poling the North and South poles on a magnet. The orientation of a d.c. poling field determines the orientation of the mechanical and electrical axes. At suitable temperature (depends on materials), when a d.c. voltage is applied to the two sides of a piezoelectric material along the x-axis as shown in Fig. 1.2, the dimension between these poling electrodes increases (x-direction), and the dimension parallel to the electrodes decreases (y-direction). This poling process permanently changes the dimensions of a piezoelectric material, even when the poling voltage is removed. By so doing, the orientation of the mechanical and electrical axes is set.

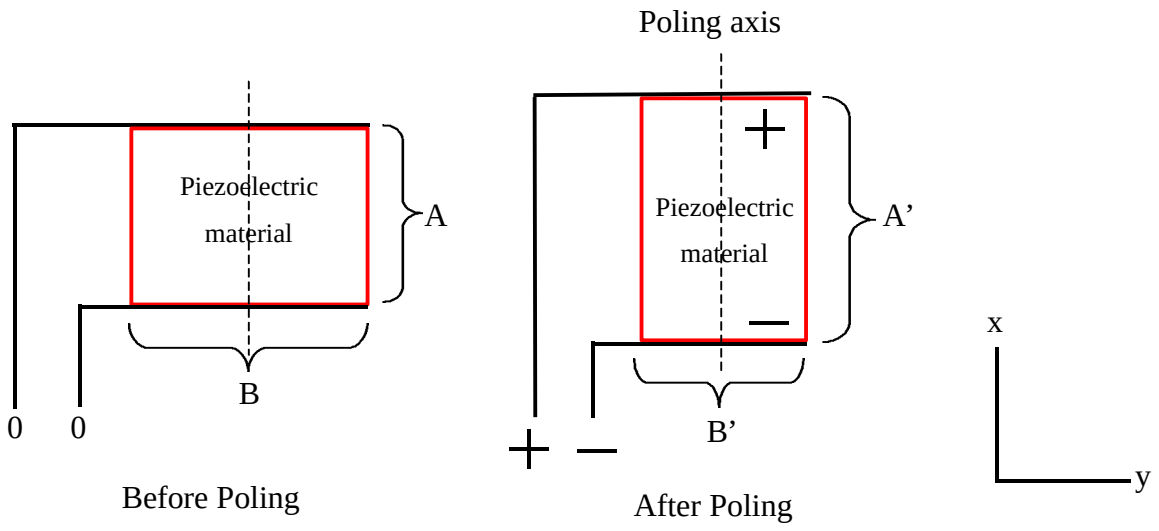


Fig. 1.2 Effects of poling

1.2 Direct Piezoelectric Effect

After the poling process is complete, at room temperature, any voltage that is lower than the poling voltage changes the dimensions of the poled piezoelectric material, as long as the voltage is applied. This is referred as the “direct piezoelectric effect”. A voltage with the same polarity as (but lower than) the poling voltage causes additional expansion along the poling axis (x-axis, Fig. 1.3) and contraction in the y-axis. Meanwhile, a voltage with the opposite polarity as the poling voltage induces contraction along the poling axis (x-axis) and expansion in y-axis. In both cases, the poled piezoelectric material returns to its poled dimensions when the voltage is removed from the electrodes. The effects are shown greatly exaggerated in Fig. 1.3 below.

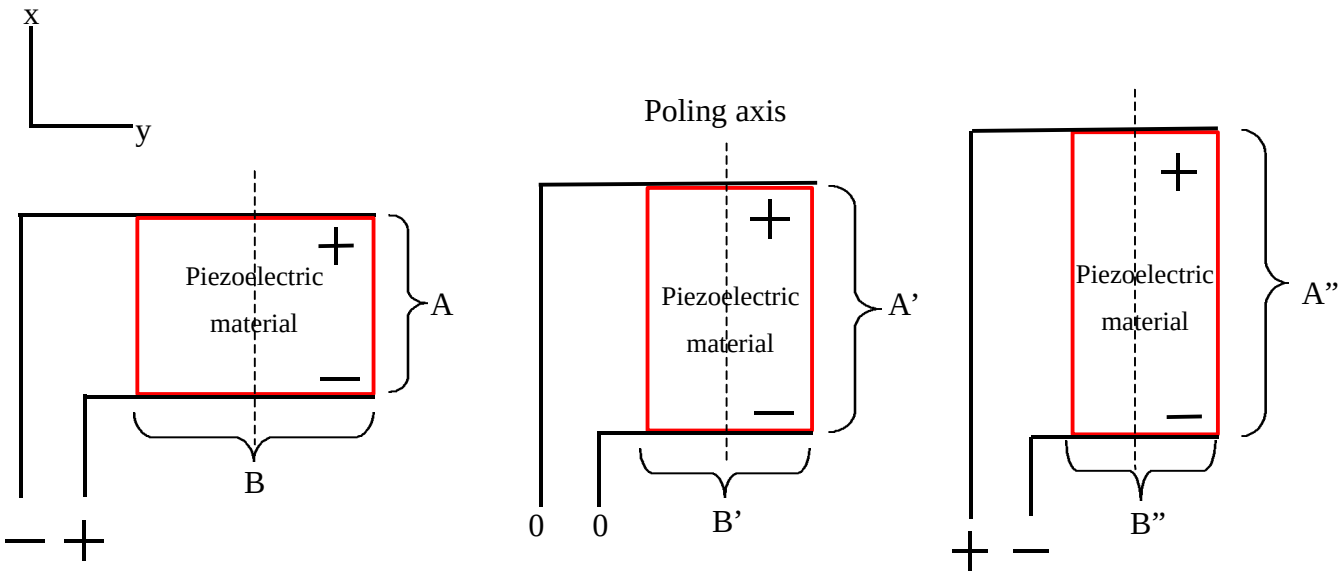


Fig. 1.3 Direct piezoelectric effect

1.3 Reciprocal Piezoelectric Effect

Conversely, a voltage is generated when a compressive and tensile force is applied to the poled piezoelectric substance. This phenomenon is referred as the "reciprocal piezoelectric effect". A voltage with the same polarity as the poling voltage is obtained either from an applied compressive force along the poling axis (x-axis, Fig. 1.4), or from an applied tensile force in the y-axis. On the other hand, a voltage with the opposite polarity is generated either from an applied tensile force along the poling axis (x-axis), or from an applied compressive force in the y-axis.

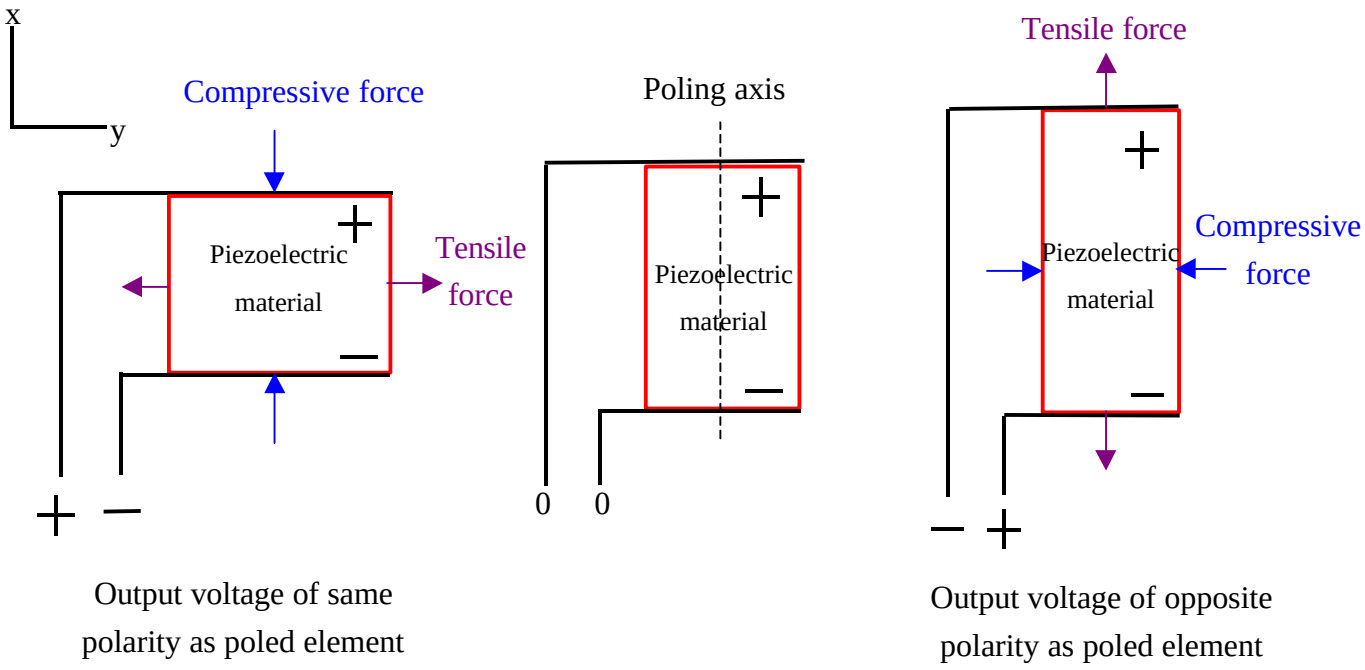


Fig. 1.4 Reciprocal piezoelectric effect

1.4 PZT Solution Preparation

A suitable piezoelectric material for fabricating microgyroscope should possess with large piezoelectric constant and electromechanical coupling factors. Meanwhile, the solution preparation method should be some common and easily handled ones. The Lead Zicronate Titanate (PZT) shows large piezoelectric constant and electromechanical coupling factors [2][3][4], and the fact that thin film PZT can be coated with sol-gel processing method or sputtered on silicon wafer [2][3], thus making it the piezoelectric material choice for the microgyroscope. Among the methods of fabricating PZT films, sol-gel processing is believed to have considerable advantages over the sputtering method, these include easier fabrication of large areas thick film, better control of PZT film composition and lower cost. Figure 1.5 outlines the flow diagram for preparing PZT solution with lead acetate trihydrate as the lead source [2][3][5][6][7].

Acetic acid is added in a beaker of lead acetate tribydrate inside a fume-cupboard. The solution is heated at 100°C until all lead acetate trihydrate is dissolved. Afterwards, the solution is put inside a dry-box for the addition of zirconium propoxide and titanium isopropoxide. This is because toxic gases are given out during the mixing of zirconium propoxide and titanium isopropoxide with the dissolved lead acetate trihydrate to form the precursor solution. Latic acid and distilled water are used as solvents, while glycerol and ethylene glycol are used as

additives to prevent cracking and to improve the surface smoothness of the films. The solution is then stored for several days to make sure that it is well stable for use. Precipitate is seen if the solution is not prepared well.

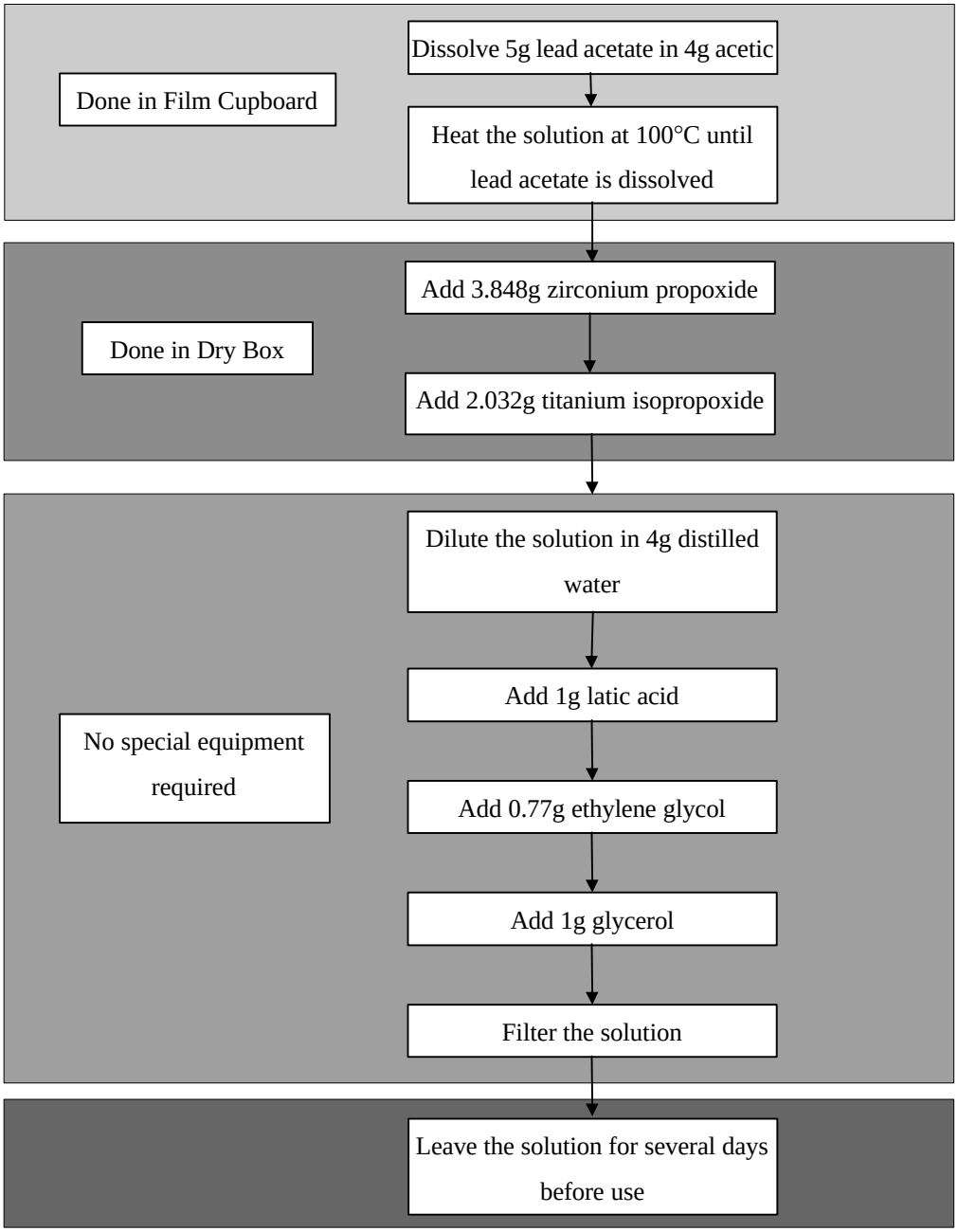


Fig. 1.5 Flowchart of PZT solution preparation

1.5 Critical Fabrication Steps of Microgyroscope

Figure 1.6 shows some critical fabrication steps of the micro-gyroscope. (Detail fabrication steps are shown in Appendix A).

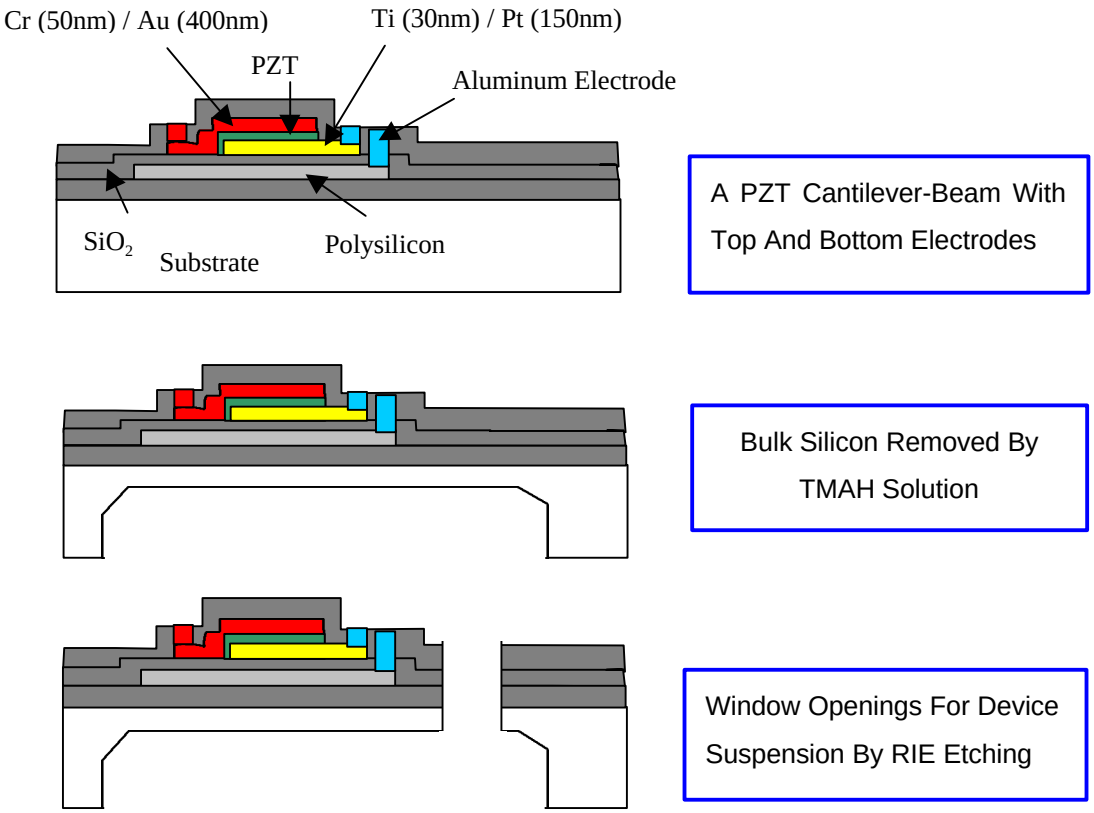


Fig. 1.6 Critical fabrication steps of piezoelectric microgyroscope

The fabrication of the microgyroscope starts with a double-side polished <100> p-type silicon wafer. A polysilicon layer is deposited to act as a mechanical ground plane for the microgyroscope. Titanium (Ti) and platinum (Pt) are sputtered on silicon dioxide to form a Pt/Ti/SiO2/Si substrate for better orientation [8][9][10][11] of the PZT thin film that is coated on top of it in next step. The titanium/platinum layer also acts as the bottom electrode to connect

with the PZT layer. A thin PZT layer is coated using sol-gel method. The PZT solution is spin-coated on titanium/platinum (Ti/Pt) electrode with a spin rate of 6000rpm and firing at 350°C for 20 seconds [7][12]. Annealing is carried out at 700°C for 3 hours [7][12] to reduce stress and cracking of the PZT layer. Chromium/silver is sputtered onto the PZT layer to act as the top electrode. The whole structure is covered with silicon dioxide and then undergoes bulk silicon etch from the backside such that the silicon underneath the structure is removed. Lastly, RIE etching of silicon is done to open up some windows such that the sensor is suspended.

1.6 Design and Operation of Microgyroscope

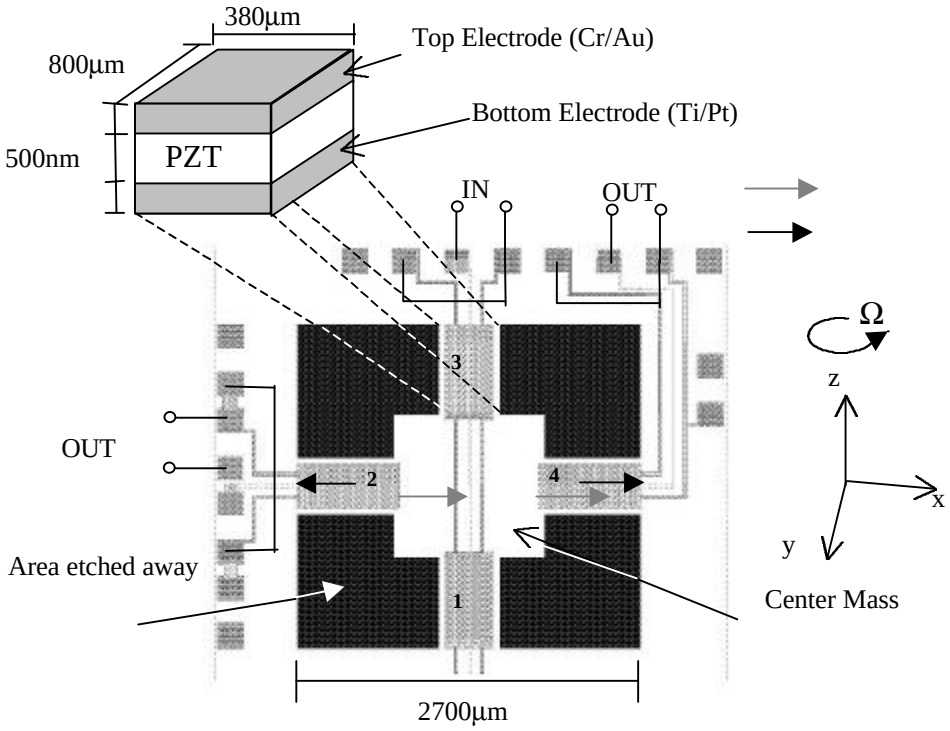


Fig. 1.7 Top view of the 4-sensor-beams microgyroscope. F1 is the force due to center mass vibration (upward direction); F2 is the Coriolis force

The top view of the piezoelectric microgyroscope is shown in Fig. 1.7 above. The die photo is shown in Fig. 1.8.

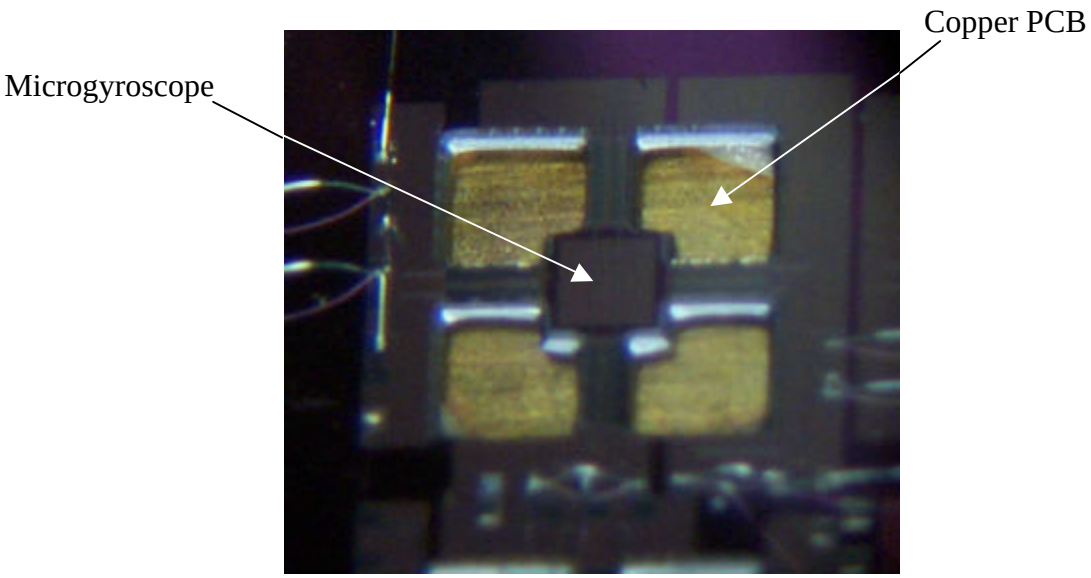


Fig. 1.8 Die photo of the 4-sensor-beam piezoelectric microgyroscope

There are four sensor beams (labeled 1-4) in this design. Each sensor beam has a layer of piezoelectric material (PZT) and the top and bottom electrodes with dimension of 380 μm x 800 μm each.

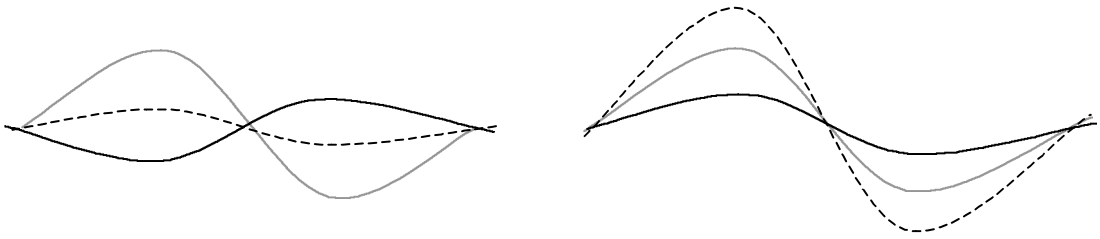
Due to the direct piezoelectric effect, when an AC input signal is applied to the "IN" terminal, the sensor beams 1 and 3 are made to compress and expand at a frequency equal to that of the input signal. This sets the central structure and the sensor beams to vibrate up and down at a frequency equal to the applied input frequency. Suppose the micro-gyroscope is put parallel to the xz-plane and the micro-gyroscope is rotated around z-axis as indicated in Fig. 1.7. Then the piezoelectric particles in beams 2 and 4 experience a moving velocity *V* in the y-

direction. The cross product of this moving velocity and the applied rotation rate Ω (z-direction) creates a Coriolis force [2] in the x-direction given by Equation 1.1:

$$\vec{F}_c = 2m\vec{V} \times \Omega \qquad \text{(Eq. 1.1)}$$

where *m* is the mass of the central structure. This Coriolis force can be treated as shear stresses, which act on the xz-plane of the piezoelectric plates in beams 2 and 4 in the x-direction and produce an electric field in the y-direction. As a result, a voltage is induced in the y-direction across the two electrodes formed at the top and bottom of the piezoelectric plate. Since the output signal is a consequence of the Coriolis force, its frequency is exactly the same as the vibration rate of the center mass, and hence exactly equal to that of the applied input frequency.

The two output-beams 2 and 4 give out differential responses for an applied rotation. Suppose the center mass is vibrating up such that beams 2 and 4 are in contraction mode. At this moment, both beams 2 and 4 experience a moving velocity V in the y-direction. By the above formula, the Coriolis force generated in beam 2 is in the positive x-direction while that generated in beam 4 is in the negative x-direction. The output signal components at the two beams are illustrated in Fig. 1.9. Since the output signal due to vibration at beam 2 is out of phase with the output component due to the center mass vibration, the net output amplitude at beam 2 decreases with rotation rate. Similarly, the net output amplitude at beam 4 increases with rotation rate.



Net output signal obtained at beam 2 Net output signal obtained at beam 4

Fig. 1.9 Output signal components at beams 2 and 4 of microgyroscope

Signal due to center mass vibration

Signal due to Coriolis force

Net output signal

1.7 Testing Procedures and Results

The testing procedure is summarized as follows:

1. The piezoelectric film is measured to have a thickness of about 1μm. It is therefore activated by poling it at the following conditions: 200°C, 1 hour with a DC bias of 0.3V across the top to bottom electrodes of all the piezoelectric plates (sensor beams 1-4). The DC poling voltage is determined by the critical E-field that the PZT layer can sustain. Typical critical E-field for PZT crystal is about100V/cm [2][4][13].

2. The resonant frequency of the microgyroscope is measured by plotting the output signals (without rotation) at various input signal frequencies.

3. The microgyroscope is put on a rotational table. An AC input signal of $0.3V_{pp}$ is applied to actuate the central structure of the gyroscope for vibration. Sensitivity of the microgyroscope is measured by obtaining differential output signal (beam 2's output - beam 4's output) amplitudes versus rotation speeds. Because the change in the output voltage is

comparable to the noise floor, a lock-in amplifier is employed to obtain the signal. The test setup is shown in Fig. 1.10.

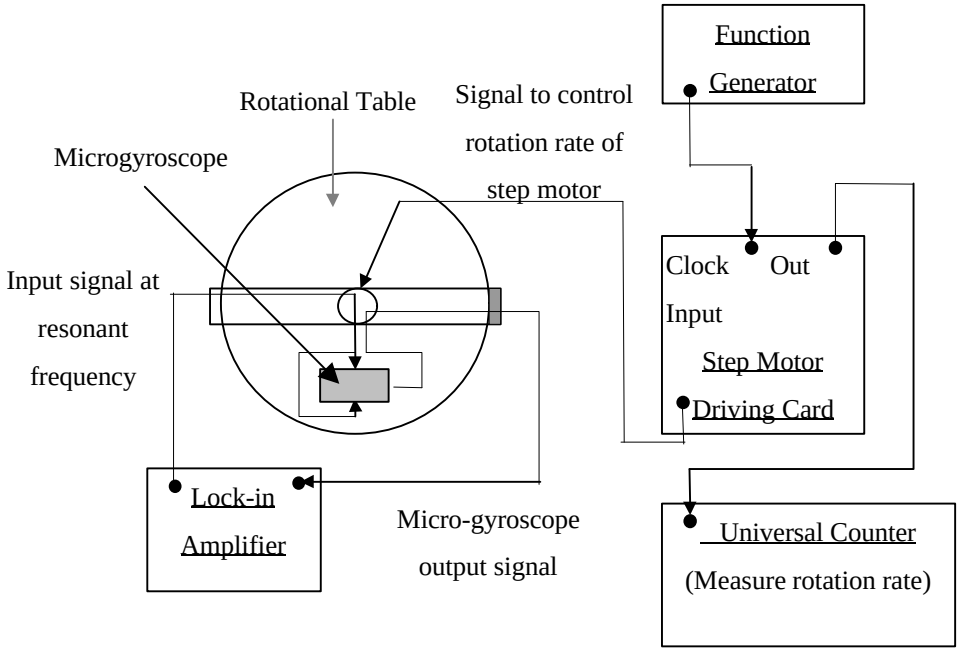


Fig. 1.10 Experimental setup for measuring sensitivity of gyroscope

Figure 1.11 shows the measured frequency response of the micro-gyroscope, from which the resonant frequency is obtained to be 73.84kHz.

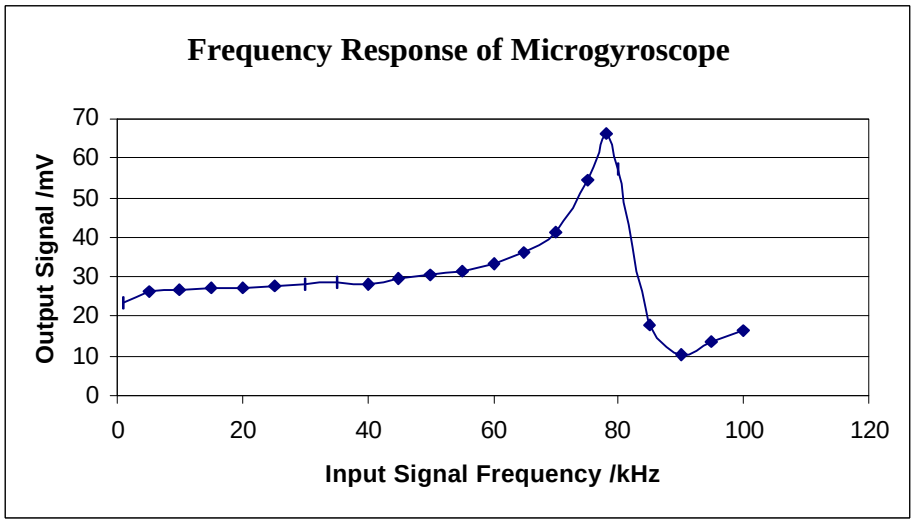


Fig. 1.11 Differential output response (measured at no rotation) at various input frequencies

Measured differential output signals (output on beam 2 – output of beam 4) that response to different rotation rates show a sensitivity of -30.8μV/V/(°/sec) at the resonant frequency (Fig. 1.12). The linear range is around 150°/sec. As predicted, the decrease in output signal with increasing rotation speed is observed.

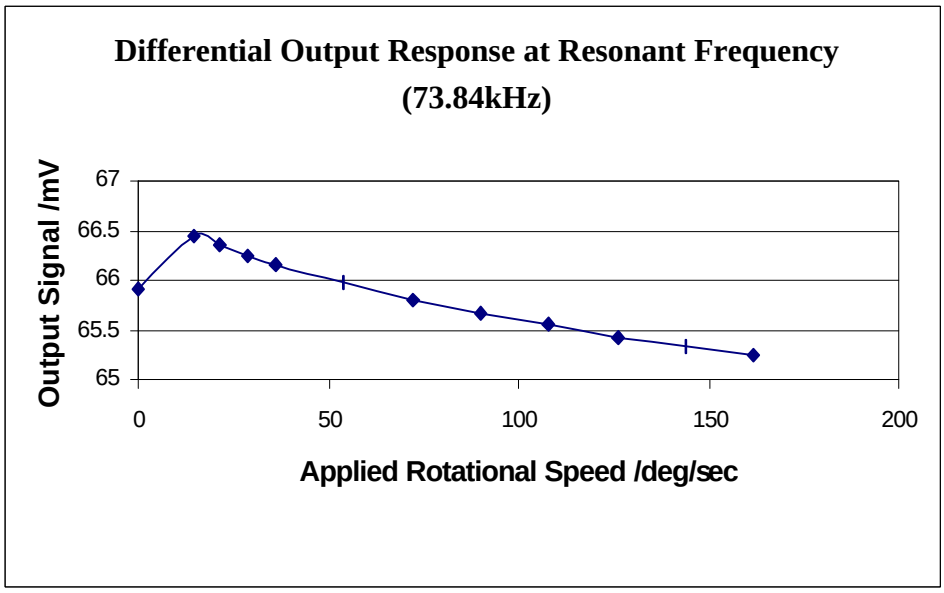


Fig. 1.12 Differential output responses of microgyroscope operating at resonant frequency

A novel vibrating micro-gyroscope is designed and fabricated on silicon crystal. It is based on the thickness-extension vibration mode of the piezoelectric material and does not use any elastic element. Lead acetate trihydrate is used as the lead source for the preparation of the piezoelectric (PZT) solution. High quality PZT thin film is deposited by sol-gel technique on Pt/Ti/SiO2/Si substrate. Due to direct piezoelectric effect, the micro-gyroscope can be driven in a resonant state with a single $0.3V_{pp}$ AC source, hence it is suitable for low voltage portable

applications. The output is detected by the reciprocal piezoelectric effect and is linearly proportional to the rotational speed. Its operation principle is given, and the theory is confirmed by experimental results. Measured sensitivity of this micro-gyroscope is -30.8μV/V/(°/sec) with a measurement range of 150°/sec at a resonant frequency of 73.84kHz. The total area of the micro-gyroscope is 2.7mm x 2.7mm.

Reference

[1] S. L. Cheung, W. Ma, H. Luong and S. W. Lee, "Design and Performance of a Piezoelectric Microgyroscope", *Proceedings of Transducers 99' - The Tenth International Conference on Solid-State Sensors and Actuators*, Vol. 2, June 1999, pp.977-980.

[2] C. M. Hui, *Integrated Micromechanical Gyroscope*, MPhil Thesis of the Department of EEE, HKUST, 1996.

[3] M. S. Wong, *Design, Analysis and Materials Preparation for Microgyroscope*, MPhil Thesis of the Department of EEE, HKUST, 1996.

[4] K. F. Etzoid, R. A. Roy, K. L. Saenger, J. J. Cuomo, "Electromechanical Conversion Efficiency of PZT Films", P*roceeding of the Ultrasonics Symposium*, Vol. 1, 1990, pp.747-751

[5] B.A. Tuttle, J. A. Voigt, T. J. Garino, D. C. Goodnow, R. W. Schwartz, D. I. Lamppa, T. J. Headley and M. O. Eatough, "Chemically Prepared Pb(Zr,Ti)O_3 Thin Films: The Effects of Orientation and Stress", *Proceedings of the Eighth IEEE International Symposium on Applications of Ferroelectrics*, 1992, pp.344-8.

[6] J. C. Cunter, S. K. Streiffer and A. I. Kingon, "Low temperature preparation of sol-gel PZT thin films for pyroelectric and other integrated devices", *Proceedings of the Tenth International Symposium on Applications of Ferroelectrics*, Vol.1, 1996, pp.223-6

[7] M. Hendrickson, T. Su, S. T. McKinstry, B. J. Rod and R. J. Zeto, "Processing of PZT Piezoelectric Thin Films for Microelectromechanical Systems", *Proceedings of the Tenth IEEE International Symposium on Applications of Ferroelectrics*, Vol.2, 1996, pp.683-6

[8] E. A. Kneer, D. P. Birnie III, G. Teowee and J. C. Podlesny, "Effects of Sol-Gel PZT Film Thickness and Electrode Structure on the Electrical Behavior of Pt/PZT/Pt Capacitors", *Proceedings of the Ninth IEEE International Symposium on Applications of Ferroelectrics*, 1994, pp.446-9

[9] Kashyap R. Bellur, H. N. Al-Shareef, S. H. Rou, K. D. Gifford, O. Auciello and A. I. Kingon, "Electrical Characterization of Sol-Gel Derived PZT Thin Films", *Proceedings of the Eighth IEEE International Symposium on Applications of Ferroelectrics*, 1992, pp.448-51

[10] K. G. Brooks, I. M. Reaney, R. Klissurska, Y. Huang, L. Bursill, N. Setter, "Orientation of Rapid Thermally Annealed Lead Zirconate Titanate Thin Films on (111) Pt Substrates", *Journal of Materials Research*, vol.9, no.10, Oct. 1994, pp.2540-53

[11] I. M. Reaney, et. al., "Use of Transmission Electron Microscopy for the Characterization of Rapid Thermally Annealed, Solution-Gel, Lead Zirconate Titanate Films", *Journal of the American Ceramic Society.*, vol. 77, no. 5, 1994, p.1209-16

[12] D. E. Lakeman, Z. Xu and D. A. Payne, "Rapid Thermal Processing of Sol-Gel Derived PZT 53/47 Thin Layers", *Proceedings of the Ninth IEEE International Symposium on Applications of Ferroelectrics*, 1994, pp.404-7

[13] S. Yoshikawa, U. Seivaraj, K. G. Brooks, and S. K. Kurtz, "Piezoelectric PZT Tubes and Fibers for Passive Vibrational Damping", *Proceedings of the Eighth IEEE International Symposium on Applications of Ferroelectrics*, 1992, pp.269-72

Chapter 2

Introduction to Lock-In Amplifier and N-Path Filters

The microgyroscope generates sensitivity in the μV range and therefore suffers a lot from noise distortion. Signal conditioning circuitry is needed to help improve the poor signal-to-noise-ratio (SNR). Intuitively, a suitable design of a narrowband bandpass filter can improve the performance of the microgyroscope by rejecting the out-of-band noise. However, the achievable Q-value of the bandpass filter is usually limited by process variations in nowadays technology. Thus the performance of the microgyroscope cannot be improved significantly by using only a bandpass filter to reject the out-of-band noise.

To improve the microgyroscope performance, we adopted to use a lock-in amplifier, which is capable to detect ac-signals all the way down to a few nano-volt. Its operation will be covered in the first section of this chapter. After that, the specifications and design considerations of a narrowband bandpass filter for the lock-in amplifier will be discussed. Lastly, the N-path and pseudo-N-path filter concepts and the corresponding design techniques will be introduced. As will be shown later, the pseudo-N-path filter concept is very useful for implementing switched-capacitor narrowband bandpass filters.

2.1 Lock-In Amplifier

Figure 2.1 shows a simple lock-in amplifier, which consists of a low-noise pre-amplifier (Pre-amp), narrowband bandpass filter (BP Filter), AC amplifier (AC amp), phase-lock-loop (PLL), mixer, lowpass filter (LP Filter) and a DC amplifier (DC amp).

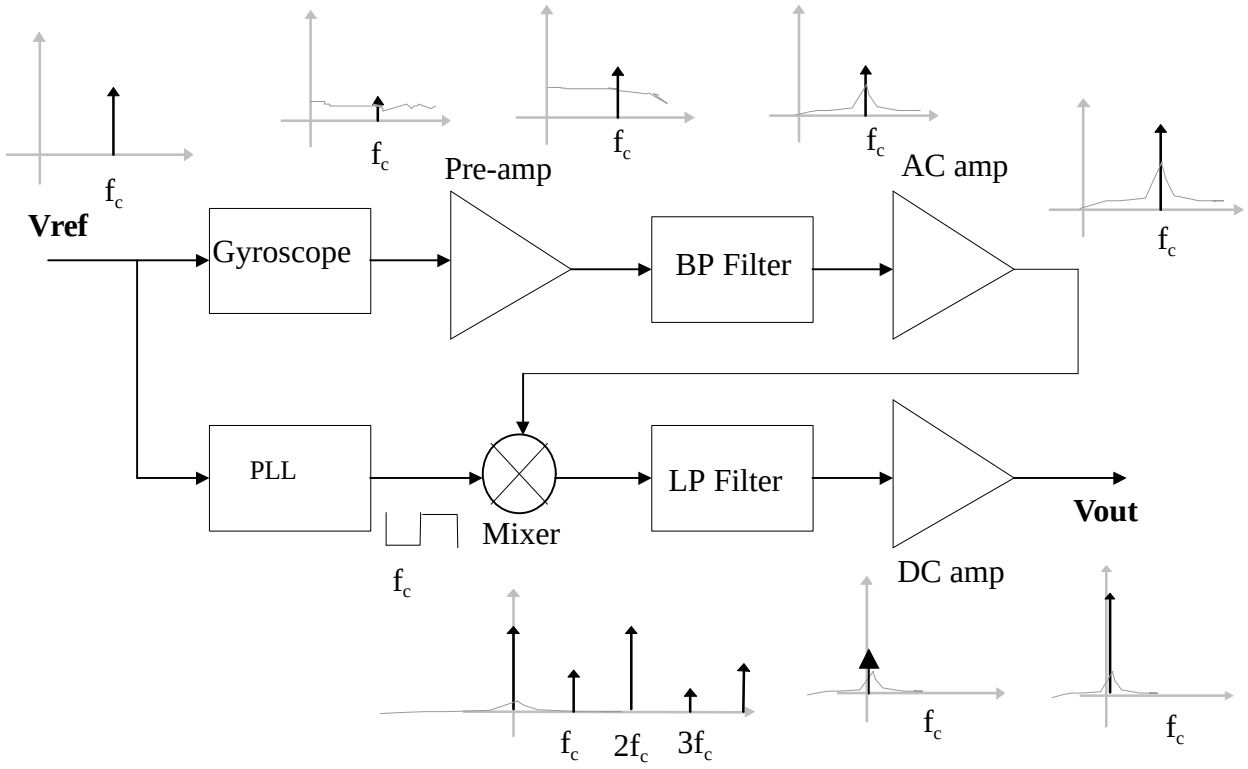


Fig. 2.1 Block diagram of a Lock-In Amplifier

The microgyroscope is activated to resonsate by a reference AC signal source (Vref) at frequency f_c as described graphically in Fig. 2.1. The low-noise pre-amplifier then amplifies the microgyroscope's output signal, which is also at the same frequency as the reference signal. The signal is extracted while the out-of-band noise is rejected by a narrowband bandpass filter before the signal is passed to another amplifying stage. The use of the mixer and PLL

implements a phase-sensitive detection technique to single-out the components of the signal at a specific reference frequency and phase. As a result, noise signals at frequencies other than the reference frequency, as well as the out-of-phase noise at the reference frequency, are rejected. The signal is mixed down to zero frequency (DC) and is extracted by a high-order lowpass filter, which suppressed the side-bands signal created by the mixer. The signal can then be further amplified by a DC amplifier to a level that depends on applications' requirements. As a result, AC signals all the way down to a few nano-volts can be detected and measured.

2.2 Narrowband Bandpass Filter

In this project, we focus on the design and implementation of the narrowband bandpass filter. In addition to be narrowband, the filter should also be low-noise so as to prevent the AC-amplifier from being saturated by the noise. Some considerations of implementation of the filter are listed below:

Low-power: The microgyroscope is mostly employed in portable applications like video-camera image stabilization, intelligent toys and so on. Obviously, the power dissipation of the signal conditioning circuitry should be low.

Low-voltage: Fundamentally, the power consumption of circuits can be reduced efficiently if the supply voltage can be cut down. Meanwhile, sub-micron CMOS technology scaling will soon require all transistors' gate-to-source (V_{GS}) voltage to operate in less than 1.5V in 2001 and 0.9V by the year 2009, as predicted by the Semiconductor Industry Association.

Filter choice: At frequency in kilo-hertz range, SC filters are more attractive over Gm-C filters. This is because, the linearity of OTAs that used in Gm-C filters worsen a lot and the filter distortion increases rapidly when the power supply voltage is reduced. More importantly, the Gm-C filter transfer function is too sensitive to process variation especially for high-Q filter implementations [1]. This is due to the fact that their transfer functions depend on the matching between absolute transconductance and capacitor values, which cannot be closely controlled in foreseeable future CMOS technology. Though automatic frequency-tuning and Q-tuning can help solve some of the mismatch problems, they introduce excessive noise to the system while burning a lot of power. For SC filter, however, the transfer function depends on capacitor ratio, and its distortion is determined by the linearity of the capacitors. In standard CMOS technology, two capacitors can be matched with an error of less than 0.1%, while the availability of linear-capacitor option in HP 0.5um process can reduce the distortion of the SC filter.

As a result, a switched-capacitor bandpass filter is built with HP 0.5um CMOS technology for the Lock-In amplifier.

2.3 SC Filters

There are several ways to realize a SC bandpass filter such as cascading simple biquadratic filters, implementing ladder bandpass filter or using N-path techniques [1][2]. Though in principle any high-order transfer function can be realized by cascading biquadratic filters and first-order section, in practice, the resulting circuit is often difficult to fabricate and very sensitive to finite opamp gain effects, stray resistance and capacitance, and element-value

variations. The capacitance-spread is also unacceptably high. Hence, in nowadays fabrication technologies, the response of such kind of narrowband filter implementation is often unacceptable, and the yield becomes too low for economical production. Hence the Q-value of this kind of filter is often limited to be about 50 and the required number of opamps is equal to the filter order.

For filters that have to realize higher-Q-values, ladder filter structure is often employed. Its principle is in utilitizing the low-sensitivity response of a doubly terminated reactance two-port network. Consequently, the resulting filters are also of low-sensitivity to element variations, and hence are capable to realize bandpass filters with Q-value up to a hundred with acceptable yield. However, it still suffers from high capacitance spread and needs the same number of opamps as the filter order for the implementation.

For achieving even higher Q-values (relative bandwidth of 1% or less), filter designs based on the N-path filter concept may be used [1][3][4][5][6]. It makes use of the alias and image frequency-translated responses of SC filters in order to achieve highly selective bandpass responses using low sensitivity SC filters with low capacitance spread. The principle is explained in next section.

2.4 N-Path Filters

To explain the principles of N-path filters we consider the schematic amplitude response A_{SCLP} of a switched-capacitor lowpass filter (SC-LPF) as shown in Fig. 2.2. This SC-LPF is a sample-data network and is sampled with the clock frequency f_c. The resulting periodical frequency response A_{SCLP} has a bandpass characteristic related to the low-pass filter at multiples of the clock frequency f_c. This characteristic suggests the use of the low-pass filter as a bandpass filter. As stated by the Nyquist theorem, sampled data filters can only correctly process any input signal up to the half of the sampling frequency f_c. The frequency range is referred to as the Nyquist range (NY).

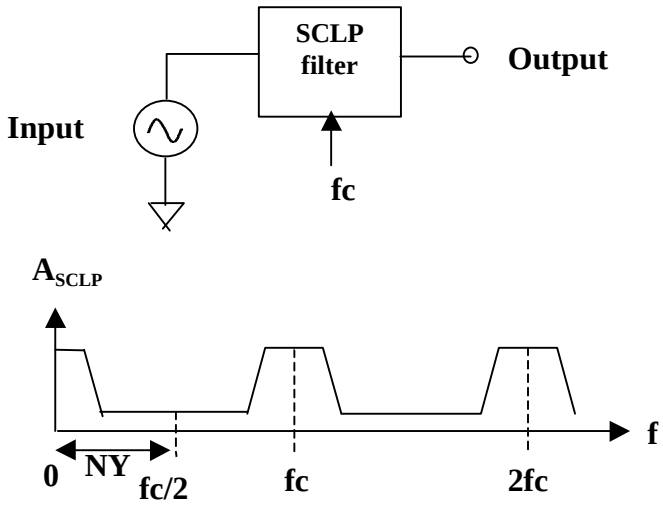


Fig. 2.2 Amplitude response (A_{SCLP}) of an SC lowpass filter

In fact, we can increase the Nyquist range of the SC lowpass filter by increasing the number (N) of samples per period. This can be achieved by using additional paths (not by over-sampling alone, as this will only enlarge the whole frequency response). Such an

expanded filter is called an N-path filter. Figure 2.3 shows an N-path (N=3) filter.

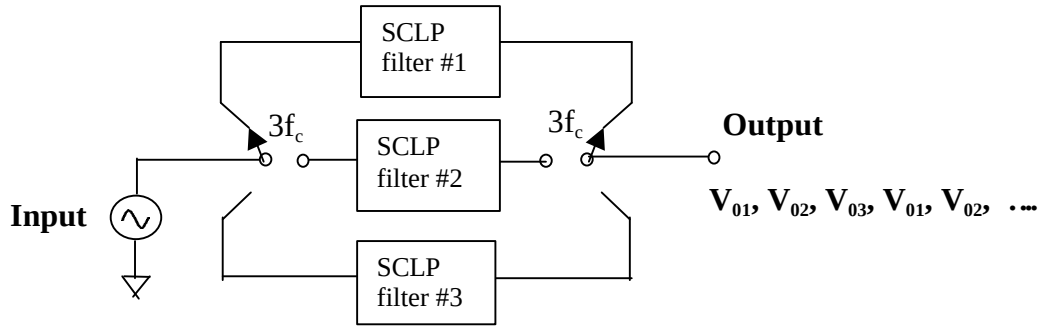


Fig. 2.3 N-path filter structure consisting of N parallel, identical, and cyclically sampled lowpass filter cells with the corresponding clock scheme (N=3 is shown)

The N-path (N=3) filter consists of 3 parallel identical filter cells, which are cyclically sampled with the frequency f_c. As such, the 3 path-filters take turn to give out its output signal V_{01}, V_{02}, V_{03}, V_{01}, V_{02}, and so and so forth. As such, the transfer characteristic as seen from the output node is the same for every switch position, and so the overall frequency response of the N-path filter is equal to the response of an individual path, which is a lowpass response in this case. However, the output signal is now composed of N samples per period, so that the Nyquist range for the N-path filter is expanded by N times. The situation can be presented graphically as shown in Fig. 2.4.

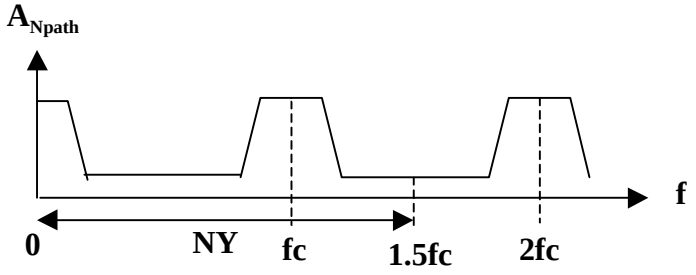


Fig. 2.4 Amplitude response A_{Npath} of an N-path filter with N=3

Now the Nyquist range (NY) has been extended by 3 times (since N=3 is used) to cover the bandpass response that centered at frequency f_c. With the use of appropriate lowpass pre-filter and bandpass post-filter, such an expanded SC low-pass filter can be used as a bandpass filter with the center frequency at f_c.

Unlike the case of using over-sampling to expand Nyquist range, the amplitude response of the N-path filter is the same as that of the lowpass filter though N times higher sampling rate is used to operate the filter. Therefore, the overall transfer function of N-path filter has the same filter coefficients and, accordingly, identical sensitivities as an individual filter path cell. More importantly, since the path cell is a lowpass filter, the sensitivities to element value variations and the resulting capacitance spread are much less than that of a conventional SC bandpass filter that implements the same transfer function as that of the N-path filter. This is one of the most important advantages of using SC N-path filters over the conventional SC bandpass filters. The low sensitivity to element value tolerances of this approach allows the design of bandpass filters with quality factor (Q - value) up to a few hundreds with acceptable yield and capacitance spread. Besides, since the center frequency of the passband is equal to a multiple of the clock frequency, a very stable and exact center frequency can be obtained. Meanwhile, by controlling the clock frequency, the center frequency of the filter can be adjusted, thus the N-path filter is tunable [7].

However, the N-path filter also has several important shortcomings:

(1) The MOS switches used in SC filters introduce clock feedthrough signal at the output. This clock feedthrough signal produces not only an undesirable offset voltage, but also additional spectral components at integer multiples of the clock frequency f_c. These spectral components reduce the maximum dynamic range in the filter passband at f_c, since the clock feedthrough noise falls into the passbands of the filter.

(2) Another disadvantage of N-path filters is that N times more components are needed and hence approximately N times more power consumption.

(3) Besides, any asymmetry among the path filters introduces spurious output signals and mirror frequency noise.

The clock feedthrough noise can be eliminated for N-path filter that uses highpass filter as filter path cell instead of lowpass one [4][6][8]. To explain this, we consider the amplitude response of a SC highpass filter (SC-HPF) as shown in Fig. 2.5.

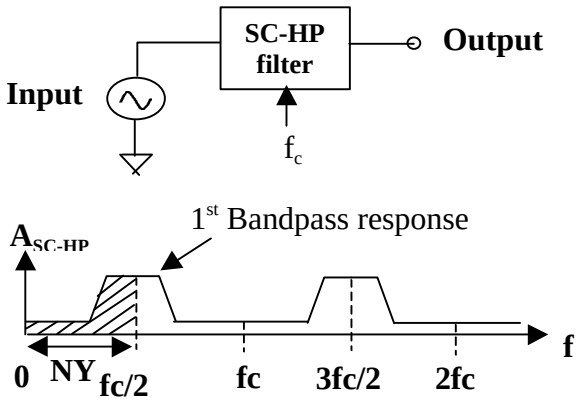


Fig. 2.5 Amplitude response (A_{SCHP}) of a SC highpass filter

For a highpass resposnse, the Nyquist range only covers up to half of the sampling frequency, and hence the bandpass response centered at $f_c/2$ cannot be used. In order to utilize

the first bandpass response, we can build a N-path (N=2) filter with two highpass filters as path cells, which is shown in Fig. 2.6 below.

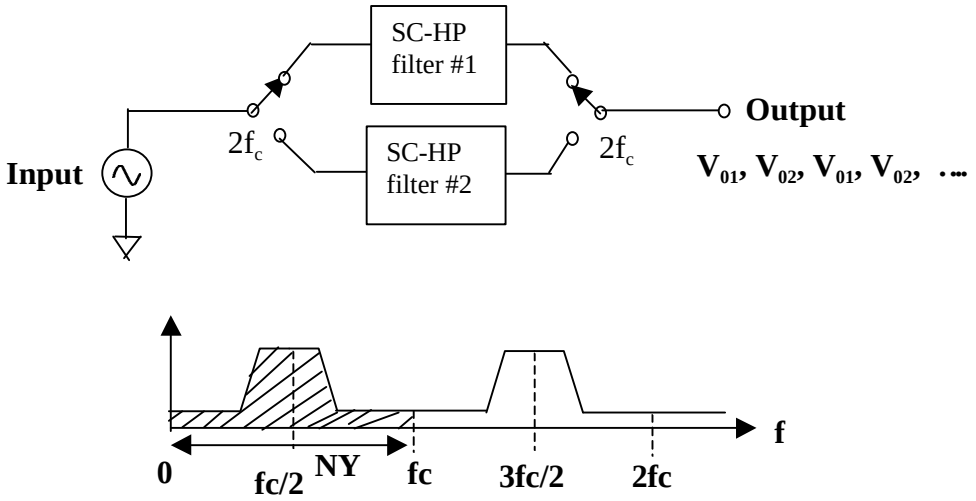


Fig. 2.6 N-path filter structure consisting of N parallel, identical, and cyclically sampled highpass filter cells with the corresponding clock scheme (N=2 is shown)

By so doing, the Nyquist range is extended to cover signal frequencies up to f_c, and hence the whole bandpass response can be used. Here, the passbands lie at frequencies $f_o=if_c/2$ (i =1,3,5 ..) while the clock frequency components are located at integer multiples of f_c. As a result, the clock feedthrough noise do not appear in the passbands and therefore can be filtered out by applying approriate post-filter, which is a lowpass filter if the first passband is being used.

2.5 Pseudo-N-Path Filters

Though N-path filters can achieve a bandpass response with Q-values as high as a few hundreds, they are power hungry as N paths are needed and hence N times more components

are required. The main idea of pseudo-N-path filter [1][9][10][11][12] is that since only one of the path filters is active at any given time, it is therefore worthy to time share all memoryless elements of the path filters, that is, opamps and the switched capacitors which are fully discharged in each cycle. Such timesharing is advantageous not only because it saves components, but it also eliminates some potential sources of path asymmetry that causes spurious output signals and mirror-frequency noise, since now the same opamps and switched capacitors can be used in all paths. A table of comparison between the properties of N-path filter and pseudo-N-path filter (using lowpass path cell or highpass path cell) can be readily obtained. This is shown in Table 2.1 below.

Table 2.1 Comparison on N-path and pseudo-N-path filter using lowpass path cells and highpass path cells

	N-Path Filter		**Pseudo-N-Path Filter**	
Parameters	**Lowpass path cell**	**Highpass path cell**	**Lowpass path cell**	**Highpass path cell**
Sampling frequency (f_s)	$N_{LP}f_c$	$2N_{HP}f_c$	$N_{LP}f_c$	$2N_{HP}f_c$
Center frequency (f_c) of resulting bandpass response	f_s/N_{LP}	$f_s/2N_{HP}$	f_s/N_{LP}	$f_s/2N_{HP}$
Bandwidth of resulting bandpass response	$2f_p$	$2(f_s-f_h)$	$2f_p$	$2(f_s-f_h)$
Minimum number of paths	3	2	3	2
Clock feedthrough	Yes	No	No**	No
Pre-filtering	Bandpass	Lowpass	Bandpass	Lowpass
Post-filtering	Bandpass	Lowpass	Bandpass	Lowpass
Number of Opamps needed (in multiple of that required in a path filter)	N times	N times	Same	Same

** Where f_p and f_h stand for passband edges for lowpass and highpass filters respectively.*

** Pseudo-N-path filter with lowpass path cells can be made free from clock feedthrough noise by using circulating delay type cells [10]

SC narrowband bandpass filters can be realized with N-path filter technique, which provides a good control on the Q-values of the filters. As such, relative bandwidths of less than 1% can be obtained with acceptable yield and capacitance spread. Meanwhile, the use of highpass path filters provides us two important advantages: the whole system is intrinsically free from clock feedthrough noise and the pre-filtering and post-filtering can be done by using lowpass filters. Though it requires a higher sampling frequency, this is not critical to the system if the frequency is already low. As a result, a pseudo-2-path filter using highpass path filters was designed and implemented. Table 2.2 summarizes the specifications of the narrowband bandpass filter.

Table 2.2 Specifications of the bandpass filter

Parameters	**Specifications**
Passband gain	≥ 0dB
Passband ripple	<0.1dB
Center frequency	75kHz (tunable range +/- 5kHz)
Bandwidth	1.5kHz
Stopband minimum loss	≥40dB
Sampling frequency (f_s)	300kHz (for N=2)
Filter type	Elliptic response
Filter order	6
Filter Q value	50

The center frequency is chosen according to the resonant frequency of the microgyroscope. The filter has a tunable range of ±5kHz so as to cope with process variations of the microgyroscope that lead to resonant frequency shift. The center frequency of the filter can be

easily adjusted by changing the clock frequency, for instance, an 80kHz center frequency can be obtained by using a 320kHz (80kHz x 4) clock frequency. Elliptic filter response is adopted to reduce the filter order requirement. Though elliptic filter response has a large passband ripple, this is not critical to our application since the microgyroscope outputs a monotonic signal. The synthesis procedures of the pseudo-2-path filter are illustrated in next chapter.

Reference

[1] R. Gergorian and G. Temes, *Analog MOS Integrated Circuits For Signal Processing*, John Wiley & Sons, New York, 1986

[2] P. V. Ananda Mohan, V. Ramachandran and M. N. S. Swamy, *Switched Capacitor Filters – Theory, Analysis and Design*, Prentice Hall International (UK) Ltd., 1995

[3] D. C. Von Grunigen, R. P. Sigg, J. Schmid, G. Moschytz, and H. Melchior, "An Integrated CMOS Switched-Capacitor Bandpass Based on N-Path and Frequency-Sampling Principles", *IEEE Journal of Solid-State Circuits*, Vol. SC-18, No. 6, Dec. 1983, pp. 753-761

[4] J. E. Ranca, "On switched-capacitor bandpass filter systems with very narrow relative bandwidths", *Proceeding of the 1985 European Conference on Circuit Theory and Design*, North-Holland, 1985, pp.745-8

[5] H. Shafeeu, A. K. Betts, J. T. Taylor, "Approaches to ultra-narrow-band analogue IC filter design using switched-capacitors", *IEE Colloquium on Advances in Analogue VLSI*, 1991, pp.21-9

[6] A. K. Betts and J. T. Taylor, "Evaluation and synthesis of ultra narrow band switched-capacitor-filters employing multirate techniques", *IEEE International Symposium on Circuits and Systems*, vol.3, 1990, pp.2197-200

[7] H. C. Patangia and J. Cartinhour, "A tunable switched capacitor N-path filter", *The 24th Midwest Symposium on Circuits and Systems*, Western Periodicals, 1981, pp.400-4

[8] J. E. Franca, "Multirate switched-capacitor N-path filtering systems using bandpass path filters", *Proceedings of the International Conference on Circuits and Systems*, vol. 1, 1991, pp.230-3

[9] G. Palmisano, F. V. G. Espinosa and F. Montecchi, "Performance comparisons of pseudo-N-path SC cells in filters with real operational amplifiers", *Proceedings of the IEEE International Symposium on Circuits and*

Systems, vol. 2, 1989, pp.1467-70

[10] G. Palmisano and F. Montecchi, "Simplified pseudo-N-path cells for z to -z/sup N/ transformed SC active filters", *IEEE Transactions on Circuits & Systems*, vol.36, no.3, March 1989, pp.461-3.

[11] H. Shafeeu, A. K. Betts and J. T. Taylor, "Implementation issues for ultra narrow band switched-capacitor filters", *Proceedings of the IEEE International Symposium on Circuits and Systems*, vol. 5, 1992, pp.2304-7

[12] H. Shafeeu, A. K. Betts and J. T. Taylor' "Implementation of a very narrow band finite gain insensitive pseudo-N-path filter", *Proceedings of the IEEE International Symposium on Circuits and Systems*, vol.5, 1994, pp.581-4

Chapter 3

Synthesis of Classical SC Pseudo-2-Path Ladder Filter

Switched-capacitor (SC) bandpass filters can be realized with SC highpass path-filters using pseudo-2-path technique or with SC lowpass path-filters using pseudo-3-path technique [1][2]. Though the pseudo-2-path filter offers better filter performances, the required SC highpass ladder filters have generally stray-sensitive structures unless those stray-sensitive switching capacitor branches are replaced by opamps [3], which certainly increases the power consumption and therefore is not desirable. Meanwhile, SC lowpass ladder filters usually have stray-insensitive structures [3][4], and thus a trade-off between power consumption and filter performances seems unavoidable when choosing between pseudo-2-path filter and pseudo-3-path filter. However, in the z-domain, a lowpass response can be transformed to a highpass response by replacing all “z” terms in the transfer function with “-z”, which is known as the “z to –z transformation”. The highpass ladder filters so derived inherently obtains the advantages of the lowpass ladder filter structure without asking for additional opamps. In this chapter, an LDI-transformed lowpass ladder filter is derived and converted to a highpass ladder filter using z to –z transformation method [2][5][6][7]. A RAM-type path cell [8] is then introduced to implement the pseudo-2-path filter.

3.1 Specifications of SC Lowpass Ladder Filter

To reduce the required filter order of the lowpass path cell, elliptic filter prototype is chosen [9]. Ladder filter structure is adopted since its transfer function is less sensitive to the opamp DC gain and unity-gain frequency as well as process variation [3][4]. As the sampling frequency is required to be four times of the center frequency of the pseudo-2-path filter, it is therefore much higher than the passband frequency of the lowpass filter. In this case LDI-transformation can be conveniently used to map the continuous-time transfer function into the discrete-time domain accurately. Unlike bilinear-transformation (which requires a sampled-and-held input signal), no sample-and-hold circuitry is required for LDI-transformed SC filters. Table 3.1 summarizes the required specifications of the discrete-time lowpass filter.

Table 3.1 Specifications of the lowpass filter

Parameters	**Specifications**
Passband Gain	10dB
Passband Ripple	< 0.1dB
Stopband Minimum Loss	> 30dB
Bandwidth	750Hz
Sampling Frequency	150kHz
Filter Order	3
Filter Type	Elliptic

3.2 Realization of SC Lowpass Ladder Filter

The SC lowpass ladder filter can be derived from an elliptic lowpass LCR filter as shown in Fig. 3.1. From filter design handbook [10], elliptic filter prototype C03, θ=11 fulfills the specifications of the required lowpass filter. Table 3.2 summarizes the parameters of the LCR filter prototype.

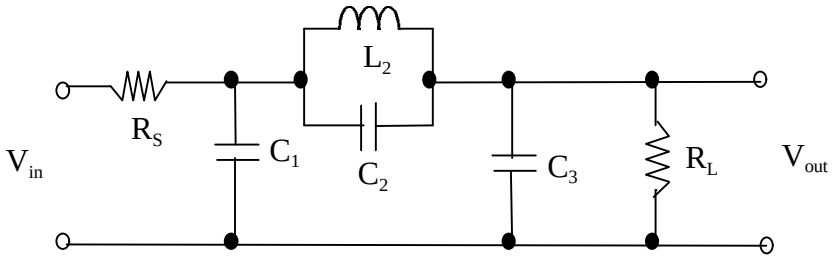


Fig.3.1 Elliptic LCR filter prototype

Table 3.2 Summary of parameters of the LCR prototype

Ω_s	A_{min}	θ	L_2	C_1	C_2	C_3	R_S	R_L
5.24	41dB	11	0.9411	0.6194	0.0291	0.6194	1	1

where Ω_s and A_{min} are the normalized stopband frequency and the stopband minimum loss of the filter respectively. Note that the passband gain is pre-set to be unity while the circuit has its passband at ω_a = 1 rad/sec. For LDI-transformation, frequency wrapping between continuous-time (ω_a) and discrete-time domain (ω) is done via Equation 3.1, where T stands for the sampling period used in the discrete-time system. By so doing, the discrete-time domain specifications are wrapped into the continuous-time domain to realize the LCR filter prototype. If the LCR filter is realized with SC circuit, the resulting SC filter possesses the desired filter specifications in the ω-domain, since SC circuit is a discrete-time system.

$$\omega_a = \frac{2}{T}\sin\left(\frac{\omega T}{2}\right) \qquad \text{(Eq. 3.1)}$$

By taking C_o=1, Z_o=1/ω_a and L_o=1/ω_a^2, the denormalized LCR filter prototype parameters can be obtained by multiplying the capacitors, inductors and resistors values with C_o, L_o and Z_o respectively. Table 3.3 summarizes the denormalized values.

Table 3.3 Summary of denormalized LCR filter parameters

Parameters	ω_a	C_1^{FT}	C_2^{FT}	C_3^{FT}	L_2^{FT}	R_S^{FT}	R_L^{FT}
Denormalized Value	6283.1	0.6194	0.0291	0.6194	0.2383n	0.159m	0.159m

The state-space equations of the LCR prototype can be written as follows:

$$-V_1 = -\frac{1}{sC_1^{FT}}\left[\frac{V_{in}-V_1}{R_s} - I_2 + sC_2^{FT}V_3\right] \quad \text{(Eq. 3.2)}$$

$$-I_2 = -\left(\frac{1}{sL_2^{FT}}\right)(V_1 - V_3) \quad \text{(Eq. 3.3)}$$

$$V_3 = \frac{-1}{s\left(C_2^{FT}+C_3^{FT}\right)}\left[-sC_2^{FT}V_1 - I_2 + \frac{V_3}{R_L}\right] \quad \text{(Eq. 3.4)}$$

The state-space equations can also be presented in a block diagram as shown in Fig. 3.2.

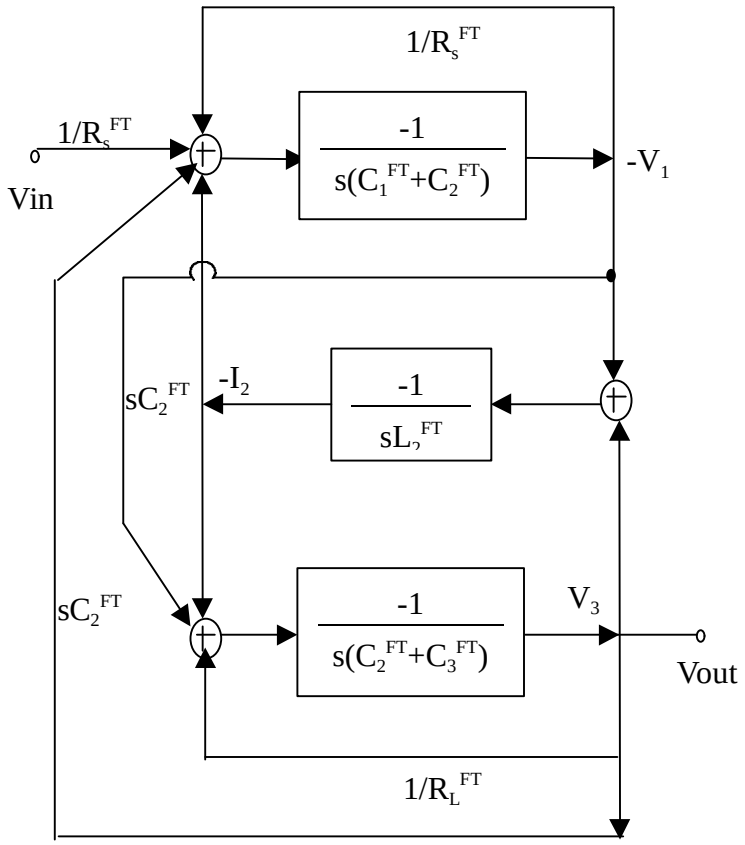


Fig. 3.2 Block diagram describing the state-space equations

To transform the block diagram into a SC circuit, the charge versus voltage relations of all blocks and branches will first be found in the s-domain. For LDI-transformation, these relations can be transformed via Equation 3.5 into the z-domain and then realized by SC components, which are presented as follows.

$$s \to \frac{z^{1/2} - z^{-1/2}}{T} \qquad \text{(Eq. 3.5)}$$

In the analog system, the charge that flows through the input branch $1/R_s^{FT}$ is given by:

$$\frac{V_{in} - 0}{R_s^{FT}} = I_{in} = \frac{dq_{in}}{dt} \qquad \text{(Eq. 3.6)}$$

which can be written in the s-domain:

$$Q_{in}(s) = \frac{V_{in}(s)}{sR_s^{FT}} \qquad \text{(Eq. 3.7)}$$

By using Equation 3.5, Equation 3.7 can be LDI-transformed into the z-domain as:

$$Q_{in}(z) = T\frac{z^{-1/2}}{1 - z^{-1}}\frac{V_{in}(z)}{R_s^{FT}} \qquad \text{(Eq. 3.8)}$$

$$\Rightarrow (1 - z^{-1})Q_{in}(z) = \frac{T}{R_s^{FT}} z^{-1/2} V_{in}(z)$$

Equation 3.8 can also be written in the time-domain as:

$$q_{in}(t_n) - q_{in}(t_{n-1}) = C_{in} V(t_{n-1/2}) \qquad \text{(Eq. 3.9)}$$

Figure 3.3 shows the stray-insensitive SC circuit implementation of the input branch using two non-overlapping clock phases ϕ_1 and ϕ_2. (Note that ϕ_1 and ϕ_2 will be used as non-overlapping clock phases throughout the whole thesis and the clock phases diagram will

therefore not be shown in all other SC circuits implementation mentioned thereafter).

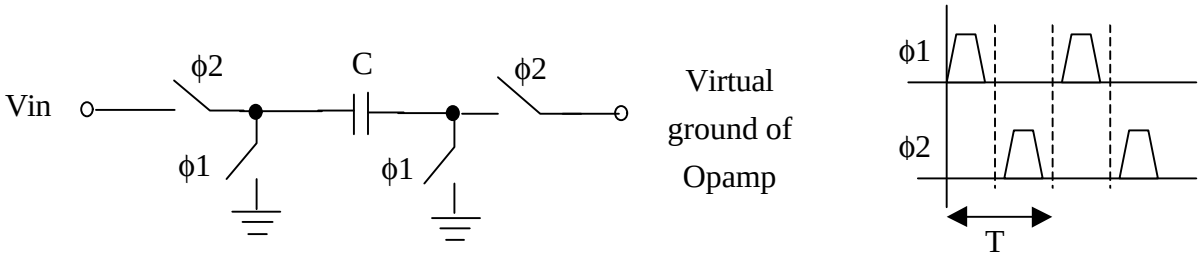


Fig. 3.3 Realization of input and feedback branches with SC circuit

Similarly, the feedback branches $1/R_S^{FT}$ and $1/R_L^{FT}$ can also be realized the same way as that of the input branch. As will be shown later, it is very useful to have memoryless resistive branches for performing z to -z transformation and hence facilitating the pseudo-N-path implementation.

The charge versus voltage relation of the coupling branches marked sC_2^{FT} is given by $Q/V=C_2^{FT}$, which is frequency independent. They can thus be realized simply by capacitors of value C_2^{FT}.

Lastly, the transfer functions of all the three blocks in the Fig. 3.2 simply correspond to integrators in both s-domain and z-domain. They can be easily realized by using op-amps with feedback capacitors as shown in Fig. 3.4.

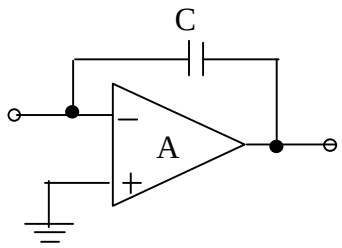


Fig. 3.4 Implementation of transfer function -1/sC

By replacing the block diagram in Fig. 3.2 with the above pieces of SC circuits, the LCR filter prototype can be transformed into a SC ladder filter, which is shown in Fig 3.5 in differential form.

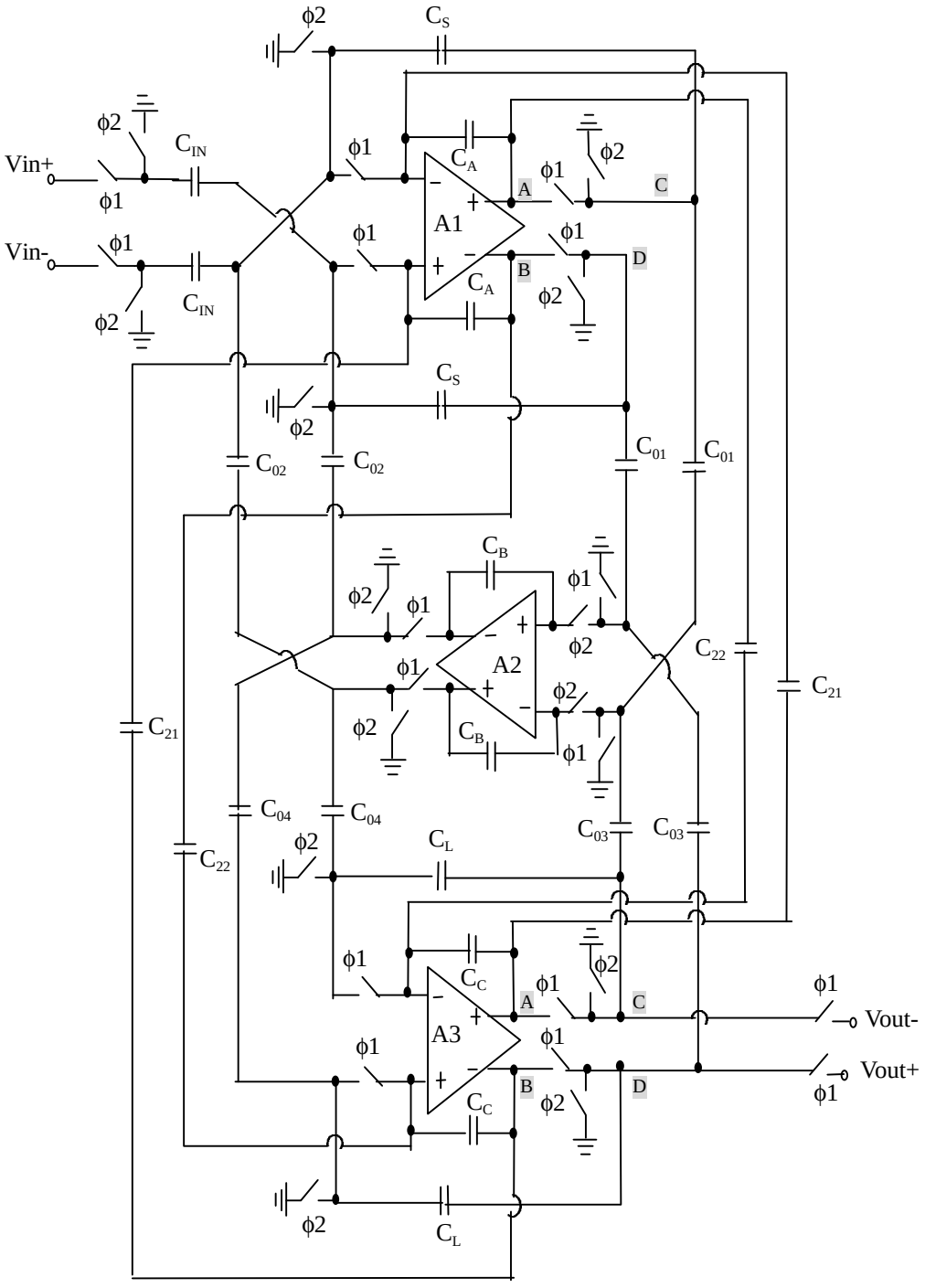


Fig. 3.5 Schematic of a fully differential LDI-transformed ladder lowpass filter

The resulting ladder lowpass filter shares the low-sensitivity properties of the LCR prototype filter and it is parasitic-insensitive. The realization of a fully-differential structure not only helps reject common-mode noise and reduces clock-feedthrough noise but it also provides a sign conversion of the output voltages, which is required in the z to -z transformation. The frequency response of the filter is simulated with SWITCAP2 [11] as shown in Fig. 3.6. Table 3.4 summarizes the derived capacitors' values.

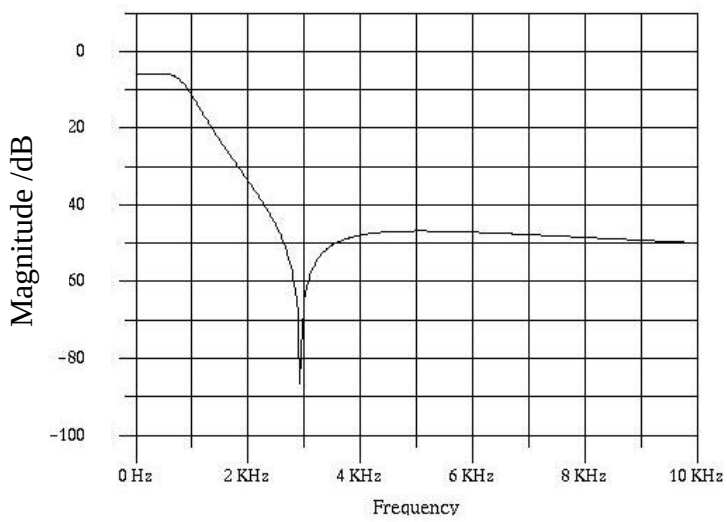


Fig. 3.6 Frequency response of SC lowpass ladder filter

Table 3.4 Summary of capacitor values of the LDI-transformed SC lowpass ladder filter

Capacitors	**Derivations**	**Values (unit capacitor)**
C_A	$= C_1^{FT}+C_2^{FT}$	= 0.6485
C_B	$= L_2^{FT}$	$= 0.23838\text{x}10^{-9}$
C_C	$= C_2^{FT}+C_3^{FT}$	= 0.6485
$C_{01}=C_{02}=C_{03}=C_{04}$	= T (sampling period)	$= 3.33\text{x}10^{-6}$
C_S	$= T/R_S$	= 0.0209
C_{IN}	$= T/R_S$	= 0.0209
C_L	$= T/R_L$	= 0.0209
C_{21}	$= C_2^{FT}$	= 0.0291
C_{22}	$= C_2^{FT}$	= 0.0291

As expected, the -3db frequency is about 750Hz and the stopband loss is 40.1dB lower than the passband. However, a passband gain of -6dB is resulted and the maximum capacitance spread of the circuit is 27.2×10^6, which is impossible to implement on chip. The actual performance of the SC filter can be improved by performing dynamic range optimization and capacitance spread optimization [3]. The resulting frequency response and the capacitors' values are shown in Fig. 3.7 and Table 3.5 respectively. Here, the passband gain is 10dB and the resulting total capacitance spread is only 50. Table 3.6 summarizes the lowpass ladder filter characteristics.

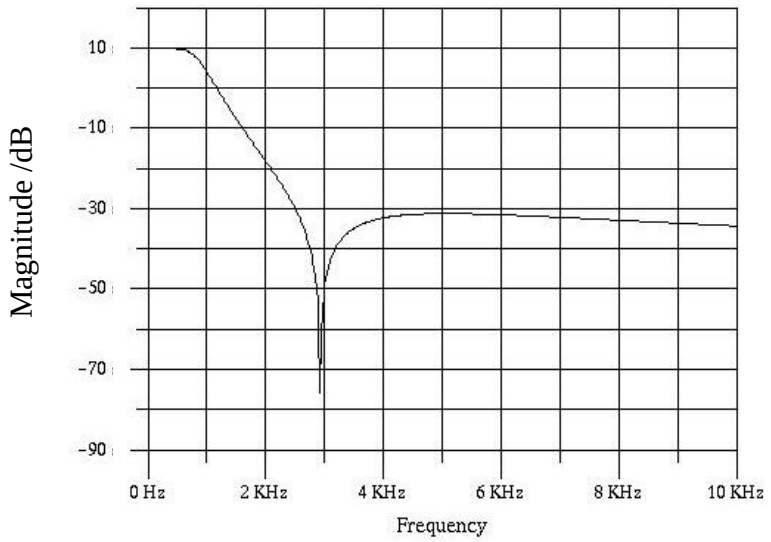


Fig. 3.7 Frequency response of the optimized SC lowpass ladder filter

Table 3.5 Summary of optimized capacitors' values

Capacitors	C_S	C_L	C_{01}	C_{02}	C_{03}	C_{04}
Values /pF	0.1454	0.1	0.152	0.1	0.1	0.1048

Capacitors	C_{IN}	C_A	C_B	C_C	C_{21}	C_{22}
Values /pF	0.588	4.5	5	3.1	0.133	0.212

Table 3.6 Summary of SC lowpass ladder filter characteristics

Parameters	**Simulated Results**
Passband Gain	10dB
Passband Ripple	< 0.1dB
Stopband Minimum Loss	> 30dB
Bandwidth	750Hz
Sampling Frequency	150kHz
Filter Order	3
Maximum Capacitance Spread	50

3.3 Z to –Z Transformation

In z-domain, a lowpass response can be transformed to a highpass response by replacing all “z” terms in the transfer function with “-z”, which is known as the “z to –z transformation”. Voltage inversion techniques designed to achieve the z to –z transformation have been reported in [2][5][6][7]. In order to obtain a stray-insensitive circuit, differential technique is adopted. Figure 3.8 shows one possible way of implementation of a z to –z transformed SC inverting integrator.

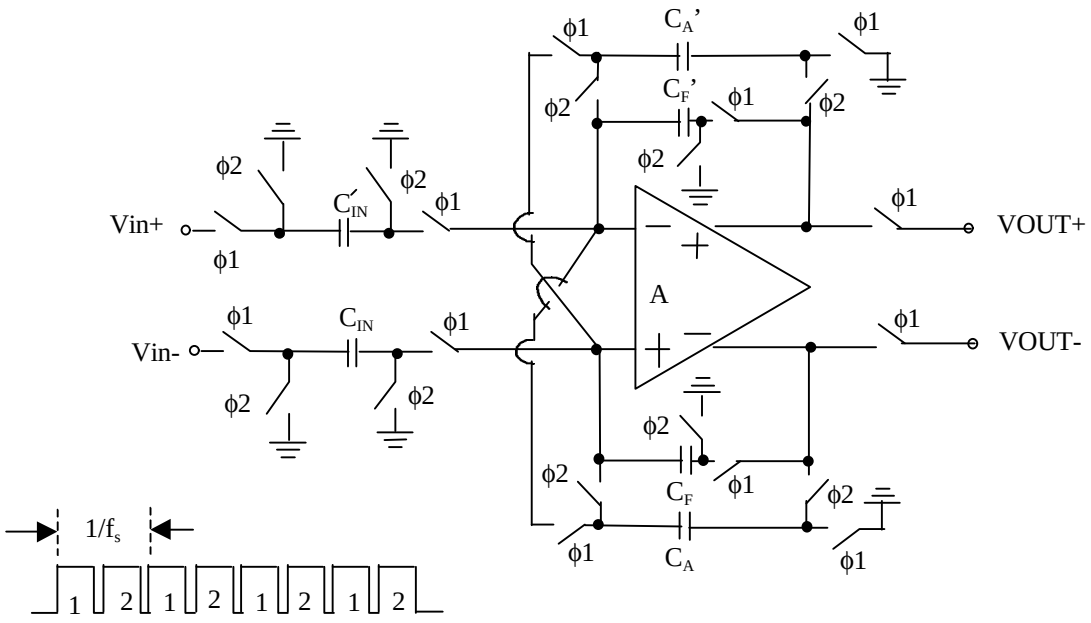


Fig. 3.8 Differential z to –z transformed SC inverting integrator

Suppose capacitors C_F and C_A are of the same size and all capacitors in differential path are perfectly matched. C_F and C_F' are the integrating capacitors while C_A and C_A' are the capacitors for temporary signal storage. The operation of the circuit is as follows: At $\phi 1$, capacitor $C_F(C_F')$ receives the new signal from the input capacitor $C_{IN}(C_{IN}')$ and the inverted old signal from the storage capacitor C_A' (C_A), which is in the opposite path. This operation gives the sign inversion required by the z to -z transformation. Equation 3.10 describes the operation mathematically.

$$\left.\begin{aligned} Vout^+(nT) &= \left(\frac{\cancel{C_A}}{C_F'}\frac{C_F}{\cancel{C_A}}\right)Vout^-(nT-T) - \frac{C_{IN}'}{C_F'}Vin^+(nT) \\ Vout^-(nT) &= \left(\frac{\cancel{C_A}'}{C_F}\frac{C_F'}{\cancel{C_A}'}\right)Vout^+(nT-T) - \frac{C_{IN}}{C_F}Vin^-(nT) \end{aligned}\right\} \quad \text{(Eq.3.10)}$$

During phase $\phi 2$, the updated charge in $C_F(C_F')$ is transferred back to $C_A(C_A')$ for storage. As a result, the transfer function of this z to –z transformed integrator can be derived as follows:

$$Vout^+(nT) - Vout^-(nT) = Vout^-(nT-T) - Vout^+(nT-T) - \frac{C_{IN}'}{C_F'}Vin^+(nT) - \left(-\frac{C_{IN}}{C_F}Vin^-(nT)\right) \quad \text{(Eq.3.11)}$$

By z-transform:

$$\frac{Vout^+ - Vout^-}{Vin^+ - Vin^-} = -\frac{C_{IN}}{C_F\left(1+z^{-1}\right)} \quad \text{(Eq.3.12)}$$

It is worth to recall here that a SC inverting integrator has a transfer function of the form:

$$\frac{Vout^+ - Vout^-}{Vin^+ - Vin^-} = -\frac{C_{IN}}{C_F\left(1-z^{-1}\right)} \quad \text{(Eq.3.13)}$$

and thus a z to –z transformation is achieved by the z to –z transformed SC integrator. As a

result, a highpass ladder filter can be realized by simply replacing all the integrators in the lowpass ladder filter (Fig. 3.5) with the z to –z transformed integrator. Figure 3.9 shows the schematic of the highpass ladder filter. Minor modifications are needed for the coupling capacitors C_{21} (C_{21}') and C_{22} (C_{22}'), which are memory elements in the system that realize z-transfer function of the type (z^{-1}-1). Therefore, when the z to –z transformation is used, their transfer functions have to change to be ($-z^{-1}$-1). This can be achieved by connecting the bottom plates of these coupling capacitors, which were connected directly to the amplifier output nodes "A-B" in the lowpass ladder filter (Fig. 3.5), to the switched nodes "C-D" [2]. In fact, the charge on these coupling capacitors is temporarily stored on the integrating capacitors C_A (C_A') and C_C (C_C'), and will be given back after each sampling periods. The frequency response of the highpass ladder filter is simulated with SWITCAP2, and the results are shown in Fig. 3.10 and Fig. 3.11. We observe that the passband is centered at 75kHz, which is half of the sampling rate (150kHz) and thus a highpass filter frequency response is obtained. The passband characteristics of the highpass filter is the same as that of the lowpass ladder filter except an about 3dB passband gain reduction due to the sin(x)/x roll-off distortion of the sample-and-hold action in the circuit [1][5]. Table 3.7 summarizes the SC highpass ladder filter characteristics.

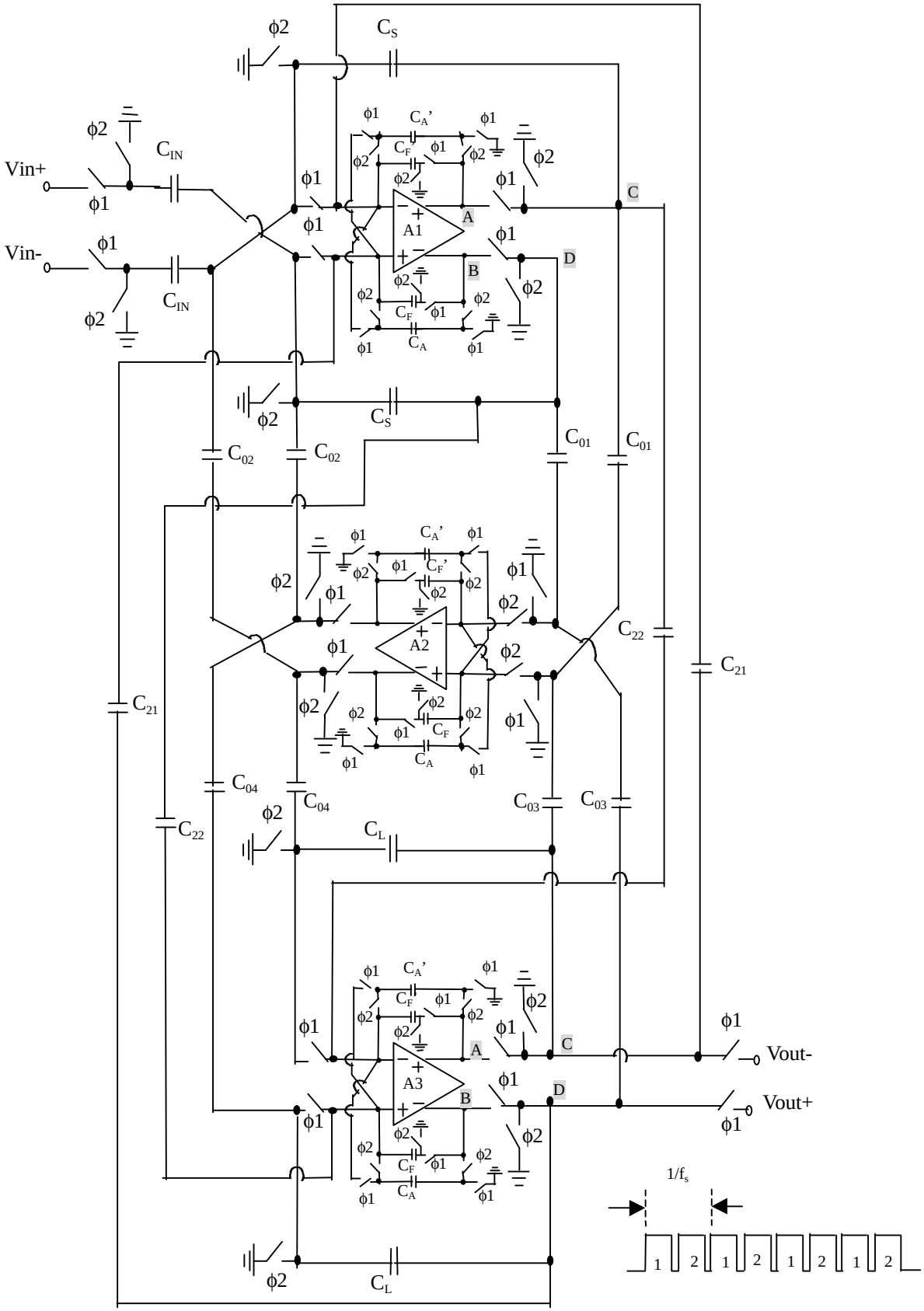


Fig. 3.9 Schematic of a fully differential highpass ladder filter

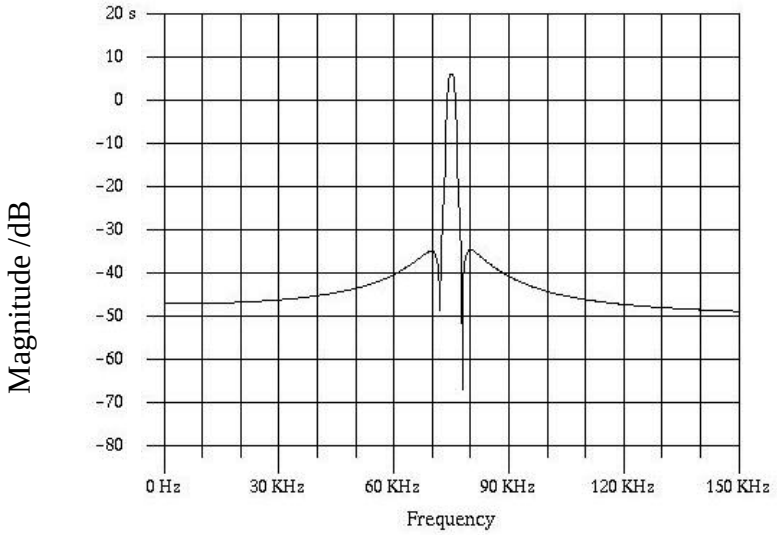


Fig. 3.10 Frequency response of a z to –z transformed SC highpass ladder filter

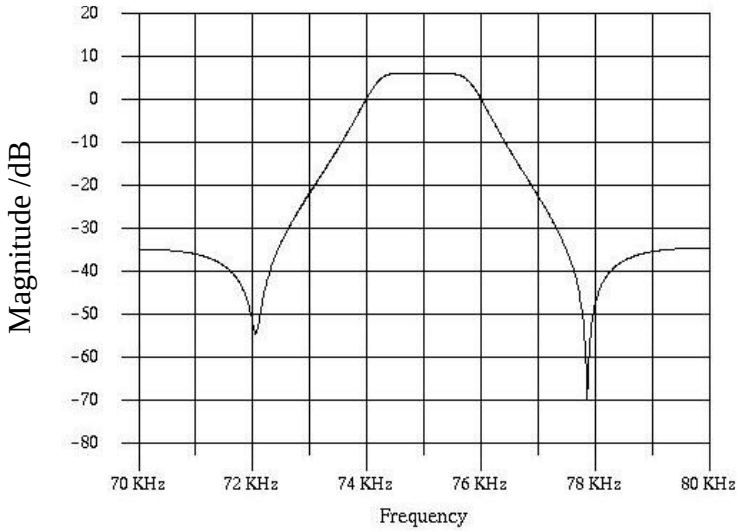


Fig. 3.11 Passband characteristics of the SC highpass ladder filter

Table 3.7 Summary of SC highpass ladder filter characteristics

Parameters	**Simulated Results**
Passband Gain	6.7dB
Passband Ripple	< 0.1dB
Stopband Minimum Loss	> 33.3dB
Bandwidth ($f_s - f_p$)	750Hz
Sampling Frequency (f_s)	150kHz
Filter Order	3
Maximum Capacitance Spread	50

where f_p and f_s are the passband frequency and sampling frequency respectively

3.4 Implementation of a Pesudo-2-path SC Filter

Theoretically, bandpass response can be realized by using two SC highpass ladder filters to operate alternatively to build a 2-path filter, the block diagram is redrawn in Fig. 3.12 for easy discussion.

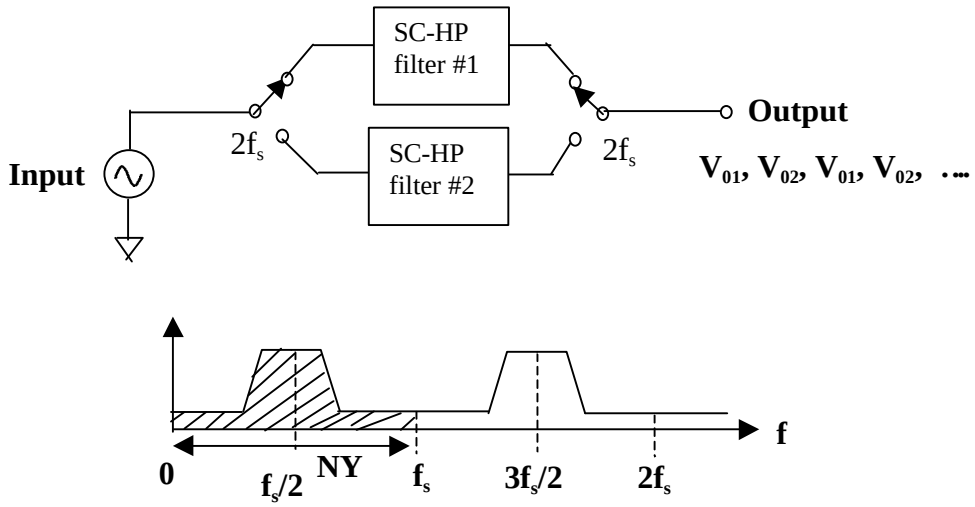


Fig. 3.12 2-path filter structure consisting of two parallel, identical, and cyclically sampled highpass filter cells with the corresponding clock scheme

The two SC highpass path filters are operating at a sampling rate of f_s (150kHz) in alternative phases, while the overall system works at a sampling frequency of (300kHz). As such the Nyquist range covers the whole bandpass response centered at $f_s/2$ (75kHz). However, as discussed in Chapter 2 Section 2.5, it is worth to time share all memoryless elements of the two highpass filters, that is, opamps and the switched capacitors which are fully discharged in each cycle since only one path is active at any clock cycle. This results in the realization of a pseudo-2-path filter [8]. By adding two more storage capacitors (C_B and C_B') into the z to –z

transformed integrator (Fig. 3.8) and two other non-overlapping clock phases ϕ_A and ϕ_B that work at half of the sampling frequency of the overall system, we can obtain a pseudo-2-path transformed integrator, which is shown in Fig. 3.13. Note that the clock phases ϕ_1 and ϕ_2 are operating at a sampling frequency of $2f_s$.

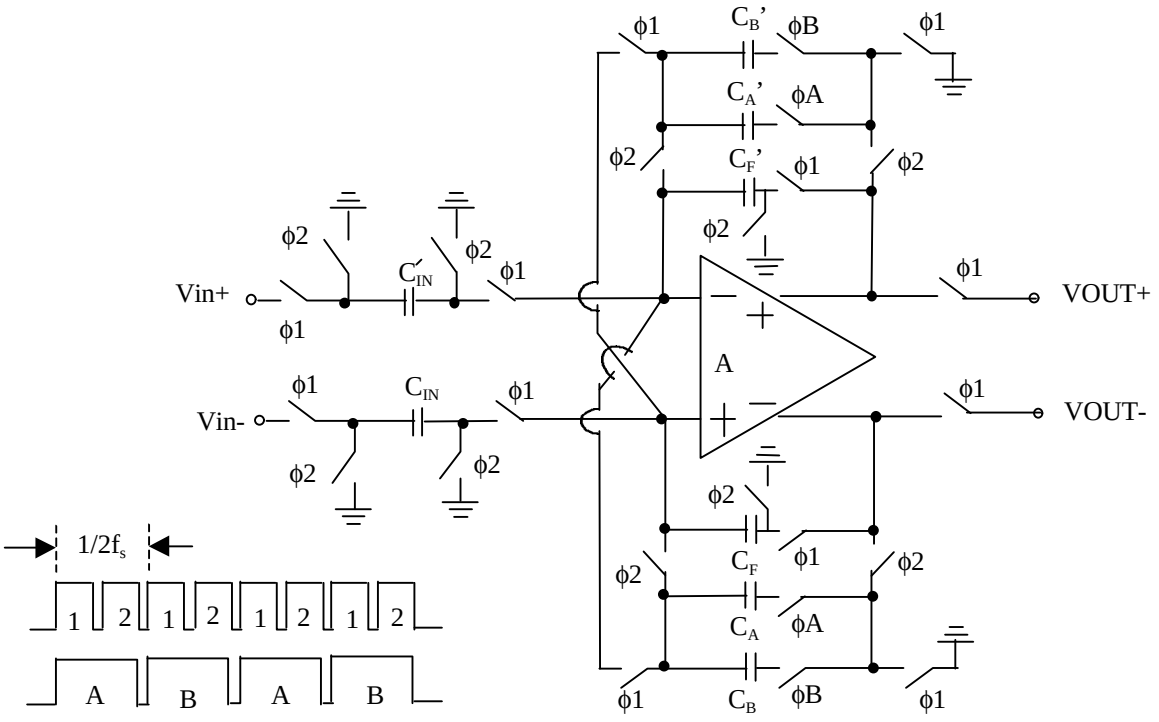


Fig. 3.13 Differential pseudo-2-path transformed SC integrator

The same integrating capacitors C_F and C_F' are used by both paths. The two paths are performed by the switching capacitors C_A and C_A', and C_B and C_B' respectively, which are also the only memory elements in the circuit. During ϕ_A, the first highpass filter is integrating the new signal and the stored signal in capacitors C_A and C_A' at ϕ_1, the resultant signal is passed back and stored in storage capacitors C_A and C_A' at ϕ_2. The second highpass filter works

similarly at ϕ_B but with C_B and C_B' as the storing elements. This is optimized to use same size capacitors for C_F, C_F', C_A, C_A', C_B and C_B'. It is because if the storage capacitors (C_A, C_A', C_B and C_B') are smaller than the integrating capacitors (C_F and C_F'), the signal will be amplified by the ratio (C_A/C_F or C_B/C_F) when it is stored. Therefore requiring more signal dynamic range from the opamp to prevent it from being distorted. Meanwhile, using storage capacitors that are larger than the integrating capacitor will slow down the speed of operation, and this is also not desirable in the chip-area point of view. Now, assume all capacitors in the differential paths are perfectly matched, at phases ϕ_A and ϕ_1, capacitor C_F (C_F') receives the charge from the input capacitor C_{IN} (C_{IN}') and from the storage capacitor C_A' (C_A) from the opposite path. This operation gives the sign inversion required by the z to -z transformation as explained before in section 3.3. During the time when both ϕ_A and ϕ_2 are on, the updated charge in C_F (C_F') is transferred back to C_A (C_A') in the storage array. This charge is then held on C_A (C_A') for *two sampling periods* since each highpass filter is operating at half sampling frequency of that of the overall system. The same operation is repeated during phase ϕ_B while the charge is stored on C_B (C_B'). By doing so, z to $-z^2$ transformation is resulted. Equation 3.14 and 3.15 mathematically describes the time-domain operation of path A and path B respectively.

$$\left.\begin{aligned} Vout^{+}(nT) &= \left(\frac{\cancel{C_A}}{C_F'}\frac{C_F}{\cancel{C_A}}\right)Vout^{-}(nT-2T)-\frac{C_{IN}'}{C_F'}Vin(nT)^{+} \\ Vout^{-}(nT) &= \left(\frac{\cancel{C_A}}{C_F}\frac{C_F'}{\cancel{C_A}'}\right)Vout^{+}(nT-2T)-\frac{C_{IN}}{C_F}Vin(nT)^{-} \end{aligned}\right\} \quad \text{(Eq.3.14)}$$

$$\left.\begin{aligned} Vout^{+}(nT+T) &= \left(\frac{\cancel{C_B}}{C_F'}\frac{C_F}{\cancel{C_B}}\right)Vout^{-}((nT+T)-3T)-\frac{C_{IN}'}{C_F'}Vin(nT+T)^{+} \\ Vout^{-}(nT+T) &= \left(\frac{\cancel{C_B}'}{C_F}\frac{C_F'}{\cancel{C_B}'}\right)Vout^{+}((nT+T)-3T)-\frac{C_{IN}}{C_F}Vin(nT+T)^{-} \end{aligned}\right\} \quad \text{(Eq.3.15)}$$

Equation 3.16 describes the transfer function of the SC pseudo-2-path integrator, which is derived by performing z-transformation on either Equation 3.14 or 3.15, since both equations give the same result towards z-transformation.

$$\frac{Vout^{+}-Vout^{-}}{Vin^{+}-Vin^{-}}=-\frac{C_{IN}}{C_F\left(1+z^{-2}\right)} \quad \text{(Eq.3.16)}$$

The SC lowpass ladder filter can now be transformed into a bandpass filter firstly via z to –z transformation to a highpass filter and then via the z to z^2 transformation into a bandpass filter using pseudo-2-path technique by replacing all the integrators with the pseudo-2-path transformed integrators. As shown in Fig. 3.14, the pseudo-2-path bandpass filter can be realized by replacing all the integrators in the lowpass ladder filter (Fig. 3.5) with the pseudo-2-path-transformed integrators.

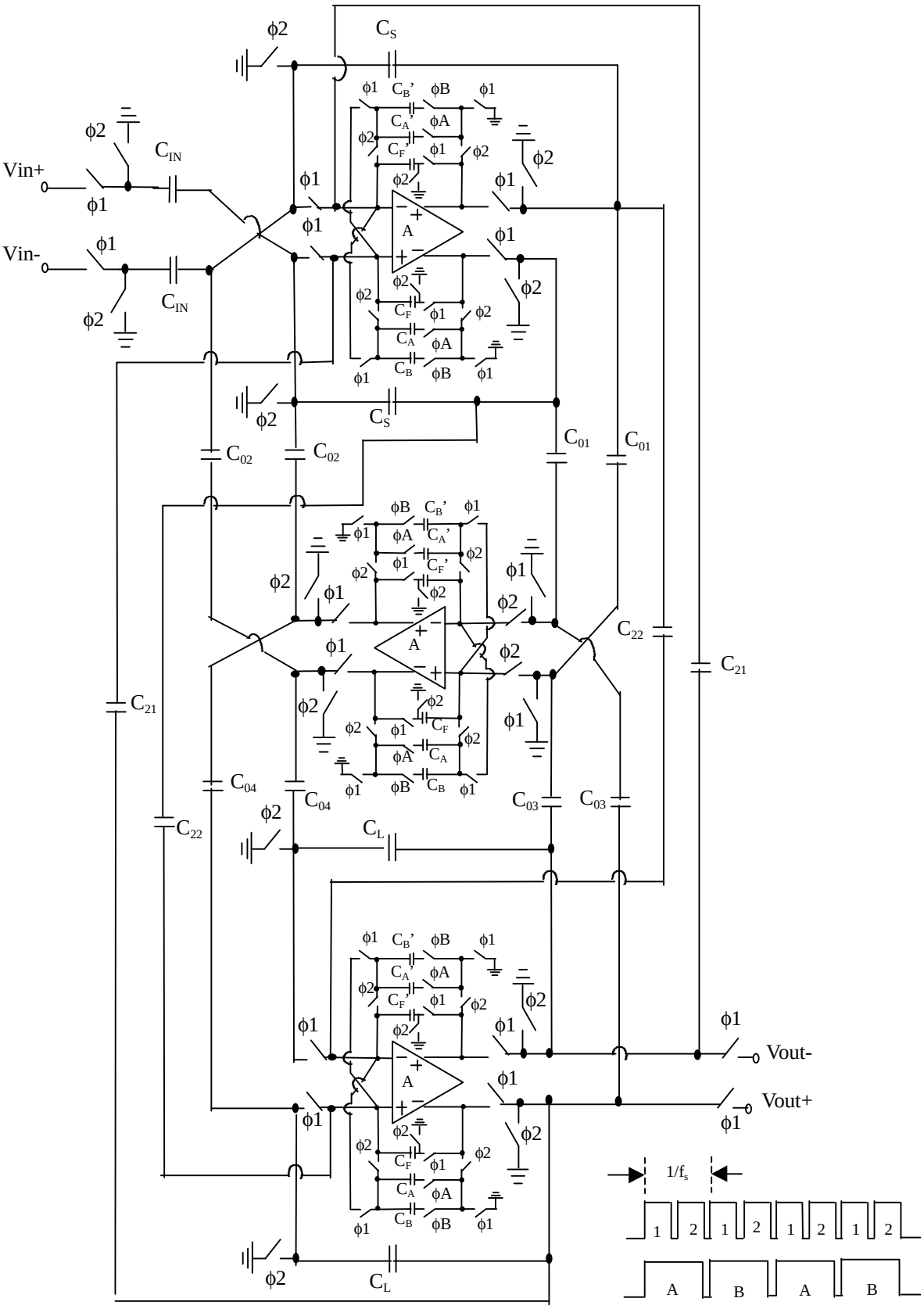


Fig. 3.14 Schematic of a fully differential SC pseudo-2-path filter

SWITCAP2 simulation result of the pseudo-2-path SC bandpass filter is shown in Fig. 3.15.

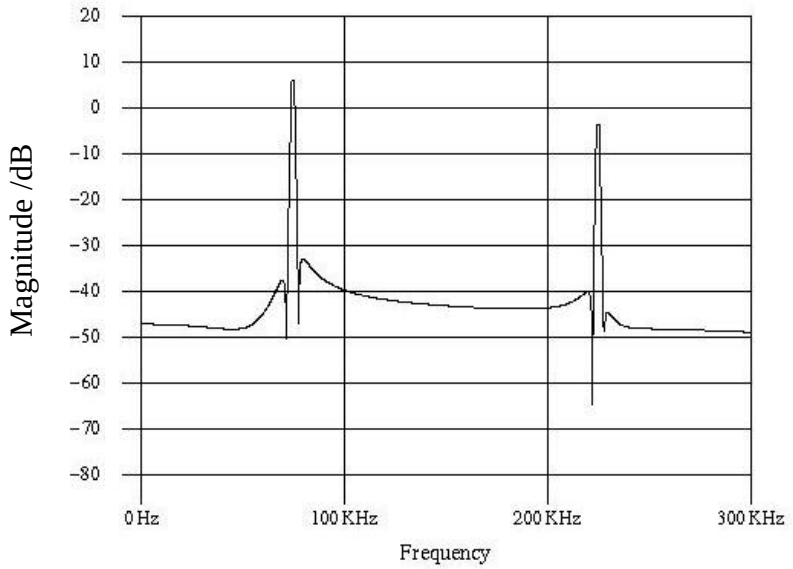


Fig. 3.15 Frequency response of the SC pseudo-2-path filter

As expected, two bandpass responses are obtained within the sampling frequency range. Interested passband is located at 75kHz, which is 1/4 of the sampling frequency of the system, while the passband at 225kHz (3/4 of the sampling frequency) is out of the Nyquist range and will therefore be suppressed by post-filtering filter. The use of the upper passband will not be discussed here.

Figure 3.16 shows the passband characteristics obtained by using three different opamp gains (10^3, 10^4 and 10^6). It can be observed that an opamp gain larger than 70dB is sufficient to preserve the filter transfer function accuracy. The center frequency is 75kHz with a bandwidth

of 1.5kHz. The passband gain is 6dB with a passband ripple less than 0.1dB. The minimum stopband loss is 34dB. Table 3.8 summaries the pseudo-2-path filter characteristics.

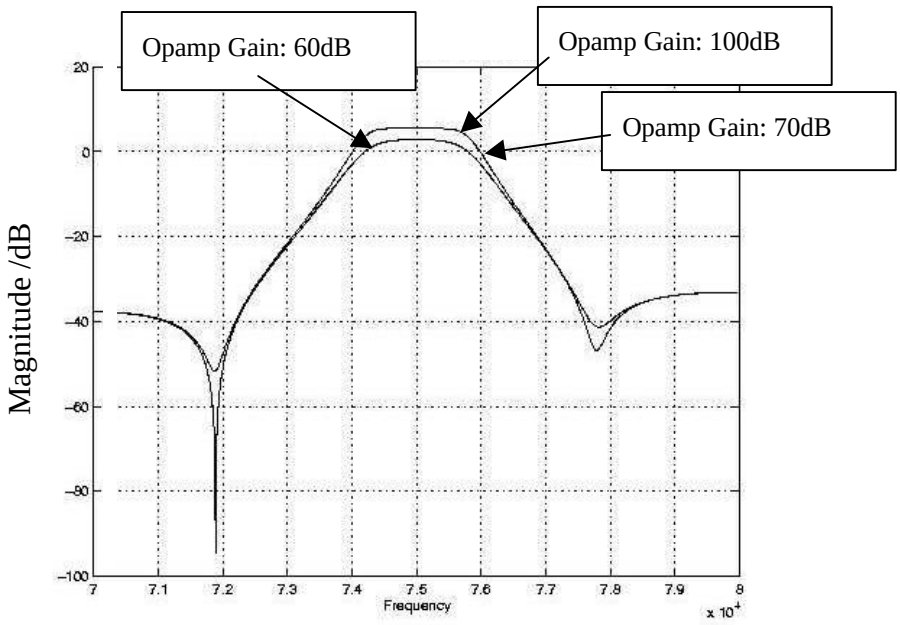


Fig. 3.16 Passband characteristics of the SC pseudo-2-path filter

Table 3.8 Summary of SC pseudo-2-path filter characteristics

Parameters	**Simulated Results**
Center Frequency	75kHz
Passband Gain	6.7dB
Passband Ripple	< 0.1dB
Stopband Minimum Loss	> 33.3dB
Bandwidth	1.5kHz
Sampling Frequency (f_s)	300kHz
Filter Order	6
Filter Q value	50
Maximum Capacitance Spread	50

As a conclusion, a SC pseudo-2-path bandpass filter has been derived from a SC lowpass ladder filter using z to –z transformation and pseudo-2-path technique. System simulations using

SWITCAP2 show good agreements with theory. The SC pseudo-2-path filter requires 3 opamps with DC gain better than 70dB in order to preserve the transfer function accuracy. The total capacitance spread is 50 only and is therefore suitable for on-chip implementation in standard CMOS process. In the next chapter, problems and solutions on low-voltage operation of SC circuits will be discussed.

Reference

[1] J. E. France, "On Switched-Capacitor Bandpass Filter Systems With Very Narrow Relative Bandwidths", *Circuit Theory and Design 85, Proceeding of the 1985 European Conference*, North-Holland, 1985, pp.745-8, Amsterdam, Netherlands

[2] G. Palmisano and F. Montecchi, "Simplified Pseudo-N-Path Cells for z to $-z^N$ Transformed SC Active Filters", *IEEE Transactions on Circuits and Systems*, Vol. 36, No. 3, March 1989, pp.461-3

[3] R. Gergorian and G. Temes, *Analog MOS Integrated Circuits For Signal Processing*, John Wiley & Sons, New York, 1986

[4] Gordon M. Jacobs, David J. Allstot, Robert W. Brodersen and Paul R. Gray, "Design Techniques for MOS Switched Capacitor Ladder Filters", *IEEE Transactions on Circuits and Systems*, Vol. CAS-25, Dec. 1978, pp. 1014-1021

[5] T. Inoue, F. Ueno, S. Masuda and t. Matsumoto, "Low-Sensitivity Switched-Capacitor Bandpass Filters Using Two-Path and Votlage Inversion Techniques", *Transactions of the IECE of Japan*, Vol. E 69, No. 11, Nov. 1986, pp.1149-1152

[6] J. C. Lin and Joseph H. Nevin, "Differential Charge-Domain Bilinear-Z Switched-Capacitor Pseudo-N-Path Filters", *IEEE Transactions on Circuits and Systems*, Vol. 35, No. 4, April 1988, pp.409-415

[7] S. E. Tan, T. Inoue and F. Ueno, "A Design of Narrow-Band Band-Pass SCF's Using a Pseudo-2-Path Principle and a Capacitor-Error-Free Voltage Inversion", *IEEE International Symposium on Circuits and Systems*, Vol. 2, May 1993, pp. 1034-7

[8] G. Palmisano, G. Espinosa F. V. and F. Montecchi, "Performance Comparisons of Pseudo-N-Path SC Cells In Filters With Real Operational Amplifier", *IEEE International Symposium on Circuits and Systems*, Vol. 2, May 1989, pp.1467-70

[9] S. Natarajan, *Theory and Design of Linear Active Networks*, McGraw-Hill Book, 1989, p.109-111

[10] B. Williams and Fred J. Taylor, *Electronic filter design handbook : LC, active, and digital filters*, McGraw-Hill Book, 1988

[11] S. C. Fang, Y. P. Tsividis and O. Wing, "SWITCAP - A Switched Capacitor Network Analysis Program", *Circuit Theory and Design, Proceedings of the 1981 European Conference on Circuit Theory and Design*, Delft University Press, 1981, pp.512

Chapter 4

Considerations of Low-Voltage Operation of SC Circuits

Over the years, the demand for low-power low-voltage integrated circuits (ICs) has rapidly grown due to the increasing importance of portable equipment in all market segments like, for instance, telecommunications, computers, and consumers. The need for low-voltage IC is also motivated by the new submicron CMOS technology scaling that requires all transistor's gate-to-source (VGS) voltage to operate in less than 1.5V in the year 2001 and 0.9V in 2009, as predicted by the Semiconductor Industry Association. In recent years, a lot of researches were done on operating switched-capacitor (SC) filters at low supply voltage [1][2][3]. The primary reason of this is that the SC filters achieve high filter accuracy with a low distortion, for which these two parameters are fairly independent of the power supply. This is in contrast to Gm-C filters where the linearity of the operational transconductance amplifiers (OTA) degrades a lot and the filter distortion increases rapidly when the power supply voltage is reduced In this chapter, fundamental limitations and solutions of operating switched-capacitor circuits at low supply voltage will be discussed. A modified switched-opamp technique is proposed to realize a 1-V SC pseudo-2-path filter.

4.1 Minimum Supply Voltage for SC Circuits

The minimum supply voltage required by most SC circuits is primarily determined and limited by the turn-on requirement of the switches that have to be able to switch the total signal swing. Typically this occurs for switches that are connected to the output of opamps. Figure 4.1 illustrates the problem with a NMOS switch connected to the output of a two-stage opamp.

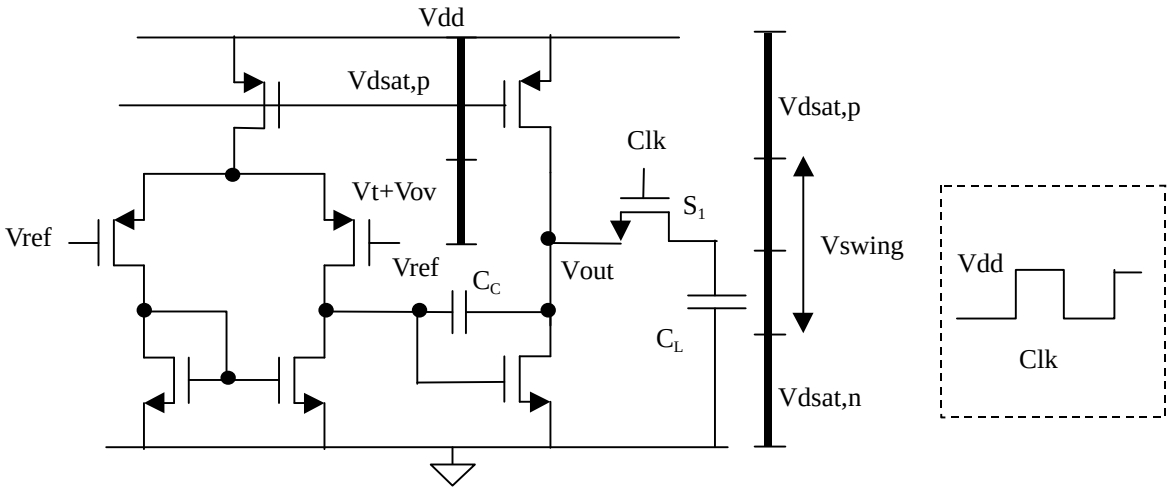


Fig. 4.1 Schematic of a 2-stage Opamp with NMOS switch connected at the output

Since the maximum voltage that appears at the source of MOS switch S_1 is $V_{swing} + V_{DSsat,n}$, the minimum supply voltage that is required to turn on this switch is given as:

$$Vdd_{S1,\min} \approx V_{DSsat} + V_{Tn} + V_{swing} + V_{DSsat,p} \qquad \text{(Eq. 4.1)}$$

Typically, for a standard CMOS process, the minimum supply voltage is 2V for a signal swing of 1V. For supply voltage below 2V, the signal swing is reduced and becomes zero when the supply voltage drops to 1V. However, a lower supply voltage can be used to drive the rest of

the switches that are connected directly to a constant reference voltage in most of the SC circuits. The situation can be substantially described by considering a simple SC integrator as shown in Fig. 4.2.

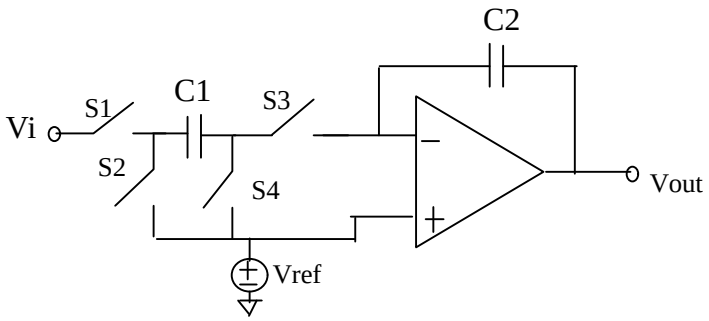


Fig. 4.2 A simple SC integrator (Vi is the Opamp output of previous stage)

In classical switched-capacitor circuits, the input voltage level of the opamp is usually set to be middle of the rails in order to achieve the largest output swing. This can be achieved by setting the reference voltage (Vref) in Fig. 4.2 to be $V_{swing}/2 + V_{dsat,n}$. As a result, the minimum supply voltage that is required for turning on these switches S2, S3 and S4 is given as:

$$Vdd_{S2,3,4,\min} \approx V_{DSsat} + V_{Tn} + \frac{V_{swing}}{2} + V_{DSsat,p} \qquad \text{(Eq. 4.2)}$$

which is about 1.5V for a signal swing of 1V. This is important to emphasize here that a two-stage opamp can still be operated with a voltage supply as low as 1V with an output swing of about 0.8V.

4.2 Switched-Opamp Technique

Obviously, by using a special process with extra low threshold (V_T) transistors, SC circuits are ready to operate with low supply voltages. However, the cost of a dedicated low-V_T process is high, and the low-V_T MOS switches suffer from off-state leakage problem, which causes the charge on the integrator capacitor to leak away. This leakage is signal dependent and consequently causes harmonic distortion. Another solution is to use an on-chip voltage multiplier or charge pump to provide a voltage higher than the supply to drive the MOS switches while keeping the rest of the circuit (mainly the opamps and the voltage multiplier) to operate in low-voltage supply [4][5][6][7]. However, the on-chip voltage multipliers occupy a large chip area and consume a lot of power. More importantly, MOS transistors in future submicron technologies will have to operate with a very low voltage supply for reliability issues since their gate oxide layers are scaled too thin to sustain high voltage (high E-field) operation. In view of these, the switched-opamp technique has been introduced by J. Crols and M. Steyaert in 1994 [8][9], and is further explored in [10][11]. The basic idea of the switched-opamp technique is that if the switch at the output of the opamp can be replaced by a switched-opamp, most of the switched-capacitor circuits can be operated in supply voltage as low as 1.5V for a 1V signal swing. An example of the switched-opamp technique is illustrated in [8] and is redrawn in Fig. 4.3 below for easy discussions.

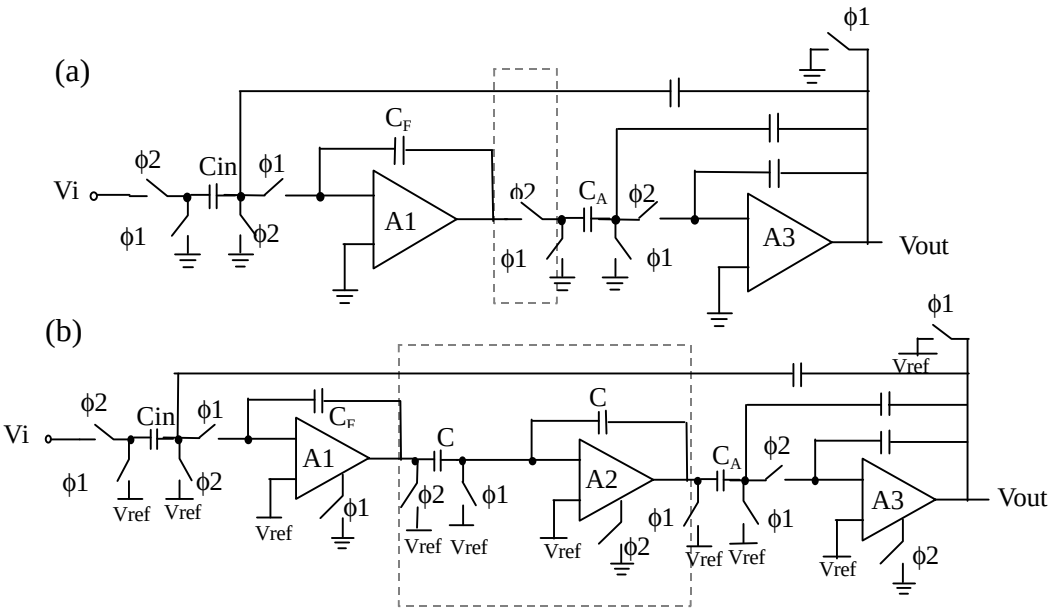


Fig. 4.3 Topology of a lowpass low-Q biquad
(a) switched-capacitor version, (b) switched-opamp [6] version

Figure 4.3 (a) shows a topology of a switched-capacitor lowpass low-Q biquad. Figure 4.3 (b) shows its switched-opamp version. It can be easily observed that the problematic switch at the output of the first stage opamp is now replaced by a non-inverting delay SC integrator. The operation is as follows: Opamp A1 is turned on at ϕ_1 while A2 and A3 are turned on at $\phi 2$. At ϕ_1, input signal stored in C_{in} is passed to the feedback capacitor C_F of the opamp A1. Output voltage of A1 is stored in input capacitor C of A2. At ϕ_2, the voltage stored in C is copied to the output of A2 through the non-inverting delay integrator with unity gain, while the opamp A1 is turned off with its output shorts to the reference voltage. By doing so, the blocked integrator acts like a switch, which is turned on at ϕ_2. Now all the switches in the circuit are connected either directly or virtually to the reference voltage (Vref). As a result, the circuit can now operate at a supply voltage of 1.5V for a signal swing of 1V in standard CMOS process without using on-chip

voltage multiplier. However, the original switched-opamp technique shows three important limitations:

1. Since the common-mode input voltages of opamps are set at middle of the rails, the minimum supply voltage is 1.5V for a signal swing of 1V. If the filter is operated in 1V supply, the common-mode input voltage has to be biased at ground for the two-stage opamp in Fig. 1. As a consequence, the available signal swing is zero.
2. Only non-inverting integrators are allowed to use. As a result, extra inverting stages used to replace the problematic switches are needed to build high-order infinite impulse response (IIR) filters. Nevertheless, all problematic switches can be simply removed if there exist only non-inverting integrators in the SC circuit and all opamps turned off after their integrating phases.
3. The opamp A1 is completely turned off for half cycle. Hence the switched-opamp technique cannot be applied to some useful switched-capacitor circuits such as pseudo-N-path and capacitance-reduction techniques that require the use of the idle phase to process the signal. Besides, the operating speed is also limited by the turn-on time of the opamp.

4.3 SC Dynamic Level Shifter

Solutions for some of the above limitations were proposed by Andrea Baschirotto and Rinaldo Castello in [10][11], in which a SC dynamic level shifter is introduced to allow the common-mode input voltage of opamp to be set independently to the quiescent output voltage of opamp. Fig. 4.4 illustrates the idea:

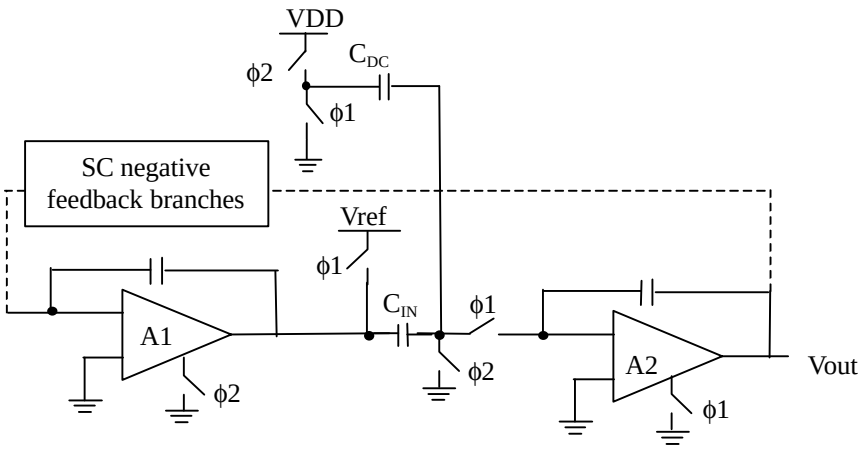


Fig. 4.4 SC Dynamic level shifter

Suppose the common-mode input voltage of opamps are set to ground and the input signal is zero, the output steady-stage voltage of opamps are forced to settle at middle of rails (0.5V in case of 1V single supply) by the switching capacitors negative-feedback branches. In another words, the steady state is reached when no charge injection from capacitor C_{IN} into the virtual ground node of opamp A2 occurs. This happens if Equation 4.3 holds:

$$C_{IN} \cdot V_{out\_dc} + C_{DC} \cdot V_{DD} = C_{IN} \cdot V_{DD} \qquad \text{(Eq. 4.3)}$$

where V_{out_dc} is the output common-mode voltage of opamp A1. The requirement is fulfilled by

choosing $C_{DC}=C_{IN}/2$. As such, if there is not input signal, the charge in C_{IN} is always kept the same at any clock cycle.

Since all MOS switches have their source terminals connected either to ground (realized with NMOS) or VDD (realized with PMOS) instead of connecting to the reference voltage, simultaneous optimization of switch operation and output swing can be achieved. By applying the dynamic level shifter, the minimum supply voltage is determined by the opamp requirement. For a two-stage opamp (Fig. 4.1), this is equal to $V_{DDmin} = V_{TH} + 2V_{ds,sat} \approx 1V$. Note that the signal swing is now determined by the output swing of opamp.

4.4 Modified Switched-Opamp Technique

Previous switched-opamp technique [10][11] requires using a fully differential approach to obtain the required sign inversion for building high-order IIR filter. This is not easy and obvious in some SC applications. Besides, the opamps still only works in the integrating phase, hence the switched-opamp technique cannot be applied to some useful switched-capacitor circuits such as pseudo-N-path and capacitance-reduction techniques that require the use of the idle phase to process the signal. We proposed a modified switched-opamp technique that can solve the above problems. The modified switched-opamp integrator is different from the previous switched-opamp integrator by the addition of an extra switchable opamp (A1') in parallel with the original switchable opamp (A1). Here, it is assumed that the common-mode input voltage of opamps are biased at ground, while the outputs, in steady state without input

signal, are biased to middle of rails by the use of dynamic common-mode feedback circuits [10][11]. Figure 4.5 shows a universal integrator (though only differential configuration is shown, single-ended version is also viable) that uses the modified switched-opamp technique for low-voltage switched-capacitor applications.

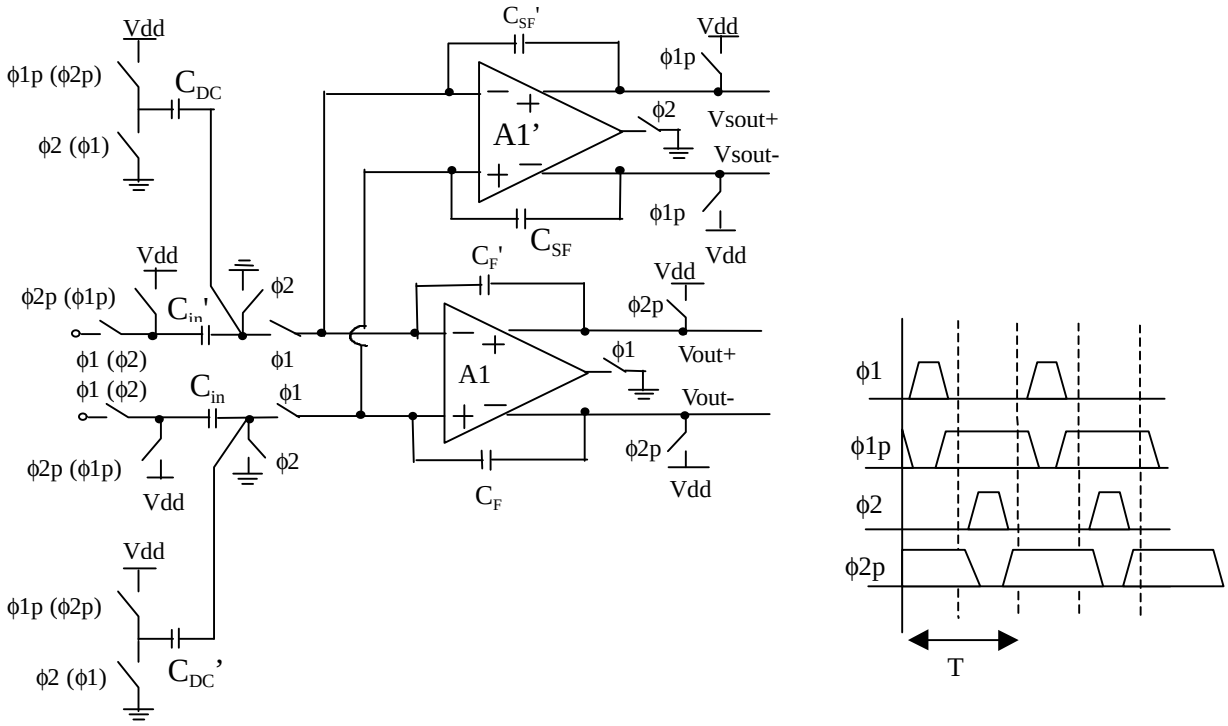


Fig. 4.5 Low-voltage universal SC integrator using modified switched-opamp technique (differential configuration is shown)

Note that ϕ_{1p} and ϕ_{2p} are for PMOS switches, and hence they are just the same clock phases as ϕ_1 and ϕ_2 respectively, which are clock phases for NMOS switches. These two switchable opamps are turned on and off alternatively in two complementary clock phases (ϕ_1,ϕ_2). In ϕ_1, opamp A1 is turned on to integrate the sampled signal from C_{IN} (C_{IN}'), and the processed signal is stored in C_F (C_F'). In ϕ_2, opamp A1' is turned on, while opamp A1 is turned off with its

outputs (Vout+, Vout-) shorted to Vdd. In this case, C_F (C_F') are charged to Vdd while the signal that stored in C_F (C_F') is passed to C_{SF} (C_{SF}'), which are also charged to Vdd in the previous clock cycle. If C_F= C_{SF} (C_F'=C_{SF}'), the signal reappears at the outputs (Vsout+, Vsout-) of opamp A1'. When ϕ_1 goes high again, opamp A1 is turned on, while opamp A1' is turned off with its outputs shorted to Vdd. By doing so, the signal is passed back to C_F (C_F') again while opamp A1 is integrating with new sampled signal from C_{in} (C_{in}').

The modified switched-opamp (SO) integrator applies the original switched-opamp technique, and hence it can also be operated with a single 1V supply. Besides, by the addition of a switchable opamp A1', output signal is available to collect in both clock phases, as in the case of classical SC integrators. As a result, this modified SO integrator can be directly applied to replace the classical SC integrators in any SC applications at low-voltage operation. This would save a lot of re-designing efforts to implement SC circuits at low-voltage because the modified SO technique can be directly applied to nearly all existing SC synthesizing methods. More importantly, due to the creation of an idle phase in this SO integrator, useful techniques like pseudo-N-path, double-sample correction and so on may be implemented in a supply voltage as low as 1-V with standard CMOS technology. To illustrate this, a RAM-type switched-opamp pseudo-N-path cell for the z to $-z^N$ transformation with N=2 is shown in Fig. 4.6 below:

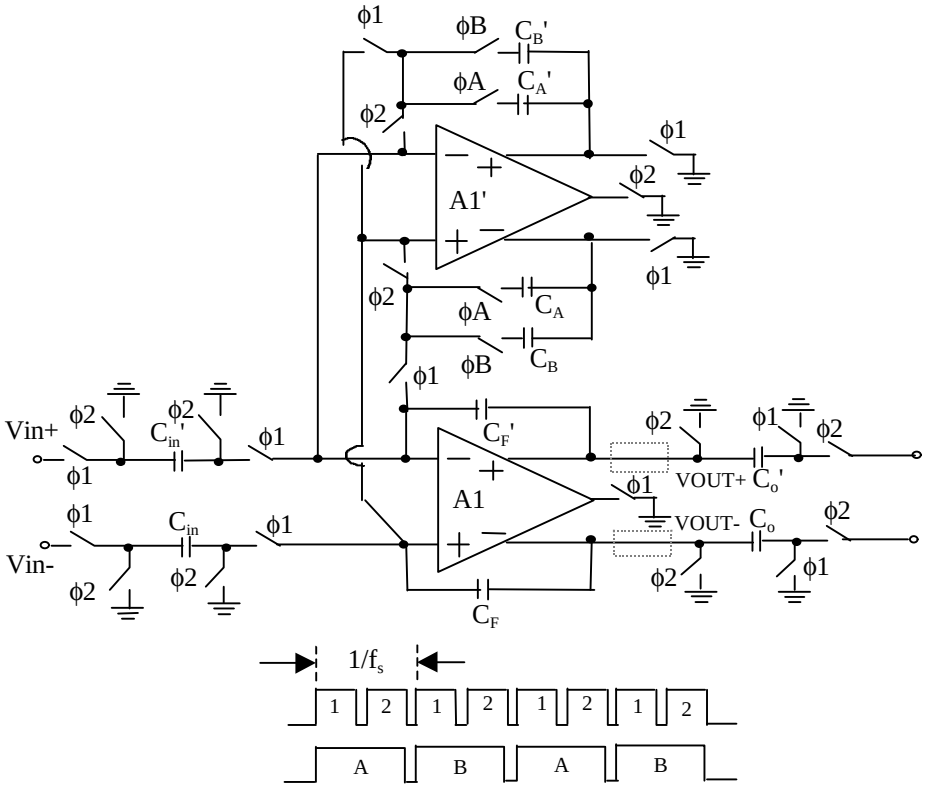


Fig. 4.6 Differential switched-opamp RAM-type pseudo-2-path transformed integrator

Again, C_F (C_F') is the integrating capacitor, C_A (C_A') and C_B (C_B') are the capacitors of the storage array. When phases ϕA and ϕ1 are on, A1' is turned off with its outputs shorted to Vdd. Capacitor C_F (C_F') receives the charge from the input capacitor C_{IN} (C_{IN}') and from the storage capacitor C_A (C_A') which is in the opposite path. This operation gives the sign inversion required by the z to -z transformation. During phase ϕ2, opamp A1' is turned on while A1 is turned off with its output shorts to Vdd. In this way, the updated charge in C_F (C_F') is transferred back to the storage capacitors C_A (C_A'). This charge is then held in C_A (C_A') for two sampling periods. The same operation is repeated during phase ϕB with the charge stored on C_B (C_B') instead of C_A

(C_A'). By doing so, z to $-z^N$ transformation is resulted with the modified switched-opamp technique. Notice that all MOS switches have their sources connected directly or virtually to ground or Vdd, this ensures the proper operation of MOS switches in the system.

4.5 The Design of Switchable Opamp

To optimize the modified switched-opamp technique, a suitable design of switchable-opamp is valuable. The idea comes from the fact that in the modified switched-opamp technique, the input terminals of the two switchable-opamps A1 and A1' are shorted together, while only one of the two opamps is on at a time. As such, it is useful to share the input stage of the two switchable-opamps. This results in the design of an amplifier with differential inputs and two pairs of differential outputs that are turned on and off alternatively (Details can be found in Chapter 5 section 5.1). For easy discussion in later sections, a symbol is created to represent the fully differential two-output-pairs opamp as shown in Fig. 4.7. Note that the fully differential opamp has embedded with a dynamic common-mode feedback, which will be covered in Chapter 5 section 5.3.

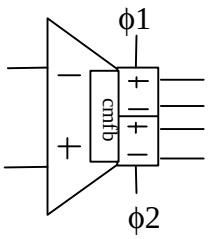


Fig. 4.7 Symbol for the fully-differential two-output-pairs switchable amplifier

Figure 4.8 shows the switched-opamp RAM-type pseudo-2-path integrator using the full-differential two-output-pairs switchable opamp. The operation of this switched-opamp pseudo-2-path integrator is similar to the one described in section 4.3 that uses two switchable opamps to work in parallel, and hence it is not repeated here. The basic difference is that the two switchable opamps are replaced by two pairs of switchable output-stages instead.

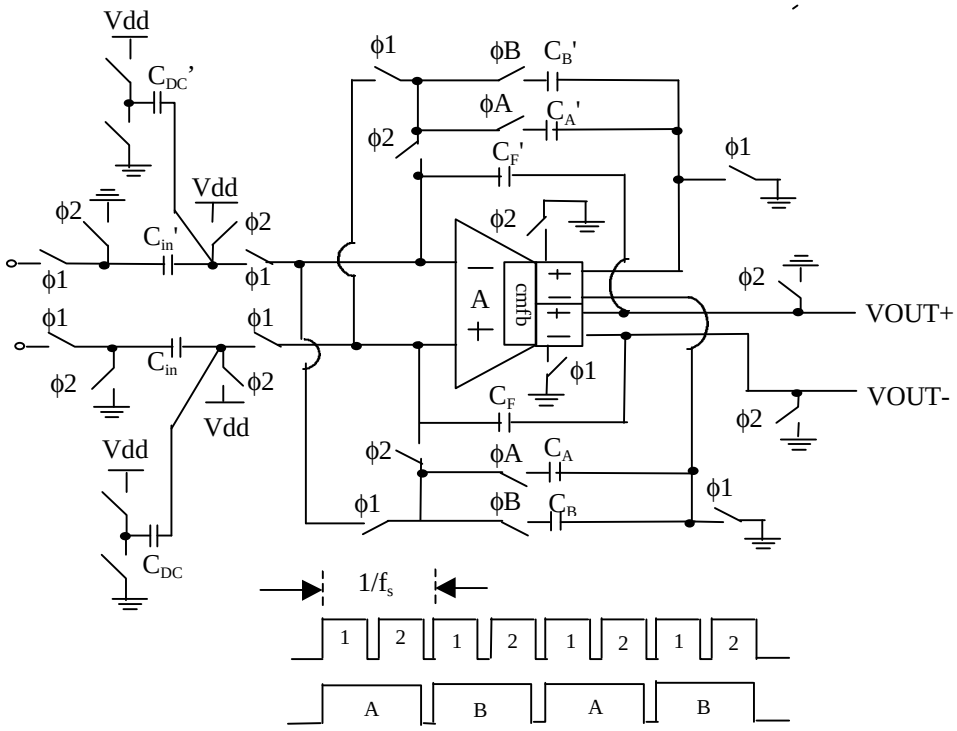


Fig. 4.8 Differential switched-opamp RAM-type pseudo-2-path transformed integrator using full-differential two-output-pairs switchable opamp

By removing all the problematic switches at the output of all opamps of the pseudo-2-path filter in Fig. 3.13 and replacing the integrators with the switched-opamp RAM-type pseudo-2-path transformed integrators, a switched-opamp pseudo-2-path filter is implemented as shown in Fig. 4.9. Table 4.1 summarizes the capacitors' size used.

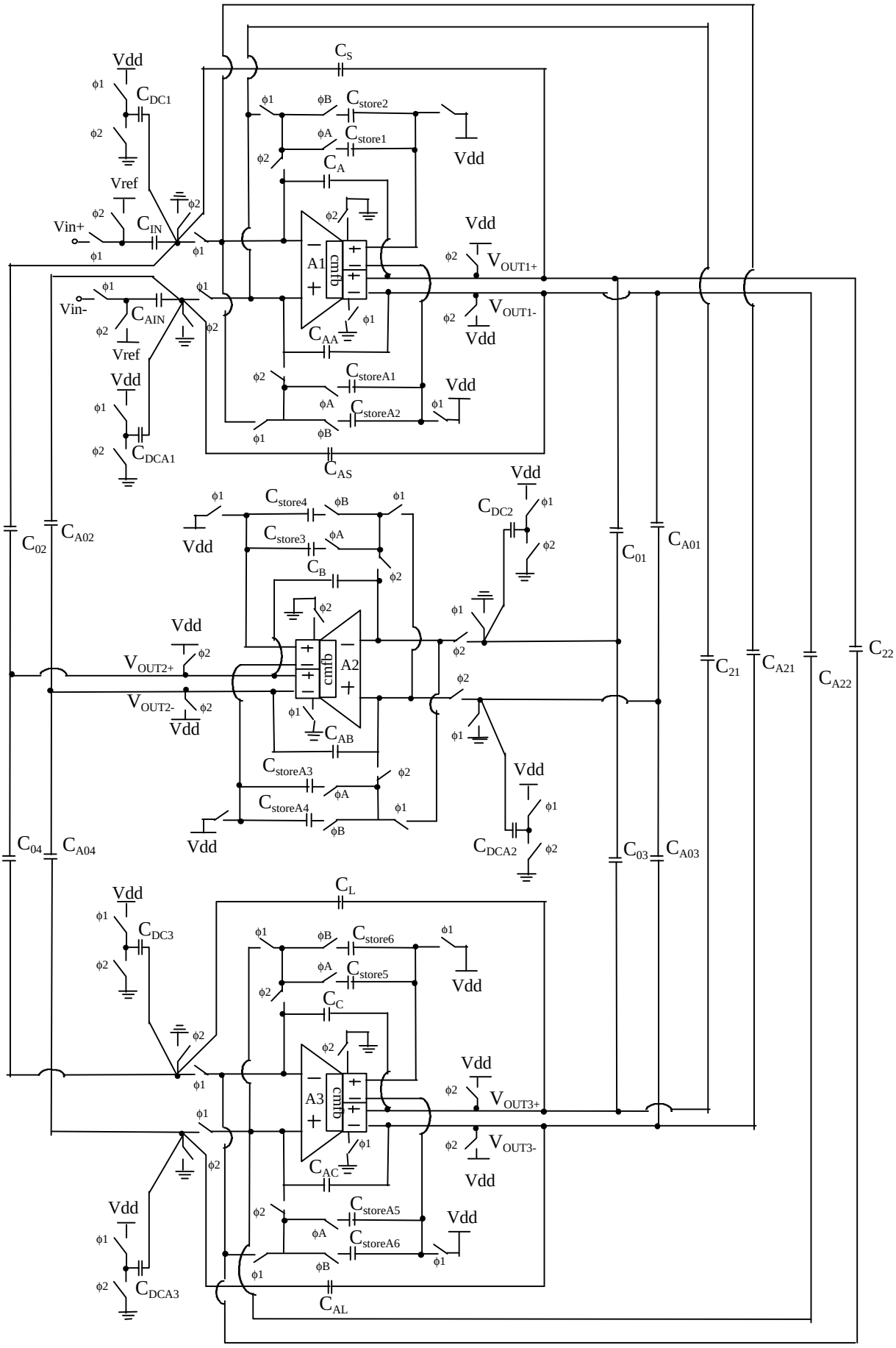


Fig. 4.9 SC Pseudo-2-path filter using modified switched-opamp technique

Table 4.1 Summary of capacitors' size of switched-opamp pseudo-2-path filter

Capacitors	**Size**
C_A, C_{AA}, C_{store1}, $C_{storeA1}$, C_{store2}, $C_{storeA2}$	4.5pF
C_B, C_{AB}, C_{store3}, $C_{storeA3}$, C_{store4}, $C_{storeA4}$	5pF
C_C, C_{AC}, C_{store5}, $C_{storeA5}$, C_{store6}, $C_{storeA6}$	3.5pF
C_{IN}, C_{AIN}	0.588pF
C_S, C_{AS}	0.1454pF
C_{02}, C_{A02}	0.1pF
$C_{DC1} = (C_S+C_{02})/2$, $C_{DCA1}= (C_{AS}+C_{A02})/2$	0.1707pF
C_{01}, C_{A01}	0.152pF
C_{03}, C_{A03}	0.1pF
$C_{DC2} = (C_{01}+C_{03})/2$, $C_{DCA2} = (C_{A01}+C_{A03})/2$	0.126pF
C_{04}, C_{A04}	0.1048pF
C_L, C_{AL}	0.1pF
$C_{DC3} = (C_L+C_{04})/2$, $C_{DCA} = (C_{AL}+C_{A04})/2$	0.1024pF
C_{21}, C_{A21}	0.133pF
C_{22}, C_{A22}	0.212pF

A switched-opamp model is created for simulations with SWITCAP2, the frequency response and the passband characteristics are shown in Fig. 4.10 and Fig. 4.11 respectively.

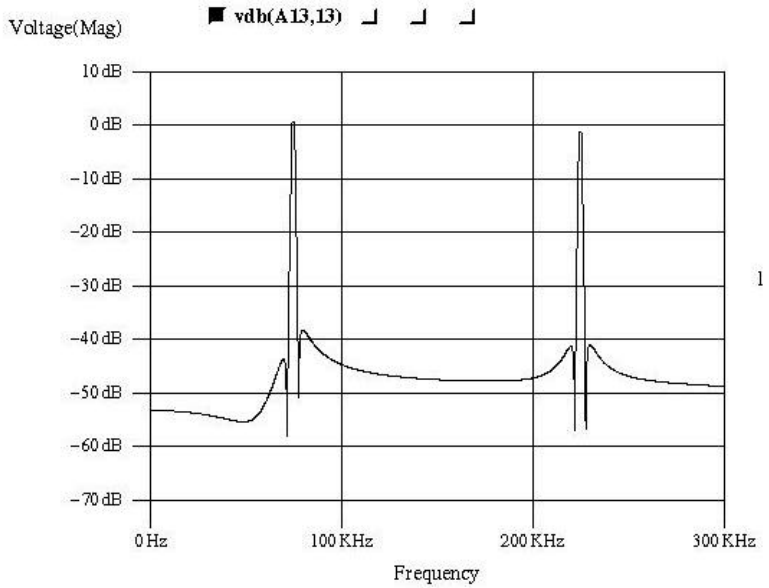


Fig. 4.10 Frequency response of the switched-opamp pseudo-2-path filter

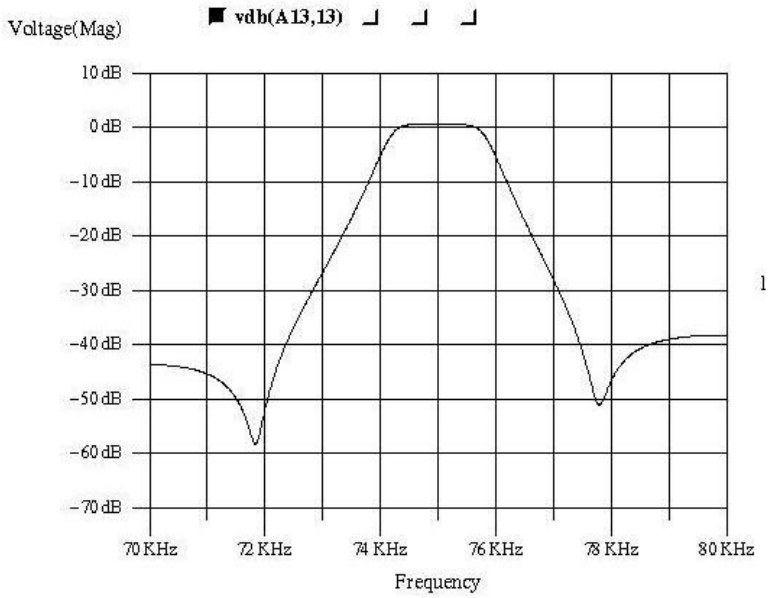


Fig. 4.11 Passband characteristics of the switched-opamp pseudo-2-path filter

The frequency response of the switched-opamp pseudo-2-path filter is basically the same as that obtained in the switched-capacitor implementation. As expected, a reduction of 3dB passband gain is resulted due to the sample-and-hold comb-response effect as discussed in section 3.2. However, a 6dB passband gain reduction is experienced in the switched-opamp system due to the existence of the return-to-zero effect, which is caused by the fact that the outputs of opamps are shorted to Vdd after the integrating phase. Hence the overall passband gain is reduced to about 1dB, though the lowpass path-filter is designed to have a gain of 10dB. Table 4.2 summarizes the switched-opamp pseudo-2-path filter characteristics.

Table 4.2 Summary of switched-opamp pseudo-2-path filter characteristics

Parameters	**Simulation Results**
Center Frequency	75kHz
Passband Bandwidth	1.5kHz
Passband Gain	1dB
Stopband Gain	-40dB
Filter Order	6
No. of switchable Opamps	3
Capacitance Spread	50
Sampling Frequency	300kHz

To sum up, a modified switched-opamp technique is proposed to operate switched-capacitor circuits in a single voltage supply as low as 1V in standard CMOS process. This is illustrated through the implementation of a 1-V switched-capacitor pseudo-2-path filter. The passband gain reduction due to the return-to-zero effect must be taken into account when the switched-opamp technique is applied. In next chapter, the transistor level implementations of the 1-V SC pseudo-2-path filter will be presented.

Reference

[1] R. Castello, F. Montecchi, F. Rezzi and A. Baschirotto, "Low-Voltage Analog Filters", *IEEE Transactions on Circuits and Systems – I: Fundamental Theory and Applications*, Vol. 40, No. 11, Nov. 1995, p.827-840

[2] V. Peluso, J. Bastos, P. Kinget and W. Sansen, "Custom Analog Low Power Design: The Problem of Low Voltage and Mismatch", *Proceeding of the IEEE 1997 Custom Integrated Circuits Conference*, April 1997, p.285-292

[3] A. Baschirotto, R. Castello and F. Montecchi, "Design Strategy for Low-Voltage SC Circuits," *Electronics Letters*, Vol. 30, No. 5, March 1994, p378-380

[4] R. Castello and L. Tomasini, "1.5-V High-Performance SC Filters in BiCMOS Technology," *IEEE Journal of Solid-State Circuits*, Vol. 26, No. 7, July 1991, p.930-936

[5] C. Y. Wu, W. S. Wey and T. C. Yu, "A 1.5V CMOS Balanced Differential Switched-Capacitor Filter with Internal Clock Boosters," *IEEE International Symposium on Circuits and Systems*, Vol. 2, May 1995,

pp.1025-8

[6] J. Steensgaard, "Bootstrapped Low-Voltage Analog Switches", *Proceeding of the IEEE International Symposium on Circuits and Systems*, Vol. 2, p.29-32

[7] M. Dessouky and A. Kaiser, "Rail-To-Rail Operation of Very Low Voltage CMOS Switched-Capacitor Circuits", *Proceeding of the IEEE International Symposium on Circuits and Systems*, Vol. 2, p.144-147

[8] J. Crols and M. Steyaert, "Switched-Opamp: An Approach to Realize Full CMOS Switched-Capacitor Circuits at Very Low Power Supply Voltages", *IEEE Journal of Solid-State Circuits*, Vol. 29, No. 8, August 1994, p.936-942

[9] V. Peluso, M. Steyaert and W. Sansen, "A 1.5-V-100μW ΔΣ Modulator with 12-b Dynamic Range Using the Switched-Opamp Technique", *IEEE Journal of Solid-State Circuits*, Vol. 32, No. 7, July 1997, p. 943-952

[10] A. Baschirotto and R. Castello, "A 1-V 1.8MHz CMOS Switched-Opamp SC Filter with Rail-to-Rail Output Swing", *IEEE Journal of Solid-State Circuits*, Vol. 32, No. 12, Dec. 1997, p.1979-86

[11] V. Peluso, P. Vancorenland, A. M. Marques, M. Steyaert and W. Sansen, "A 900-mV Low-Power ΔΣ A/D Converter with 77-dB Dynamic Range", *IEEE Journal of Solid-State Circuits*, Vol. 33, No. 12, Dec. 1998, p.1867-97

Chapter 5

Transistor Level Implementation of a 1-V SC Pseudo-2-Path Filter

While the proposed switched-opamp technique eliminates all the problematic switches in the SC circuits, a high-gain fast-settling switchable opamp that can be operated in a single 1-V supply is required. For very low voltage operation, multi-stage amplifier approach [1][2] (by cascading gain stages to obtain high gain) is more attractive than using cascode topology [3] (by cascoding transistors to obtain high output resistance for high gain), which is usually applied in classical SC circuits. The latter one provides too small effective output dynamic range due to its cascode structure at the output stage. Meanwhile, the former one gives a high amplification with only two transistors in the output stage, which delivers the maximal possible signal swing. The difference here becomes significant when the power supply voltage is reduced to 1-V. This is because every transistor that is cascoded in the output stage would reduce the maximum dynamic range by more than 10%. In this chapter, the design issues and implementation of a 1-V fully-differential two-output-pair switchable amplifier that bases on a two-stage amplifier approach are discussed. The HSPICE simulation results of a 1-V SC pseudo-2-path filter that utilizes the switchable amplifier are presented.

5.1 Opamp Specifications and Justifications

Most of the specifications of the opamp are chosen according to the requirements of the 1-V SC pseudo-2-path filter. Table 5.1 summarizes the performance requirements of the switchable opamp.

Table 5.1 Summary of opamp specifications

Parameters	**Specifications**
Supply Voltage	Single 1V
Low Frequency Gain	> 75dB
Unity-Gain Frequency	> 5MHz
Phase Margin	> 60°
Output Swing	> 0.8V
Settling Time	< 250n sec
Slew Rate	> 1.2V/μ sec
Input Offset Voltage	< 5mV
Load Capacitor	4pF
Power Consumption	< 100μW
Turn-On/Turn-Off Time	< 167n sec

Voltage supply & power consumption: The opamp should operate at a single 1-V supply for the 1-V SC pseudo-2-path filter. For portable applications, the opamp is designed to dissipate less than 100μW such that the filter, which consists of 3 opamps, consumes no more than 300μW.

Low-frequency gain and phase margin: The low frequency gain of the opamp must be high enough to preserve the filter transfer function accuracy, especially for high Q filter

implementation. Simulation results from SWITCAP2 show that a low frequency gain of more than 75dB is required. For stability issue, the phase margin should be larger than 60° as the opamps are connected in feedback.

Unity gain frequency: The unity gain frequency is chosen based on the settling time requirement and to minimize filter transfer function sensitive to the opamp gain-bandwidth. In general, the larger the unity gain frequency, the shorter the opamp settling time and the more accurate the filter transfer function. However, too large the unity gain frequency creates serious noise aliasing effect in the SC system. In fact, to avoid excessive noise aliasing effect while preserving the filter transfer function, the unity gain frequency is generally set to be about 5 to 10 times larger than the sampling frequency in most of the switched-capacitor filters [4]. In our case, the required unity gain frequency of the opamp is 10x300kHz = 3MHz. This is the requirement of a classical switched-capacitor circuit that uses a sampling frequency of 300kHz. For any SC circuits that utilize switched-opamp technique, the unity-gain frequency should be made larger to reserve more time for turning on the switchable opamps. Here, a unity gain frequency of 6MHz is chosen.

Settling time: The settling time is set to be less than 1/3 of the sampling period (555nsec) with an accuracy of 0.1%. This can be achieved if the time constant of the opamp τ is smaller than 555nsec/7 = 106nsec [4]. In general, the settling time is dependent on the –3dB bandwidth, which in turn depends on the unity-gain frequency and the closed-loop gain of the opamp, and

hence it may be configuration dependent. This is because, for some opamp configurations like the folded-cascode amplifier, their unity-gain frequencies depend strongly on the load capacitance. As a result, the settling time for these amplifiers will also depend on the equivalent load capacitance when it is capacitively fed-back (usually happens in switched-capacitor and Gm-C applications). However, for classical two-stage opamps, the unity-gain bandwidth mainly depends on the compensation capacitor but not on the load capacitor, hence it is unnecessary to take into account the equivalent load capacitance to calculate the settling time in this case.

Slew rate: Sine the opamp is used to implement a switched-opamp filter with sampling frequency (switching frequency) *fc* of 300kHz with the highest signal passband w_B and signal swing V_{swing} of 75kHz and 0.8V respectively. Then the sampling time T_{sample} is found to be 1/2*fc* = 1.67u sec. According to the switched-opamp operation principle, the output voltage must reach its final value within the sampling time since the opamp will be off after the sampling phase. This can be achieved only if the total amount of time for turning on the opamp plus the slew time t_{slew} plus the settling time t_{settle} is less than the sampling time, as described in Equation 5.1:

$$T_{switching\_on} + T_{slew} + T_{settle} < T_{sampling} = \frac{1}{2 f_s} \qquad \text{(Eq. 5.1)}$$

The slew time is determined by the slew rate of the opamp and the output voltage $V_{out}t(t)$ change $\Delta V_{out} = V_{out}(nT)-V_{out}(nT-T)$ that must undergo in each step, as defined in Equation 5.2:

$$T_{slew} = \frac{\Delta V_{out}}{SR} \qquad \text{(Eq. 5.2)}$$

It is no doubt that the largest step ΔV_{out} occurs when the highest passband frequency signal is under processing. In the worst case, $V_{out(t)}$ will be a sampled-and–held sine wave with a frequency w_B and a sampling time T_{swing}. This is actually a result of sampling and holding a continuous time voltage $V(t)=V_{swing}\sin w_B t$. Hence the maximum step which $V_{out}(t)$ must take every $T=1/fs$ seconds is given by Equation 5.3:

$$\Delta V_{out,mzx} = T\left|\frac{dV(t)}{dt}\right|_{\max} = \frac{\omega_B V_{swing}}{f_s} \; where T = \frac{1}{f_s} \qquad \text{(Eq. 5.3)}$$

Let x be the allowed portion of T_{hold} for slew time, we have the slew rate requirement given by Equation 5.4:

$$SR \geq \frac{V_{out.\max}}{T_{slew}} \approx \frac{\omega_B V_{swing}}{x f_s T_{hold}} = \frac{2\omega_B V_{swing}}{x} \qquad \text{(Eq. 5.4)}$$

In our case, x=10%, V_{swing}=0.8V, w_B=75kHz, this requires a slew rate of 1.2V/μsec. Note that this slew rate requirement has to be fulfilled for each of the compensation capacitor that exists in the circuit. There are of course also signals of higher frequencies than w_B present internally in the SC circuit. However, they and their harmonics fall into the stopband of the SC filter, and hence the resulting distortion will normally not affect the output signal of the whole circuit.

CMRR, PSRR and noise consideration: Fully differential architecture is used to increase CMRR, PSRR and minimize the noise problem. Meanwhile**, t**he noise performance of a 2-stage

opamp can be improved by making a better noise performance for the first stage, given that the first stage gain is high. This is because the noise generated by later stages will be divided by the gain of the first stage when it is transferred back to calculate the equivalent input voltage noise. To achieve better CMRR, the input stage can be implemented with a differential pair, which ideally has a common-mode gain of zero. At low frequencies, the supply noise that can be coupled to the output is mainly due to variation in bias circuits and mismatches in differential structures. At high frequencies, coupling from parasitic capacitors becomes more important. To reduce the noise gain due to the parasitic capacitors, it is desirable to maximize the input and feedback capacitors and to minimize the parasitic capacitors by employing good layout techniques.

Turn-on time of switchable opamp: 20% (335nsec) of the sampling time is allocated for the opamp to turn on from off state. While looking for fast switching time, the power consumption should be minimized.

5.2 Opamp Design and Operation Principle

Figure 5.1 shows the schematic of the proposed 1-V fully-differential two-output-pair switchable opamp. The opamp is implemented with HP 0.5μm CMOS N-well process with NMOS and PMOS threshold voltages of 0.7V and 0.85V respectively. A PMOS differential pair is used as the input stage for smaller Flicker noise [5][6].

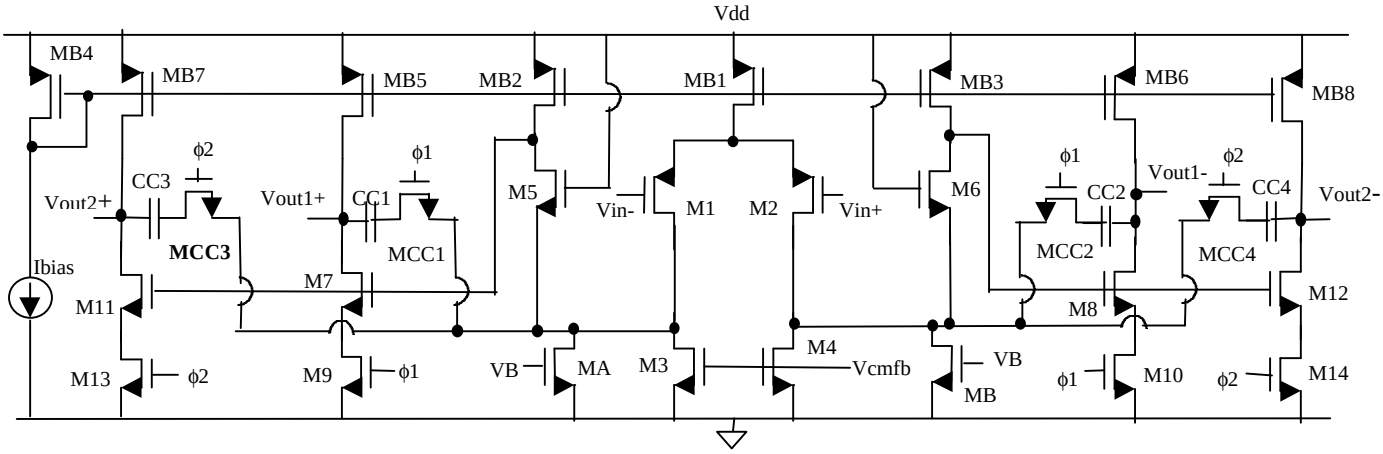


Fig. 5.1 Schematic of a fully differential two-output-pair switchable opamp

To cope with the already tight voltage budget, the body effect that tends to increase the threshold voltage of the PMOS input transistors has to be eliminated by connecting the PMOS bodies to their sources. This is possible in N-well process when the PMOS input transistors are laid-out with a separate N-well from other PMOS transistors.

In order to obtain a low frequency gain of better than 75dB to maintain the filter transfer function accuracy, this is necessary to ensure that both input (M1 and M2) and load (M3 and M4) transistors operate in saturation region. Therefore, the gates of output stage transistors (M7, M8, M11 and M12) are not connected directly to the output nodes of the input stage as in the case of conventional two-stage opamp configuration. Instead, level shifters formed by M5, MB2 and M6, MB3 respectively are inserted in between such that M3 and M4 are biased with one V_{DSsat} higher than ground while ensuring M1 and M2 operate in saturation region [7][8]. Capacitors CC1, CC2, CC3 and CC4 are compensation capacitors for the two pairs of output stages. The output stages are turned on and off by the transistors M9, M10, M13 and M14,

which are controlled by the two non-overlapping clock phases $\phi 1$ and $\phi 2$. When the output stages are cut-off, compensation resistors MCC1 and MCC2 (or MCC3 and MCC4) are turned off to prevent the compensation capacitors from discharging or charging up for faster switching operation. Since the switches that connect at the outputs of opamps in the proposed 1-V SC pesudo-2-path filter are tied to Vdd when the output stages are in off phase, thus preventing static current from flowing through those switches and the output stages.

A dynamic common-mode feedback circuitry (will be explained in next section) can adjust the output common-mode voltages to 0.5V (middle of rails) by negatively feeding back signal to the gates of transistors M3 and M4. Transistors MA and MB are used to adjust the common-mode feedback loop-gain by drawing currents from M3 and M4 respectively. As such the transconductance of M3 and M4 can be adjusted. Table 5.2 summarizes the transistor sizes of the proposed switchable opamp.

Table 5.2 Summary of transistors sizes of switchable opamp

Transistors	Unit size	Quantity
M1, M2	12μ/2.1μ	12
M3, M4	3μ/3μ	12
MA, MB	3μ/3μ	20
M5, M6, M7, M8, M11, M12	3.3μ/2.1μ	20
MB4	10.2μ/2.1μ	4
MB1	10.2μ/2.1μ	24
MB2, MB3, MB5, MB6, MB7, MB8	10.2μ/2.1μ	20
M9, M10, M13, M14	3.3μ/2.1μ	8
MCC1, MCC2, MCC3, MCC4	5.1μ/0.6μ	10

It is worth to mention that, with a single 1-V supply, the input common-mode voltage of the switchable opamp has to be set at ground, which results in zero input common-mode range. But this is not critical to the operation of SC circuits, since the inputs of opamps are operating near the virtual ground in steady state, therefore no input common-mode range is required.

5.3 Simulation Results of the 1-V Switchable Opamp

The proposed fully differential two-output-pair switchable opamp is simulated with Hspice using HP 0.5μm CMOS model. Figure 5.2 shows the frequency response of the switchable opamp. The DC gain is 81.8dB with a unity gain frequency of 7.5MHz. The phase margin is 54°.

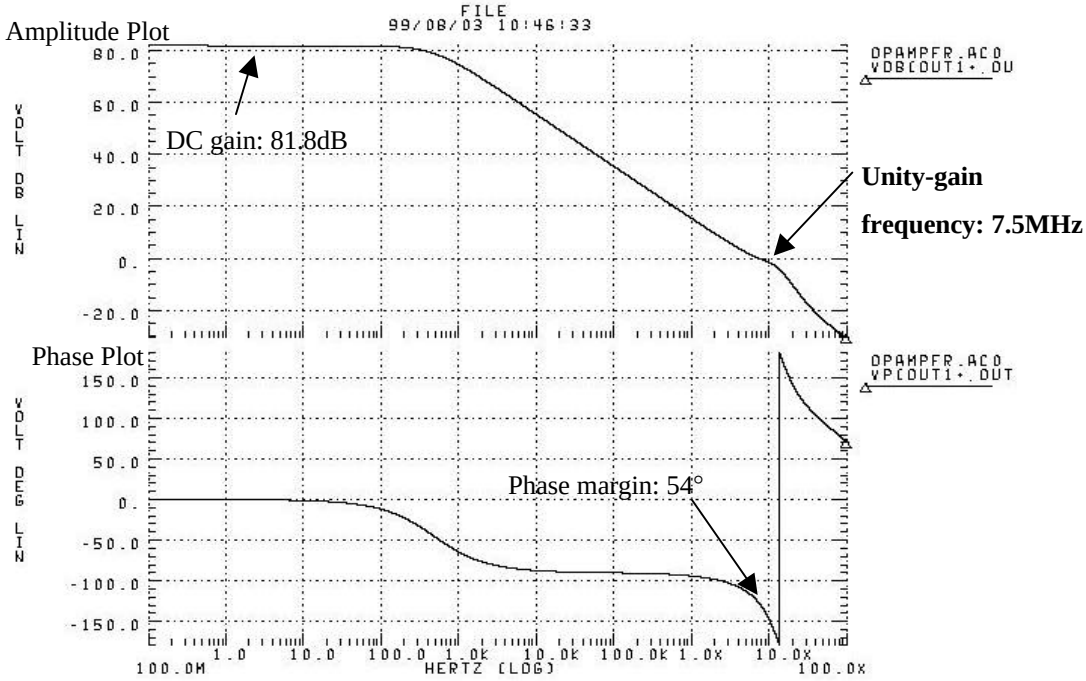


Fig. 5.2 Frequency response of the fully differential two-output-pair switchable opamp

The test circuits for simulating the settling time for a switched-capacitor filter is shown in Fig. 5.3 [4]. The feedback C_F and input capacitors C_I are chosen to be 3pF, C_P (0.2pF) is the parasitic capacitance while C_L (1pF) is the loading capacitance. This is the SC integrator configuration in the SC pseudo-2-path filter that has the largest time constant.

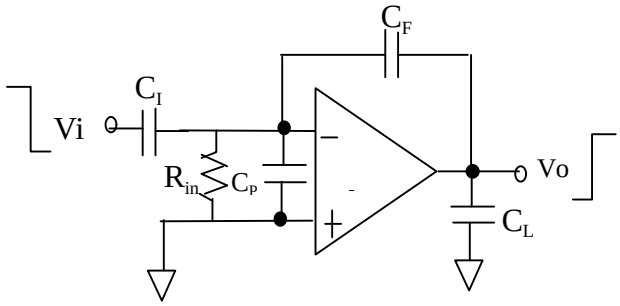


Fig. 5.3 Testing circuit for settling time measurement of SC integrator

In this case, the output node will experience the same step voltage that appears at the input node. The time constant of the integrator can be estimated as:

$$\tau = \frac{1}{\omega_{-3dB}} = \frac{1}{A_f \omega_o}$$
$$A_f = \frac{C_F}{C_F + C_I + C_P} \qquad \text{(Eq. 5.5)}$$

Obviously, the -3dB frequency of the system depends on the feedback factor. In general, CF >> CP and CF≈CI for SC pseudo-2-path filter, therefore $A_f \approx 0.5$. As a result, the time constant can be estimated as:

$$\tau \approx \frac{2}{\omega_o} \qquad \text{(Eq. 5.6)}$$

In order to achieve a settling error of less than 0.1%, a settling time of 7τ is required, this is

estimated to be 300nsec (10% of the sampling period) for a unity gain frequency of 7.5MHz. The simulated settling time is about 350nsec.

The test circuit for checking slew rate of the opamp is shown in Fig. 5.4.

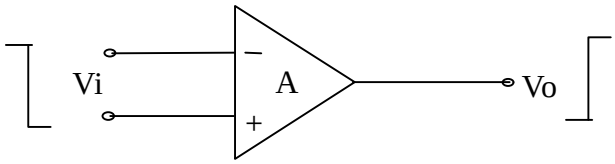


Fig. 5.4 Test circuit for opamp slew rate measurement

Since the DC operating point of the input terminals and the outputs of opamp are different, the opamp cannot be connected in unity-feedback configuration for slew rate measurement. Instead, a step voltage is applied to directly to observe the rise and fall times of the response at the outputs. Figure 5.5 shows the simulation results.

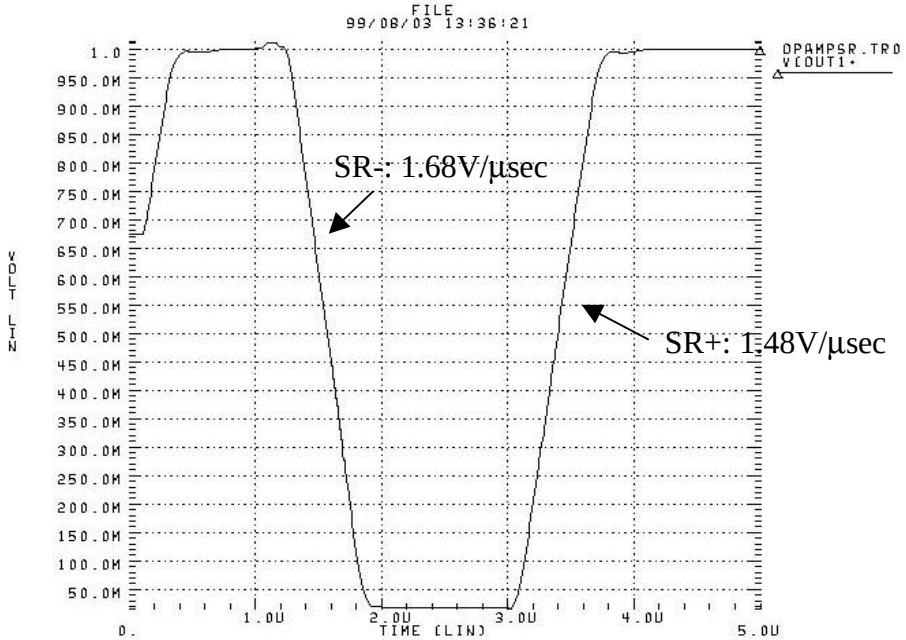


Fig. 5.5 Slew rate measurement of the switchable opamp

The simulated slew rate of the opamp is 1.68V/μs with a positive input triggering step and 1.48V/μs with a negative input-triggering step. With the worst case slew rate, the slew time is 470nsec (about 1/6 of the sampling time) for a maximum signal step of 0.7V.

The noise performance of the amplifier can be determined by analyzing the noise performance of the first gain stage, given that the first stage gain is high (~100). This is because the noise generated by output stages will be divided by the gain of the first stage when it is transferred back to calculate the equivalent input voltage noise. Take into account the thermal noise and flicker noise in the analysis, the noise generated by the first gain stage (differential pair) can be derived as shown in Equation 5.7:

$$\overline{V_{IT}^{\,2}} = \left(\overline{V_{eq1}^{\,2}} + \overline{V_{eq2}^{\,2}}\right) + \left(\frac{gm_{3-4}}{gm_{1-2}}\right)^2 \left(\overline{V_{eq3}^{\,2}} + \overline{V_{eq4}^{\,2}}\right) \qquad \text{(Eq. 5.7)}$$

where

$$\overline{V_{eqi}} = 4KT\frac{2}{3gm}\Delta f + \frac{Kf}{WLCox^2}\frac{\Delta f}{f} \qquad \text{(Eq. 5.8)}$$

It can be easily observed from Equation 5.8 that the white noise (thermal noise) component is inversely proportional to transconductance of the MOS transistors (gm α W/L) while the flicker noise is inversely proportional to the gate area (W*L). As a result, these two noise components can be optimized separately. For better noise performance, PMOS transistors should be used as the input devices as it has lower flicker noise coefficient (Kf) [5] [6]. The

calculated total input referred noise (with no flicker noise) is 76nV/√Hz. The calculated result agrees very well with the simulation result (77.4nV/√Hz). Since the flicker noise coefficients have not be obtained, no hand calculation can be done. Meanwhile, the input transistor gate areas are made reasonably large to minimize the flicker noise.

The input offset voltage of the opamp is determined by estimating the offset voltage due to the first gain stage, given that the first stage gain is high (~100). This is because the offset generated by later stages will be divided by the gain of the first stage when it is transferred back to calculate the total input offset voltage. The analysis is thereby the same as that for a differential pair and therefore the estimated offset voltage of the switchable opamp is given by Equation 5.9:

$$V_{os} = \Delta V_{TP} + \Delta V_{TN}\left(\frac{gm_3}{gm_1}\right) + \frac{\left(V_{GS_p} - V_{TP}\right)}{2}\left[-\frac{\Delta(W/L)_p}{(W/L)_p} - \frac{\Delta(W/L)_n}{(W/L)_n}\right] \quad \text{(Eq. 5.9)}$$

Assume that, for standard CMOS technology, the worst case mismatch for active devices is 3% and that of the threshold voltage is 2mV for a good layout technique. The offset voltage is found to be 7mV. To reduce the offset voltage, low V_{GS}-V_T should be used for M1 and M2 to reduce the geometry mismatch effect while making gm_1>>gm_3 to reduce V_T mismatch. Table 5.3 summarizes the specifications and simulation results of the fully differential two-output-pair switchable opamp:

Table 5.3 Summary of simulation results of the switchable opamp

Parameters	**Specifications**	**Pre-Simulation Results**
Low frequency gain	> 75dB	81.4dB
Unity gain frequency	> 7MHz	7.5MHz
Phase margin	> 60°	54°
Power consumption	< 100μW	63.8μW
Supply voltage	1V	1V
Settling time	< 300nsec	350nsec
Slew rate	> 1.2V/μsec	(+ SR) 1.53V/μsec (- SR) 1.65V/μsec
Output swing	0.7V	0.75V
Input offset voltage	< 10mV	7mV (calculated)
Equivalent input noise	NA	31.6nV/√Hz
Loading capacitor	4pF	4pF
Switching time	< 300nsec	290nsec

5.4 SC Dynamic Common-Mode Feedback

For fully differential topology, an additional common-mode feedback circuit (CMFB) is required to control the opamp outputs dc voltage. This can be done using continuous-time or sample-domain approach. For a continuous-time solution, the key problem is due to the fact that the inputs of the CMFB circuit must be dc-connected to the opamp output nodes that are located around Vdd/2 [9][10]. For supply voltage as low as 1-V, Vdd/2 is lower than threshold voltages of transistors, thus continuous-time solution is not viable. For sample-domain approach, a dynamic CMFB circuit can be used [7][8]. The proposed CMFB circuit that is

suitable for the fully-differential two-output-stage switchable opamp is shown in Fig. 5.6.

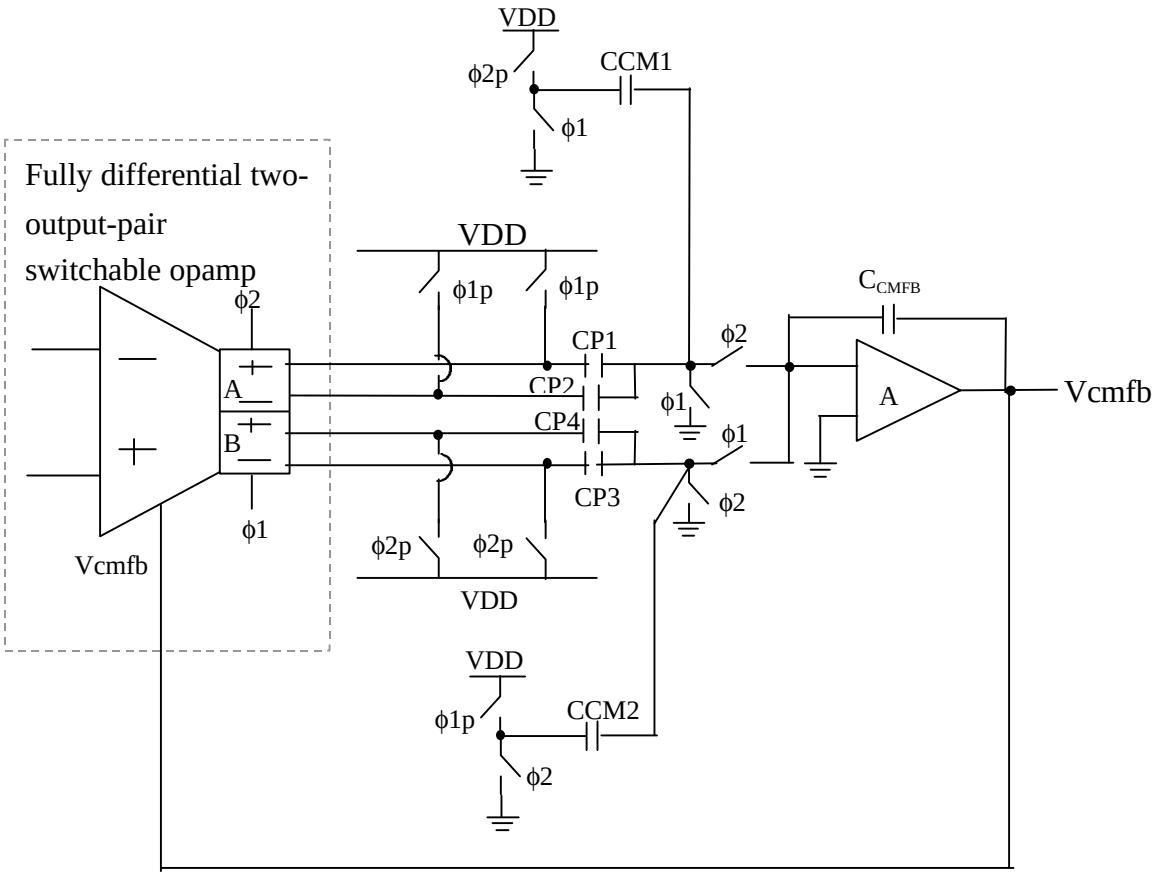


Fig. 5.6 Dynamic common-mode feedback circuits for fully differential two-output-pairs switchable opamp

To explain the operation of the dynamic CMFB circuit, let's consider only output pair "A". During phase ϕ1, the output pair "A" is off, and capacitors CP1 and CP2 (CP1=CP2=0.1pF) are charged to Vdd while the capacitor CCM1 is completely discharged. During phase ϕ2, the loop is closed with the output pair "A" turned on, capacitors CP1 and CP2 discharged from Vdd to the DC output voltage of the opamp and thus injecting charge to the capacitor CCMFB (CCMFB = 0.2pF). On the other hand, capacitor CCM1 is charged from ground to VDD and thus collecting charge from capacitor CCMFB. As a matter of fact, the CMFB circuit steady

state occurs during phase ϕ2 when no charge is injected into or collected from the integration capacitor CCMFB. Therefore, with CCM1=CP1=CP2, the opamp output pair "A" common-mode voltage will be forced to Vdd/2 by the common-mode feedback circuit. The output pair "B" common voltage is also set in a similar manner, but using a complementary clock phases. A differential pair is implemented to act as the opamp for the CMFB integrator. The differential pair has a low frequency gain of 120, which is sufficient for proper operation of the dynamic CMFB circuit. Figure 5.7 shows the Hspice simulation result of the proper operation of the dynamic CMFB circuit.

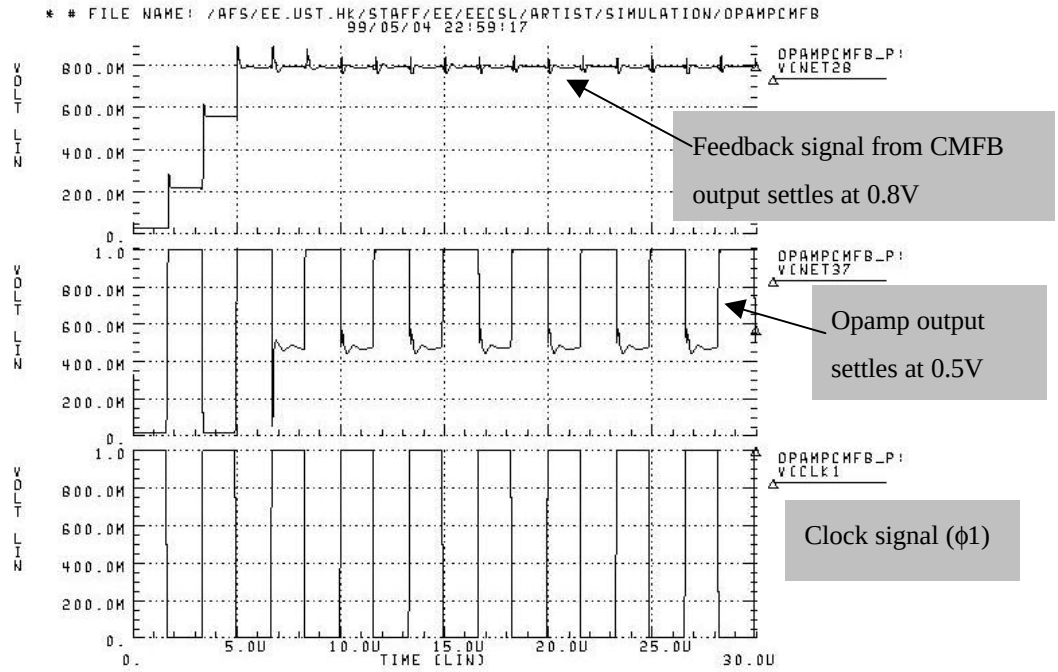


Fig. 5.7 Operation of dynamic CMFB circuit on switchable opamp

It can be observed that all outputs common-mode voltages are settled at 0.5V (Vdd/2) in steady state when the output pairs are turned on. The common-mode feedback voltage settles at

about 0.8V in 600μsec. The output stages can be properly turned off.

5.5 Transistor Level Simulation of the 1-V SC Pseudo-2-Path Filter

The 1-V SC pseudo-2-path filter can then be built with the fully-differential two-output-pair switchable opamp and the dynamic CMFB circuit. Figure 5.8 shows the transient response of the filter without any input signal applied, it can be observed that the outputs of filter settle at 0.5V when that output pairs are turned on.

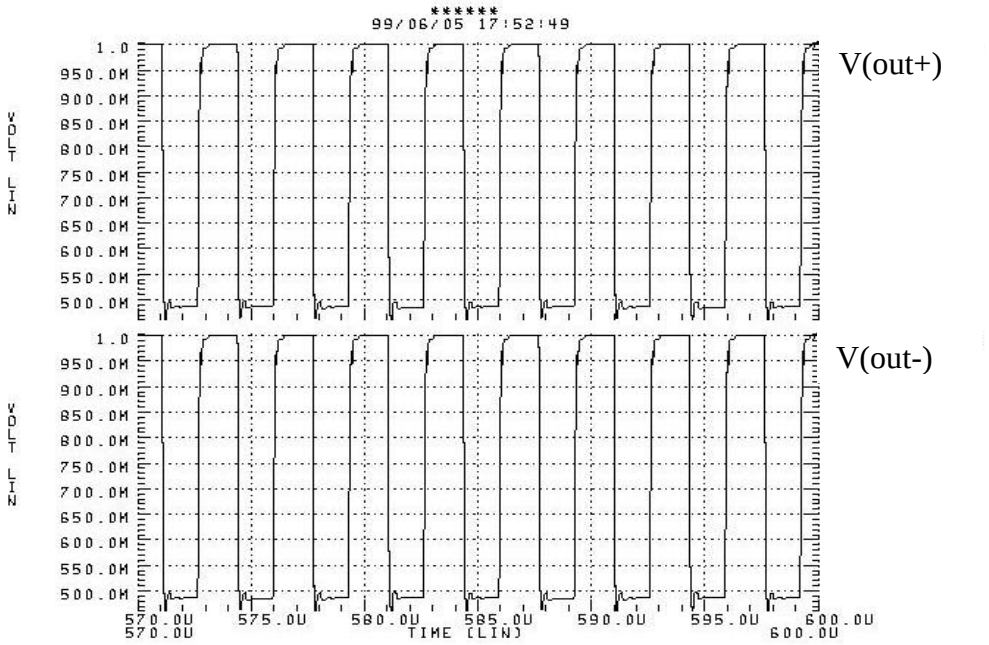


Fig. 5.8 Filter transient response without input signal

With a sampling frequency of 301.2kHz (clock period 3.32μ sec), two transient responses of the filter are obtained and shown in Fig. 5.9 and Fig. 5.10 with 0.3Vpp input signal at 75.3kHz (passband response) and 70kHz (stopband response) respectively.

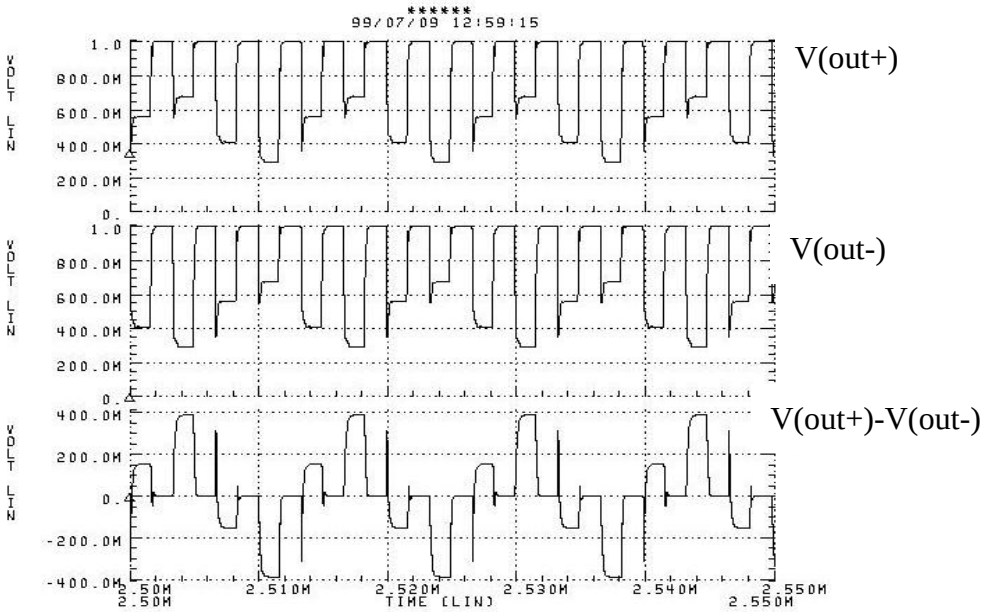


Fig. 5.9 Filter transient response with 0.3Vpp 75.3kHz input signal

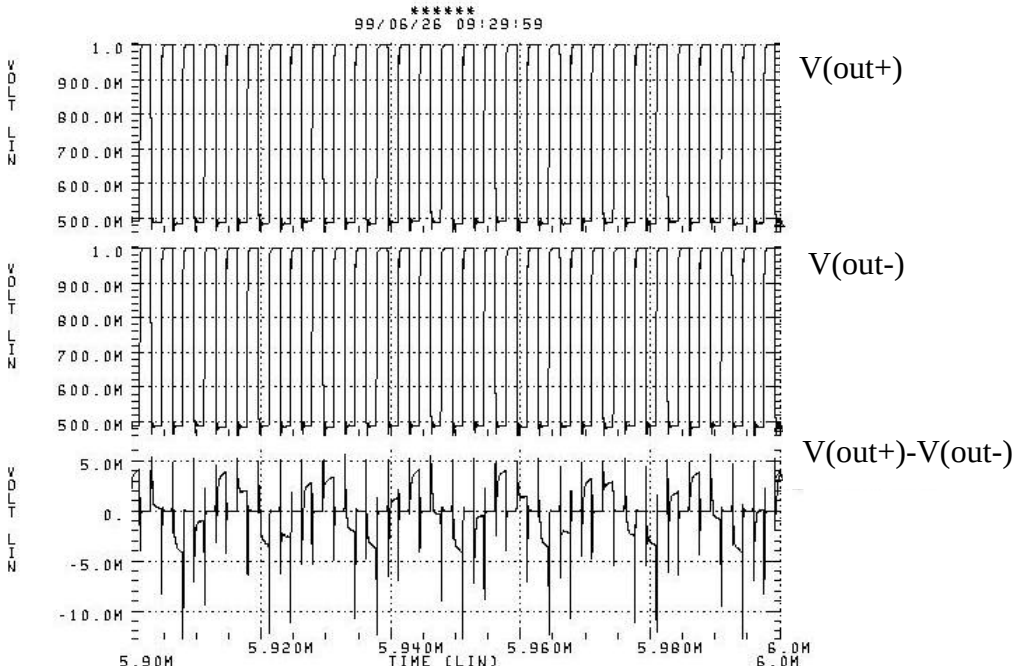


Fig. 5.10 Filter transient response with 0.3Vpp 70kHz input signal

The differential output signal has about 0.9Vpp swing with 75.3kHz input signal. This is due to the 10dB gain of the lowpass path-cell frequency response, though the overall filter

passband gain is about 0dB due to the comb-response effect and the return-to-zero effect in this system. Meanwhile, the output signal is less than 10mVpp in response to a 70kHz input signal, which is in the stopband of the system.

By performing Fast-Fourier-Transformation (FFT) on the transient response, we obtain the frequency spectrum of the output of the filter. Two FFT analysis are performed, one with 75.3kHz 0.3Vpp input signal, another with 70kHz 0.3Vpp input signal, the results are shown in Fig. 5.11(a) and Fig. 5.11(b) respectively.

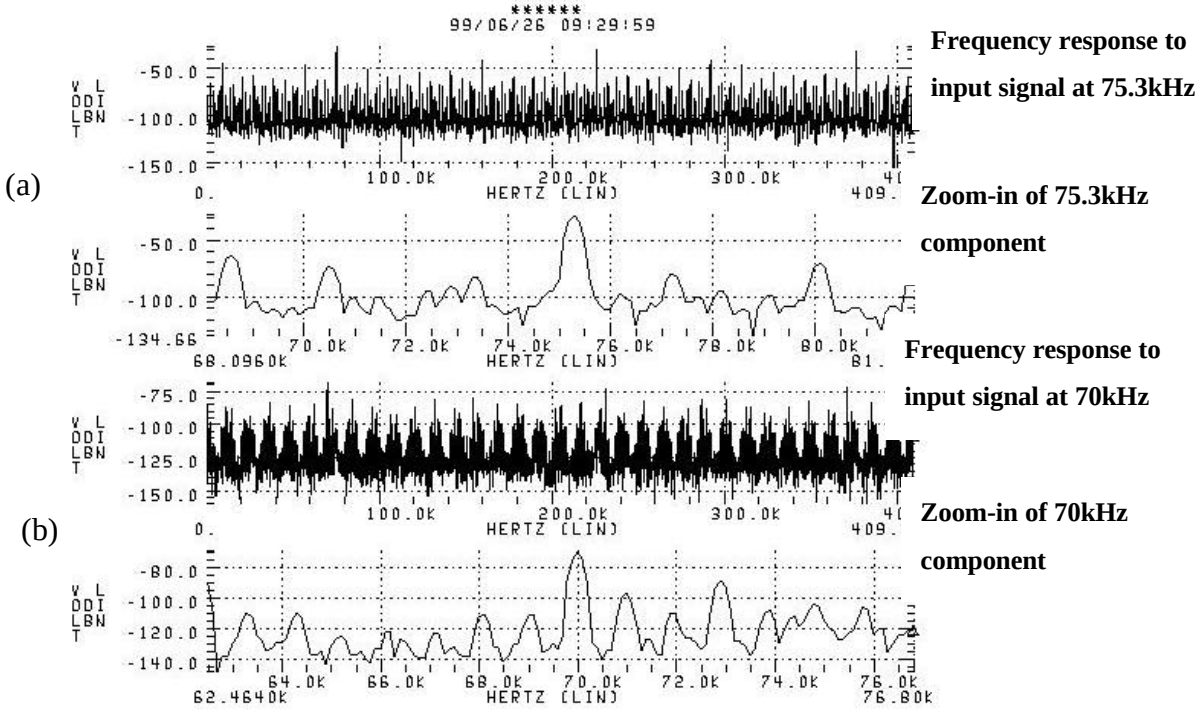


Fig. 5.11 Frequency spectrum of filter to input signal at (a) 75.3kHz, (b)70kHz

As expected, the signal at stopband is attenuated by 40dB relative to the signal at the passband. The –3dB drops are observed from other simulations with input signals of

frequencies 74.5kHz and 76.1kHz are used, this corresponds to a bandwidth of 1.5kHz (Q=50). Table 5.4 summarizes the simulation results of the 1-V SC pseudo-2-path filter.

Table 5.4 Summary of simulation results of the 1-V SC pseudo-2-path filter

Parameters	**Simulation results**
Supply voltage	1V
Center frequency	75.3kHz
Sampling frequency	301.2kHz
-3dB frequency	74.5kHz and 76.1kHz (1.5kHz bandwidth)
Stopband loss	>40dB relative to signal at passband
Power consumption	229μW (63.8μW @ opamp, 12.5μW @ CMFB circuit)
Q-value	50
Capacitance spread	50 (unit capacitor of 0.1pF is used)

5.6 Design and Implementation of On-Chip Buffer

An on-chip buffer is designed to drive capacitor loading up to 100pF for testing purposes. Meanwhile, the input capacitance of the buffer should be kept low such that no severe capacitance loading is experienced at the filter output. The differential voltage buffers are made up with PMOS transistors. The input terminals are connected to the filter outputs, which has a signal swing from 0V to 1V (rail-to-rail operation). The signal is thus level-shifted up to appear at the outputs of the buffer, which has a gain of about unity. The schematic of the buffer is shown in Fig. 5.12. Table 5.4 summarizes the transistors' size of the voltage buffer.

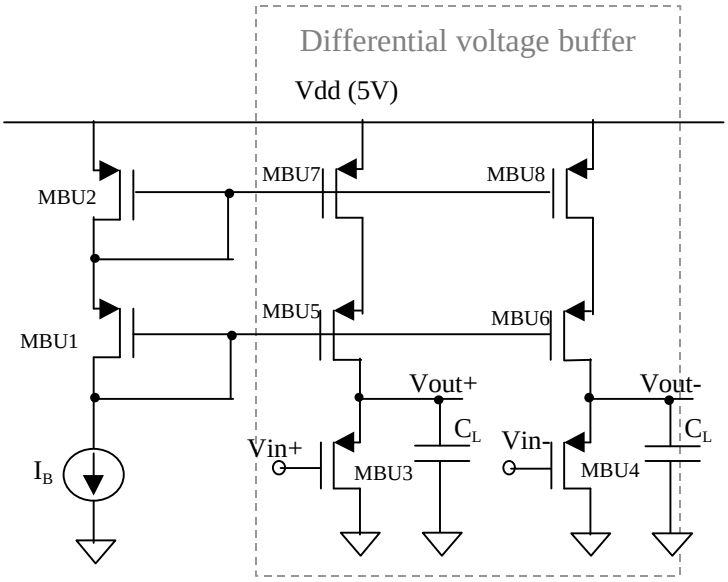


Fig. 5.12 Schematic of an on-chip differential voltage buffer

Table 5.4 Transistors' size of voltage buffer

Transistor	**Size**
MBU1, MBU5, MBU6	$\frac{12.6m}{2.1m}$
MBU3, MBU4	$\frac{12.6m}{1.2m}$
MBU2, MBU7, MBU8	$\frac{12.6m}{2.1m}$

The buffer is operated with a 5-V supply instead of 1V. This is because it is fundamentally impossible to implement a voltage buffer in a single 1V supply with both input and output signal swings of 1V. Nevertheless, the 1V SC filter does not require strong buffering stages if it is connected monolithically with other circuitries. Table 5.5 summarizes the simulation results of the differential voltage buffer.

Table 5.5 Summary the simulation results of the differential voltage buffer

Parameters	**Simulation Results**
Supply voltage	5V
Input signal swing	0V to 1V
Output signal swing	2.4V to 3.4V
Buffer gain	0.984V/V @ Input signal at 0V 0.981V/V @ Input signal at 1V
Buffer –3dB bandwidth	6MHz
Slew rate	(+SR) 8.9V/μsec (-SR) 11.4V/μsec
Max. capacitance loading	100pF

The proper operation of the voltage buffer with the 1-V SC pseudo-2-path filter is verified with Hspice simulation. Figure 5.13 (a) and 5.13 (b) show the transient response of the filter after buffer with input signal of 0.3Vpp 75.3kHz and the corresponding frequency spectrum respectively.

(a) Transient (differential) output of filter after buffer

(b) Frequency spectrum of filter after buffer (input signal 75.3kHz)

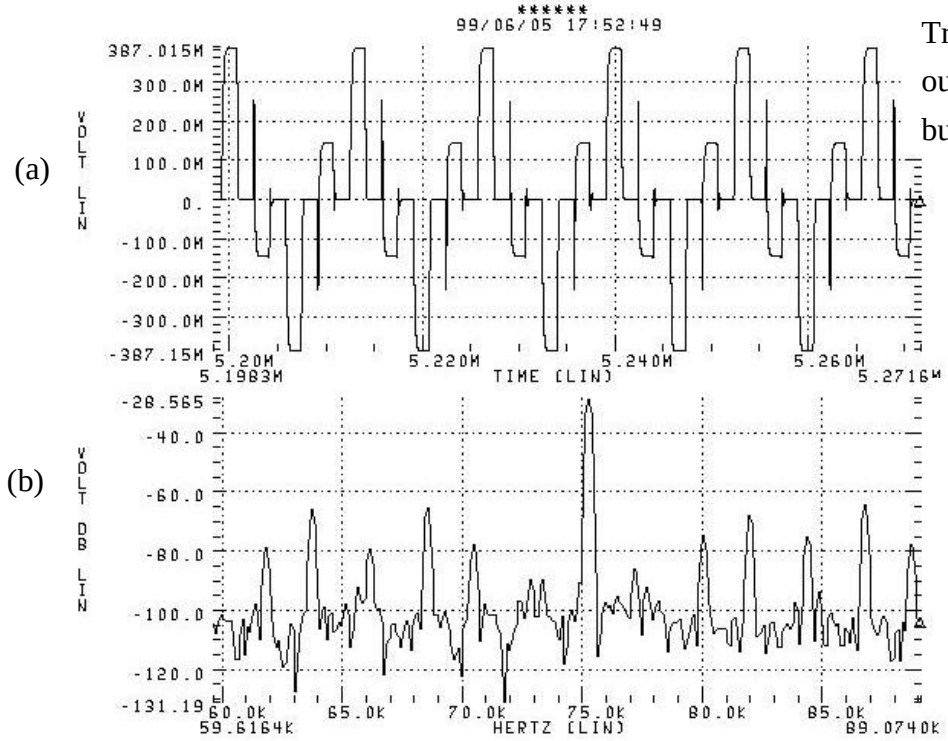


Fig. 5.13 (a) Filter transient response after buffer with 75.3kHz input signal
(b) Corresponding frequency spectrum of filter after buffer

In this chapter, the realization of the 1-V SC pseudo-2-path filter in standard CMOS (HP 0.5μm N-well) process is presented. A 1-V fully differential two-output-pair switchable opamp is designed to achieve a DC gain of 81dB and unity-gain bandwidth of 7.5MHz with a phase margin of 54°. A dynamic common-mode feedback circuit is introduced to operate with the

proposed switchable opamp. Hspice simulation results show proper operation of the 1-V SC pseudo-2-path filter. An on-chip voltage buffer is designed to drive external input capacitance of measuring equipment. The operation of the buffer with the filter is verified by simulation.

Reference

[1] G. H. Eschauzier, L. P. T. Kerklaan and J. H. Huijsing, "A 100-MHz 100-dB operational amplifier with multipath nested miller compensation structure", *IEEE Journal of Solid-State Circuits*, Vol. 27, No. 12, Dec. 1992, p.1709-1717.

[2] F. You, H. K. Embabi and E. S. Sinencio, "Multistage amplifier topologies with nested Gm-C compensation", *IEEE Journal of Solid-State Circuits*, Vol. 32, No. 12, Dec. 1997, p.2000-2011.

[3] S. M. Mallya and J. H. Nevin, "Design procedures for a fully differential folded-cascode CMOS operational amplifier", *IEEE Journal of* S*olid-State Circuits*, Vol. 24, No. 6, Dec. 1989, p.1737-1740.

[4] R. Gregorian and G. C. Temes, *Analog MOS integrated circuits for signal processing*, John Willy & Sons, New York, 1986

[5] L. K. J. Vandamme, X. Li, and D. Rigaud, “1/f Noise in MOS Devices, Mobility or Number Fluctuations?”, *IEEE Transactions on Electron Devices*, Vol. 41, No. 11, Nov. 1994, p.1936-1945

[6] K. K. Hung, P. K. Ko, C. M. Hu, and Y. C. Cheng, “A Unified Model for the Flicker Noise in Metal-Oxide-Semiconductor Field-Effect Transistors”, *IEEE Transactions on Electron Devices*, Vol. 37, No. 3, March 1990, p.654-665.

[7] A. Baschirotto and R. Castello, “A 1-V 1.8MHz CMOS Switched-Opamp SC Filter with Rail-to-Rail Output Swing”, *IEEE Journal of Solid-State Circuits*, Vol. 32, No. 12, Dec. 1997, p.1979-86

[8] R. Castello, F. Montecchi, F. Rezzi and A. Baschirotto, “Low-Voltage Analog Filters”, *IEEE Transactions on Circuits and Systems – I: Fundamental Theory and Applications*, Vol. 40, No. 11, Nov. 1995, p.827-840

Chapter 6

Layout Considerations and Post-Simulations

In this chapter, the layout considerations of the switchable opamp, common-mode feedback circuit, voltage buffer and the SC pseudo-2-path filter are discussed. Cadence is used as the drawing tool for the transistor layouts. Post-simulations showed the functionality and performances of the building blocks and the filter.

6.1 Layout and Post-Simulation of Switchable Opamp

The schematic of the 1-V fully-differential two-output-pair switchable opamp is redrawn in Fig. 6.1 for easy discussion.

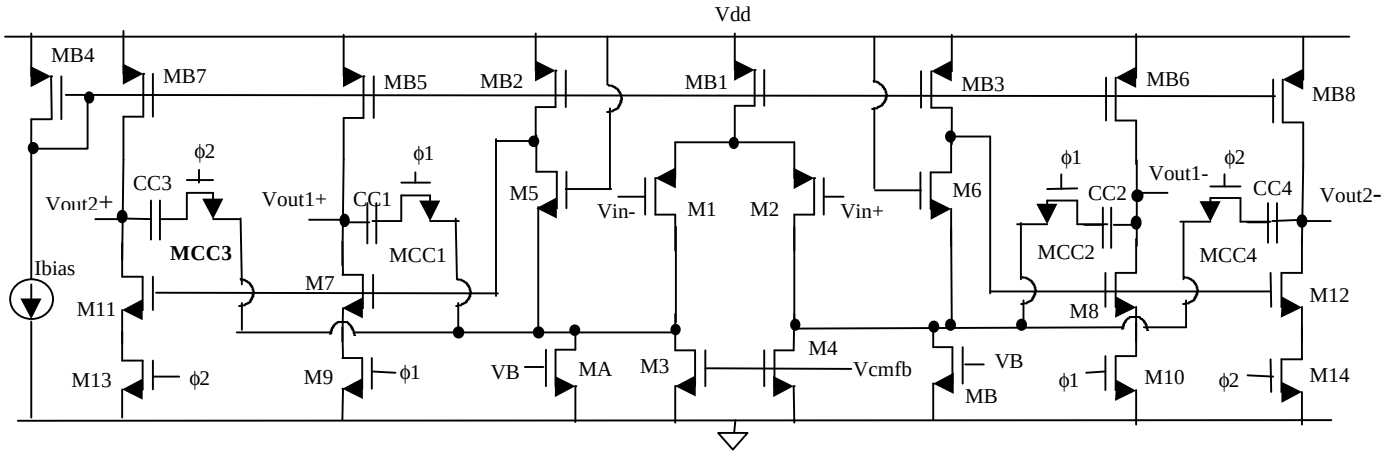


Fig. 6.1 Schematic of a fully differential two-output-pair switchable opamp

To reduce the offset voltage of the switchable opamp, the input transistors M1 and M2 are splitted into eight equal parts and laid out with common-centroid symmetry [1] as shown in Fig. 6.2.

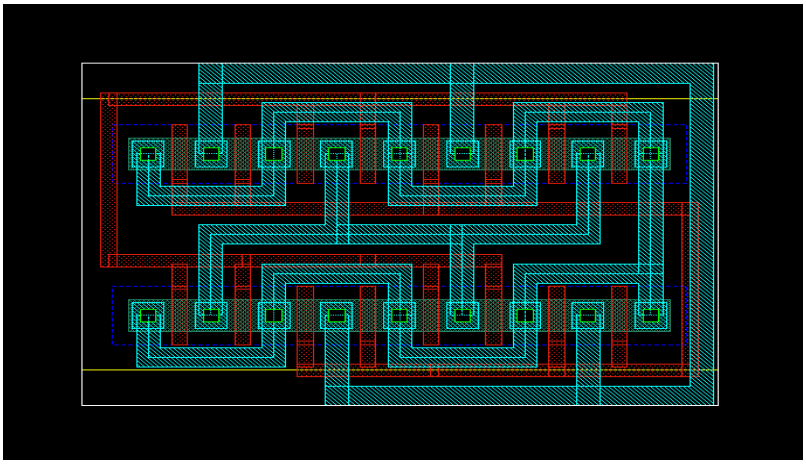


Fig. 6.2 Opamp input transistors matched with common-centroid

Meanwhile, for fully-differential circuit, the differential path should also be matched. This can be achieved by adopting the layout floorplan as shown in Fig. 6.3.

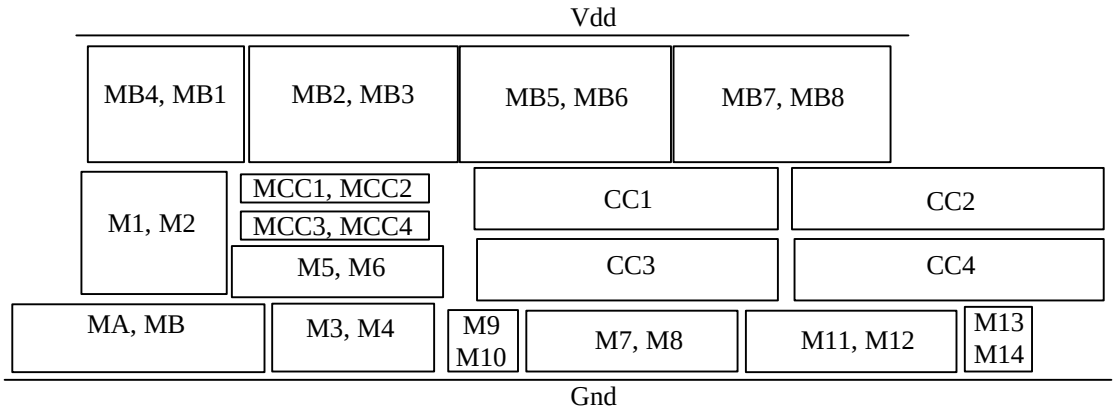


Fig. 6.3 Layout floorplan of switchable opamp

Inside each block, two transistors in the differential path are paired up (e.g. transistor pair M5 and M6 corresponds to the same functionality in the differential path) and laid out with

common-centroid symmetry. The layout of the switchable opamp is shown in Fig. 6.4. The switchable opamp occupies a chip area of 50μmx120μm.

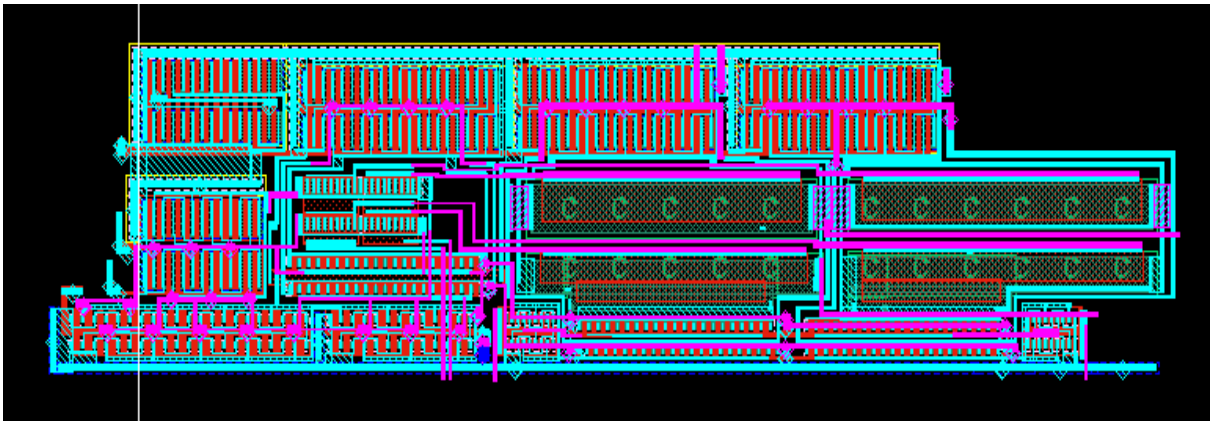


Fig. 6.4 Layout of switchable opamp

Figure 6.5 shows the post-simulation frequency response of the switchable opamp, which achieves a low-frequency gain of 81db with a unity-gain frequency of 7.4MHz with a phase margin of 60.2°.

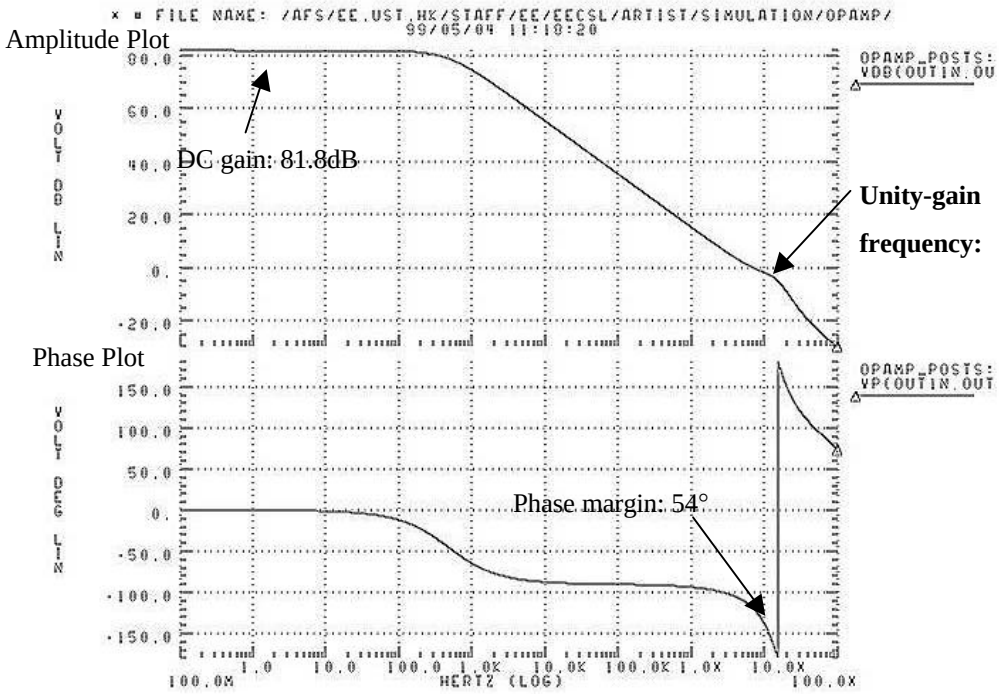


Fig. 6.5 Frequency response of the fully differential two-output-pair switchable opamp

Other characteristics of the switchable opamp are obtained, and the results are summarized together with the pre-simulation results in Table 6.1. Good agreements between pre-simulation and post-simulation are achieved.

Table 6.1 Post-simulation results of the switchable opamp

Parameters	**Specifications**	**Pre-Simulation Results**	**Post-Simulation Results**
Low frequency gain	> 75dB	81.4dB	81.4dB
Unity gain frequency	> 7MHz	7.5MHz	7.4MHz
Phase margin	> 60°	54°	60.2°
Power consumption	< 100μW	63.8μW	63.8μW
Supply voltage	1V	1V	1V
Settling time	< 300nsec	350nsec	360nsec
Slew rate	> 1.2V/μsec	(+ SR) 1.53V/μsec (- SR) 1.65V/μsec	(+ SR) 1.51V/μsec (- SR) 1.63V/μsec
Output swing	0.7V	0.75V	0.75V
Input offset voltage	< 10mV	7mV (calculated)	7mV (calculated)
Equivalent input noise	NA	31.6nV/√Hz	31.6nV/√Hz
Loading capacitor	4pF	4pF	4pF
Switching time	< 300nsec	290nsec	300nsec

6.2 Layout of the SC Dynamic Common-Mode Feedback (CMFB) Circuit

The schematic of the SC dynamic CMFB circuit is redrawn as shown in Fig. 6.6. The required opamp is made with a PMOS differential pair, which is laid out with common-centroid symmetry. Each of the capacitors CP1, CP2, CP3, CP4, CCM1 and CCM2 are 0.1pF. For accurate operation, capacitors CP1 and CP2 should be matched with CCM1 while CP3 and CP4 should be matched with CCM2, otherwise the DC common-mode voltage of the outputs of

opamp will not be accurately set at the middle of the rails. Figure 6.7 and Fig. 6.8 show the floorplan and layout of the SC dynamic CMFB circuit respectively.

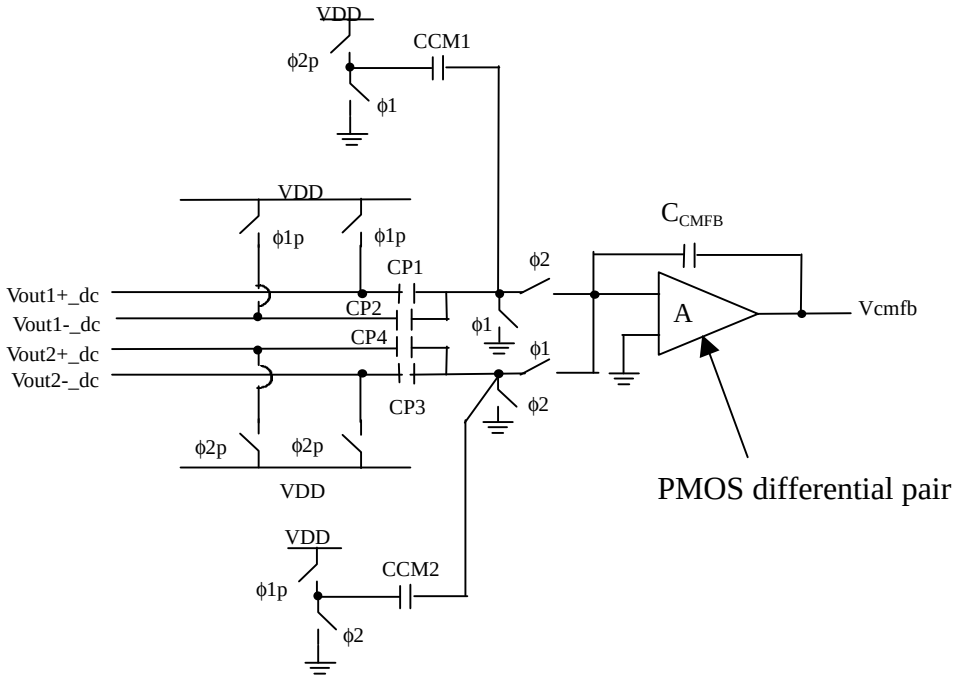


Fig. 6.6 Dynamic common-mode feedback circuits

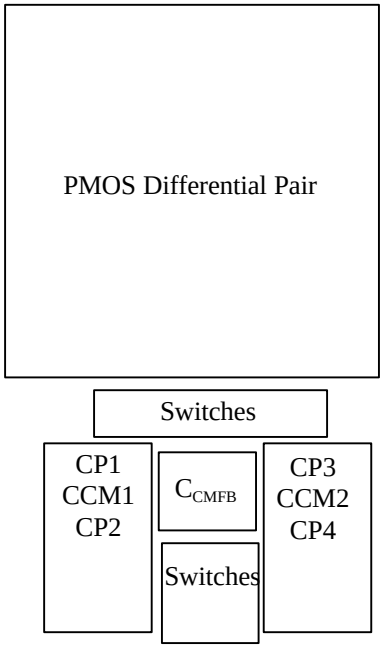


Fig. 6.7 Layout floorplan of SC dynamic CMFB circuit

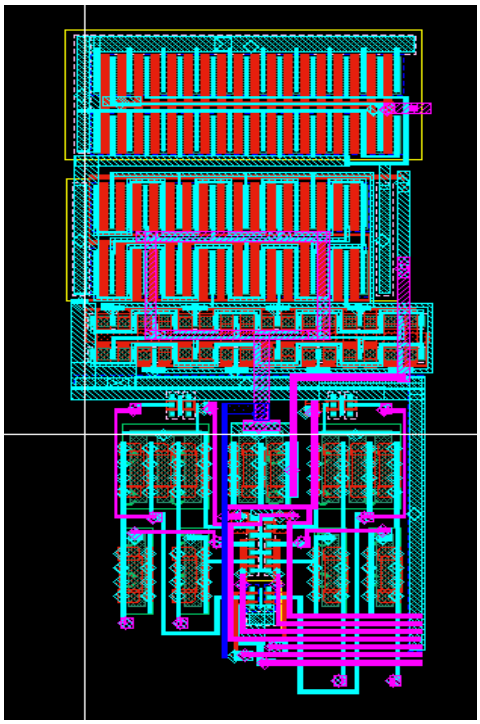


Fig. 6.8 Layout of SC dynamic CMFB circuit

6.3 Layout Considerations of Capacitors

Linear capacitors can be fabricated in HP 0.5μm CMOS process using linear-cap option. The structure and the equivalent model of the linear capacitor C_{linear} are shown in Fig. 6.9 (a) and 6.9 (b) respectively.

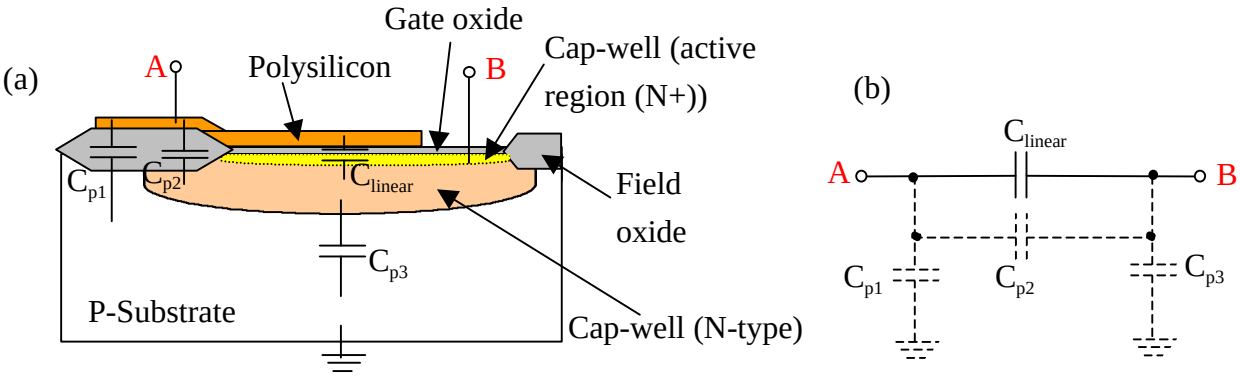


Fig. 6.9 (a) Linear capacitor cross-section (b) Capacitor model with parasitic capacitors

The capacitor C_{linear} is realized across the thin gate oxide between the polysilicon and the active N+ region of the Cap-well. Parasitic capacitors appear at both terminals A and B of capacitor C_{linear}. Parasitic capacitor C_{p1} is very small because of the thick field oxide layer (about two orders of magnitude larger than the gate oxide), and hence can be ignored. Parasitic capacitor C_{p2} is formed between the polysilicon, field oxide and the cap-well, and hence its capacitance is directly added to the total capacitance as seen between terminals A and B. But its effect is small because the field oxide is much thicker than the gate oxide. Nevertheless, if too small polysilicon is used to make capacitor C_{linear} because too small capacitance value is desired, it can happen to affect the total capacitance value significantly because the routing area

(redundancy for contacts and spacing, etc.) of the polysilicon may not be reduced with capacitance value. In this case, polysilicon strips should be avoided to 0route on top of the cap-well region. Lastly, parasitic junction capacitor C_{p3}.appears at the bottom plate of C_{linear}, it has a value of about 20% of that of capacitor C_{linear} because of the highly doped cap-well region. To avoid extra capacitance loading to the opamps, the bottom plates of the capacitors should not connect to the outputs of the opamps. A unit-capacitor layout is shown in Fig. 6.10. A squared structure [1][2] is adopted to minimize the capacitor error due to over-etching. The unit-capacitor is 0.1pF with dimensions of 6.75μm x 6.75μm.

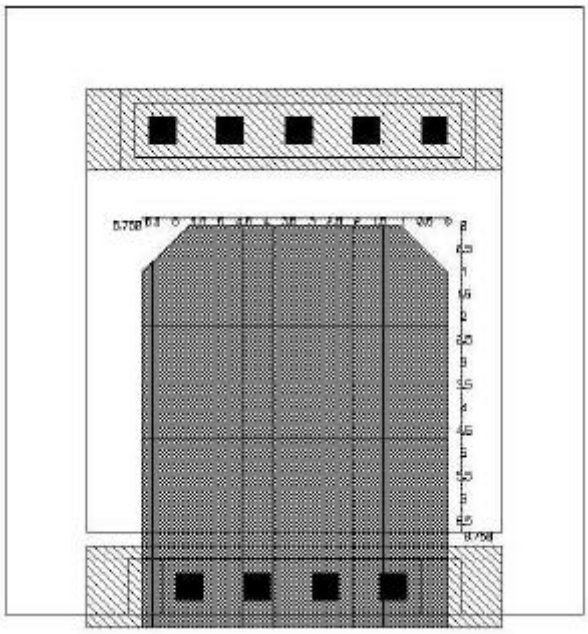


Fig. 6.10 Layout of a unit capacitor

The capacitor is defined by the overlapping region between the polysilicon layer and the active-area inside the cap-well. As the corners of the polysilicon layer are likely to suffer from higher etching rate than the edges, the corners are made with 45° [1] to obtain a better shape

control. All capacitors used in the SC pseudo-2-path filters are made up with numbers of unit-capacitors. For better matching between capacitors with non-integer ratio, the ratios of perimeter to area of the two capacitors are made the same.

6.6 Layout of Differential Voltage Buffer

Good matching of the differential voltage buffer pair is necessary because the differential output signals of the filter are level-shifted up by them before the signals are measured by equipment. Therefore, transistors in differential path (MBU3 and MBU4, MBU5 and MBU6, MBU7 and MBU8 in Fig. 5.11) are matched with common-centroid symmetry. Figure 6.11 and 6.12 show the floorplan and layout of for the differential buffer pair respectively.

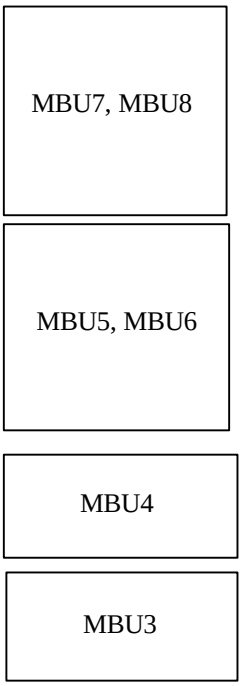


Fig. 6.11 Layout floorplan of differential voltage buffer

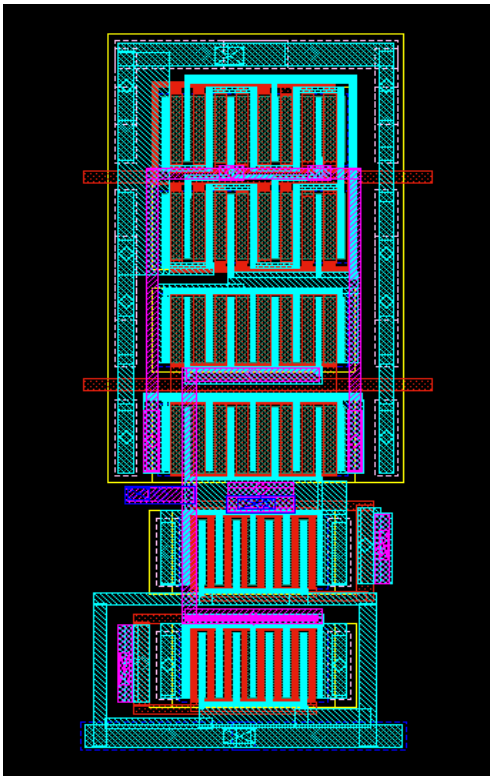


Fig. 6.12 Layout of differential voltage buffer

6.7 Layout and Post-Simulation of 1-V SC Pseudo-2-Path Filter

The floorplan and layout of the SC pseudo-2-path filter are shown in Fig. 6.13 and 6.14 respectively.

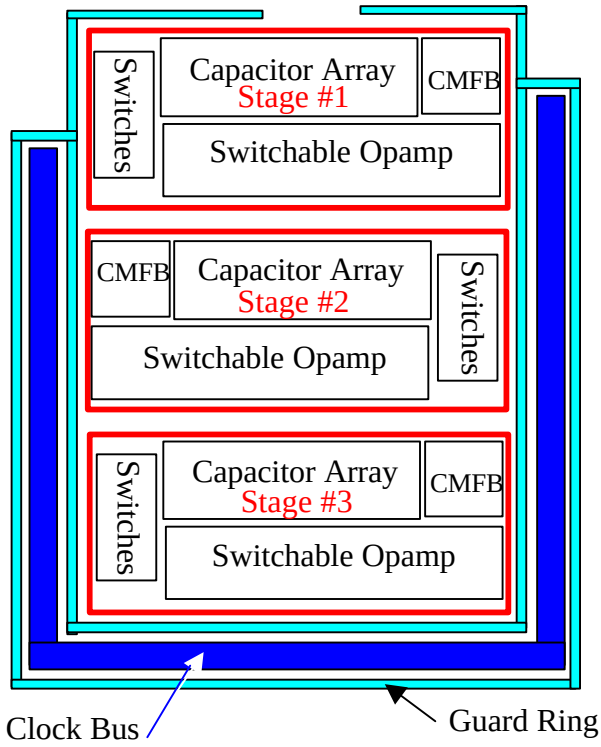


Fig. 6.13 Layout floorplan of the 1-V SC pseudo-2-path filter

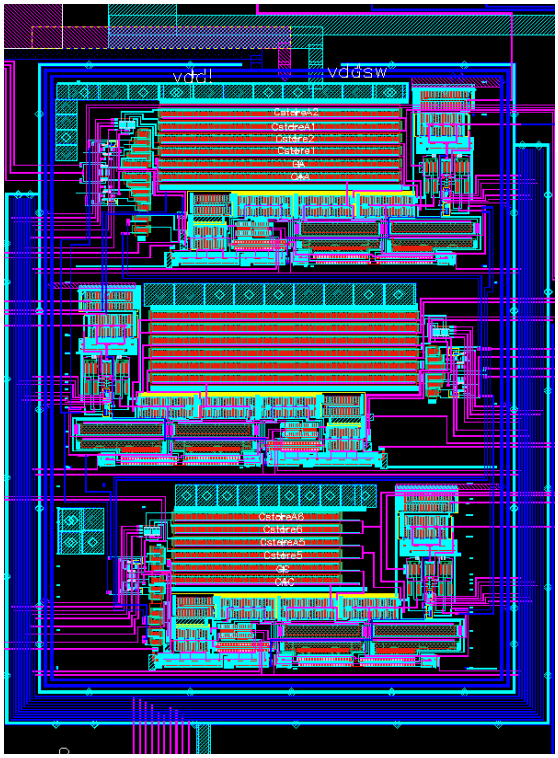


Fig. 6.14 Layout of the 1-V SC pseudo-2-path filter

To minimize the noise from the clocking signals to inject into the filter, a ground-shielded guard ring is used to surround the clock lines. The filter consists of three stages, each of which has a switchable opamp, CMFB circuit, capacitor array and switches. The post-simulation shows proper operation of the SC pseudo-2-path filter. Figure 6.14 (a) and 6.14 (b) show the transient response and frequency (FFT) spectrum of the filter respectively with a 0.3Vpp input

signal at 75.3kHz. Table 6.2 summarizes the post-simulation results of other filter characteristics.

Table 6.2 Summary of post-simulation results of the 1-V SC pseudo-2-path filter

Parameters	**Post-simulation results**
Supply voltage	1V
Center frequency	75.3kHz
Sampling frequency	301.2kHz
-3dB frequency	74.5kHz and 76.1kHz (1.5kHz bandwidth)
Stopband loss	>40dB relative to signal at passband
Power consumption	229μW (63.8μW @ opamp, 12.5μW @ CMFB circuit)
Q-value	50
Capacitance spread	50 (unit capacitor of 0.1pF is used)
Chip area	800μm x 1000μm

Reference

[1] M. Ismail and T. Fiez, *Analog VLSI – Signal and Information Processing*, McGraw-Hill Book, 1994

[2] H. C. Luong, *Elec 304 Course Notes*, HKUST, 1998

Chapter 7

Testing Considerations and Methodologies

Figure 7.1 shows the die photo of the testing chip, which consists of the SC pseudo-2-path filter, switchable opamps and buffers (the voltage-control oscillator (VCO) is for another

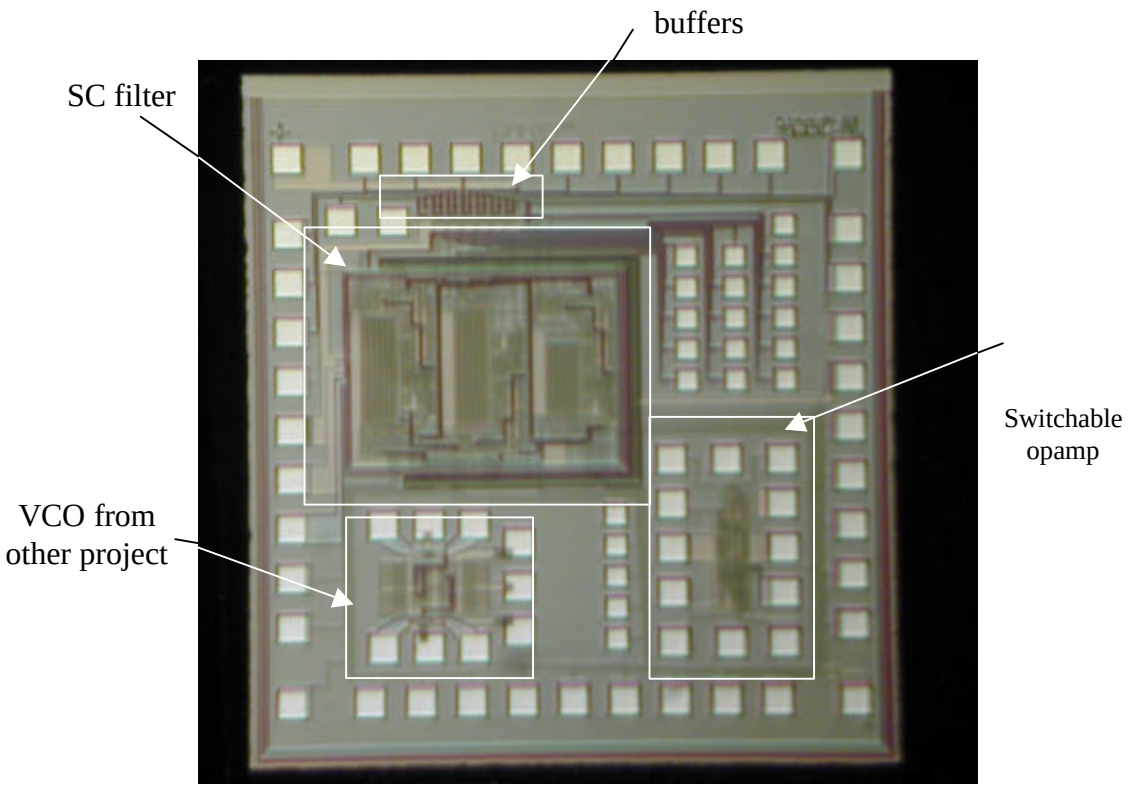


Fig. 7.1 Die photo of the circuit test chip

project and so is not related).

In this chapter, the testing results of the buffer and switchable opamp are discussed in the

first two sections. The 1-V SC pseudo-2-path filter performance is then presented. By turning off one of the paths in the SC pseudo-2-path filter, the SC pseudo-1-path highpass response is also tested. From the testing results, the possibility of operating SC pseudo-2-path filter in a single 1-V supply is verified.

7.1 Measurement Results of Voltage Buffer

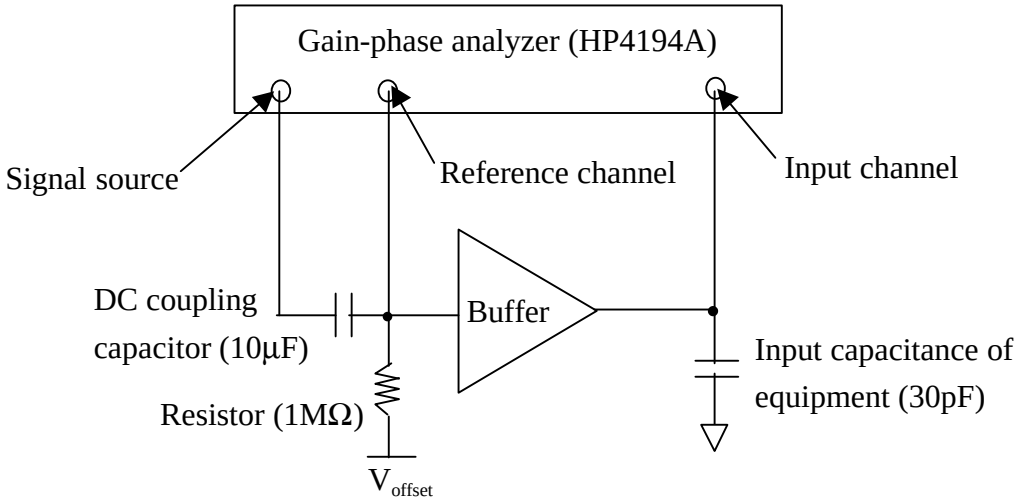


Fig. 7.2 Testing setup for measuring bode plot of buffer

Gain-phase analyzer (HP4194A) is used to measure the Bode plots of the voltage buffer. The testing setup is shown in Fig. 7.2.

An AC sweep is performed by the gain-phase analyzer through varying the input signal source frequency. The Bode plots are obtained by plotting the relative amplitude and phase between the signals at the input channel (output signal of buffer) and the reference channel (input signal of buffer) against frequency. The voltage source V_{offset} biases the input of the buffer

to 0.5V, which is the middle of opamp output DC level. The Bode plots are obtained and shown in Fig. 7.3.

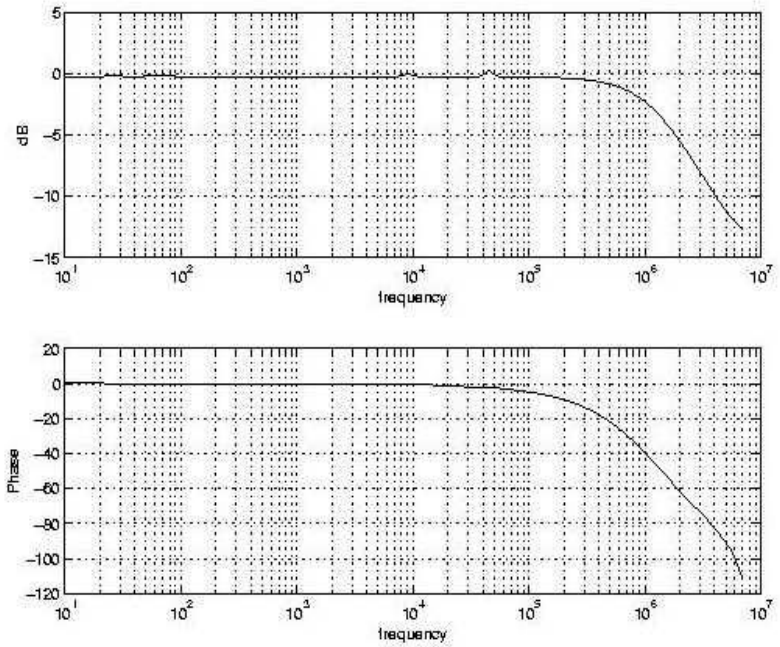


Fig. 7.3 Frequency response of voltage buffer

The slew rate of the buffer is measured by applying a step voltage from 0V to 1V through V_{offset}. The output step response is obtained with CRO and the result is shown in Fig. 7.4. Table 7.1 summarizes the buffer performance.

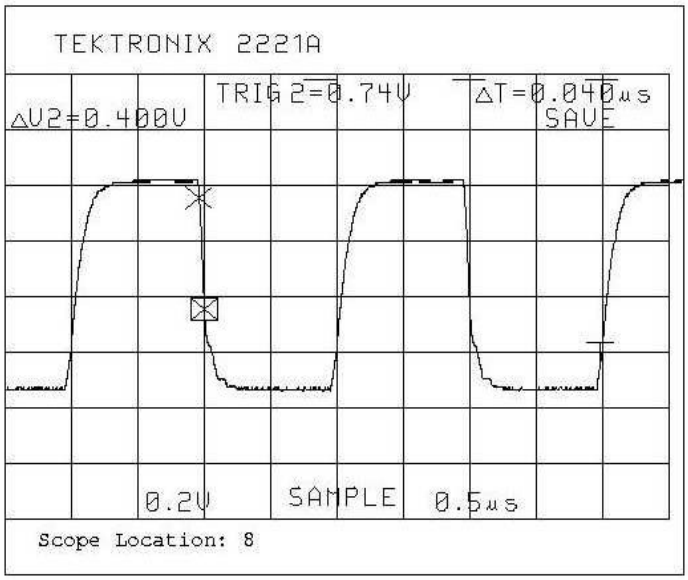


Table 7.1 Summary of testing results of voltage buffer

Parameters	**Results**
Technology	HP 0.5-μm CMOS
Low frequency voltage gain	0.98V/V
-3dB bandwidth	1MHz
Slew rate	10V/μsec (-ve) 9V/μsec (+ve)

7.2 Measurement Results of Switchable Opamp

The gain-phase analyzer is again used to obtain the transfer curves of the fully-differential switchable opamp with only one of the output pairs activated for the measurement. However, only single-ended configuration is used in the measurement as there is no appropriate power splitter (to convert single-ended signal to differential form) and power combiner (to combine differential signal at outputs of opamp to single-ended form for the equipement). Figure 7.5 shows the testing setup for measuring the Bode plots of opamp.

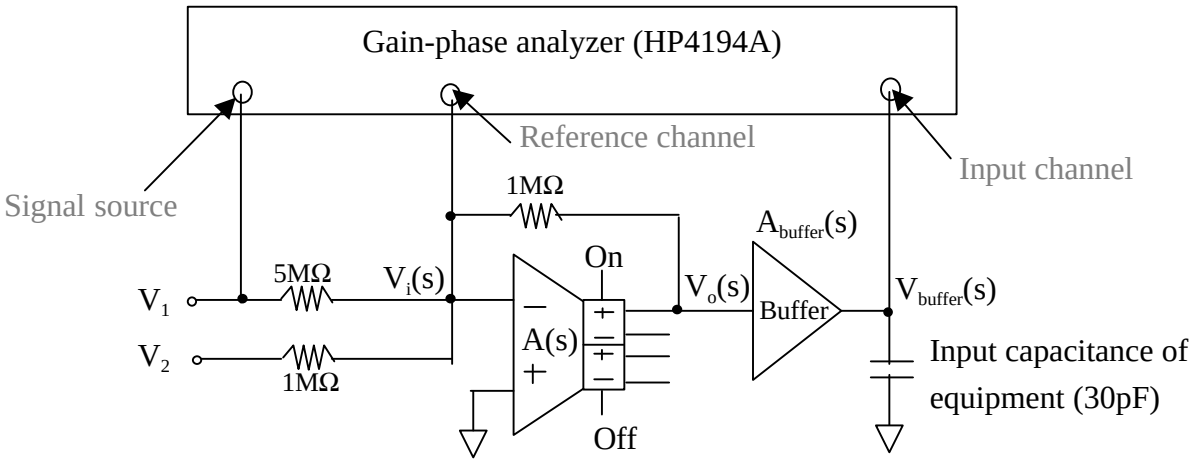


Fig. 7.5 Testing setup for measuring Bode plots of switchable opamp

A resistor feedback configuration is adopted for the measurement. By superposition, the output transfer functions of the opamp and buffer can be derived as shown in Equation 7.1 and Equation 7.2 respectively.

$$V_o(s) = -\frac{A(s)}{6+5A(s)}V_1(s) - \frac{A(s)}{2+A(s)}V_2(s) \qquad \text{(Eq. 7.1)}$$

$$V_{buffer}(s) = A_{buffer}(s)V_o(s) \qquad \text{(Eq. 7.2)}$$

where A(s) and $A_{buffer}(s)$ are the transfer characteristics of opamp and buffer respectively. Input signal is applied at V_1 while a DC voltage of –0.5V is applied at V_2 to set the opamp output DC operating point at 0.5V (middle of rail). Instead of measuring the transfer curves of opamp directly, the gain-phase analyzer measures the Bode plots of buffer output signal against the opamp input signal (i.e. $V_{buffer}(s)/V_i(s)$). This is because the opamp cannot drive the heavy capacitive loading from the measuring equipment and thus the on-chip buffer is used. Since the transfer curves of the buffer ($A_{buffer}(s)$) has been obtained in previous section of this chapter, the amplitude plot and phase plot of the opamp can thus be obtained by using Equation 7.3 and 7.4 respectively. The bode's plots of the opamp is shown in Fig. 7.6 below.

$$|A(s)| = \left|\frac{V_o(s)}{V_i(s)}\right| = \left|\frac{V_o(s)}{V_{buffer}(s)}\right| x \left|\frac{V_{buffer}(s)}{V_i(s)}\right| = \frac{1}{|A_{buffer}(s)|}\left|\frac{V_{buffer}(s)}{V_i(s)}\right| \qquad \text{(Eq. 7.3)}$$

$$\angle A(s) = \angle\frac{V_o(s)}{V_i(s)} = \angle\frac{V_{buffer}(s)}{V_i(s)} - \angle\frac{V_o(s)}{V_{buffer}(s)} = \angle\frac{V_{buffer}(s)}{V_i(s)} - \angle A_{buffer}(s) \qquad \text{(Eq. 7.4)}$$

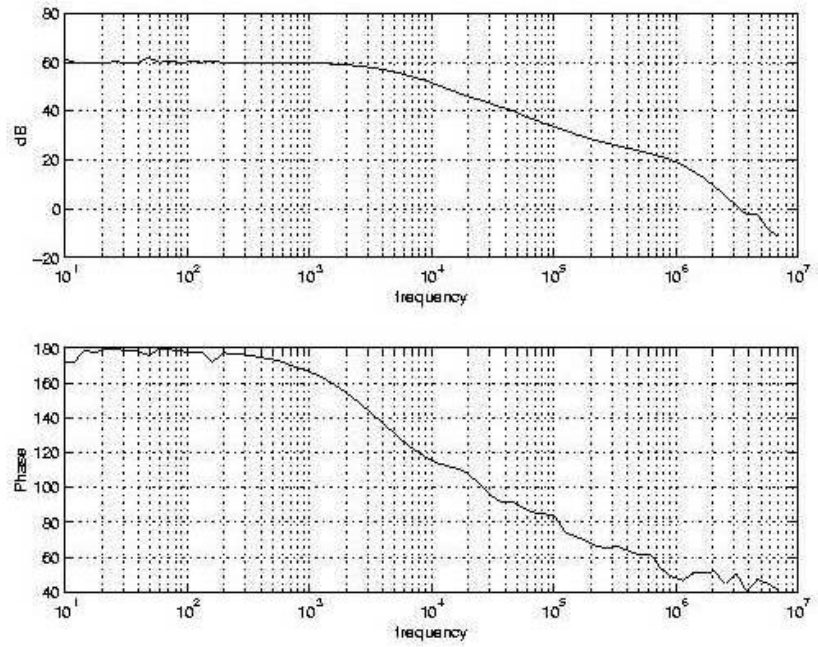


Fig. 7.6 Frequency response of switchable opamp

The measured single-ended low-frequency gain of the opamp is 63dB with a unity-gain frequency of 7MHz. Therefore, for differential configuration, the opamp achieves a low-frequency gain of 69dB. The opamp achieves a phase margin of 45° and consumes only 75μW in a single 1V supply. The measurement results agree with simulations.

Figure 7.7 shows the testing setup for measuring the settling time of the opamp [1].

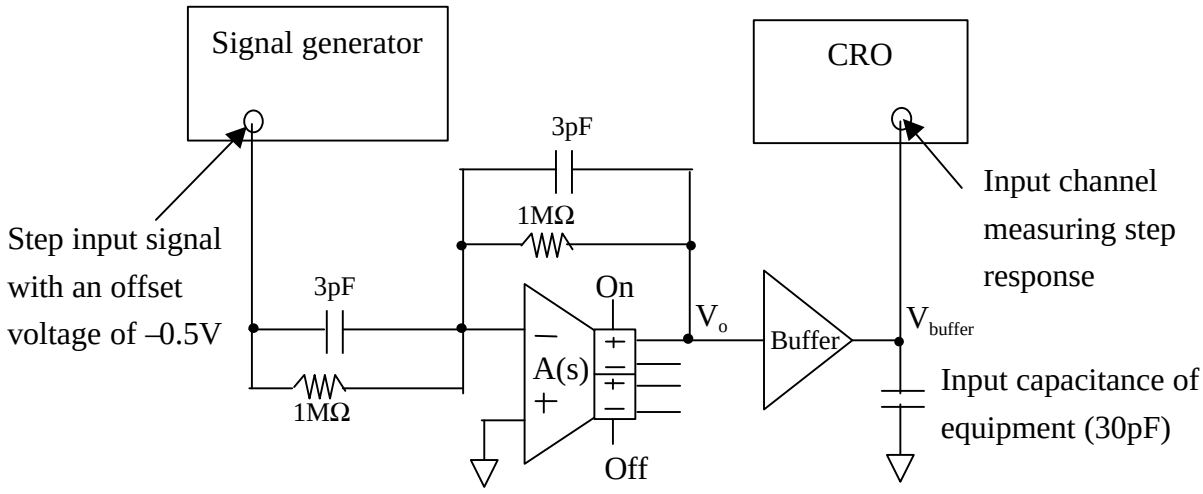


Fig. 7.7 Testing setup for measuring settling time of opamp

The opamp is capactively fed back with capacitor values of 3pF, which models the integrator configuration used in the filter that gives out the longest settling time (the case with the largest feedback capacitor) towards a step input. The feedback resistors provide a DC path to the input of opamp. An DC offset voltage of –0.5 is applied so such the opamp output DC level is set to 0.5V, which is the middle of rail. The step response of the opamp cannot be measured directly by CRO due to its large input capacitance. Instead, the CRO measures the step response of the opamp through the on-chip buffer, which is supposed to reflect the settling phenomence of the opamp. Since the buffer has a large bandwidth, it should not affect the overall settling time of the system. The measurement result is shown in Fig. 7.8 below.

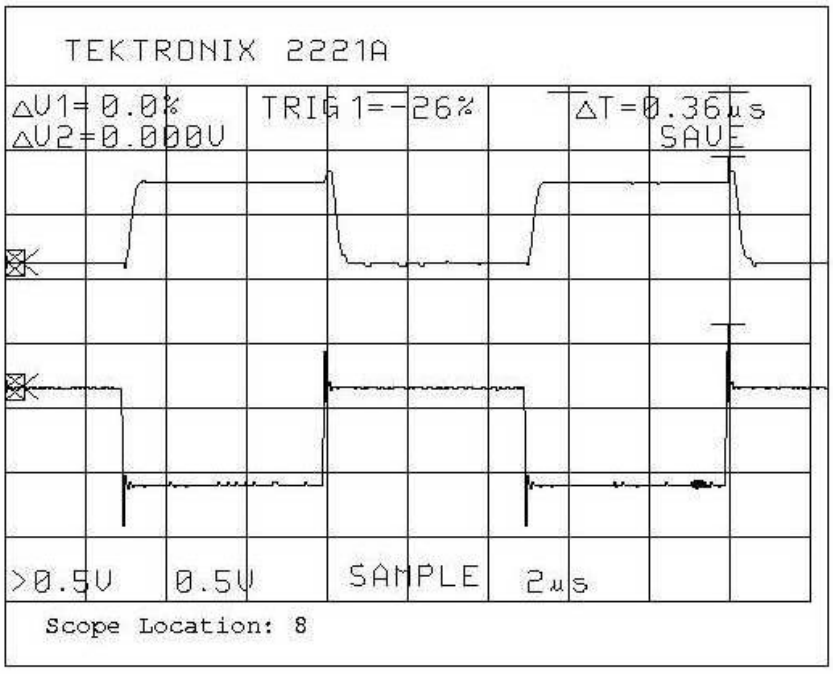


Fig. 7.8 Measurement of settling time of switchable opamp

The measured settling time with a positive input step voltage is 450n seconds while it is about 500n seconds for a negative input step voltage. The opamp performance is summarized in Table 7.2.

Table 7.2 Summary of testing results of opamp

Parameters	**Results**
Technology	HP 0.5-μm CMOS
Supply voltage	1V
Low-frequency gain (open-loop)	69dB
Unity gain frequency	7MHz
Phase margin	45°
Power consumption	75μW
Output swing	0.7V
Settling time	500n sec
Chip area	150μm x 50μm

7.3 Generating Differential Signal for SC Filters

The operation of the SC pseudo-2-path filter requires differential input signal, which can be converted from a single-ended signal source using Mini-Circuits 2-way 180° power-splitter (ZF8CJ-2-2). Meanwhile, the output signal amplitude of the power splitter is 3dB lower than the input signal amplitude, so we have to adjust the input signal amplitude until the desired outputs of the power splitter are achieved. A DC offset voltage is required to apply along with the input signal for proper operation of the switched-capacitor filter. Figure 7.9 shows the testing setup for generating differential input signal with DC offset voltage from a single signal

source:

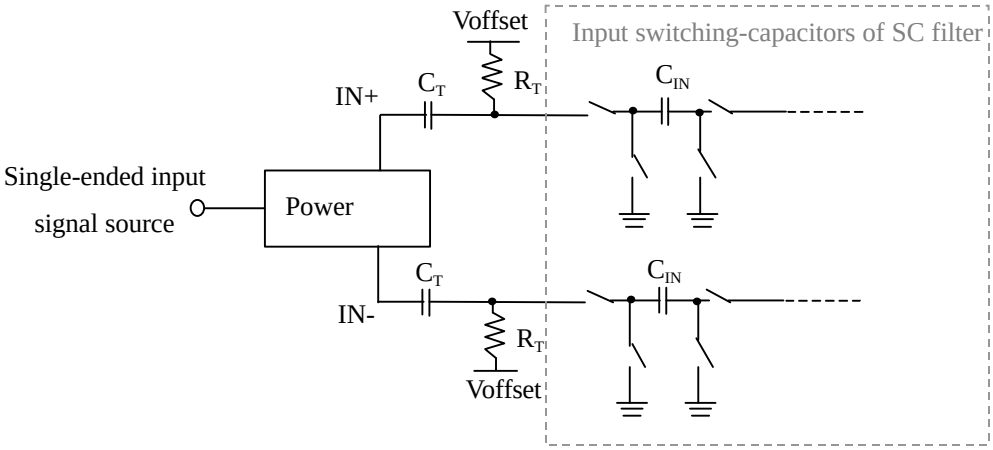


Fig. 7.9 Setup for generating differential input signal with DC offset voltage

DC offset voltages can be applied to the SC filter through the use of the resistors R_T while the capacitors C_T ac-couple the input signal. The input capacitor C_{IN} of SC filter is about 0.6pF, which corresponds to an impedance of 2.6MΩ at 100kHz. As a result, the resistors R_T are chosen to be about 100MΩ in order to reduce their loading effect. Meanwhile, capacitor value of 10uF is used for C_T such that most signal can drop across input capacitor C_{IN}.

7.4 Measurement Results of the 1-V SC Pseudo-1-Path Filter

Figure 7.10 shows the clocks diagram to turn off one of the two paths of the SC pseudo-2-path filter to realizes the SC pseudo-1-path filter, which is actually the SC highpass filter that was shown in Fig. 3.9.

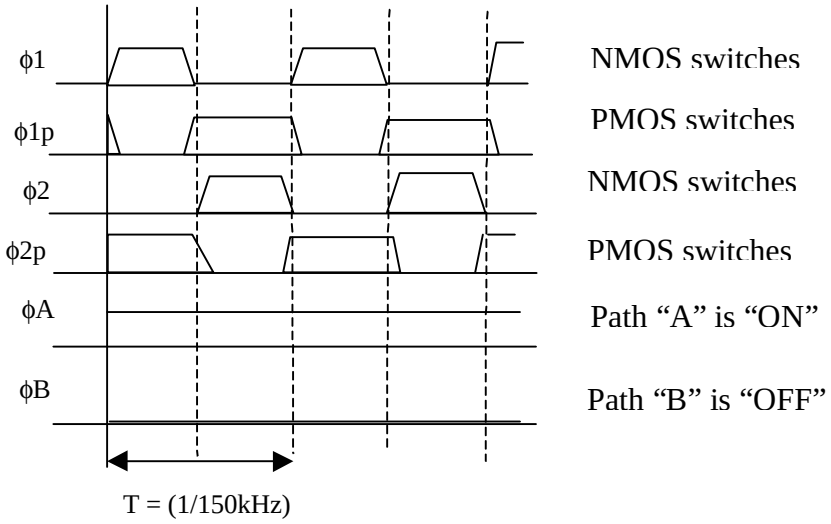


Fig. 7.10 Clock diagram for operating the SC pseudo-1-path filter

The frequency reponse of the SC pseudo-1-path filter can be obtained directly by performing an AC signal sweep from 100Hz to 100kHz using the network analyser (SR770), where the input signal is generated by the network analyser. The testing setup is shown in Fig. 7.11.

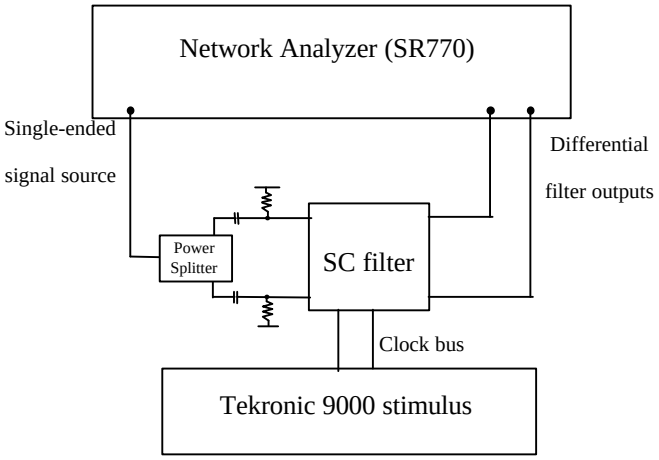


Fig. 7.11 Setup for measuring SC filter frequency response

The network analyser accepts true differential inputs, and hence no power-combiner is needed to combine the differential output signals of the filter to single-ended form before

further processing. By plotting the frequency response of the filter, we obtain the passband bandwidth and passband gain of the SC pseudo-1-path highpass filter. The measured frequency response is shown in Fig. 7.12. Table 7.3 summarizes the 1-V SC pseudo-1-path filter characteristics.

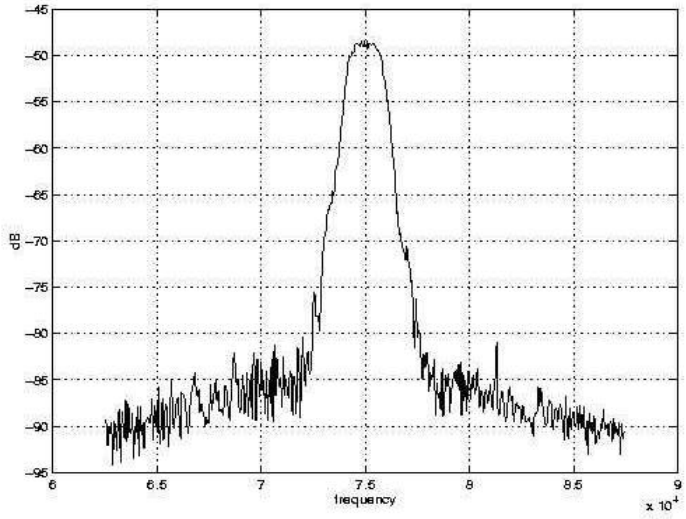


Fig. 7.12 Frequency response of SC pseudo-1-path highpass

Table 7.3 Summary of testing results of 1-V SC pseudo-1-path filter

Parameters	**Results**
Technology	HP 0.5-μm CMOS
Supply voltage	1V
Filter type	Highpass
Center frequency	75kHz
Passband	850Hz
Passband gain	1dB
Sampling frequency	150kHz

7.5 Measurement Results of the 1-V SC Pseudo-2-Path Filter

The clocks diagram shows in Fig. 7.13 operates the SC pseudo-2-path filter.

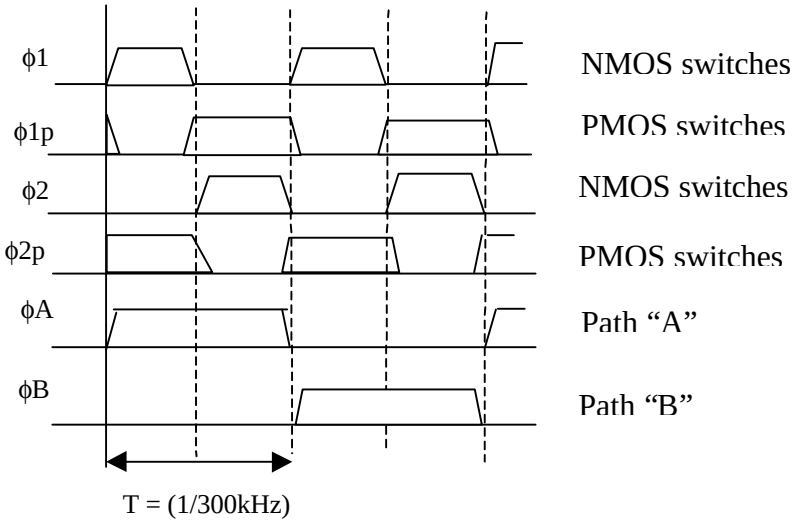


Fig. 7.13 Clock diagram for operating the SC pseudo-2-path filter

Again, an AC signal sweep is performed to obtain the frequency response of the SC pseudo-2-path filter using the testing setup in Fig. 7.11. The measured frequency response is shown in Fig. 7.14.

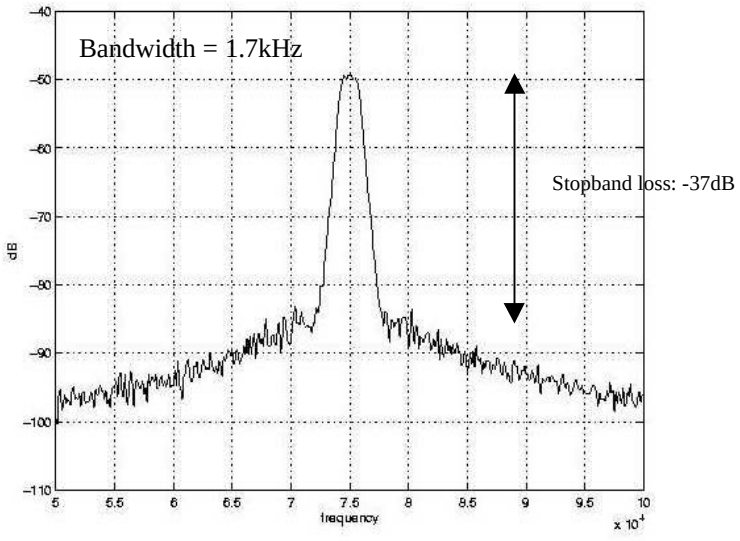


Fig. 7.14 Frequency response of the SC pseudo-2-path filter

As expected, the center frequency of the SC pseudo-2-path filter is located at 75kHz (1/4 of the sampling frequency) with a bandwidth of 1.7kHz (Q=45). The filter achieves a minimum stopband loss of -37dB.

Transient Response of the 1-V SC Pseudo-2-Path Filter

Figure 7.15 show the single-ended output transient response of the 1-V SC pesudo-2-path filter without input signal. It can be observed that the output common-mode voltage of the filter is well controlled at about 0.5V by the dynamic common-mode feedback circuit.

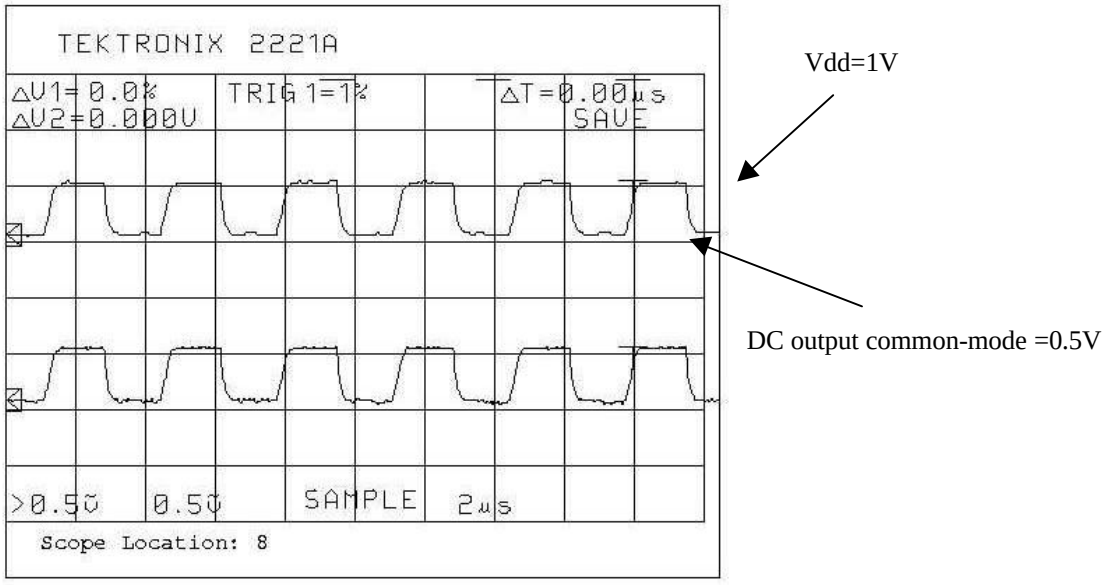


Fig. 7.15 Output transient response of the SC pseudo-2-path filter without input signal

The differential output transient response of the filter with a $0.3V_{pp}$ input signal at 75kHz (passband) and the corresponding frequency spectrum are shown in Fig. 7.16 (a) and (b) respectively. It can be seen that the signal is settling even for a signal amplitude as large as $1.2V_{pp}$. We observe a passband gain of 1dB by comparing the output signal magnitude with the

input signal.

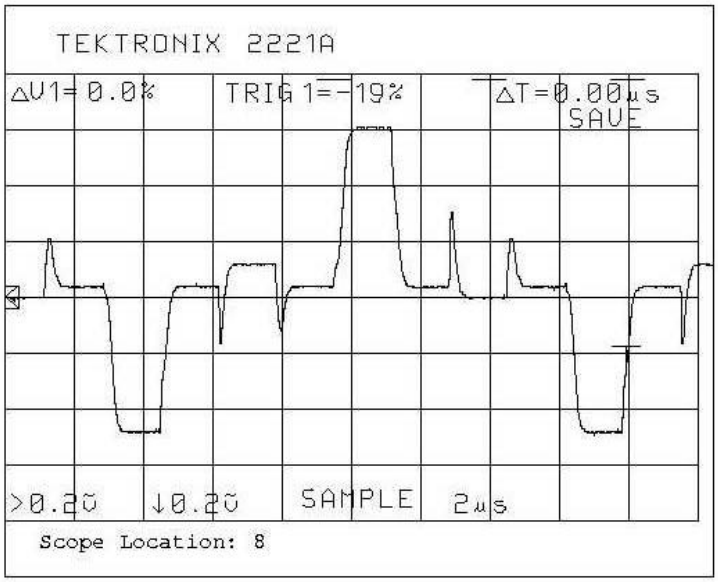


Fig. 7.16(a) Output transient with a single 75kHz 150mV input signal

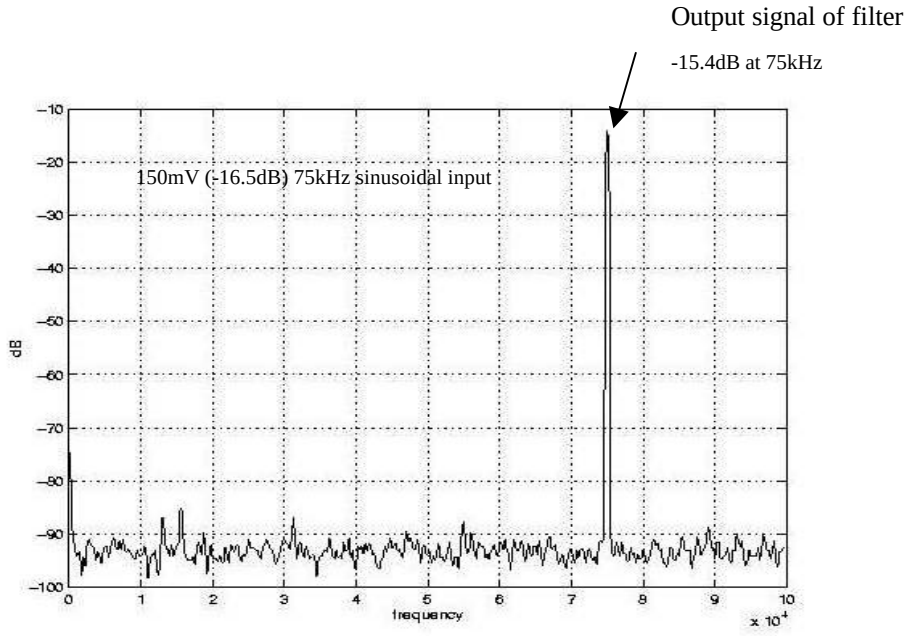


Fig. 7.16(b) Frequency spectrum with a single 75kHz 150mV input signal

From the above waveforms, it is evident that the switched-opamp mechanism is based on the fact that during one clock phase the output signal is not available and the output node is tied to the power supply (return-to-zero).

Measuring Inter-Modulation of the 1-V SC Pseudo-2-Path Filter

Two sinusodial signals of frequencies f_1=74.6kHz and f_2=75.3kHz are applied to measure their inter-modulation (IM) at the output of the filter. The modulated signals are located at f_{m1} and f_{m2}, which are given by Equation 7.5 [2].

$$f_{m1} = 2f_1 - f_2 = 74.1kHz$$
$$f_{m2} = 2f_2 - f_1 = 76kHz \qquad \text{(Eq. 7.5)}$$

Here, the first modulated signal f_{m1} is located out of the passband of the filter while another modulated signal f_{m2} is in the passband. Figure 7.17 (a) and (b) show the one-percent and three-percent inter-modulation measurement results.

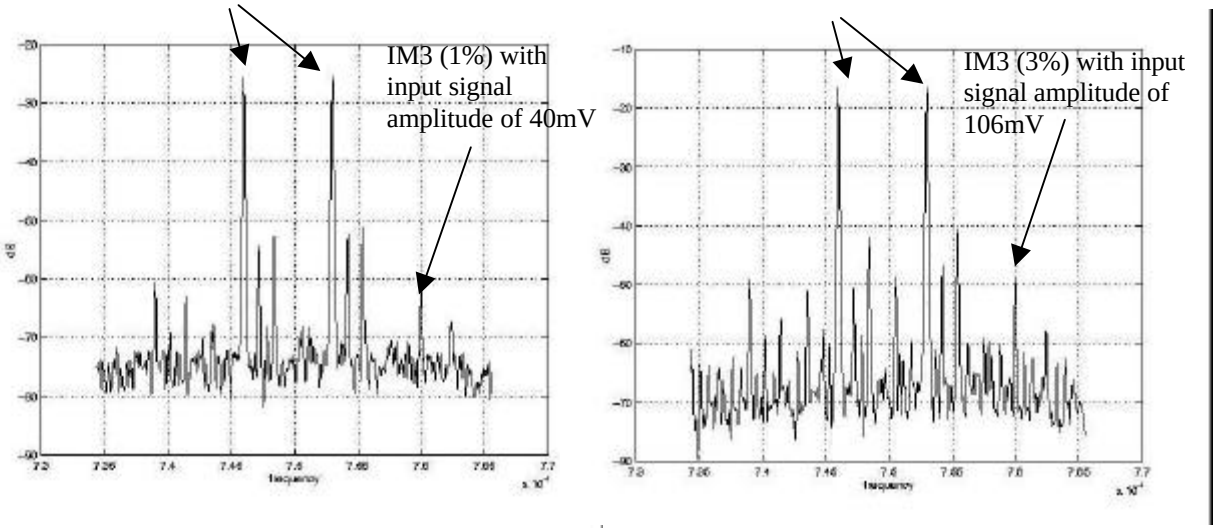


Fig. 7.17 Measurement of inter-modulation (a) 1% plot, (b) 3% plot

The one-percent IM is measured with an input signal amplitude of $80mV_{pp}$, which causes the output signal amplitude of f_{m2} 40dB lower than the output signal amplitude at frequency of either f_1 or f_2. While the three-percent IM is measured with an input signal amplitude of $212mV_{pp}$, which causes the output signal amplitude of f_{m2} only 30dB lower than that of the frequency components at either f_1 or f_2. The dynamic range (defined as $signal^{rms}/noise^{rms}$) for 3% IM is 47dB.

Measuring Third Harmonic Distortion of the 1-V SC Pseudo-2-Path Filter

The total harmonic distortion (THD) is measured with an input frequency at f_{in}=75.9kHz. The third harmonic at $3f_{in}$ cannot be directly measured since it is located out of the passband, which results in heavy suppression by the filter itself. Instead, due to the 2π periodic phenonmence at the frequency-domain of discrete-time system, the thrid harmonic component of f_{in} is folded at (f_s - $3f_{in}$ = 75.3kHz, where f_s is the sampling frequency) which for the specific bandpass filter (with sampling frequency f_s = 300kHz) is in the passband [2]. The 1% THD corresponds to a 200mVpp input signal and the 3% THD to a 226Vpp input signal, as shown in Fig. 7.18 (a) and (b) respectively. Table 7.4 summarizes the filter performance, which is compared with the two reported 1-V SC filters [2][3] in literature.

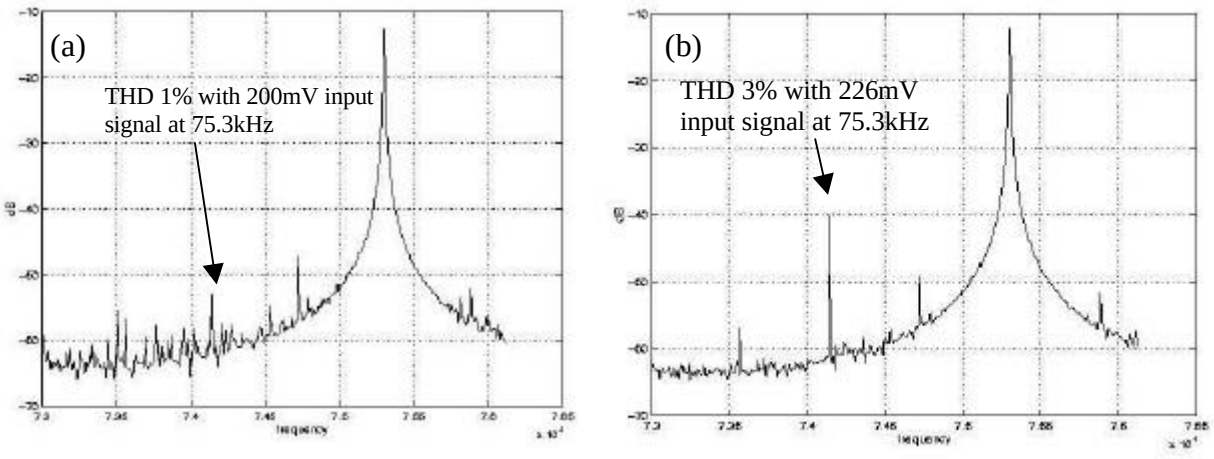


Fig. 7.18 Third harmonic distortion measurement (a) 1% THD (b) 3% THD

Table 7.4 Summary of testing results of 1-V SC pseudo-2-path filter

Parameters	**Simulations**	**Test Results**	**Results from [1]**	**Results from [2]**
Technology	HP 0.5-µm CMOS	HP 0.5-µm CMOS	0.5-µm CMOS	2.4-µm CMOS
Supply voltage	1V	1V	1V	1.5V
Power consumption	260µW	310µW	160µW	110µW
Sampling frequency	300kHz	300kHz	1.8MHz	115kHz
Q	50	45	6.6	NA for lowpass filter
Center frequency	75kHz	75kHz	435kHz	NA
Passband gain	1dB	1dB	NA	6dB
Minimum stopband loss	-39dB	-37dB	NA	NA
Total output noise	NA	1m Vrms	0.8mVrms	140µVrms (input)
THD 1%	NA	@ 416mV input	@725mVpp input	NA
THD 3%	NA	@ 452mV input	@1.1Vpp input	(-60dB @ 0.6Vpp input)
IM3 1%	NA	With two 40mV input signals at 74.6kHz and 75.3kHz (Δ = 700Hz)	With two 40mV input signals at 427kHz and 441kHz (Δ = 12kHz)	NA

IM3 3%	NA	With two 106mV input signals at 74.6kHz and 75.3kHz	With two 106mV input signals at 427kHz and 441kHz	NA
Dynamic range (IM3 3%)	NA	46dB	52dB	69dB
Capacitance spread	50	50	7.5	9
Chip Area	0.8mm^2	0.8mm^2	0.15mm^2	2.1mm^2

The filter is also tested with a single 900mV voltage supply. The transient differential output response with a 150mV 75kHz input signal and the frequency response of the filter are shown in Fig. 7.19 (a) and (b) respectively. We observe that the output signal is still settled correctly even the supply voltage is reduced to 900mV and the filter frequency response is similar to the one measured with 1V supply.

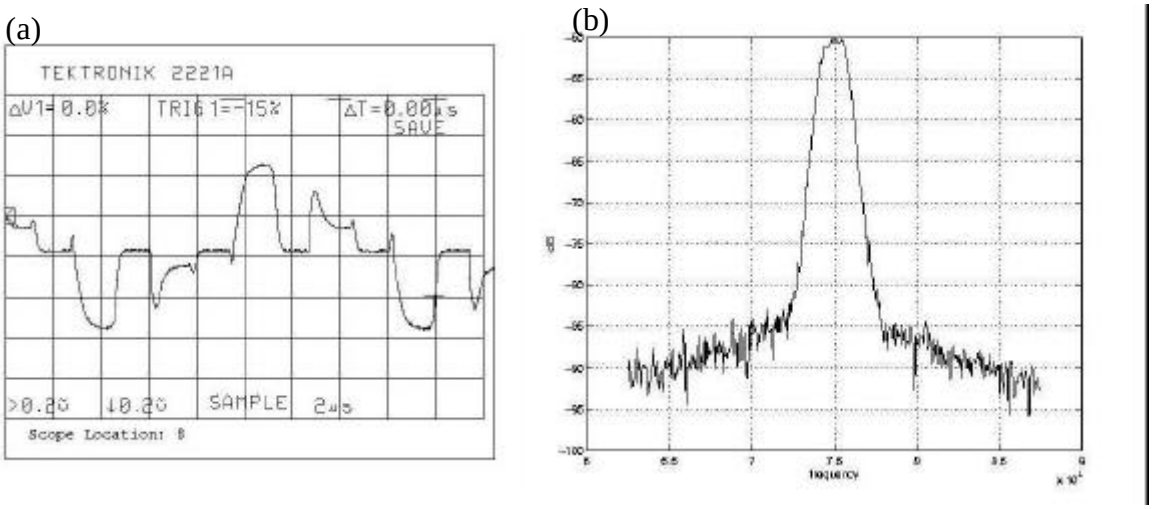


Fig. 7.19 Filter performance at 900mV
(a) transient with 75kHz 0.3Vpp input signal, (b) filter frequency response

To conclude, an SC pseudo-2-path filter is implemented in 0.5μm standard CMOS process in a single 1-V supply using the proposed modified switched-opamp technique. The switchable

opamp achieves a low-frequency gain of 69dB with a phase margin of 45°, which agrees with simulation results. With a sampling frequency of 300kHz, the filter achieves a passband bandwidth of 1.7kHz at center frequency of 75kHz (Q=45). A measured THD of 1% is measured with input signal amplitude of 200mV. The filter dissipates a power of 310μW and occupies a chip area of 0.8mm^2. Finally, testing result shows proper operation of the SC pseudo-2-path filter even with supply voltage as low as 900mV.

Reference

[1] K. Bult and J. G. M. Geelen, "A Fast-Settling CMOS Opamp for SC Circuits with 90-dB DC Gain", *IEEE Journal of Solid-State Circuits*, Vol.25, No. 6, Dec. 1990, p. 1379-1384

[2] A. Baschirotto and R. Castello, “A 1-V 1.8MHz CMOS Switched-Opamp SC Filter with Rail-to-Rail Output Swing”, *IEEE Journal of Solid-State Circuits*, Vol. 32, No. 12, Dec. 1997, p.1979-86

[3] J. Crols and M. Steyaert, “Switched-Opamp: An Approach to Realize Full CMOS Switched-Capacitor Circuits at Very Low Power Supply Voltages”, *IEEE Journal of Solid-State Circuits*, Vol. 29, No. 8, August 1994, p.936-942

Conclusion

A novel vibrating micro-gyroscope is designed and fabricated on silicon crystal. It is based on the thickness-extension vibration mode of the piezoelectric material and does not use any elastic element. Lead acetate trihydrate is used as the lead source for the preparation of the piezoelectric (PZT) solution. High quality PZT thin film is deposited by sol-gel technique on Pt/Ti/SiO2/Si substrate. Due to direct piezoelectric effect, the micro-gyroscope can be driven in a resonant state with a single 0.3Vpp AC source, hence it is suitable for low voltage portable applications. The output is detected by the reciprocal piezoelectric effect and is linearly proportional to the rotational speed. Its operation principle is given, and the theory is confirmed by experimental results. Measured sensitivity of this micro-gyroscope is -30.8μV/V/(°/sec) with a measurement range of 150°/sec at a resonant frequency of 73.84kHz. The total area of the micro-gyroscope is 2.7mm x 2.7mm. The results have been presented in the Transducers' 99 – The Tenth International Conference on Solid-State Sensors and Actuators, Sendai of Japan, June 1999.

Based on the performance of the microgyroscope, a 1-V switched-capacitor (SC) pseudo-2-path bandpass filter is designed and implemented. The filter is applied in the lock-in amplifier, which is used as the signal conditioning circuitry for improving the signal-to-noise-ratio (SNR) of the microgyroscope. A modified switched-opamp technique is proposed to operate the SC pseudo-2-path filter in a single 1-V supply. Testing results show proper operation of the filter, from which the proposed switched-opamp technique is verified. As expected, the center frequency (75kHz) of the filter is located at exactly one quarter of the sampling frequency (300kHz). The measured passband gain and bandwidth of the filter are 1dB and 1.7kHz respectively, with a minimum stopband loss of 37dB. The whole filter consists of

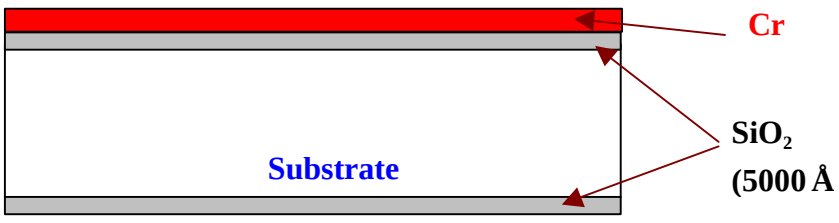
three switchable opamps, which has a measured low-frequency gain of 69dB with a unity-gain frequency and phase margin of 7MHz and 45° respectively. The filter is realized with HP 0.5μm CMOS (N-well) process. A 1% THD is measured with an input signal amplitude of 200mVpp while a 1% IM3 is measured with two 80mVpp input signals at frequencies of 74kHz and 75.3kHz. The filter consumes a power of about 310μW and occupies a chip area of 0.8mm^2. The filter is still functional properly at a single 900mV supply.

Appendix A

Piezoelectric Microgyroscope Fabrication Process

1	***Pre-process Preparation***	1.1 Check-out double-side polished wafers from MFF	
Remark: Wafer type: Double-side polished P-type <100> Initial Doping Conc. $1x10^{15}cm^{-3}$.			

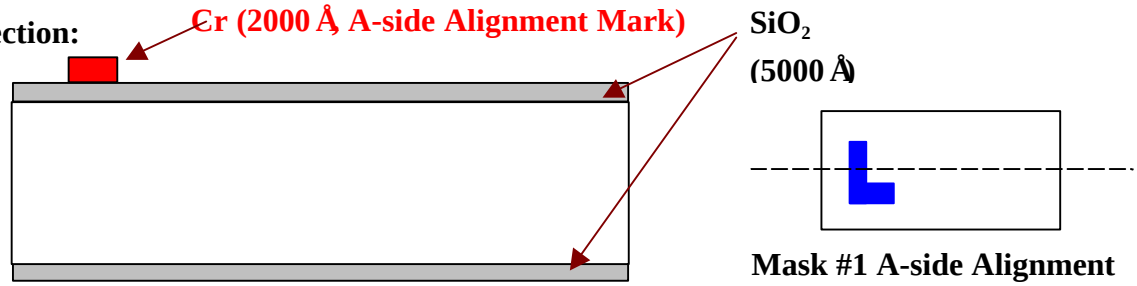
2	***Thermal Oxidation***	2.1 Wet Oxidation (*Target=500nm/5000Å*) • TCA clean furnace for 8 hours the night before • Standard wafer cleaning (include a new control wafer [1]) • Wet oxidation @ 1100ºC, 5'/35'/5' dry/wet/dry O2 and 20 minutes N2 anneal • Measure oxide thickness on control wafer	**MFC Phase:** **I**
Remark: The oxide thickness on both front side and back side can be measured either on the control wafer or on the device wafer directly using nanospec			

3	**Cr Deposition**	3.1 Deposition of Cr (*Target=200nm/2000Å*)	**MFC Phase:** **I** **ARC**
Remark: **Cross-section:** 			

4	***A-side Alignment Mark Formation (Lithography & Etching)*** *Mask #1 (AL)*	4.1 Standard Lithography with A-side Alignment Mark (#1) • Spin photo-resist (PR204) on A-side, soft-bake, expose, develop and hard-bake • No alignment is necessary for this is the first mask	**MFC Phase:** **II Yellow Room**
		4.2 Wet Etching Cr (*Target 200nm/2000Å*) • Put wafers in a large beaker of EDP-200 (stored in yellow room) • Experiment done outside yellow to observe color changes for end-pt - SiO2 color (green)	**MFC Phase:** **II**
		4.3 Photo-resist Strip • Remove photo-resist in O2 plasma Can also use 2001 in yellow room standard bath	**MFC Phase:** **I** **II**

Remark:

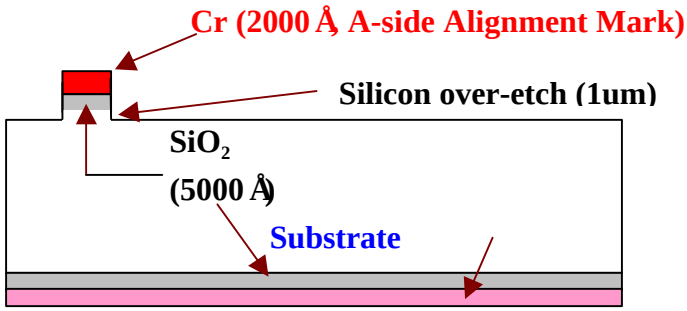
Cross-section:



5	***A-side BOE Wet Etching SiO_2 & A-side Plasma Dry Etching Silicon***	5.1 B-side Photo-resist Spinning for B-side Protection • Spin photo-resist (PR204) on B-side and hard-bake	**MFC Phase:** **II**
		5.2 BOE Wet Etching SiO2 (*Target=500nm/5000Å*)	**MFC Phase:** **II**
		5.3 Plasma Dry Etching Silicon (*Target=300nm/3000Å*)	**MFC Phase:** **II**

Remark:

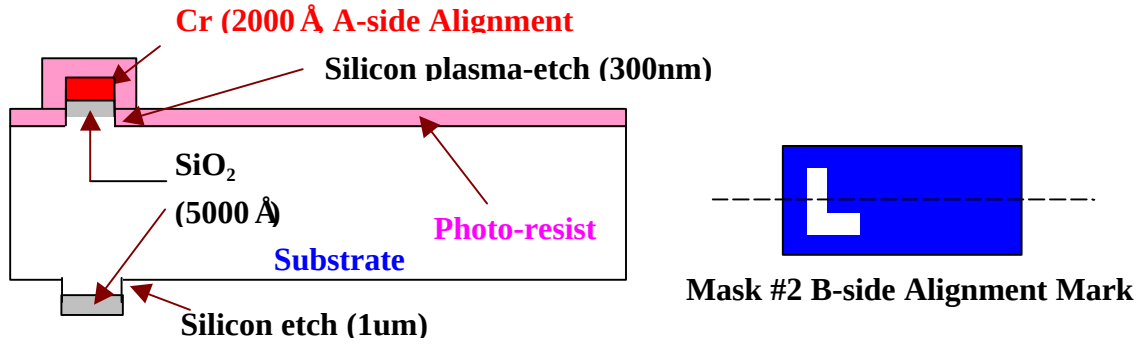
Cross-section:



6	***B-side Alignment Mark Formation*** *Mask #2 (BA)*	6.1 B-side Photo-resist Removal	**MFC Phase II**
		6.2 Spin photo-resist (PR204) on A-side for protection, and hard-bake	**MFC Phase II**
		6.3 ***Non-Standard*** Lithography with B-side Alignment Mark (#2) Using ***A/B-M Contact Aligner*** • Spin photo-resist (PR204) on B-side, soft-bake, expose, develop and hard-bake	**MFC Phase II**
		6.4 BOE Wet Etching SiO2 (5000 Å) and Silicon (1um)	**MFC Phase II**
		6.5 Photo-resist Strip	**MFC Phase II**

Remark:

Cross-section:



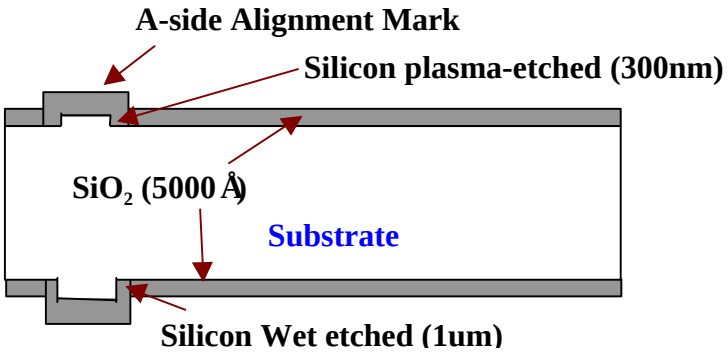
7	***A/B-side Cr and SiO_2 Removal***	7.1 A-side Photo-resist Strip (2001)	**MFC Phase: II**
		7.2 Cr Removal (EDP-200)	**MFC Phase: II**
		7.3 BOE Wet Etching SiO2 to Removal SiO_2 on Both Sides	**MFC Phase: II**

Remark:

8	***A/B-side LTO Deposition and Densification***	8.1 Standard Clean Wafers	**MFC Phase: I**
		8.2 LTO Deposition (*Target=500nm*)	**MFC Phase: I**
		8.3 Stand Clean Wafers (Not necessary if directly transferred from LTO tube)	**MFC Phase: I**
		8.4 LTO Densification • Transfer wafers to oxidation furnace, densify at 950ºC, 20 minutes O2, 10 minutes N2 • Measure LTO thickness	**MFC Phase: I**

Remark:

Cross-section:



9	***A/B-sides LPCVD Polysilicon***	9.1 Standard Clean Wafers	**MFC Phase: I**
		9.2 LPCVD Polysilicon (*Target=400nm*)	**MFC Phase: I**

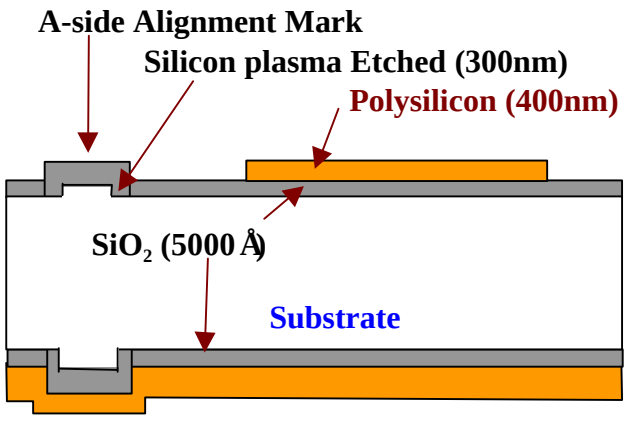
Remark:

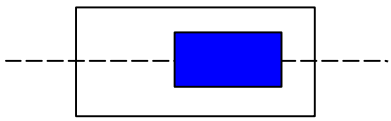
10	***Doping Polysilicon***	10.1 N+ Doping of Polysilicon (Target=10-20Ω/sq.) • Standard clean wafer (not necessary if directly transferred from polysilicon deposition furnace • Phosphorus diffusion at 950°C, 30 minutes $POC1_6$, 5 minutes N_2	**MFC Phase: I**
		10.2 PSG Removal on A/B sides • BOE Wet Etching (180sec)	**MFC Phase: I**
Remark:			

11	***A-side Making Ground Electrode***	11.1 Standard Lithography with A-side Making Ground Electrode Mask (#3) • Spin photo-resist (PR204) on A-side, soft-bake, expose, develop and hard-bake	**MFC Phase: II**
		11.2 Plasma Dry Etching Polysilicon (*Target=400nm*)	**MFC Phase: I**
	Mask #3	11.3 Photo-resist Strip (2001)	**MFC Phase: II**

Remark:

Cross-section:



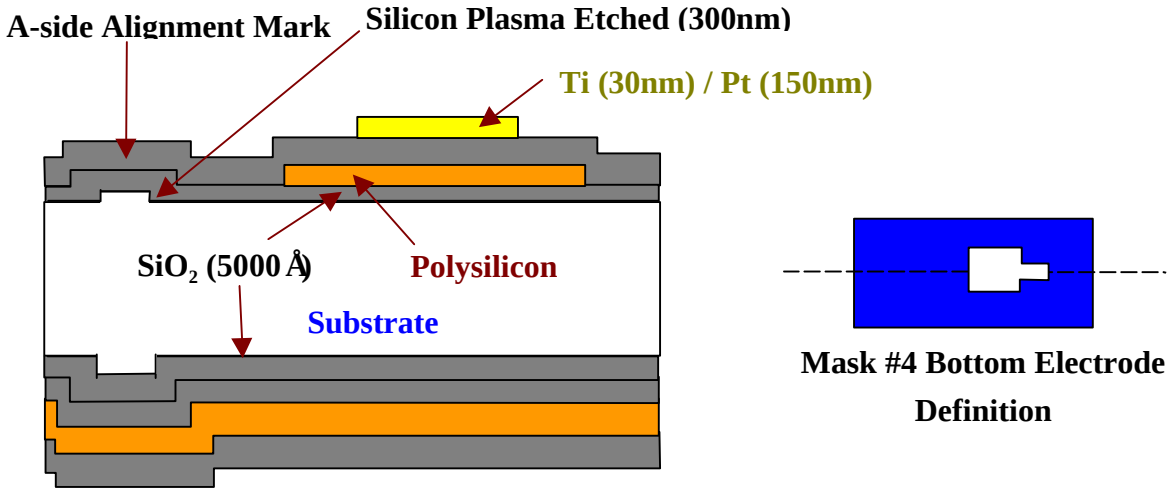


Mask #3 Ground Electrode Definition

12	***A/B sides LTO Deposition and Densification***	12.1 Standard Clean Wafers	**MFC Phase I**
		12.2 LTO Deposition (*Target=500nm*)	**MFC Phase I**
		12.3 Stand Clean Wafers (Not necessary if directly transferred from LTO tube)	**MFC Phase I**
		12.4 LTO Densification • Transfer wafers to oxidation furnace, densify at 1050ºC, 20 minutes O2, 10 minutes N2 • Measure LTO thickness	**MFC Phase I**
Remark:			

13	***A-side Bottom Electrode Formation (Lift-off process for patterning Pt/Ti)*** *Mask #4*	13.1 Standard Lithography with A-side Bottom Electrode Mask (#4) • Spin photo-resist (PR1518) on A-side, soft-bake, expose, develop • No hard-bake step is required (for lift-off process)	**MFC Phase: II**
		13.2 Sputtering Ti (30nm) / Pt (150nm) on A-side	**MFC Phase: II**
		13.3 Photo-resist Strip • Lift-off process: Put wafers in cassette in a beaker of acetone for a day • Observe Ti/Pt lift-off	**MFC Phase: II**
		13.4 Annealing • 600-800°C for 15mins	**MFC Phase: I**

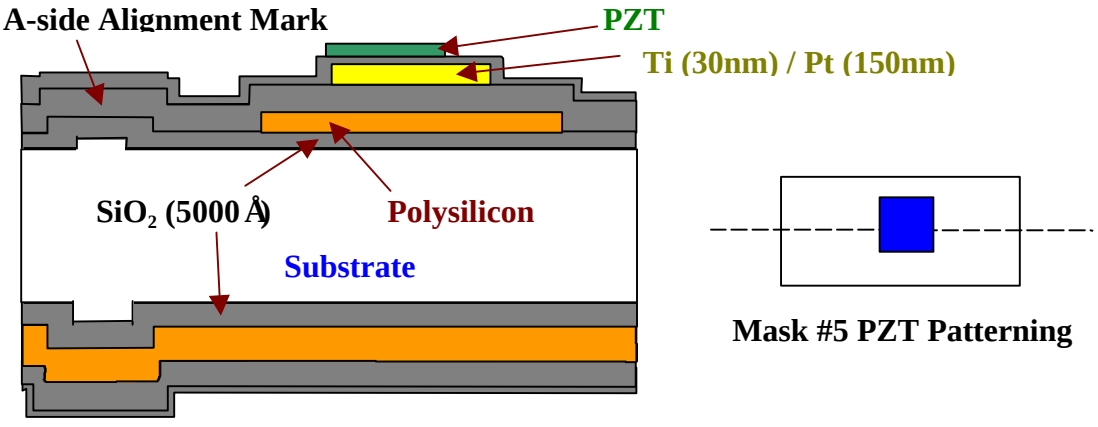
Remark:
Cross-section:



14	***Coating PZT***	14.1 Sputtering SiO2 (*Target=300Å*) • For preventing shorting between top and bottom electrodes	**MFC Phase: II**
		14.2 PZT Spinning (*Target=500-800nm*) • Standard wafer cleaning • Bake in over for 10mins at 120ºC • **HMDS deposition for 10mins** • Spin coating at 500rpm for 5sec followed by 6000rpm for 30sec	**MFC Phase: II**
		14.3 Firing of PZT • 350°C for 2mins on heater (heater reading 4-5) • ***(seems not necessary to do so long, 15 sec may be good enough)*** • (Try to repeat coating and firing)	**MFC Phase: II**
		14.4 Annealing • Put wafer into an oven at 400ºC. • Rise to 700°C and stay for 3 hours in oven • Allow cooling down to room temperature	**MFC Phase: II**
Remark:			

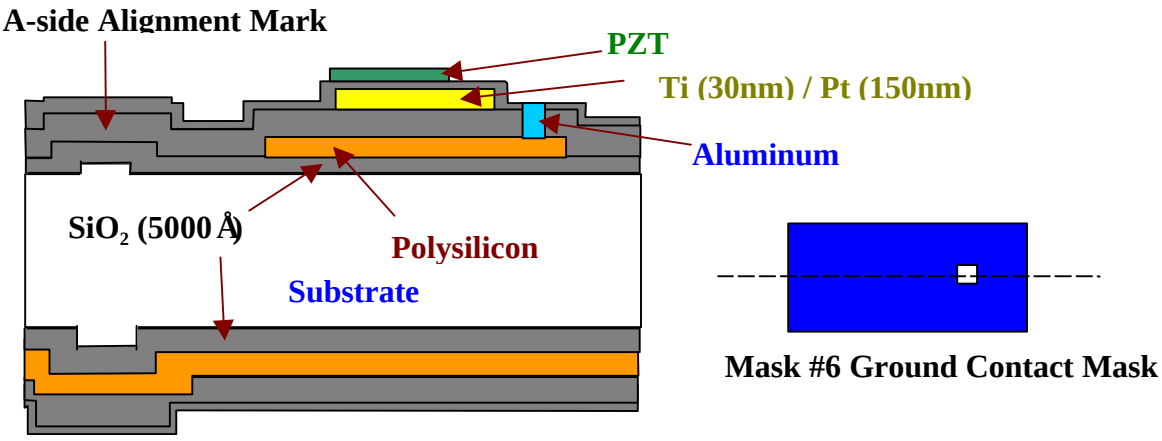
15	***PZT Patterning*** *Mask #5*	15.1 Standard Lithography with PZT Patterning Mask (#5) • Spin photo-resist (PR204) on A-side, soft-bake, expose, develop and hard-bake	**MFC Phase:II**
		15.2 Wet Etching PZT • HNO_3:HF:H_20=15:8:500, 35°C	**MFC Phase:II**
		15.3 Photo-resist Strip	**MFC Phase:II**
		15.4 Measure PZT thickness	**MFC Phase:II**

Remark:



16	***Making Contacts for Ground Electrode***	15.1 Standard Lithography with Ground Electrode Contact Mask (#6) • **Spin photo-resist (PR204) on B-side as protection** • Spin photo-resist (PR204) on A-side, soft-bake, expose, develop and hard-bake	**MFC Phase: II**
		16.2 BOE Wet Etching Pads LTO (*Target=500nm*) • About 6 mins	**MFC Phase: II**
		16.3 Deposition Aluminum (*Target=800-1000nm*) • Lift-off of aluminum • Remains aluminum as contact to ground	**MFC Phase: II**
	Mask #6	16.4 Photo-resist Removal (both A and B sides)	**MFC Phase: II**

Remark:



17	***Top Electrode Formation (Lift-off process for patterning Cr/Au*** *Mask #7*	17.1 Standard Lithography with A-side Making Top Electrode Mask (#7) • Spin photo-resist (PR1518) on A-side, soft-bake, expose, develop • No hard-bake step	**MFC Phase: II**
		13.2 Sputtering Cr (50nm) / Au (400nm) on A-side	**MCPC Room**
		13.3 Photo-resist Strip (Acetone 10-15hrs) (Lift-off process)	**MFC Phase: II**

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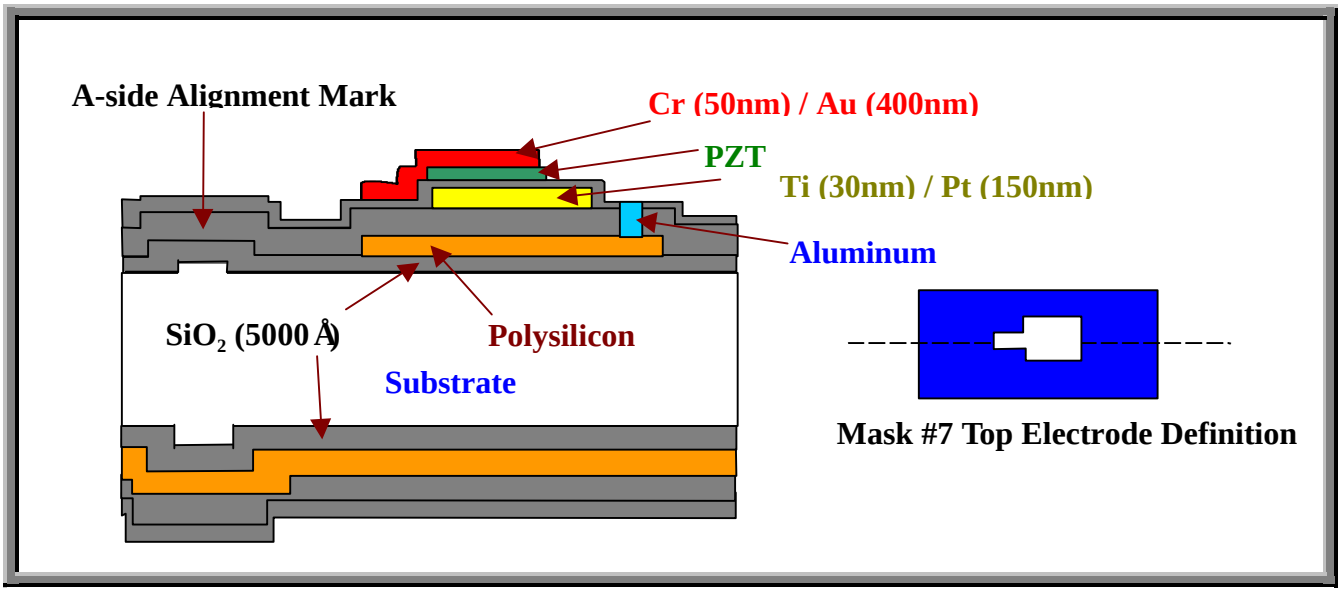

18	***A-side Open Bonding Windows*** *Mask #8*	18.1 Sputtering SiO2 (Target=300nm) on A-side B-side oxide thickness remains unchanged	**MFC Phase: II**
		18.2 Standard Lithography with A-side Bonding Windows Opening Mask (#8) • Spin photo-resist (PR207) on A-side, soft-bake, expose, develop and hard-bake	
		18.3 BOE Wet Etching Pads SiO_2	**MFC Phase:II**
		18.4 Photo-resist Strip	**MFC Phase:II**

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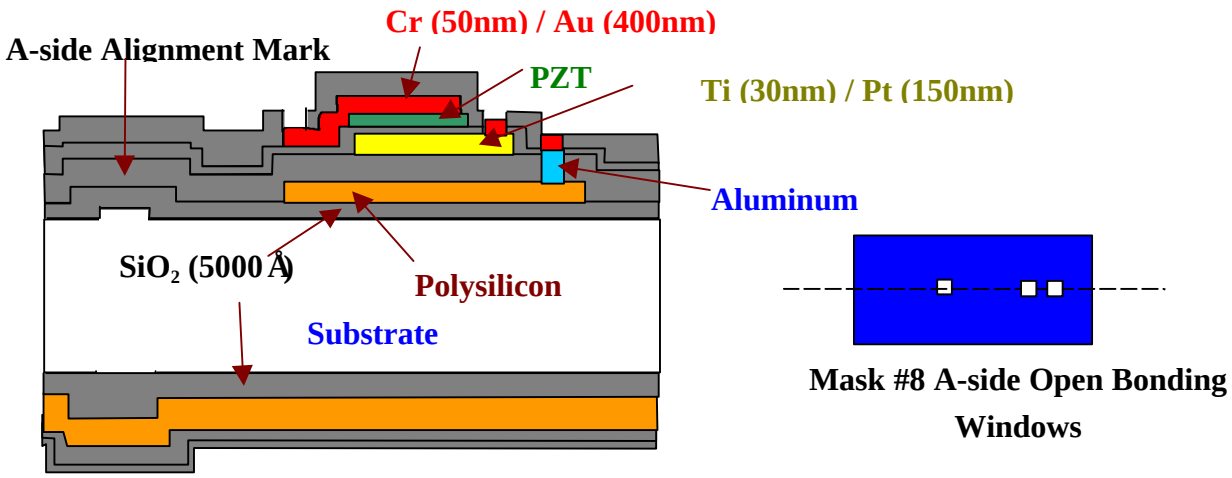
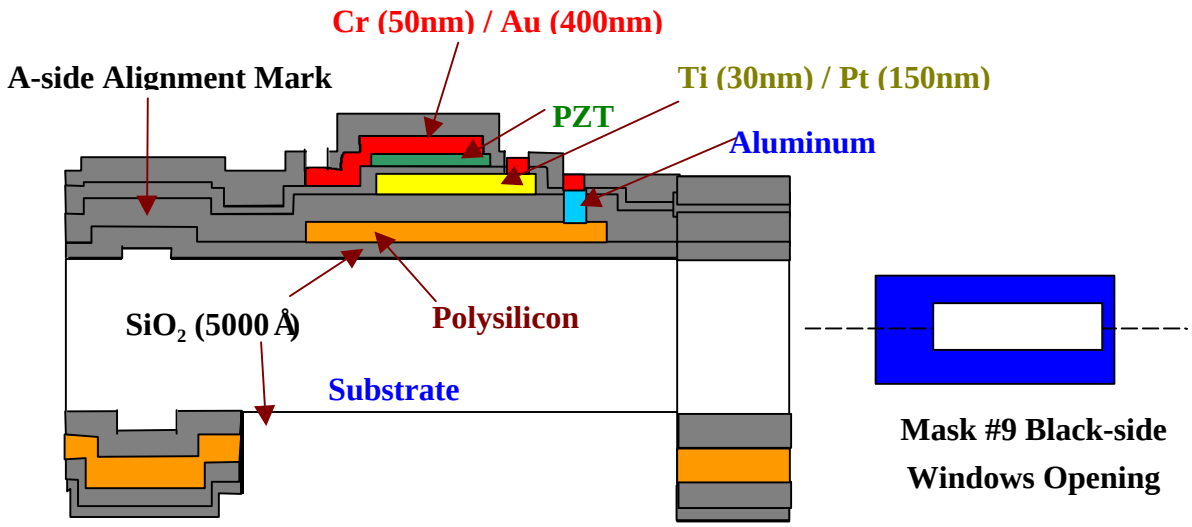


19	***B-side Back Windows Opening***	19.1 Standard Lithography with B-side Back Windows Opening Mask (#9) • Spin photo-resist on A-side as protection, hard-bake • Spin photo-resist (PR207) on B-side, soft-bake, expose, develop and hard-bake	**MFC Phase: II**
		19.2 Backside Etch • BOE Wet Etching SiO_2 (6 mins) • Plasma Dry Etching of Polysilicon (observe color change for end-point detection, needs lot of over-etch) • BOE Wet Etching SiO_2 (6 mins)	**MFC Phase: II I II**
	Mask #9	19.3 Photo-resist Strip	**MFC Phase:II**

Remark:

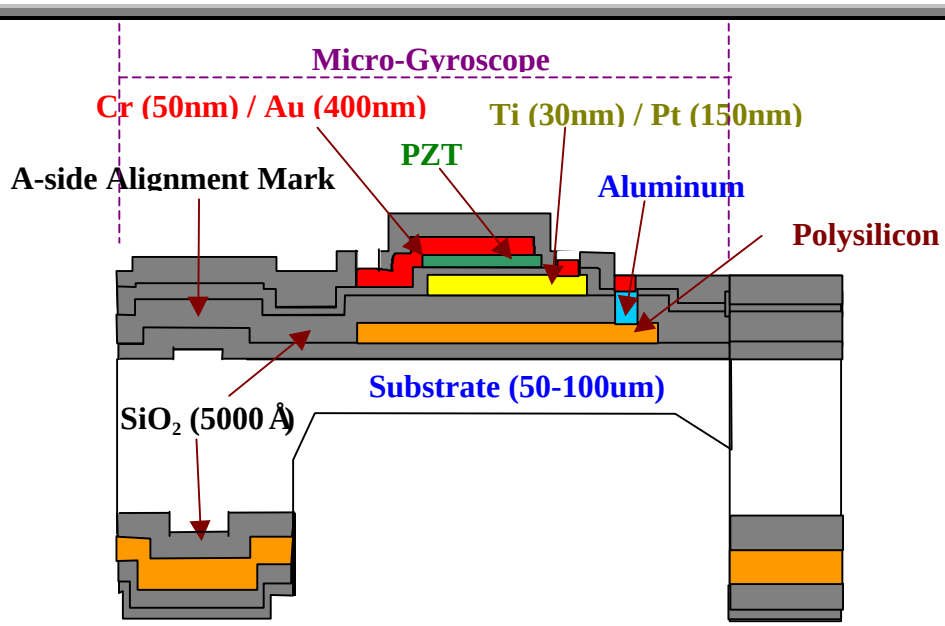
Cross-section:



20	***Bulk Silicon Removal***	20.1 TMAH Anisotropic Etching Silicon (***Target=Si 50 - 100um left***) • Measure wafer's thickness to estimate the required time • Put wafers in the TMAH standard bath (change solution first because the bath is dirty as it is seldomly used) • 85ºC for about 10 hours (5 hours per day in MFC, needs two days to finish) depends on wafer's thickness • Monitor temperature every hour	**MFC Phase: II**

Remark:

Cross-section:



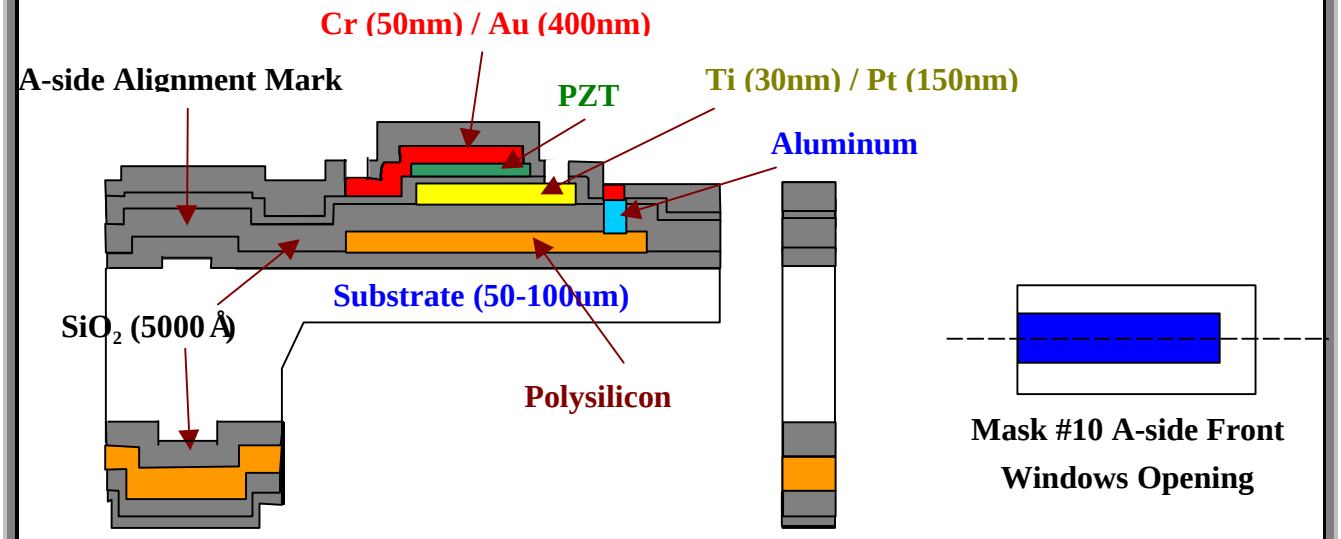
21	**Al Deposition**	21.1 Deposition of Aluminum (*Target=1500-2000nm*) ***Prefer to do in phase I (important for quality control in the meantime)***	**MFC Phase** **I**
Remark:			

22	***A-side Front Windows Opening***	22.1 Standard Lithography with A-side Front Windows Opening Mask (#10) • Spin photo-resist (PR204) on B-side and attach the B-side to a dummy wafer for ***one day*** such that the device wafer is glued with the dummy wafer. This is done because the B-side is already etched by TMAH, there are a lot of holes there and so it cannot be fixed on the resist-spinning machine which uses vacuum pump to fix wafer for high-speed spinning. • The dummy wafer becomes the back-side of the device wafer. Now, we can spin photo-resist (PR204) on A-side, soft-bake, expose, develop and hard-bake	**MFC Phase:** **II**
		22.2 Wet Etching Al (H_3PO_4 in standard bath)	**MFC Phase:II**
		22.3 Photo-resist Strip	**MFC Phase:II**
	Mask #10	22.4 BOE Wet Etching of SiO_2	**MFC Phase:II**

	22.5 RIE Dry Etching Silicon (*Target=100um*) • Pressure: 130, • 115: 150 • SF_6: 150 • Time: 200mins (takes wafer out of plasma chamber every 20 mins and let the chamber to rest for 5-10mins before next run, needs a total of 10 runs in other words).	**MFC Phase: I**
	22.6 Al Removal (H_3PO_4 in standard bath)	**MFC Phase: II**

Remark:

Cross-section:



23	**Die Separation**	23.1 Separate the Die by a Careful Cut **May be able to break the wafer into pieces of die manually.**	**Sensor Lab**
24	**Wire-bonding**	24.1 Gold-wire-bonding for Testing	**Sensor Lab**
25	**Testing**	25.1 Testing For Sensitivity and Functionality of Gyroscope	**Analog Research Lab**

Remark:

~ END OF PROCESS ~